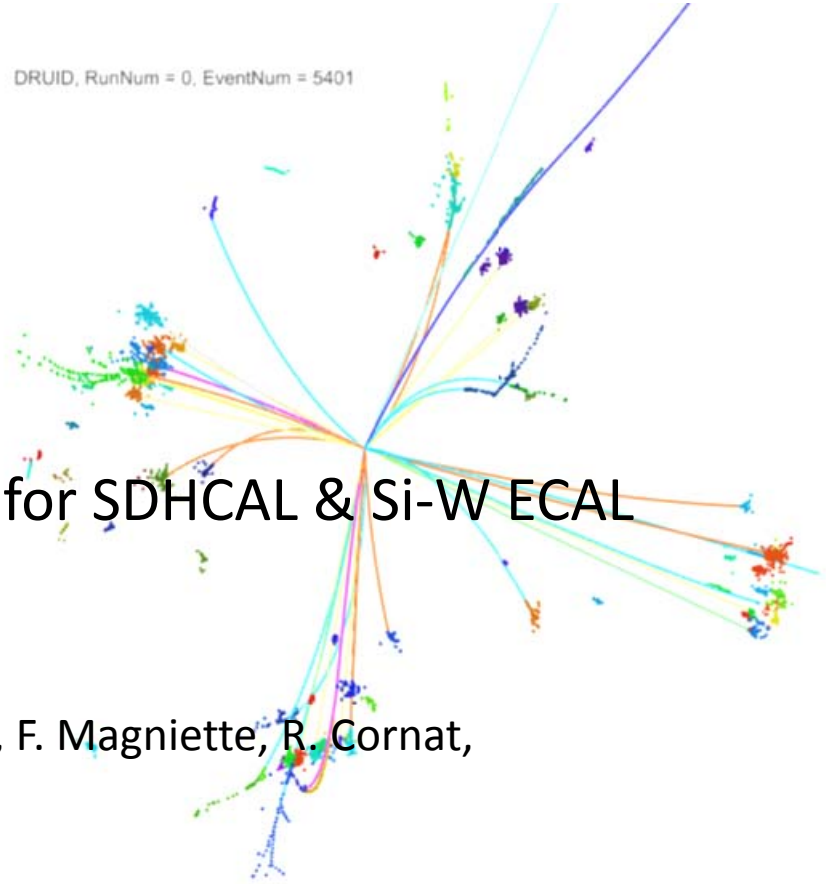

Status of Common DAQ for SDHCAL & Si-W ECAL

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Goals

Preparation of a common test-beam (june'16) without modifying the existing systems

- Keep all existing HW & SW interfaces
- Access through high level functions (configuration, calibration, acquisition)

Evaluation of EUDAQ software

- Common GUI for configuration
- Central Run control and data collection

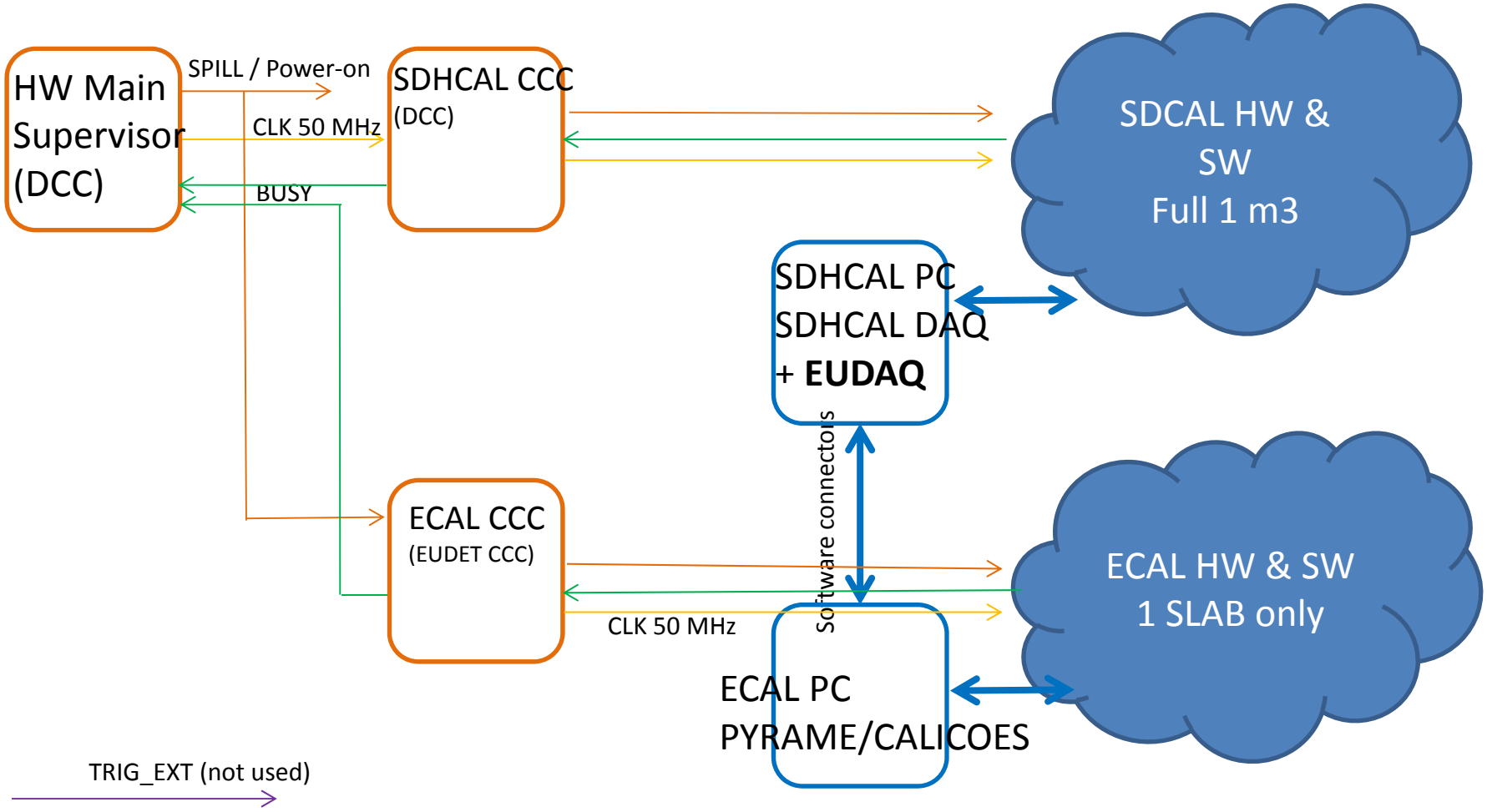
First approach of unified timings

- HW main supervisor kindly prepared by IPNL (SPILL generator & fan-out, clocks signals, combination of BUSYs)
- Mapped to a DCC

First test campaign

- IPNL 1-2 March 2016

HW architecture



Test results : HW setup for synchronisation

Alignment of acquisition windows

- SPILL triggers the power-up then a “start-acquisition” validated with a “val_event”
- A proper alignment of the “val_event” windows is mandatory in order to get the same BCIDs, ECAL is about 1.4 ms late wrt. SDHCAL
- SDHCAL “val_event” can be delayed (programmable in SDHCAL CCC)
- Alignment within one slow clock period possible and done
- 400 ns skew on ECAL side (< 1 BCID)
- 2.5 µs skew on SDHCAL side has been fixed : now < 1 BCID

Synchronization of SPILL ID

- SPILL counters are reset during the configuration procedures
- Runs start with the ECAL and SDHCAL counters set to stable and knows values (0)

Use of BUSY to optimize the dead-time

- SPILL restarted immediately after end of busy
- OK on SDHCAL
- BUSY not transmitted by ECAL (fixed & now working at LLR)

Central clock

- Even if it is not mandatory
- ECAL CCC can be feed with the 50 MHz clock from the main HW supervisor (common clock)

Test results : Software

Control of configuration from EUDAQ

- EUDAQ sends appropriate global configuration orders to detector systems
- Configuration done is reported ok to central SW
- EUDAQ state machine is not appropriate for a refined control

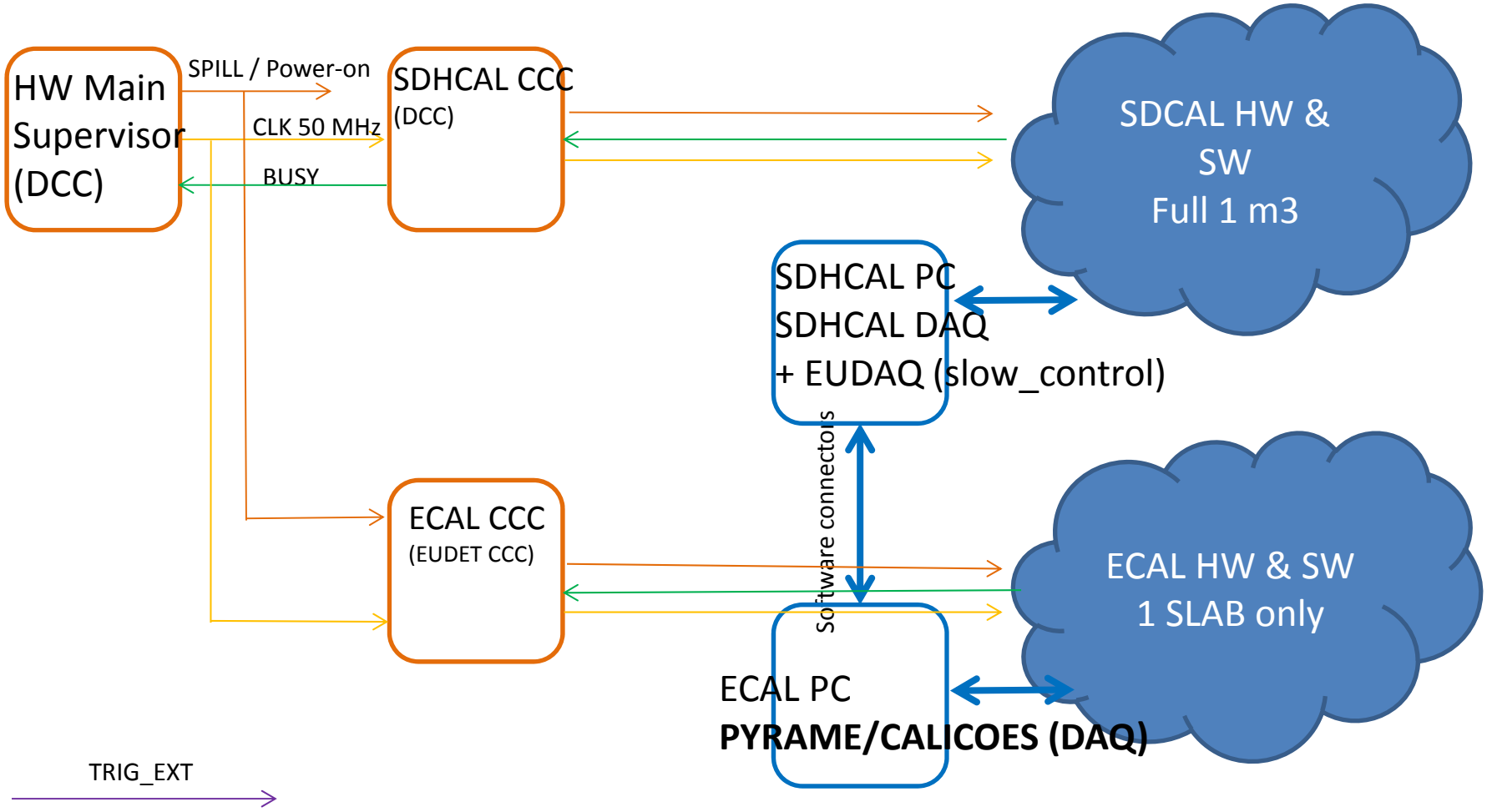
Run control and DAQ

- EUDAQ generates a run id, sends appropriate orders to detector systems and collects data
- Seen working independently for ECAL and SDHCAL alone
- Several remarks sent to EUDAQ community
- Showstopper issues when declaring two data collectors (may be our misunderstanding)
- **Support from EUDAQ community is asked for on-site debugging**

Alternate Run Control and DAQ

- Detector subsystems can be configured to collect data from other subsystems
- ECAL SW collects data from SDHCAL (Preliminary test successful)
- SDHCAL SW is able to collect data from ECAL SW (under development)

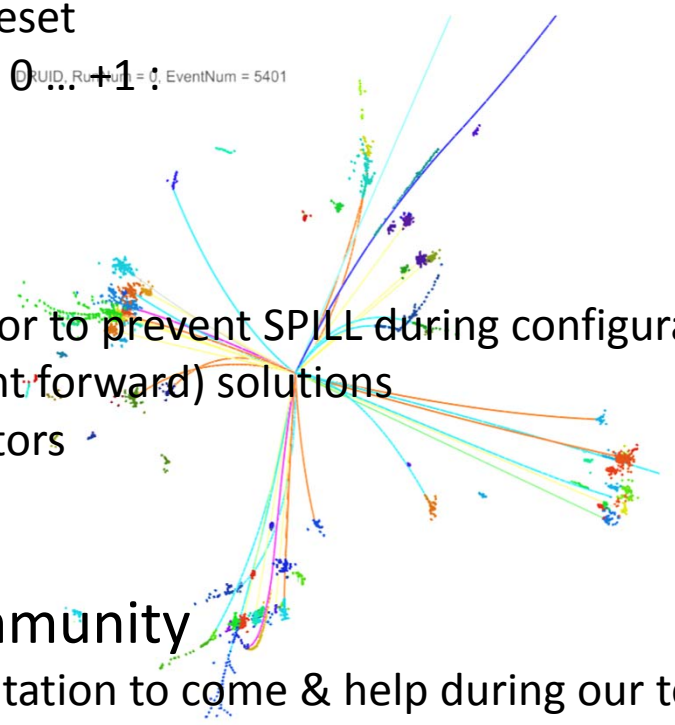
HW architecture for common DAQ at the end of the first test period



Conclusion : SiWECAL/SDHCAL Common DAQ

First attempts are satisfactory

- Successfully configured detectors from central EUDAQ SW
- Successfully acquired data from central SW (PYRAME) and attempts with EUDAQ
- Seen issues fixed now at lab. (ECAL BUSY ; SDHCAL jitter)
- Run starts with time_stamp counters properly reset
- Acquisition windows (and BCIDs) aligned within 0 … +1 :
  - to be checked using several GDCC (ECAL)



Forthcoming tasks

- Add a SW controlled veto on Main HW supervisor to prevent SPILL during configuration
- Debug EUDAQ and/or develop alternate (straight forward) solutions
- Add more ECAL slabs and assemble the 2 detectors
- Monthly tests campaigns

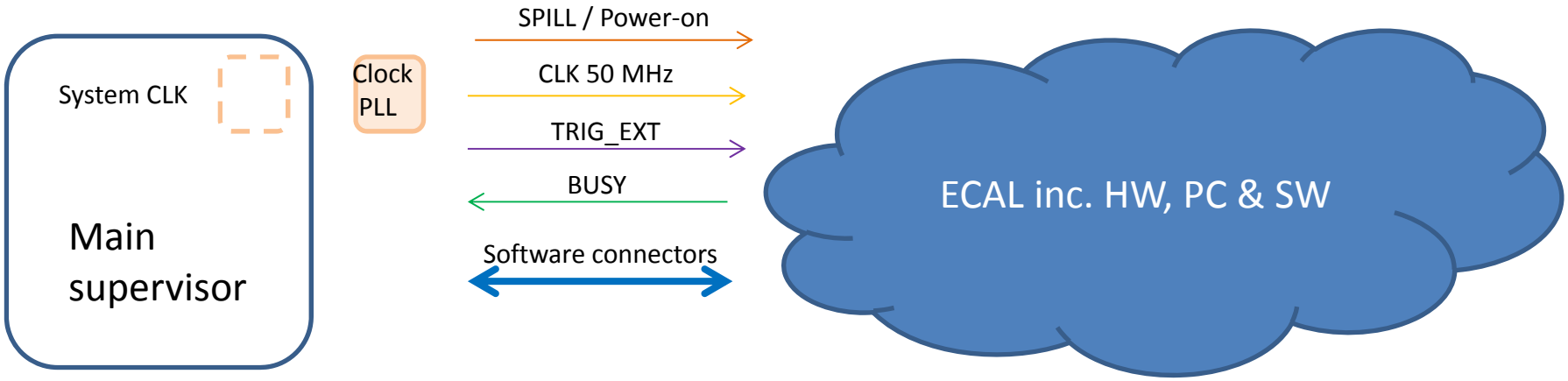
Remarks have been sent to EUDAQ community

- Together with a demand for support and an invitation to come & help during our tests

Si-W ECAL

The Si-W ECAL system will not be modified

- Can be considered as a black box
- Known hardware & software interfaces
- External master system provides necessary signals/software orders
- Conversion from system clock to 50 MHz **not** provided (can be external or internal to the main supervisor)

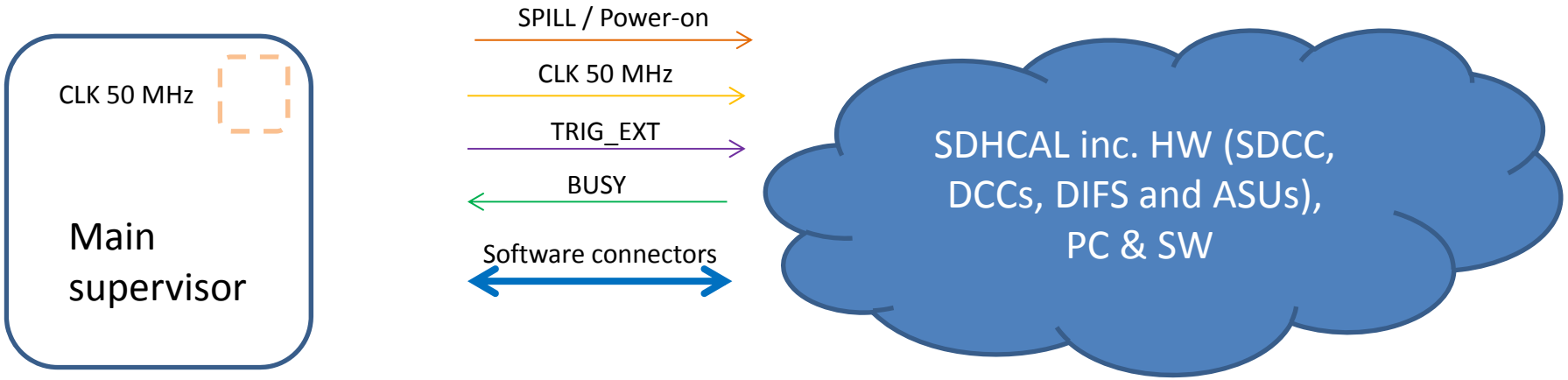


SDHCAL

RC1

The SDHCAL system will not be modified (except at its interfaces)

- Can be considered as a black box
- Known hardware & software interfaces
- External master system provides necessary signals/software orders



RC1 A ADAPTER pour SDHCAL

rcornat; 03/03/2016