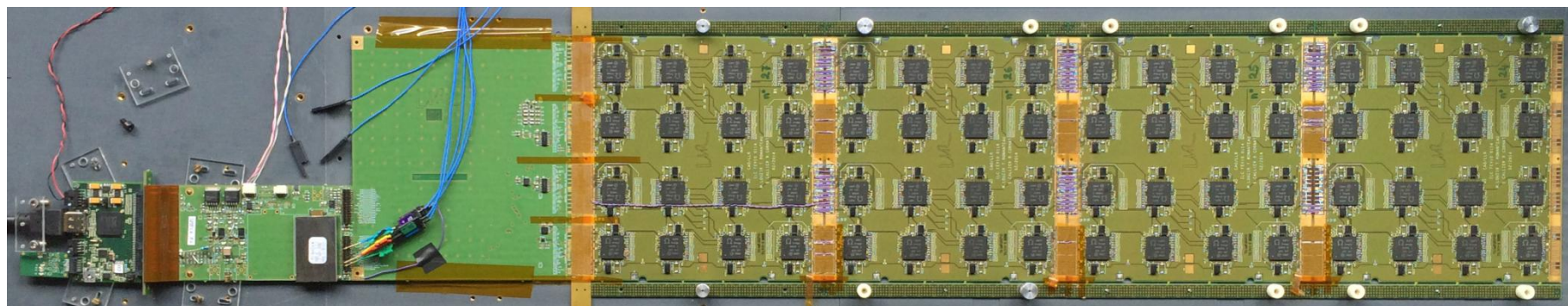




# SI-W ECAL Long SLAB results

By

J. NANNI & M. LOUZIR



CALICE Meeting 7-9 March 2016



# SI-W ECAL Long SLAB

## Topics




- Status
- Interconnexions
- Clock spreading
- Problems observed
- Next steps



# SI-W ECAL Long SLAB

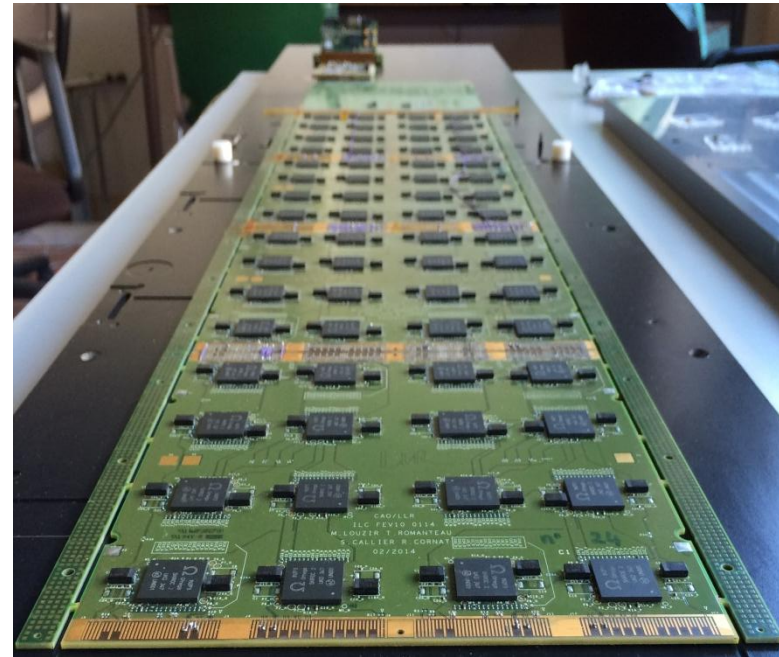


## Status

- 4 cards connected
  - Control command: ✓
    -  calicoes/pyrame: <https://llr.in2p3.fr/sites/pyrame/calicoes/documentation/index.html>
  - Slow control: ✓
  - Readout: ✓ (only 3 ASU)
  - Clock spreading: ✓
  - Analysis: on going (root script to upgrade) ✓



Readout problem:  
no start readout signal on 4th ASU;  
short circuit or PCB damaged (due  
to too many attempts for  
interconnects).



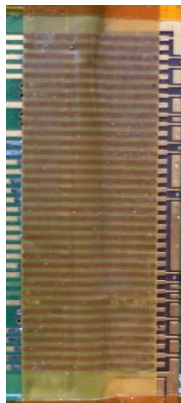
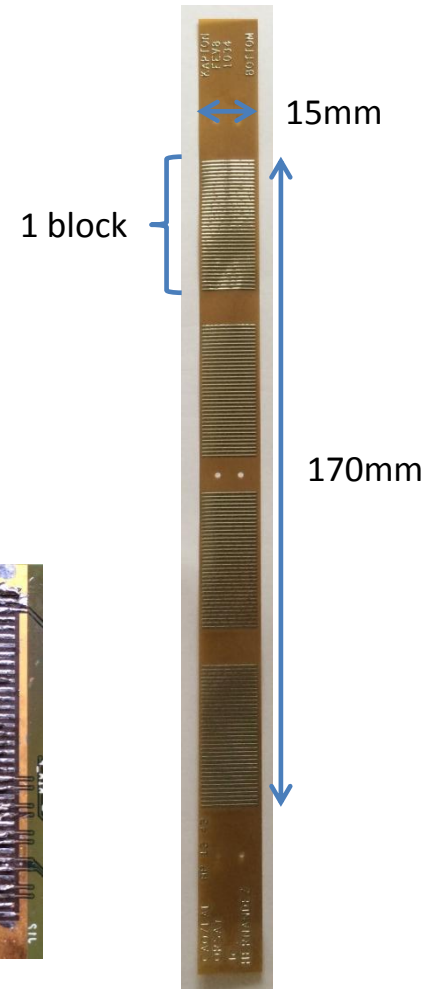


# SI-W ECAL Long SLAB

## Interconnexions



- Solution used: kapton
  - Solder per block at  $T > 450^{\circ}\text{C}$
  - Unappropriate temperature profile
    - Short circuit under BGA possible
    - Problem fixed
  - Short circuit detected under Kapton
    - Kapton replaced by small wires



Remove kapton



Solder small wires



Short-circuits detected

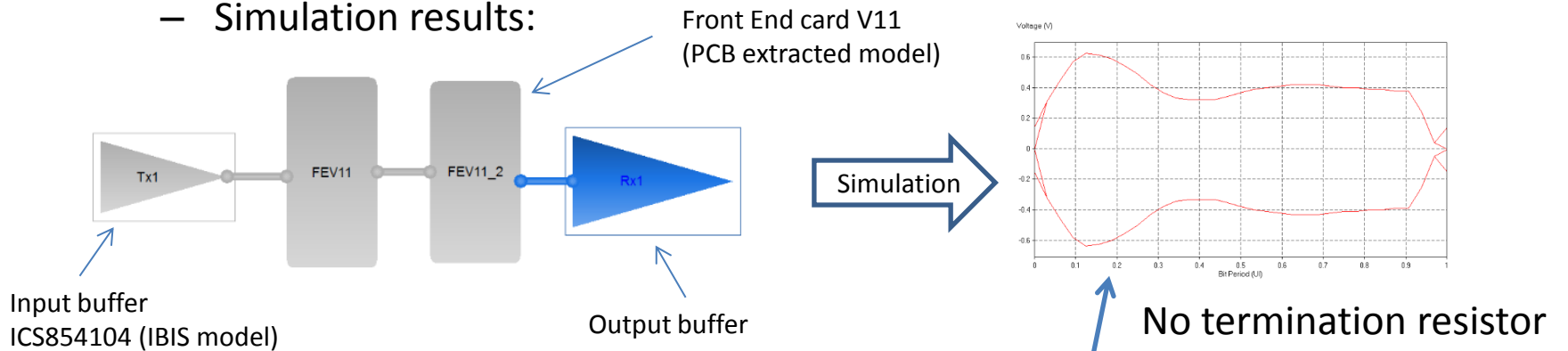


# SI-W ECAL Long SLAB

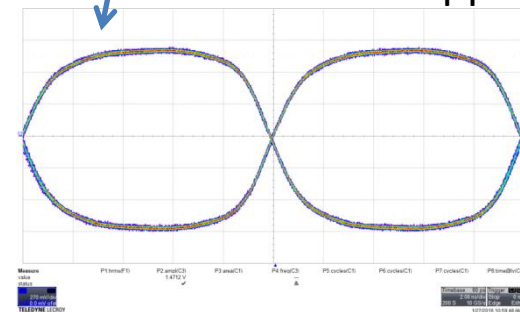


## Clock spreading

- Simulation analysis for 2 ASU:
  - R-C Modelisation of clock transmission line for each ASU (included bounding, pad, packaging and PCB trace and via): **50pF ; 2,7Ω** using **Cadence® Sigrity**
  - Simulation results:



- Measurements: fast clock after 4 ASU
  - Skew: 400ps
  - Jitter: 150ps
  - Eyes well opened
  - Clock parameters keep ( $F$ ,  $T_r$ ,  $T_f$ ,  $V_{pp}$ )
  - **100Ω termination resistor needed**



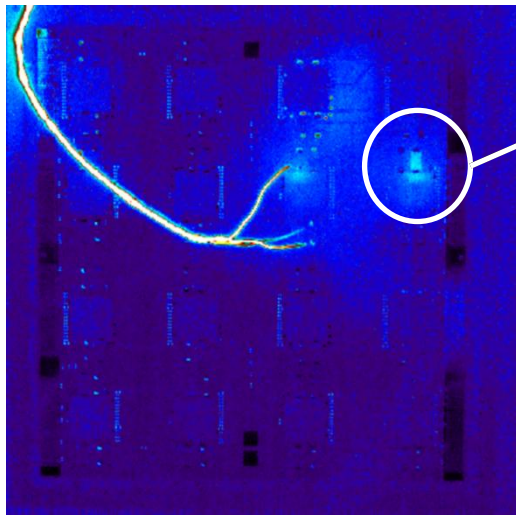


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## Problems observed



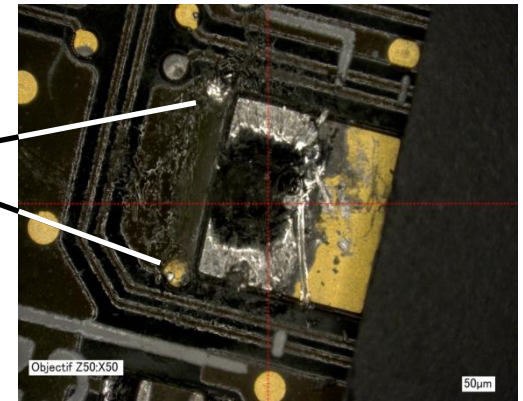
- Short circuits:
  - 5 ASU received March 2015
    - 2 ASU in short circuits V<sub>dd</sub>! – gnd!



Problem around decoupling capacitance for SKIROC chip

2 vias of gnd! too close from v<sub>dd</sub>! capacitance connexion.

Problem fixed ✓





# SI-W ECAL Long SLAB



## Next steps

- Get 8 to 10 cards chained
- Glue baby wafers on edges
  - Adapt mechanical support
  - Analyse: Scurves, Noise and Cosmic ray detection
- Update root scripts => data analysis
- HV kaptons (studies and conception done, wait for production)
- Long slab clock spread integrity simulation for 8/10 ASU
- Power supply analysis for 8 cards



# SI-W ECAL Long SLAB

The end



Thanks for your attention

Any question ?