AHCAL electronics.

Status and outlook

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AHCAL main meeting

DESY, Nov. 10th, 2015

HELMHOLTZ GEMEINSCHAFT

CALICE Calorimeter for ILC

AIDA

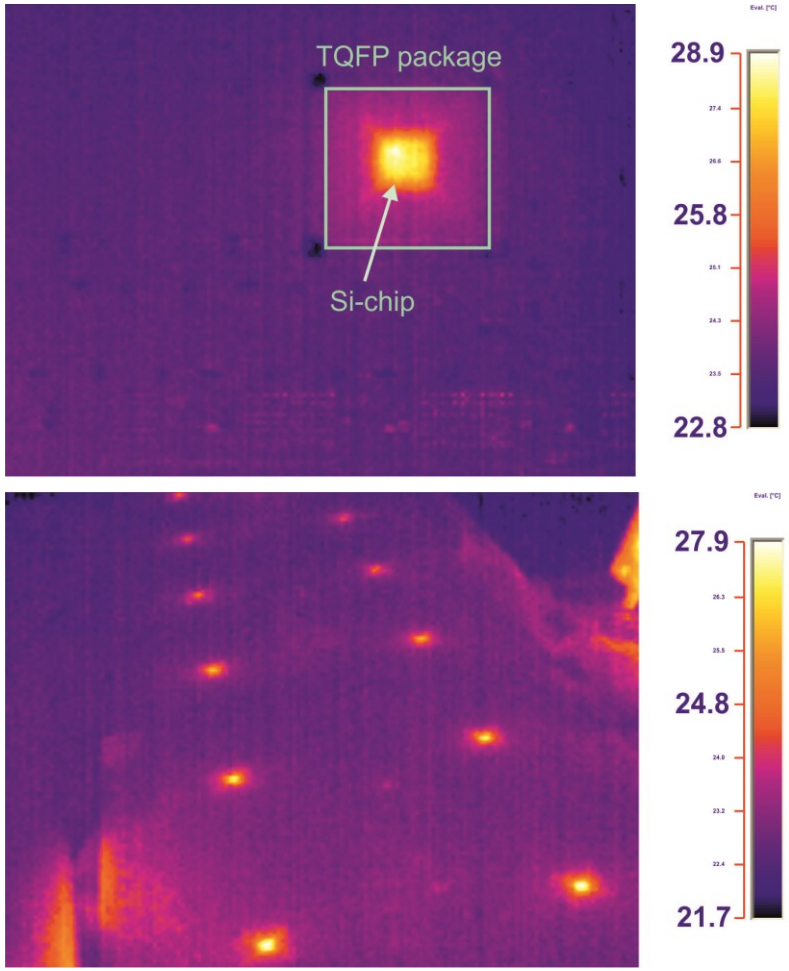
DESY

Contents

- Reset of Probe-Register
- SP2D/SP2E in BGA package
- New Generation of Electronics
- HBU3 – LED system
- Power Pulsing – Status

RESET of Probe Register

- Problem: With probab. of 50% all SP2bs of full slab have high currents on VDDD after switching on (1A in total).
- SPIROC current consumption different on each switch-on.
- Solution: Reset of the probe register was implemented not correctly (i.e. the SPIROC sc_select input).
- Check if other effects (e.g. stuck TDCs) have the same origin.
- All DIF firmwares and Labview control programs need update!



SP2B(s) in high-current state

SP2D – very first look to the newest SPIROC

- 4 SP2Ds mounted on HBU2, 230 in a box.
- Commissioning started at FEB in close cooperation with LAL/Omega.
- First results, including testbeam available. Results preliminary.
- See Stephane‘s talk for detailed results.
- SP2D candidate for next HBU!

SP2D on HBU2

SP2D – Status so far

SP2D Pros

- First memory cell works.
- Pedestal shift much smaller.
- inDAC uniformity much better, in two modes.

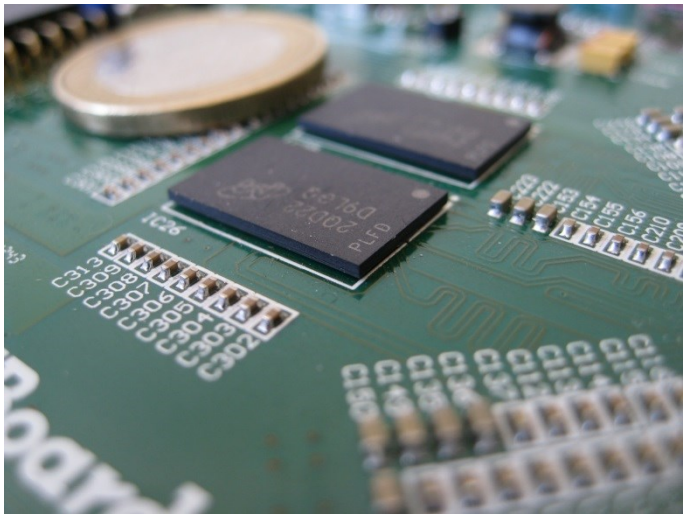
SP2D Cons

- Chip triggers to undershoot of shaped pulse (time walk)
- 3 memory cells show strange behaviour, workaround (HBU change) needed. Tested successfully on HBU2.
- Pinout different to SP2B: Cannot integrate preamp filter (higher noise), HBU change needed. Tested successfully on HBU2.

- SP2E with corrections produced end of December.
- SP2E in BGA package only.

SPIROC2E in BGA

- Aim: Remove HBU cavities. HBU simplification!
- BGA package needs interposer, definition by OMEGA.
- OMEGA: Check if SKIROC package can be used. Long bondwires.
- Costs: New package ~15k, SKIROC package: 4-5k
- New package: We can define all parameters, e.g. free row of ball pins for vias on HBU. Avoid via-in-pad.



1.0mm BGA packages

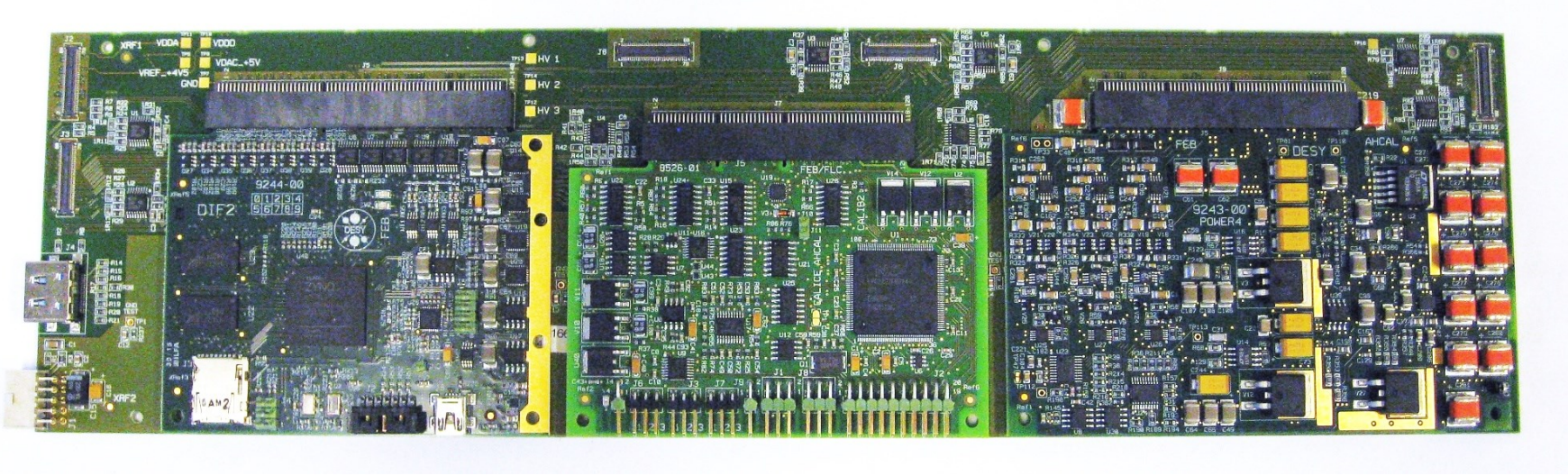
- Probably: HBU thickness increases by 0.1-0.2mm.
- Timeline for BGA development critical. Chip needed in 2nd half 2016.

HBU redesign (HBU4_SMD)

- HBU4_SMD ordered (8x).

- Newest Hamamatsu MPPCs (SMD, 4 pads)
- HBU4 configurable to use SP2B or SP2D (TQFP package in cavity)
- Less many (two) LED positions, special ridge and fiducials (Mainz)
- New LEDs (Lighthouse not licensed in Europe): Bivar SM0603UV_395.
- Blocking caps removed from bias points (power pulsing setup as default).
- Tiles without alignment pins!

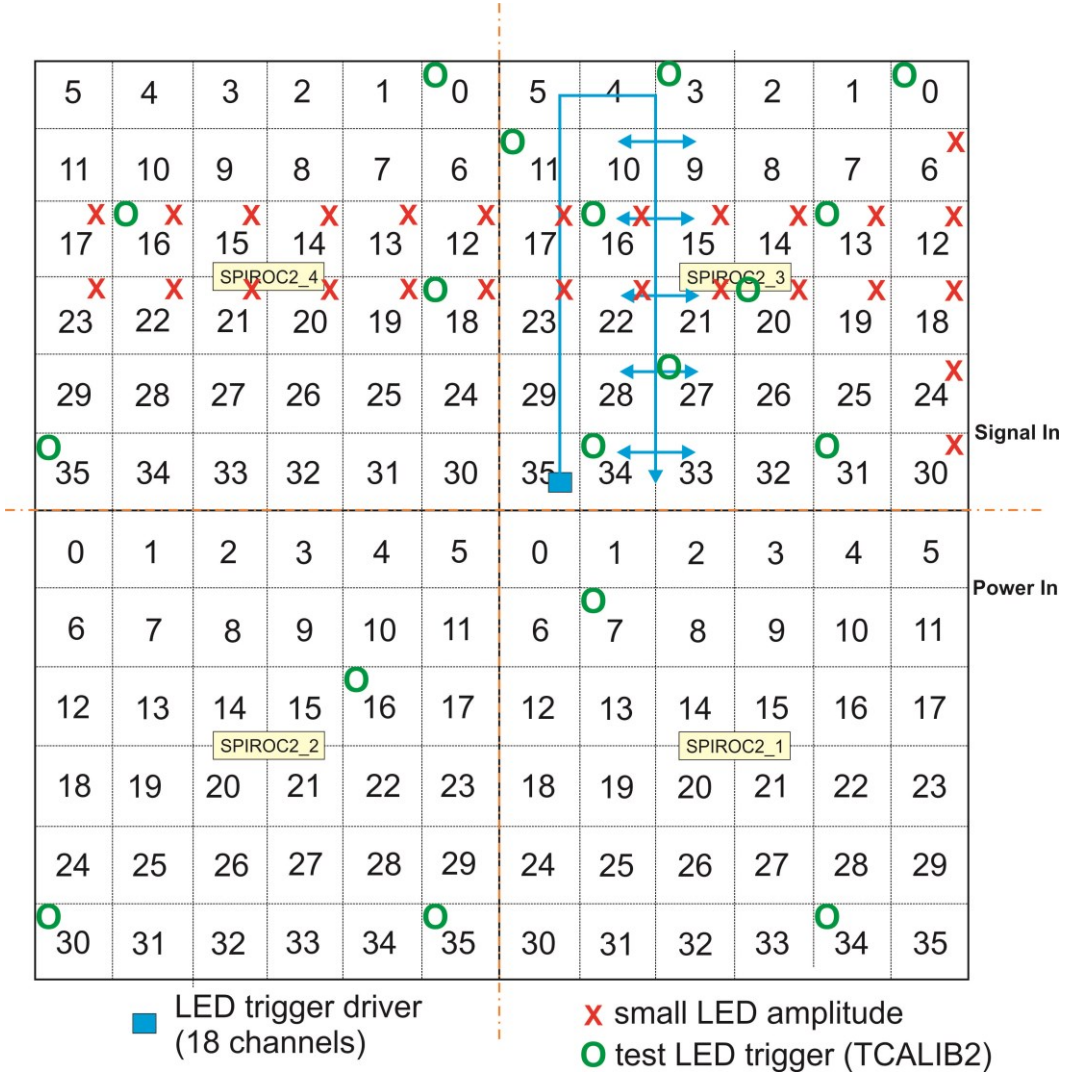
Interface Electronics



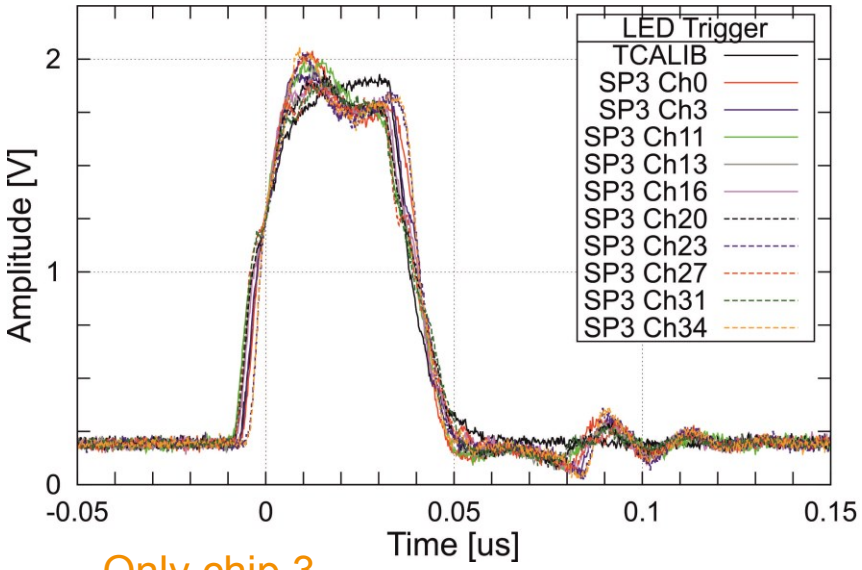
- Redesign of all DAQ interface modules finished.
- DIF: Xilinx Zynq FPGA, POWER: Optimized power pulsing.
- Commissioning beginning 2016
- Needed for final power pulsing studies: Test power-supply side.

LED driver HBU3

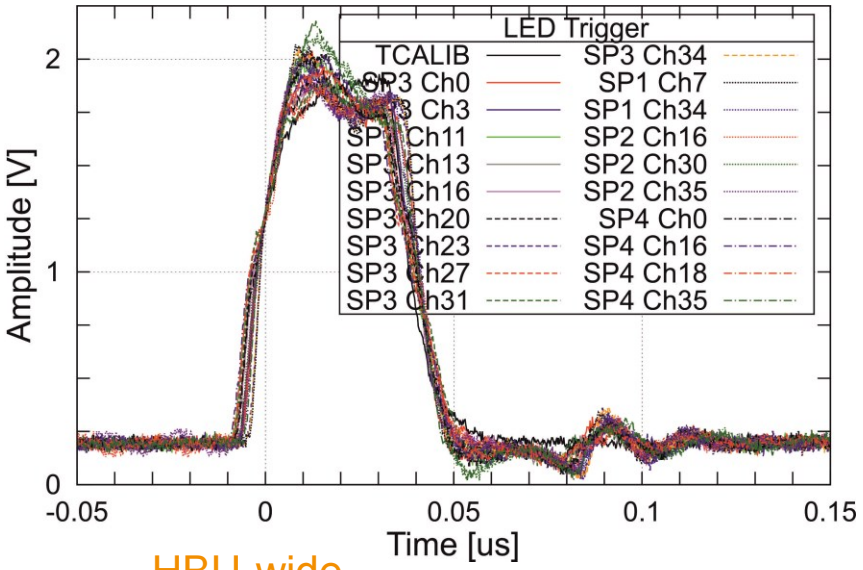
- Problem: Channels with low LED amplitude (see red crosses)
- No special relation to position. Not all HBU3s concerned. Quality control: Support from Wuppertal welcome!
- Reason? Should be LED trigger. Test: green circles.



LED driver HBU3



Only chip 3

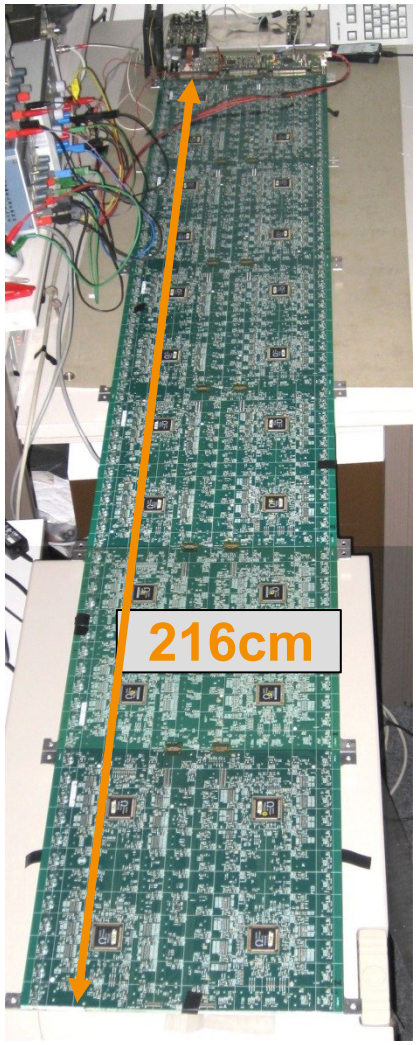


HBU-wide

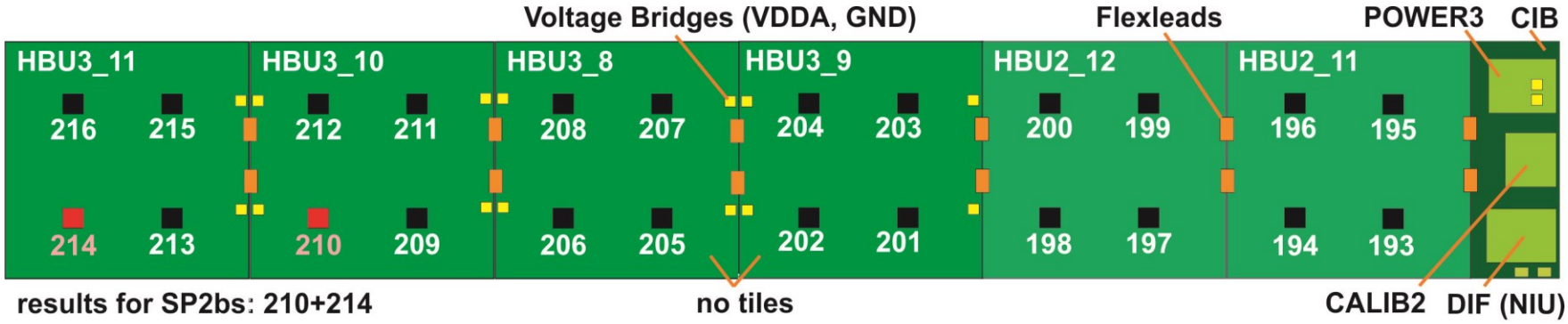
- No difference for 0% - 80% amplitude. Does not explain factor 5-10.
- HBU3: manual correction of LED soldering. Reason e.g. damaged lens?
- HBU4_SMD: Same LED setup.

Power Pulsing

- Power Pulsing setup in FEB-lab in operation.
- Started with USB DAQ – ok!
- Power Pulsing tests include three parts:
  - HBU3 qualification, tested now.
  - POWER / CIB / cable setup qualification. Cannot be tested without new DAQ interface modules.
  - SPIROC qualification with aim 40µW per channel. Will be tested with new DAQ interface modules.



Power-Pulsing – DC parameters

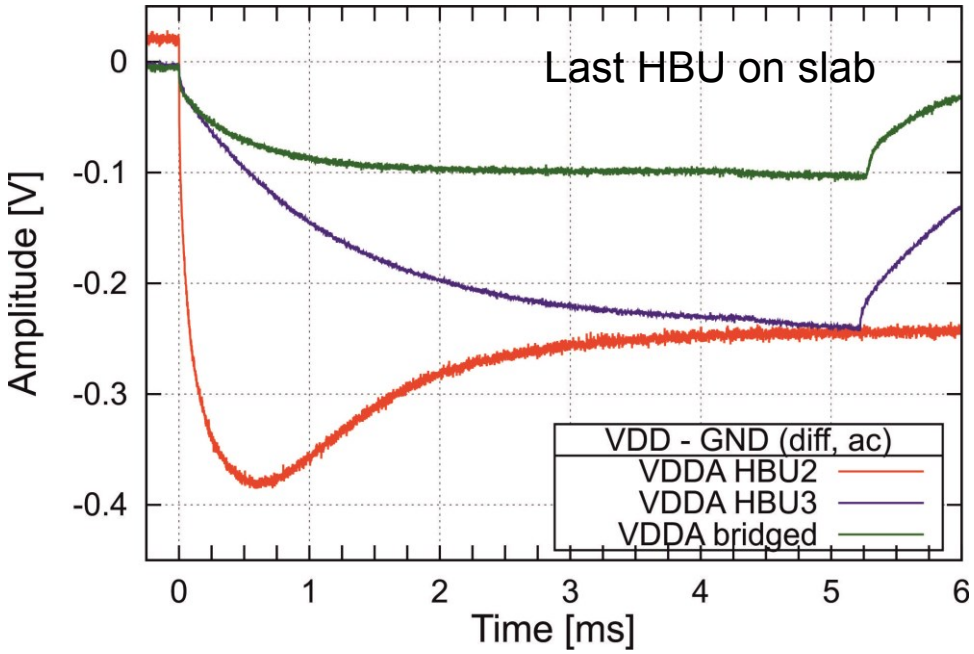


- Voltages measured on last HBU of the slab, no voltage bridges.
- Currents are for 24 SPIROCs.

	V - SPIROCs off [V]	V - SPIROCs on [V]	I - SPIROCs on, [mA]	I - SPIROCs off, [mA]
VDDA	3.30	3.10	2000	18
VDDD	3.30	3.26	225	24
VDAC	5.0	5.0	2.06	2.06
VREF	4.68	4.68	0.8	0.8
+6V input	-	-	4360	1220

Power-Pulsing – AC parameters

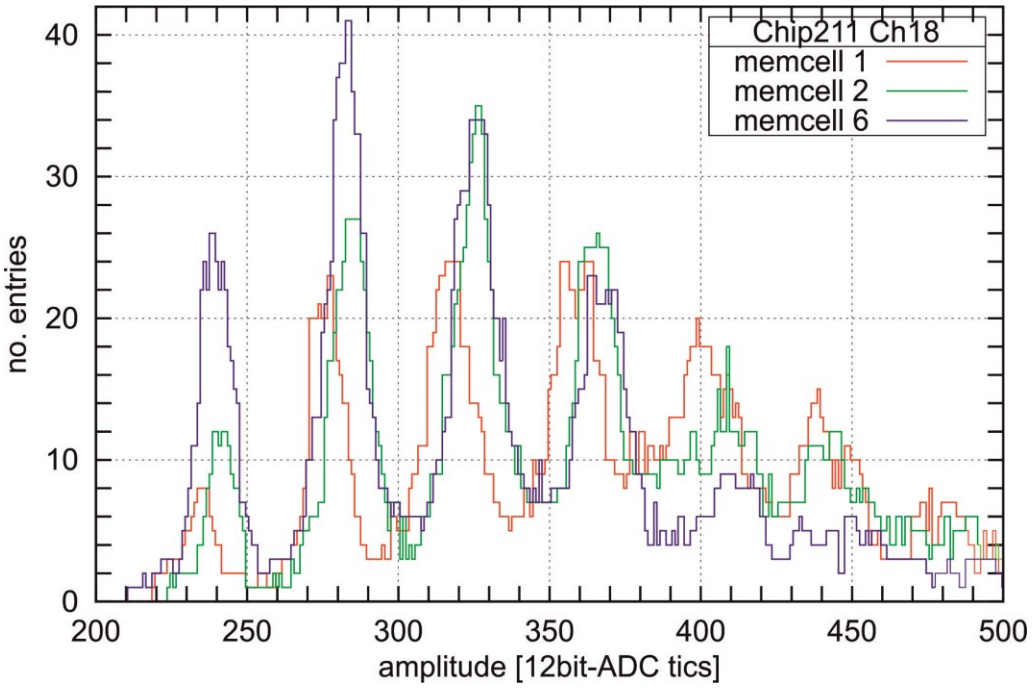
- Drop of the supply voltages on the last HBU in power-pulsing:
  - VDDA: 19mΩ, GND: 4mΩ per HBU+flexlead, no bridges.



- Gain and SPS-quality with respect to **switch-on time**?
  Aimed: Ton=20µs

SPS quality

- Ton=21µs, trigger (memcell) distance = 300µs (old setup: 2ms necessary)

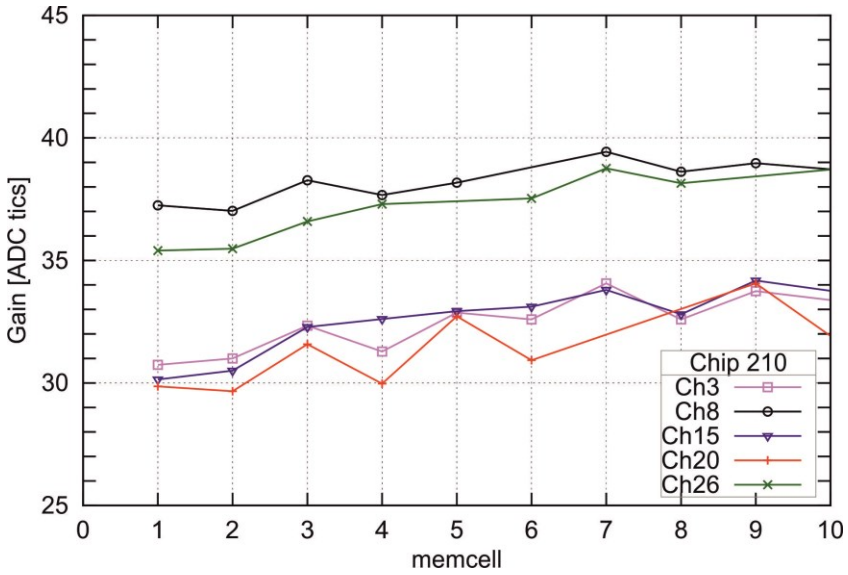


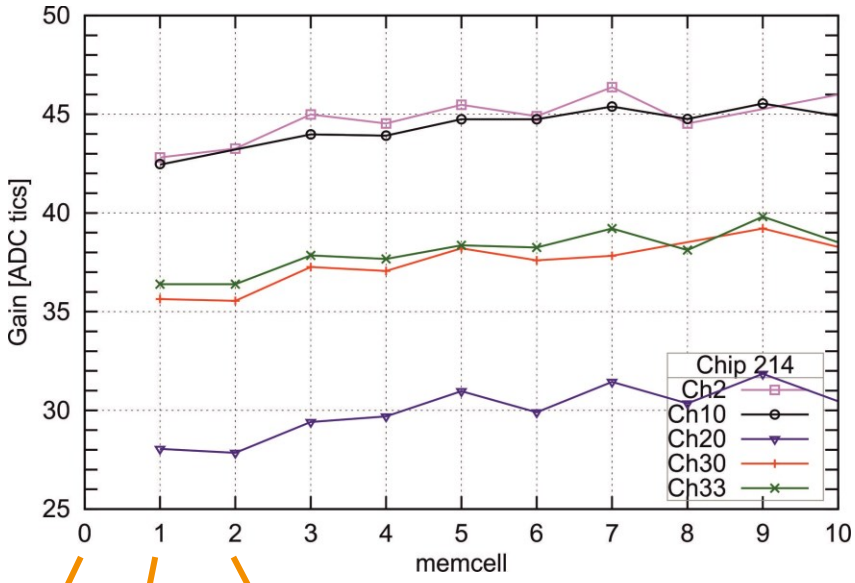
Switch-on time:
memcell 1: 300µs
memcell 2: 600µs
memcell 6: 1.8ms

- SPS quality does not change too much over time (only few channels checked). Much better than for HBU2 (Ton>2ms).

Power Pulsing – Gain drop

- Drop of gain i.e. for switch-on times <1ms (300µs per memcell):

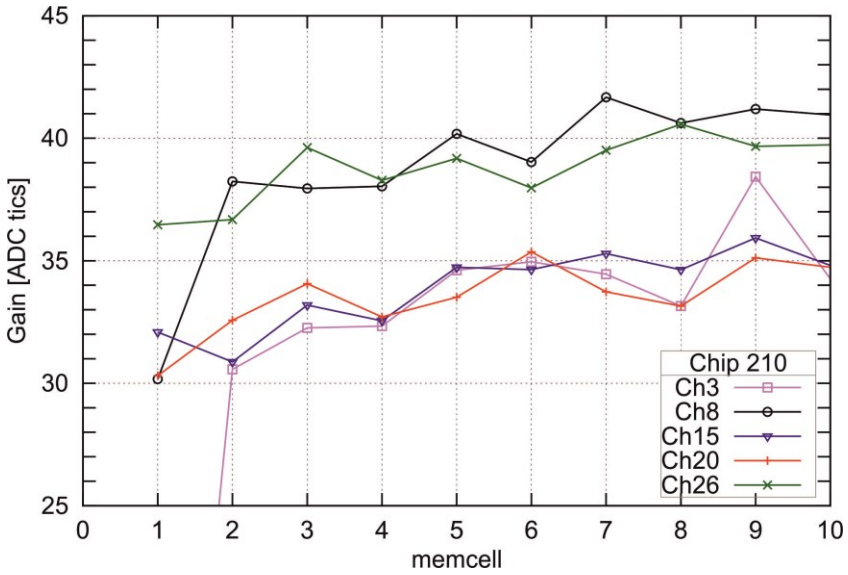


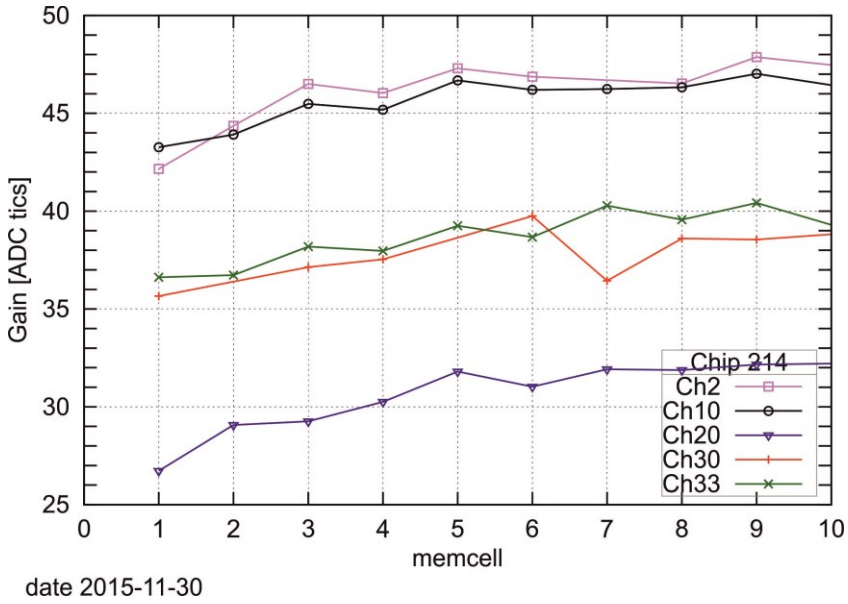


Switch-on time 0 300µs 600µs …

Power Pulsing – Gain drop

- Terminate SiPMs to VDDA only (300µs per memcell):



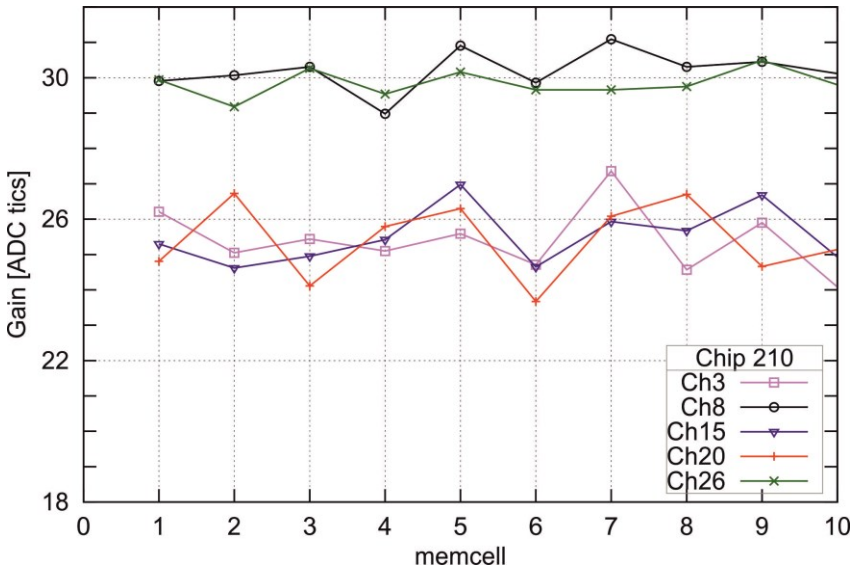


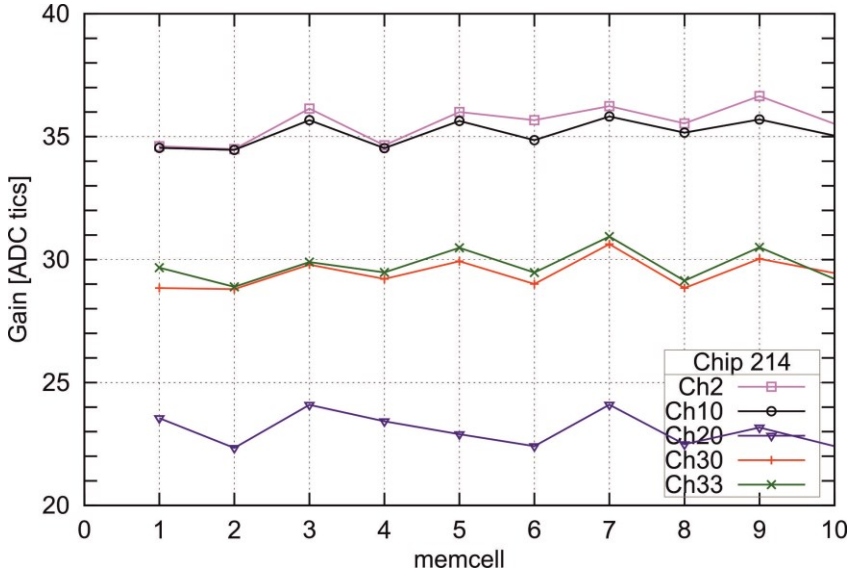
- No improvement.

Power Pulsing – Gain drop

- Close voltage bridges (300µs per memcell):

Many thanks to Adrian for the data evaluation!!

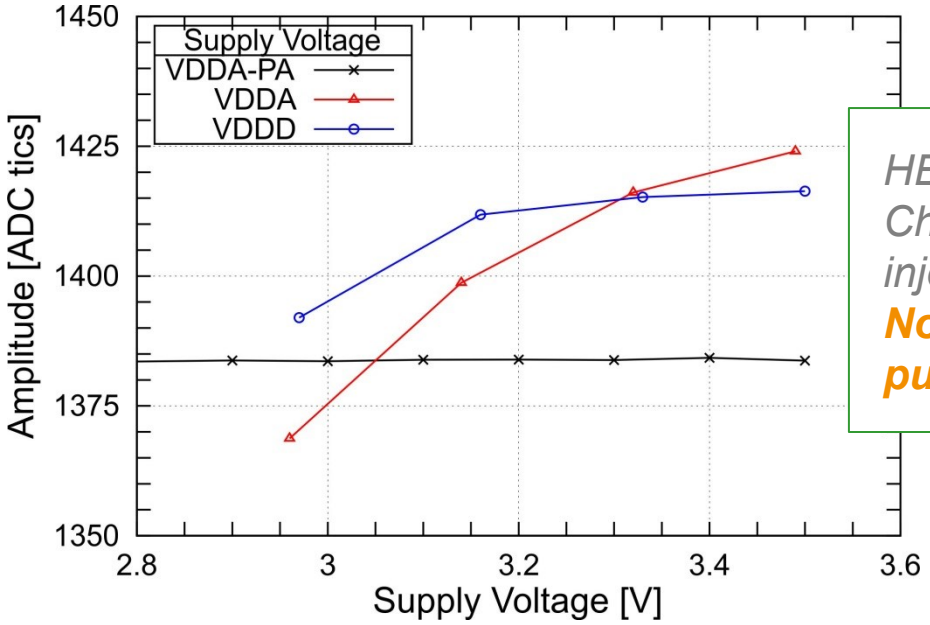




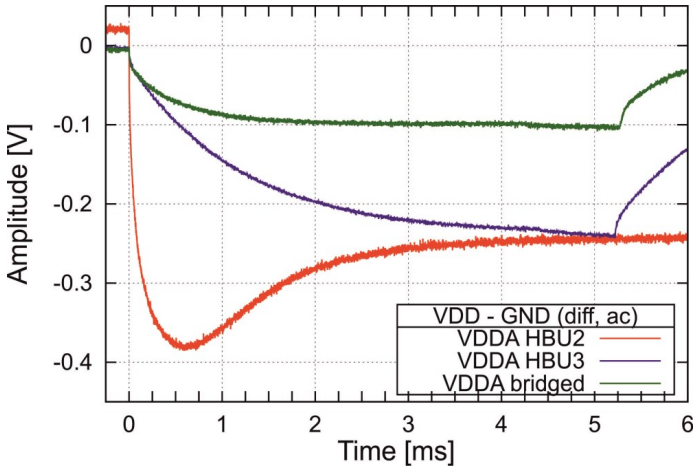
- Gain drop reduced significantly. Gain change observed – origin not clear up to now (maybe due to repair of POWER board?).
- Bridging the preamplifier filter did not improve behaviour => RC from flexleads and filter caps dominant. Trade-off noise – switch-on time.
- Flexleads main reason for gain drop. HBUs ok!

Gain SPIROC - STATIC

- How does SPIROC gain change with supply voltage?



HBU2_IX. Charge injection. ***No power pulsing.***



- Gain change in the same order as in power pulsing without voltage bridges.
- Strategy Power-pulsing: <u>Reduce voltage drop and transition time of VDDA:</u> Reduce RC (flexlead-filter caps and preamp filter).

Status and Outlook

- HBU4_SMD has been ordered. We can use SP2B or SP2D (including all possible bug fixes).
- 2016 2nd half: HBU without cavities, BGA package, HBU module thicker (0.1-0.2mm)
- Voltage bridges improve power pulsing. Important: Reduce RC.
  - Sensitivity of SPIROCs to VDDA changes?
  - Disadvantage in slab assembly (solder bridges).
- The SPIROC POD module has been commissioned successfully.
- NEW DAQ interface modules – commissioning in 2016.