KLauS3 ASIC

Implementation Status,
Characterization &
Plans

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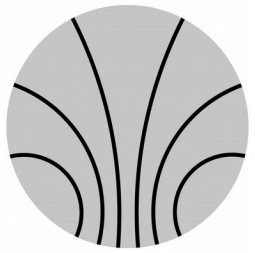


Prototypes in 180nm UMC CMOS

Reminder:

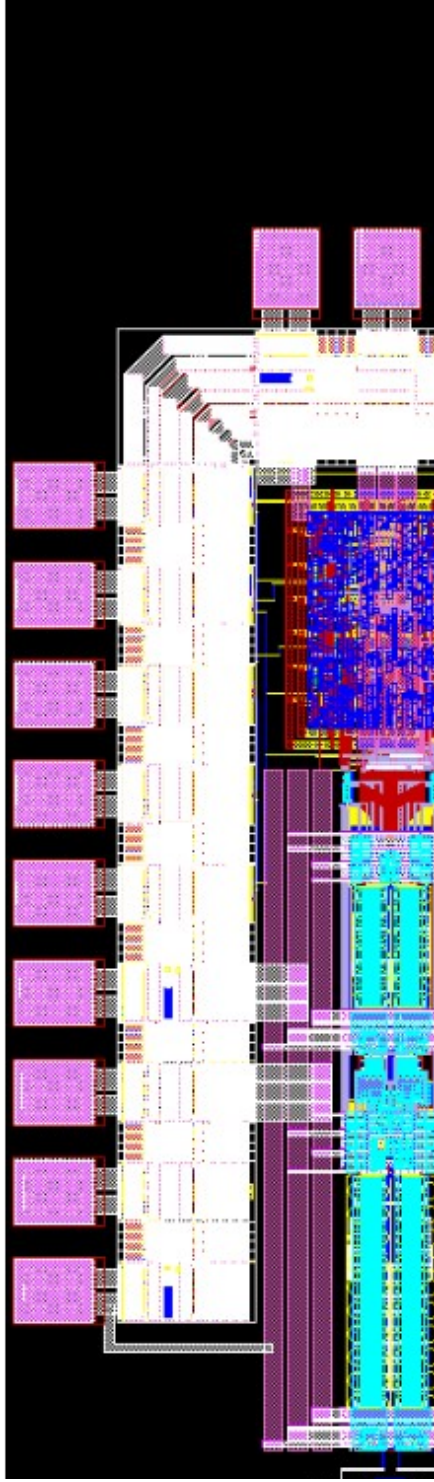
Front-end
SiPM charge measurement, time stamping
Optimize for low gain SiPMs (>10^5)

→ *SiPM bias tuning presented in Munich: 2V range*

ADC development
Two operation modes:

SiPM gain calibration – 12bit resolution
MIP quantization – 10bit resolution

→ *10 bit operation mode results presented in Munich*



Prototypes in 180nm UMC CMOS

Submission March / 15

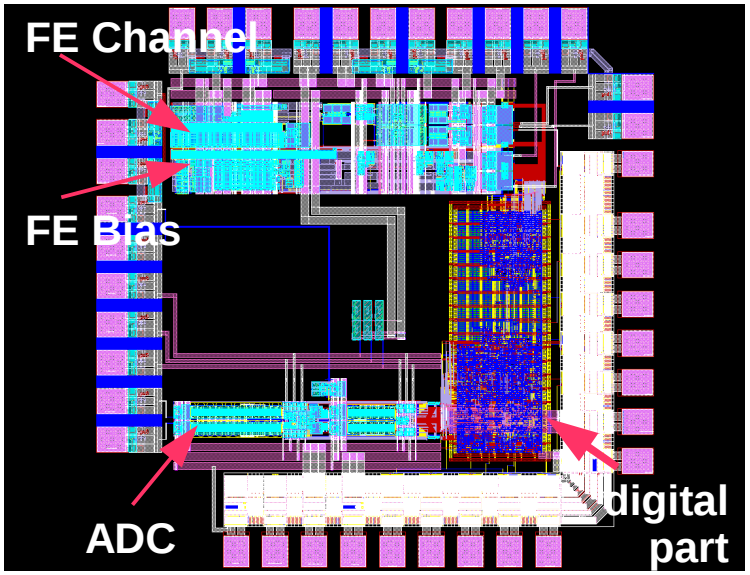
- Front-end
  - Most critical blocks implemented
- ADC channel

Received in July

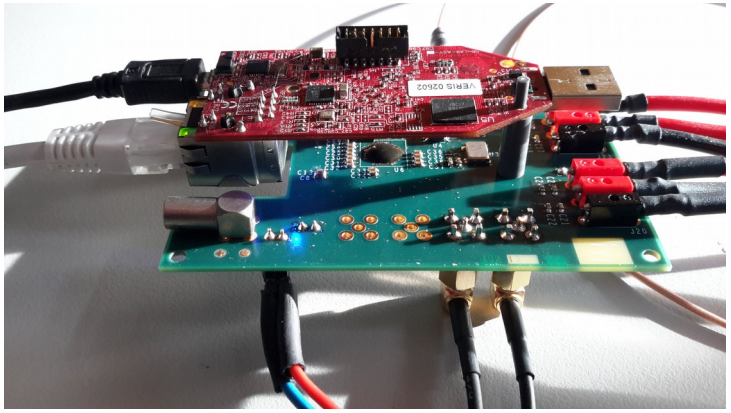
Submission May / 15

- Front-end
  - Most remaining front-end blocks added
  - [Low gain stage & Trigger]
- ADC
  - bug fix in control logic
  - → 12b mode now working

Received in October

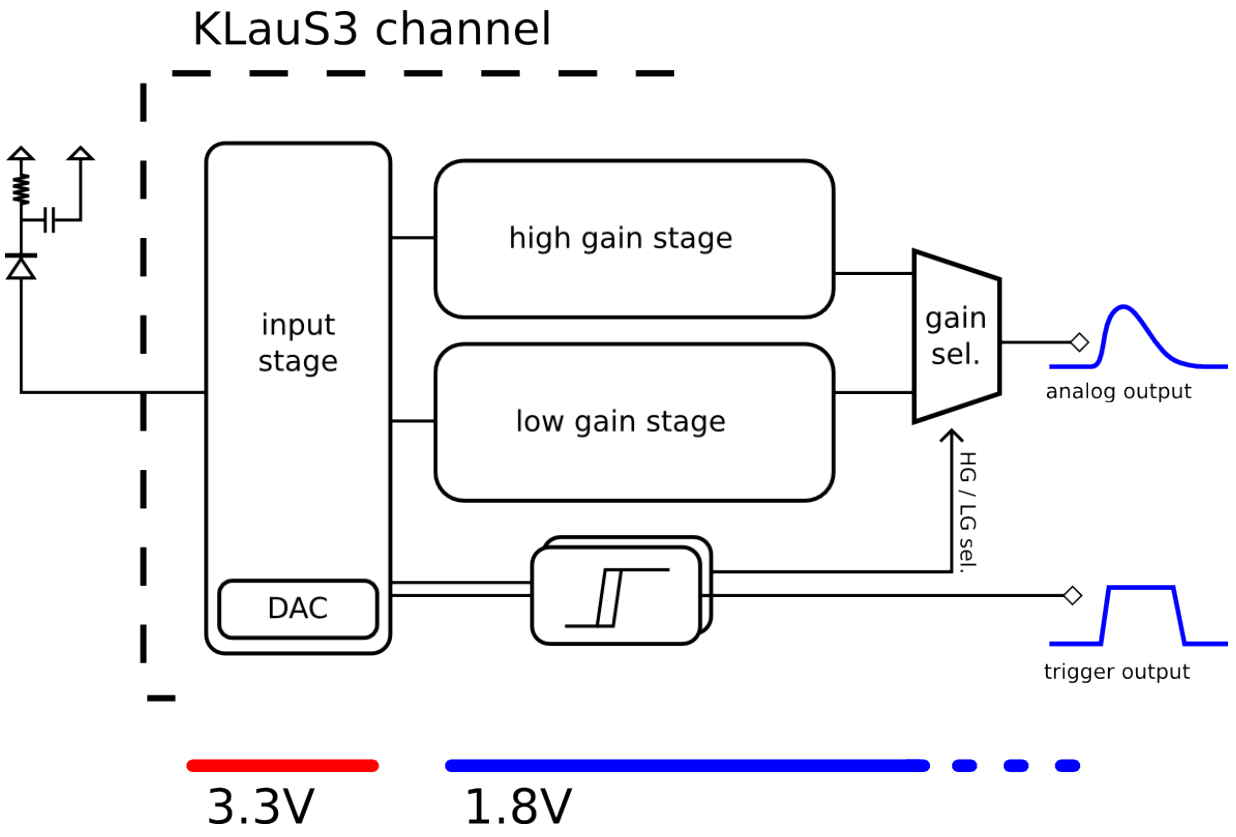


[KLauS3.0 – frontend & ADC]



[KLauS3.0 test setup]

Front-end: Blocks



[Channel front- end blocks]

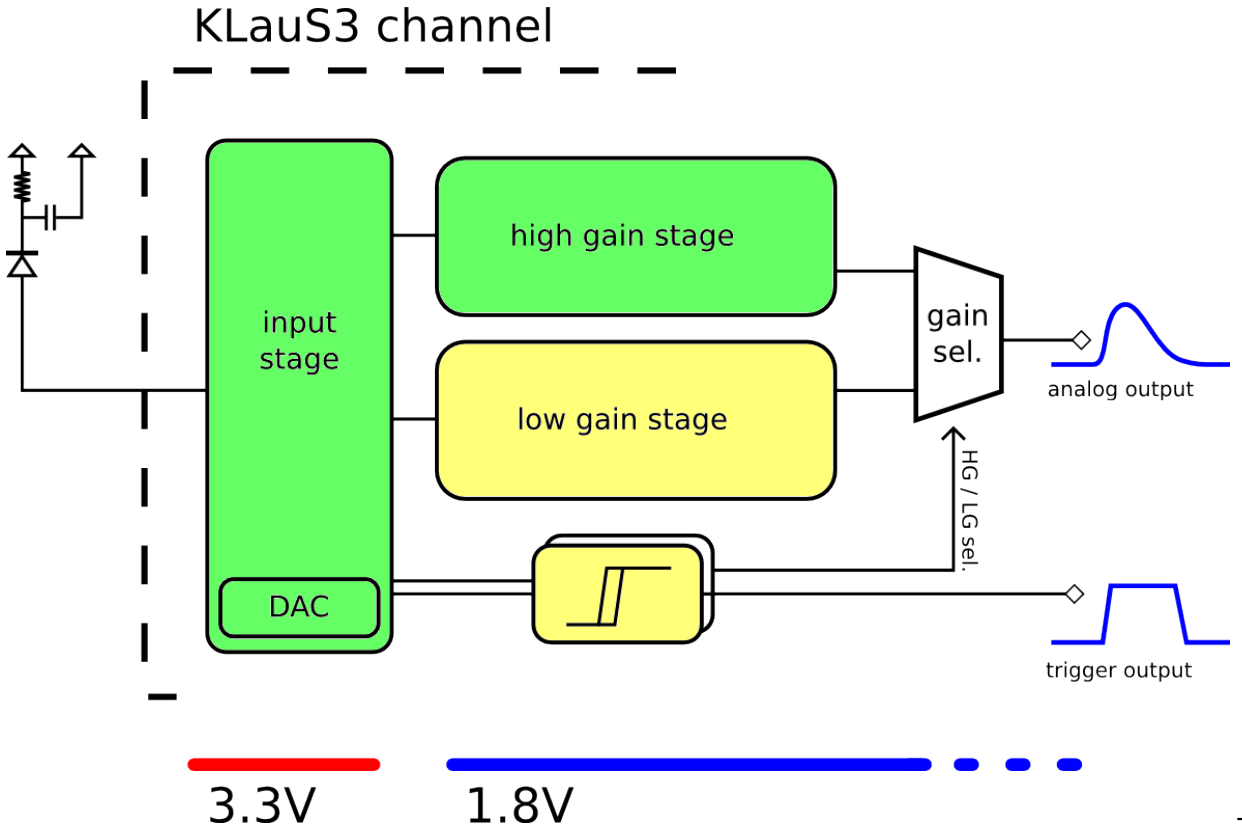
Input stage:
- Low input impedance
- SiPM bias voltage DAC

High gain stage:
- Single pixel spectra
- O(10ths of pixels)

Low gain stage:
- Full SiPM dynamic range

2 **Trigger** branches:
- Event trigger
- HG/LG selection

Front-end: Blocks



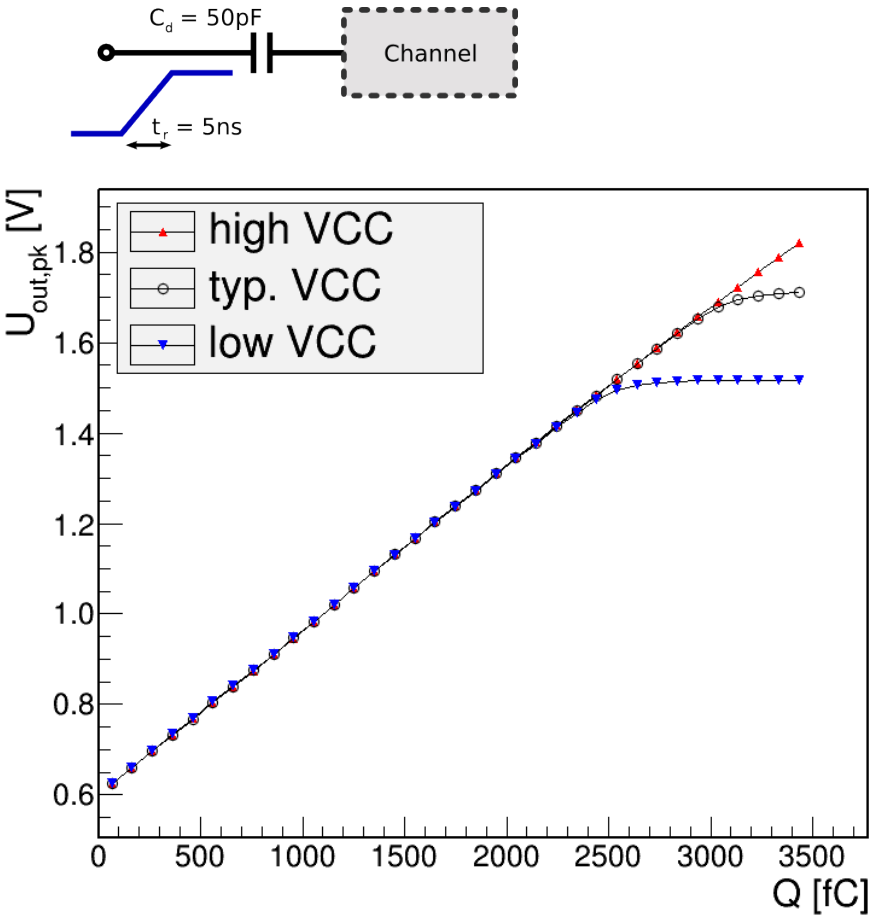
[Channel front- end blocks]

State of implementation

- Miniasic submission in March
- Miniasic submission in May
- Planned for next Submission (Schematic finished)

→ **After validation:**
Ready for combination with ADC

Linear range vs. VCC (High gain)



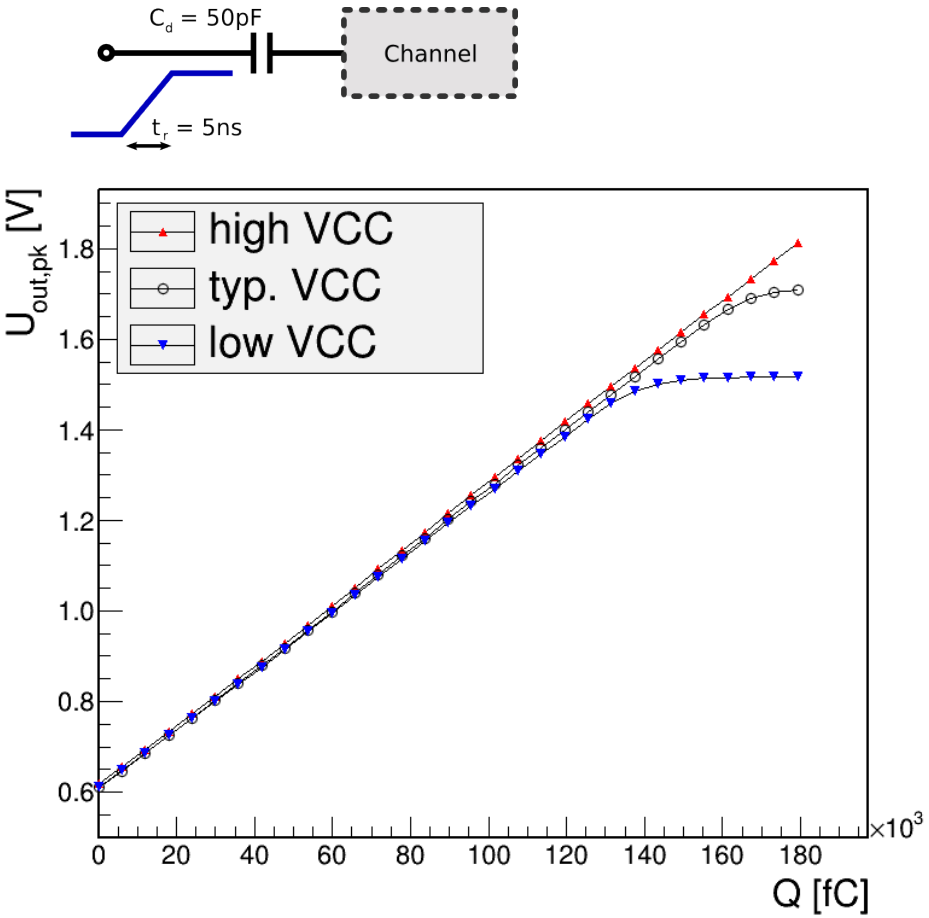
Charge injection measurements
Cd=33pF

Linear range @ max INL = 1%:
≈ 2.8pC

Voltage drop in supply lines expected

→ Check linearity for **different VCC**
"LL" corner: VCC18=1.6V ; VCC33=3.1V
"TT" corner: VCC18=1.8V ; VCC33=3.3V
"HH" corner: VCC18=2.0V ; VCC33=3.5V

Linear range vs. VCC (Low gain)



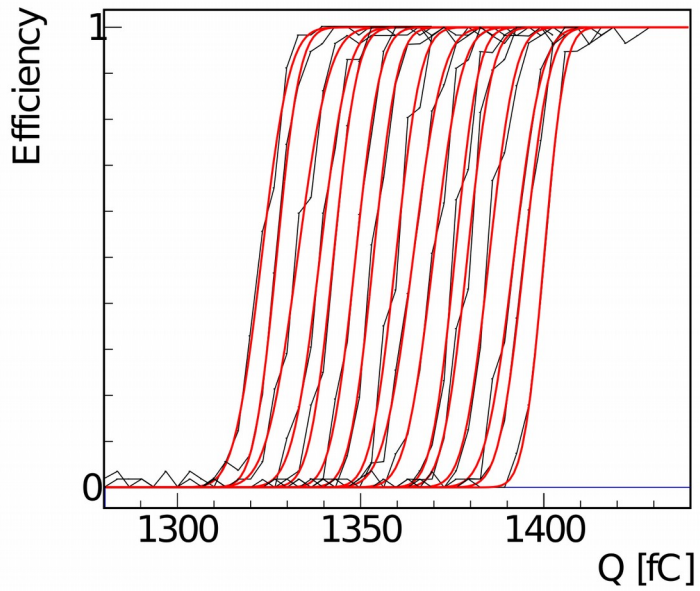
Charge injection measurements
Cd=33pF

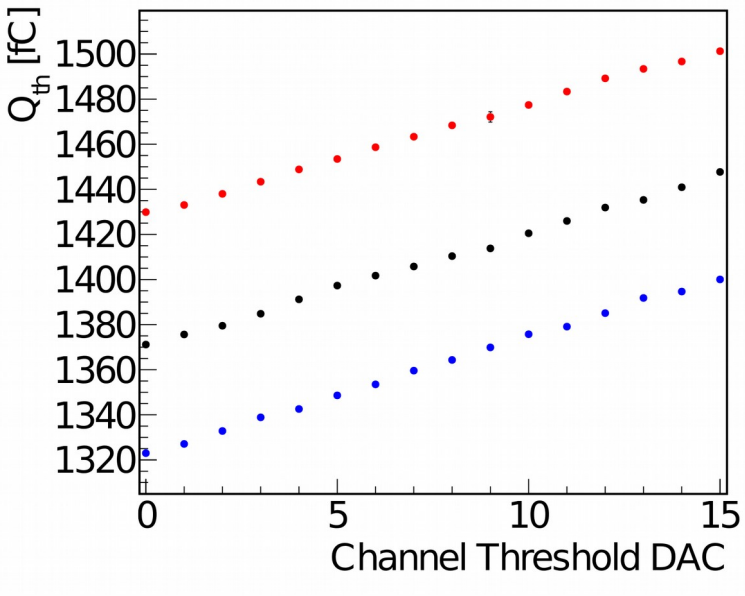
Linear range @ max INL = 1%:
≈ 160pC

Same VCC corners
Again changed linear range with VCC18

Small gain & pedestal change
→ To be investigated

Trigger branch: Threshold setting



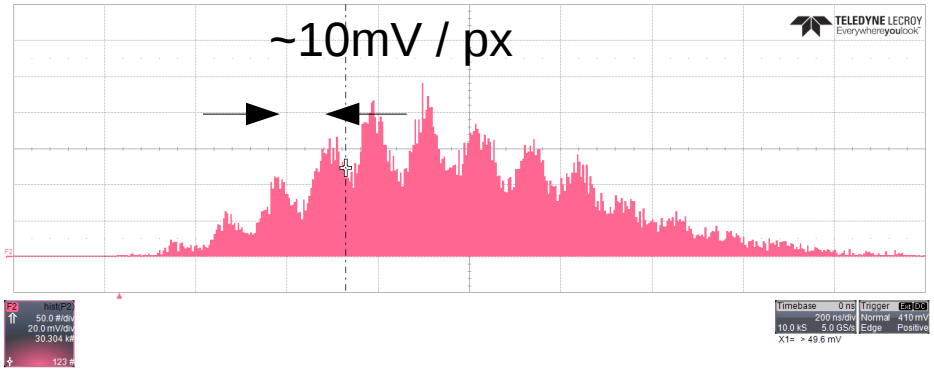


Two DACs to tune threshold:
- Global 6 bit DAC + scaling bit (for all channels)
- 4 bit DAC for fine-tuning (each channel)

→ Charge noise: 8fC typ.
→ Threshold configuration resolution (4b DAC): 5fC

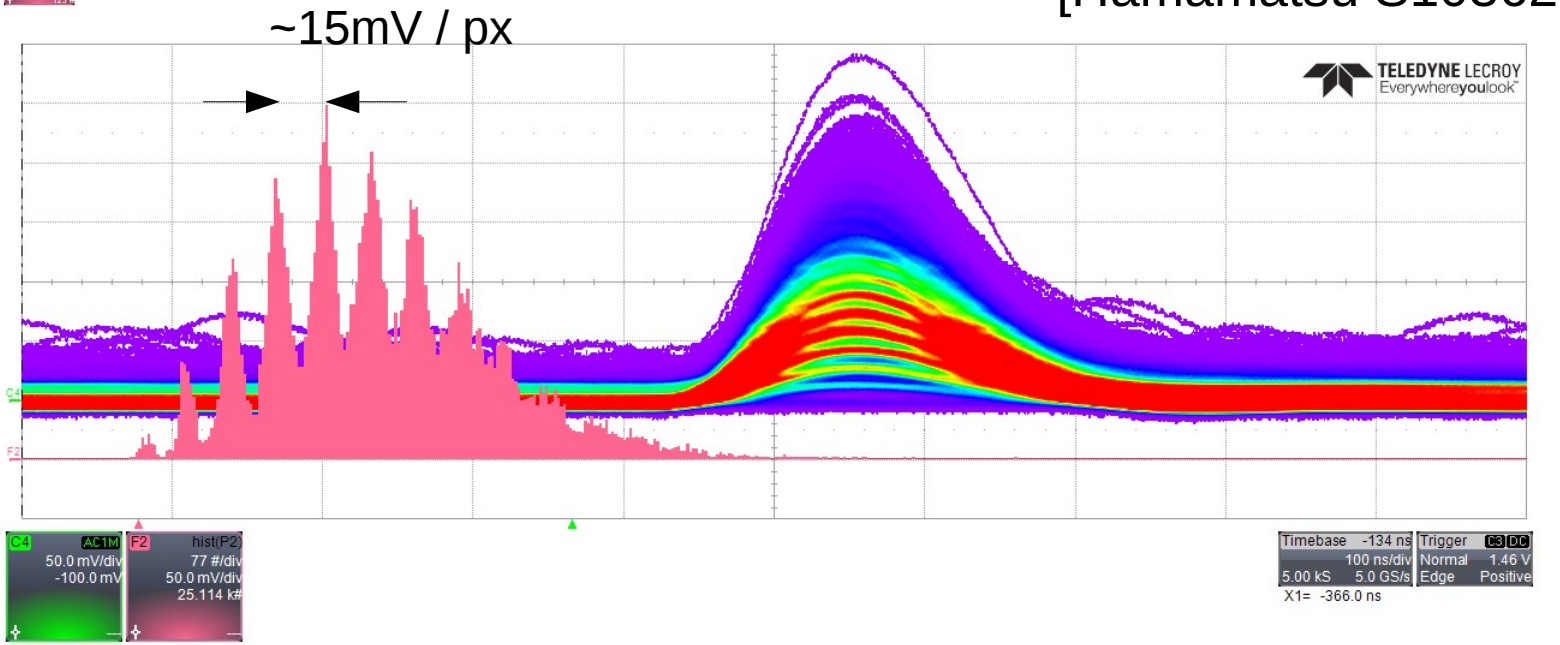
Front-end measurements: test with sensors

Two SiPM models tested



10µm pixel device [Gain ~1.5x10^5]
[Hamamatsu S12571-010C]

25µm pixel device [Gain ~2.75x10^5]
[Hamamatsu S10362-11-025C]

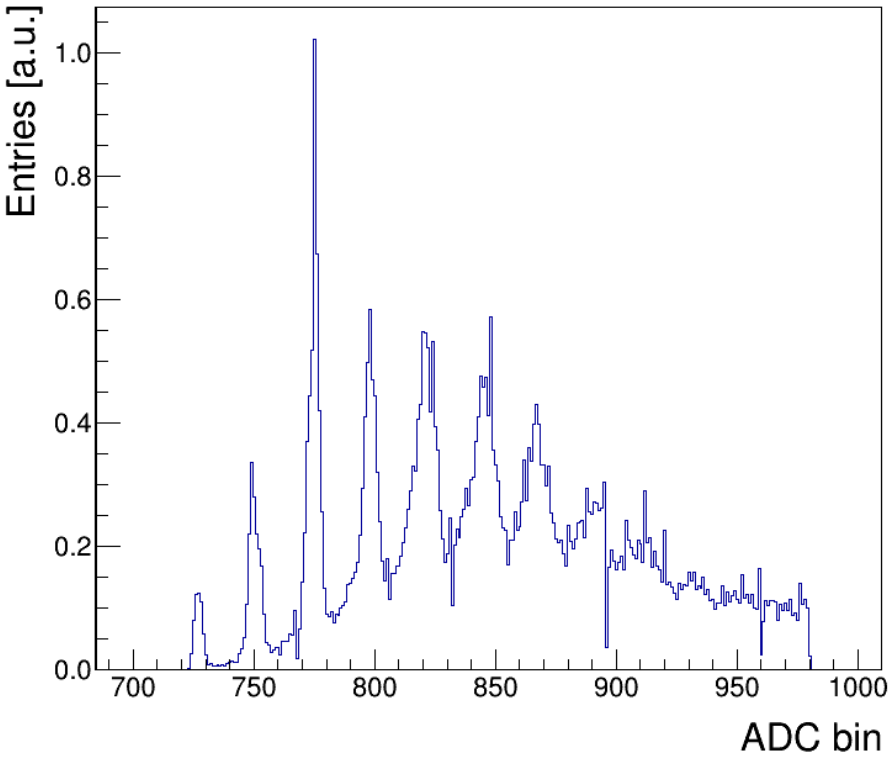


Front-end & ADC

Combined operation:
Connect front-end & ADC on PCB level (same chip)

ADC response in 10bit quantization mode

Large gain (50um pixel) SiPM used
- Simple DNL correction
- (not free of remaining effects)
- → Visible spectrum



ADC: Pipeline (SiPM calibration) mode

Previous meeting:

ADC linearity in 10 bit mode

12 bit (SiPM calibration) mode not Accessible due to bug in digital part

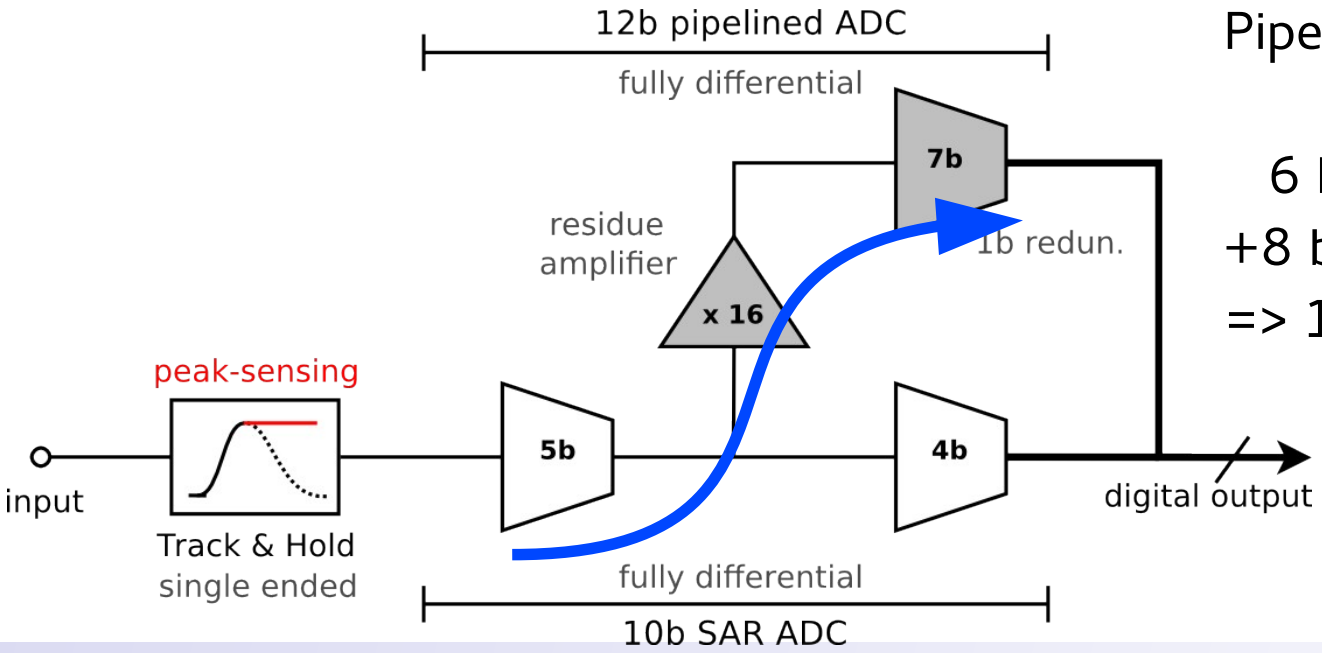
Updated version (2nd submission):

Pipeline stage working:

6 bit from 1st stage

+8 bit from 2nd stage

=> 12bit quantization *(2 bit redund.)*



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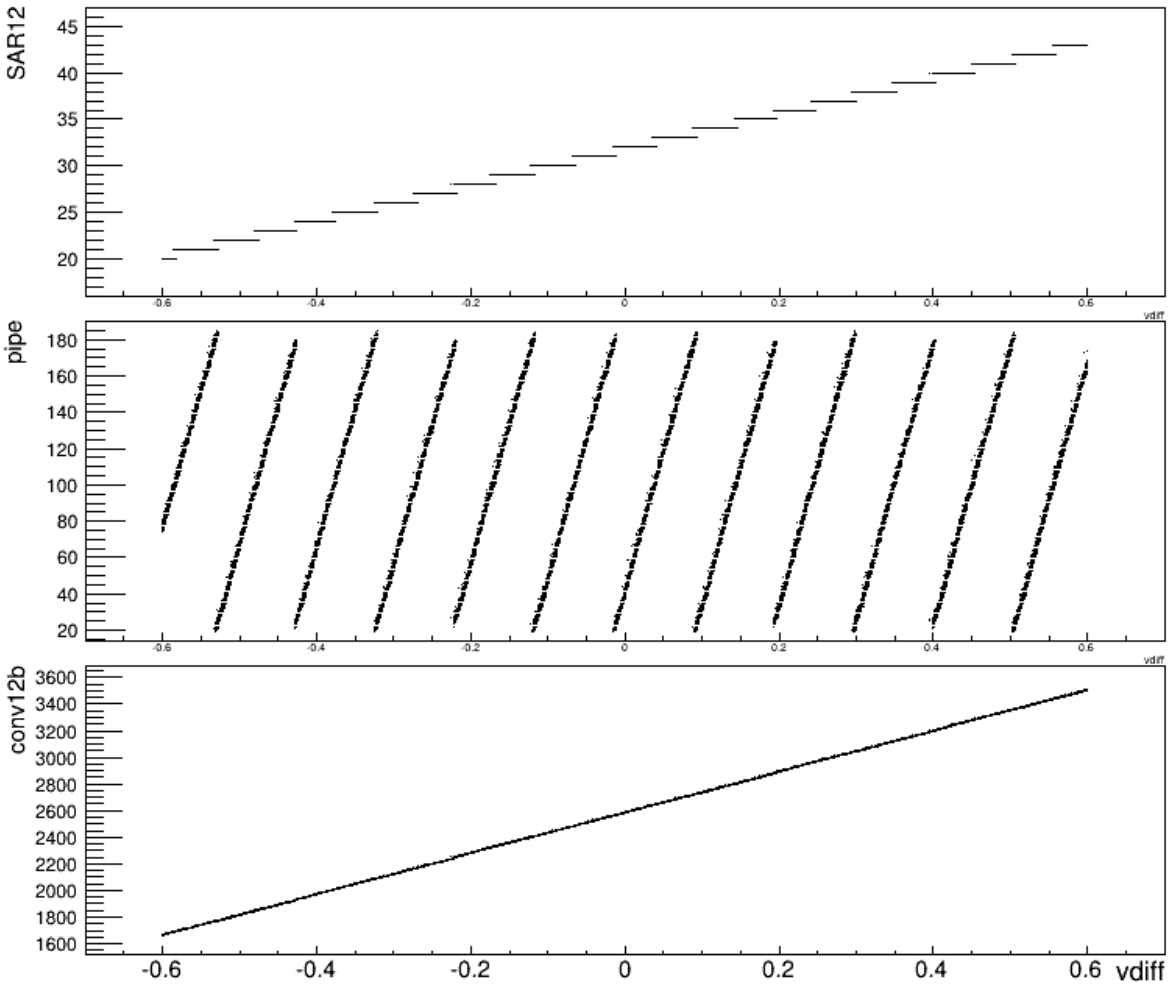

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Pipeline stage working:

6 bit from 1st stage
+8 bit from 2nd stage
=> 12bit quantization *(2 bit redund.)*

Some analysis to be done to estimate nonlinearities

Summary & Plans

KLauS in new technology

Two protoypes submitted and tested

ADC: working in 12b mode

Front-end: Most blocks implemented & characterized

- 2V SiPM bias tuning (last meeting)
- Good linearity
- Visible single pixel spectra for 10um SiPMs

→ Encouraging results to go for multi-channel ASIC

Next version planned

≤12 channels:

Front-end & ADC + Digital, combined simulation in place

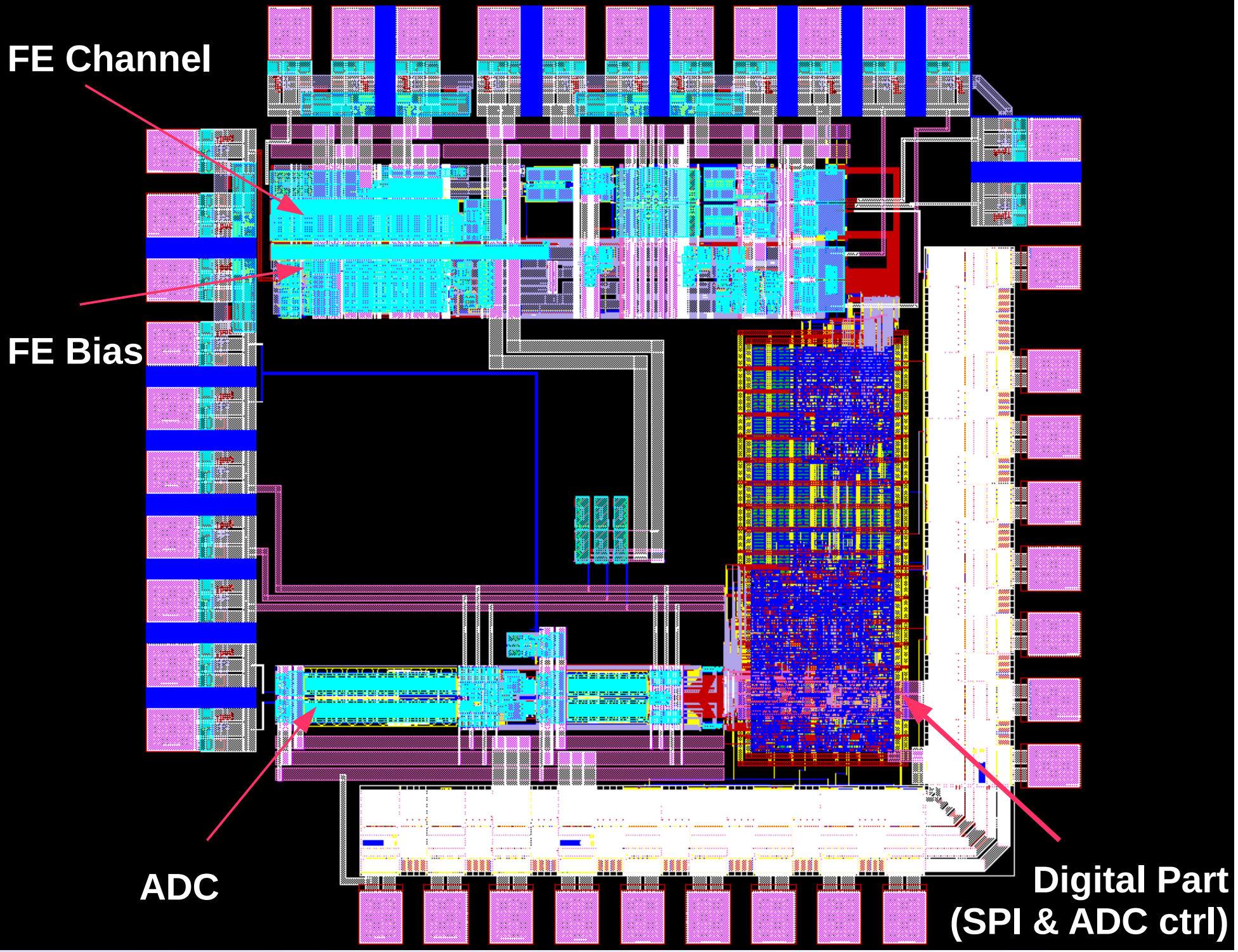
TDC development will be staged:

coarse counter (~50ns binning, 16b) in next version

Submission: March '16

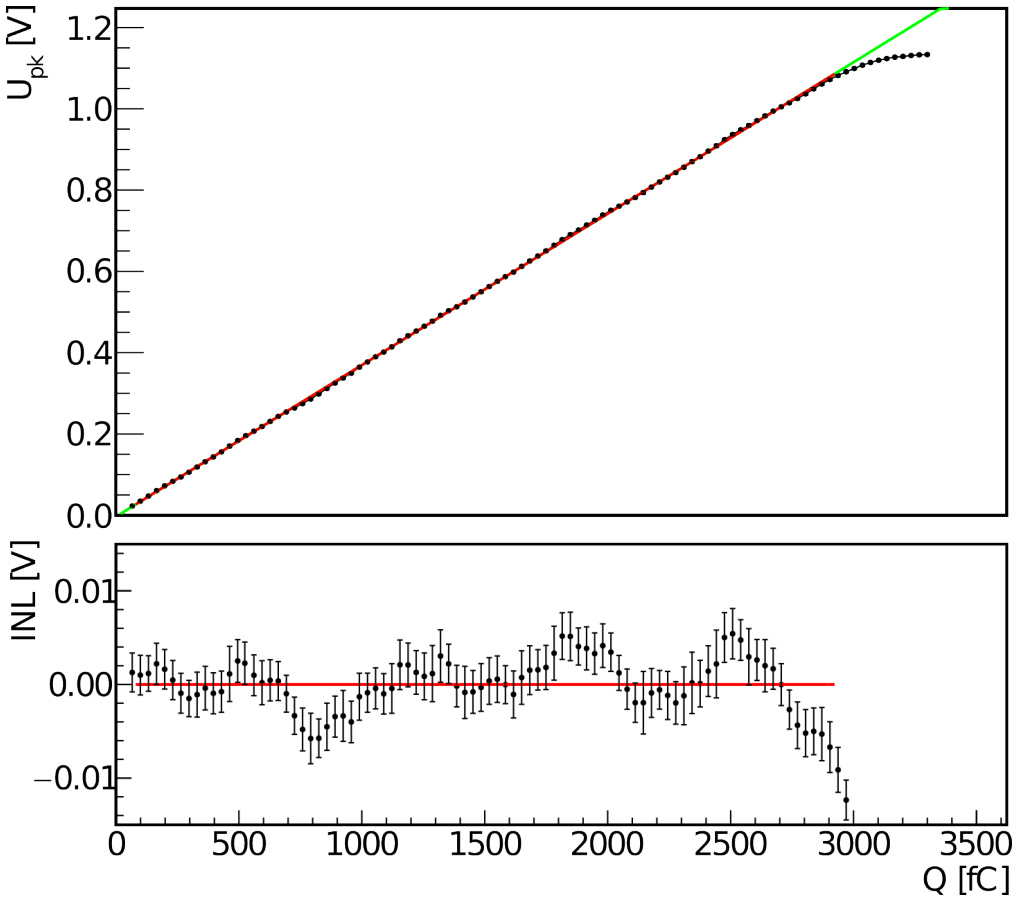
Thank you!

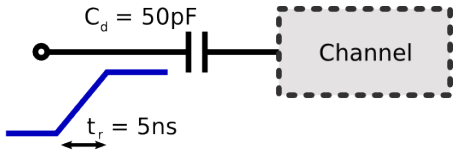
Backup



[Layout of the 1.5x1.5mm miniASIC]

HG stage: Linearity (Fine scan)





Charge injection measurements

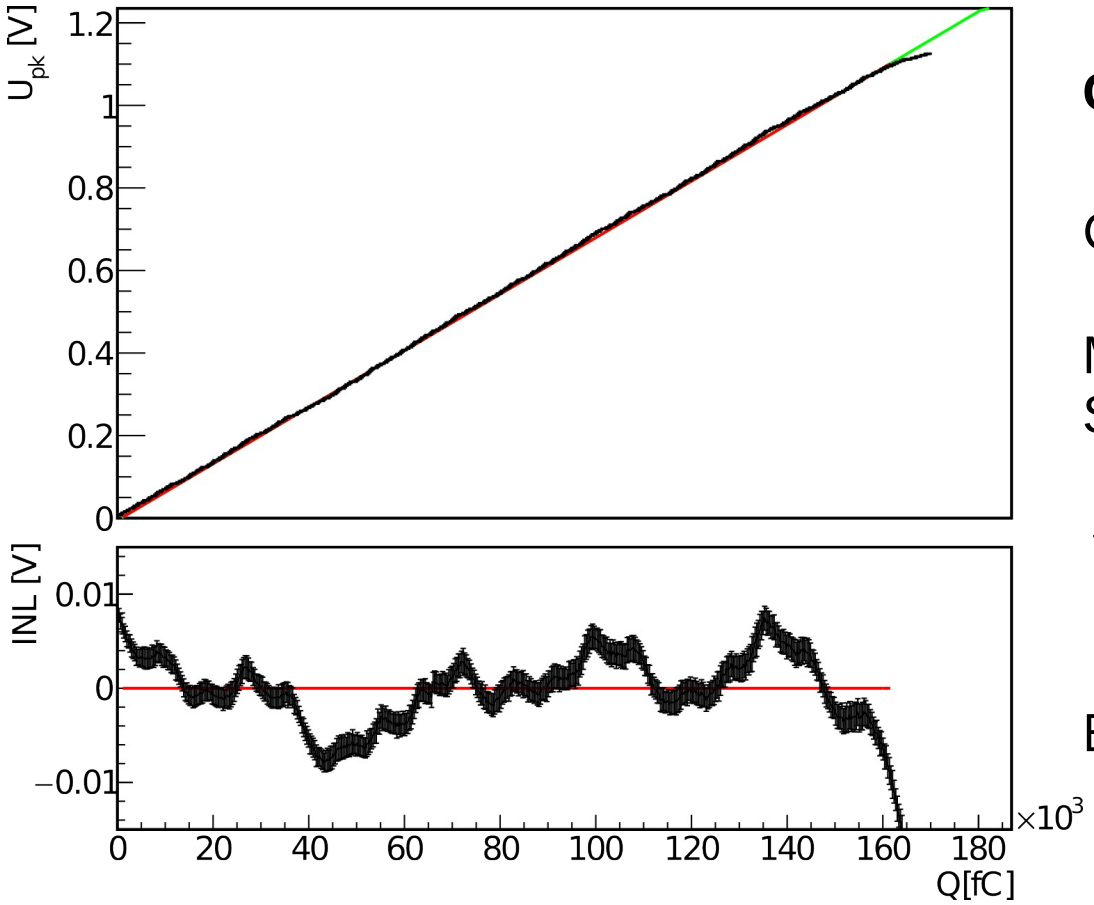
Cd=33pF

Measure Peak voltage – Pedestal
Scope (8b, some nonlinearity from this)

→ Linear range @ max INL = 1%:
2.8pC

Nonlinearities when reaching VCC18
Other nonlinearities seem to come from scope

LG stage: Linearity (Fine scan)



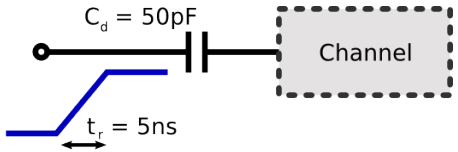
Charge injection measurements

Cd=33pF

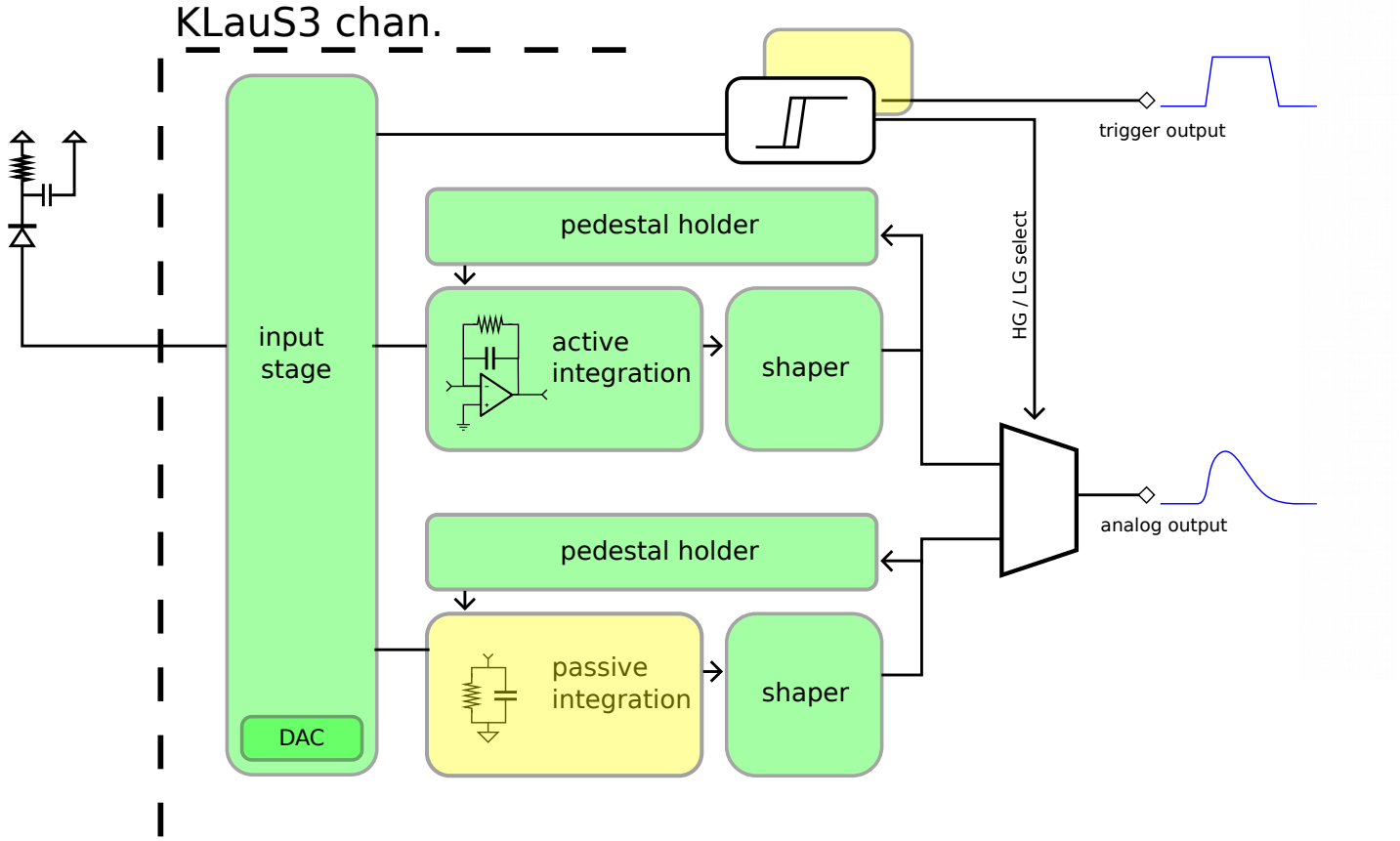
Measure Peak voltage – Pedestal
Scope (8b, some nonlinearity from this)

→ Linear range @ max INL = 1%:
160pC

Expected from simulations: > 140pC



State of implementation



Miniasic submission in March

Miniasic submission in May

Planned for next Submission (Schematic finished)