CERN TB'2015 data analysis

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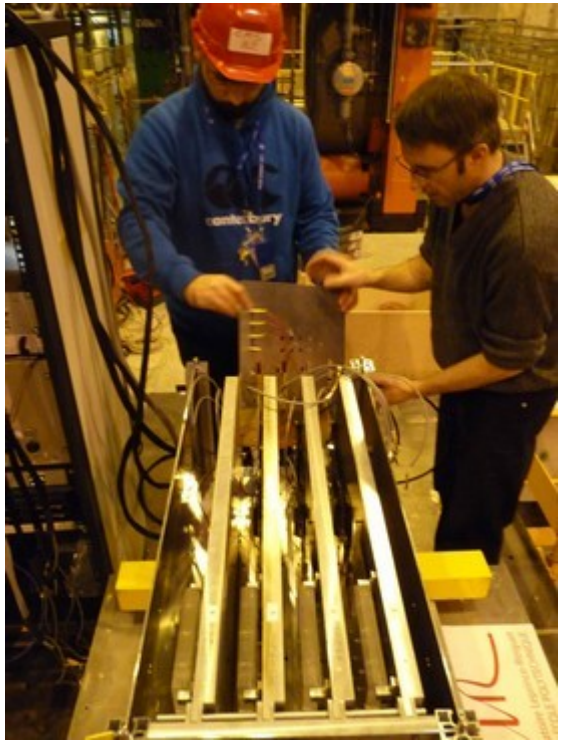
Outline

1. Experimental setup
2. Running conditions
3. Bugs and features
4. Pedestals
5. Plans



Online resources, manpower

1) Twiki:
https://twiki.cern.ch/twiki/bin/view/Main/SiW-ECAL
In particular:
https://twiki.cern.ch/twiki/bin/view/Main/SiWECALAnalysis

2) TB e-log: https://llrelog.in2p3.fr/calice/
User: ecal Password: calice

3) Weekly analysis meetings (together with CMS participants):
first meeting
https://indico.in2p3.fr/event/12487
use arrow left/right buttons on top to navigate through all meetings .

15 participants in the first meeting; by now less, though
Active contributors:
Andreas Psallidas (National Taiwan University, CMS) – developing GEANT4 MC simulation, repository: https://github.com/apsallid/SiWEcal
Very useful contribution, very advanced and can already be used!

Kostya Shpak – next talk
V.B. - this talk

Sandhya Jain, Shilpi Jain – started to look at the data, willing to contribute

Running conditions

4 layers ready for TB and put in the setup, the last layer was not operational and was not used.
Position of layers: beam → DIF1, DIF2, DIF0
Markers on Al plates from photo: beam → ASU 23, 43, 42, 34 or numbers 4, 5, 3, 2 (last not used).

Connection to adaptor board and HV using springs (temporary solution until reliable soldering realized in LAL).

Each layer had 4 x 256 pixels / channels.

All layers were always power pulsed. Several spill settings tried, mainly long spills (eg. 200 + 50 msec = data taking + readout, dead time) to increase statistics with SPS spills of a few seconds, so, effectively corresponding to quasi-continuous mode.
Also, some special runs with short spills 2.5 + 247.5 msec.
Here, 2.5 = 0.9 + 0.5 + 1.1 msec =
(delay before BX=0) + (1250 empty, dead BX) + (2750 BX with data),
roughly corresponding to ILD power pusling mode. Such a spill allowed unique coding of BX number with 12 bits (1250+2750 = 4000 BX).

No problems with configuration of the setup.

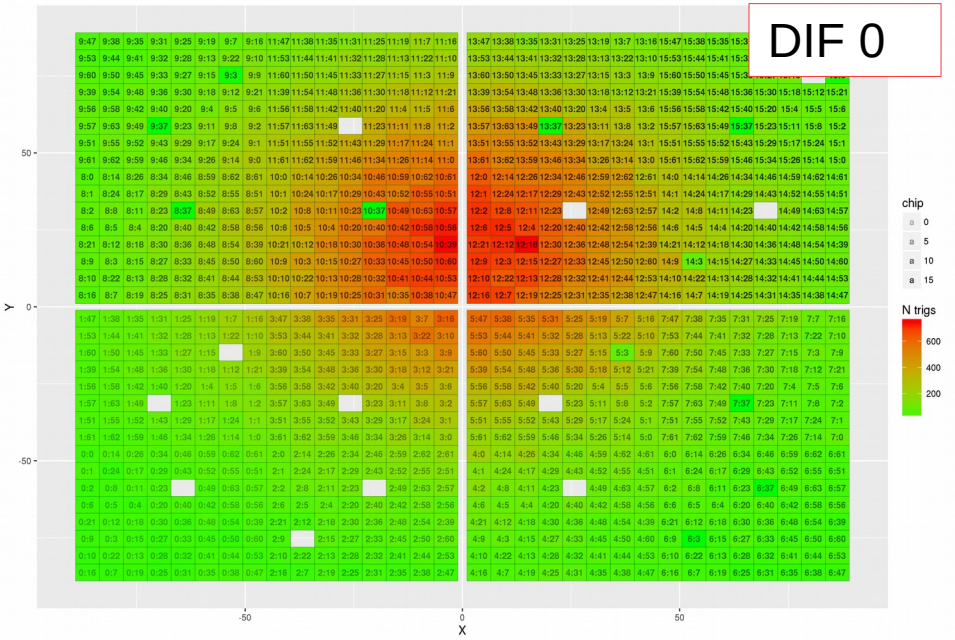
All data have been taken with feedback C=1.2 pF (nominal value is 6 pF).
This gives 5 times higher gain and (not one would expect, though well established) better S/N, but lower dynamic range (more comfortable running but not nominal).

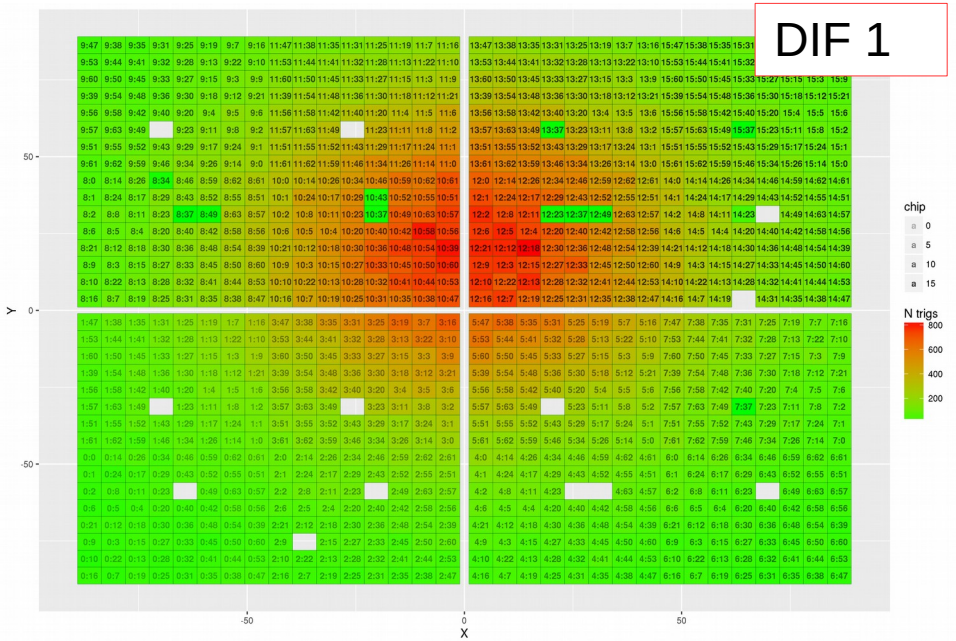
Selected trigger threshold = 230, much better than in cosmic runs one year ago (290), but slightly more than 220 in cosmic runs in 2013 of previous PCB FEV8.

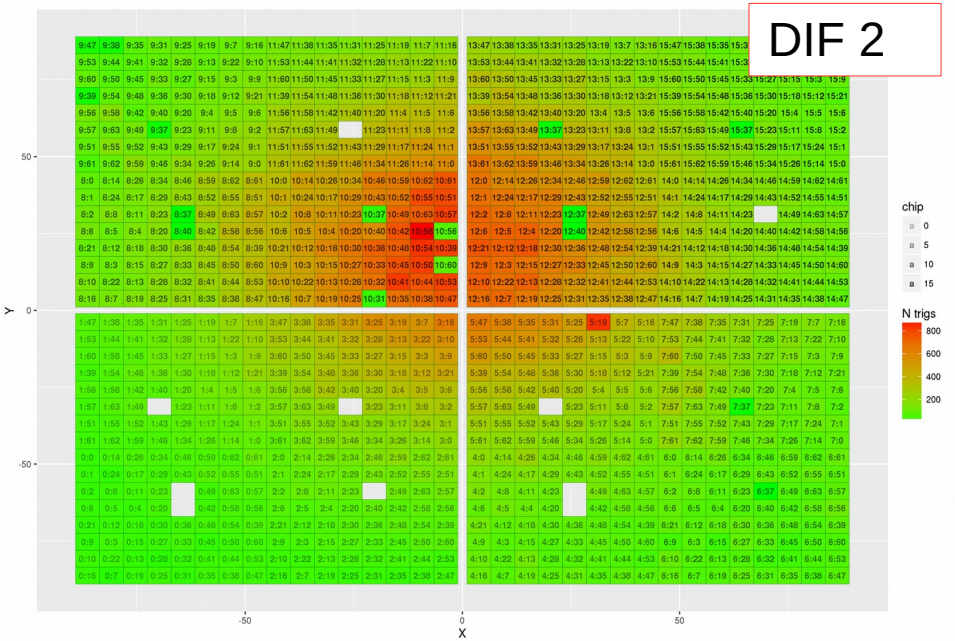
Running conditions

Masking:
DIF0: 18 channels out of 1024
DIF1: 22
DIF2: 28
In total: **2.2% of all channels.**

Muon beam spots (X-Y distribution of
N triggers, requiring ADC-pedestal>10)
from typical muon run 361 as example



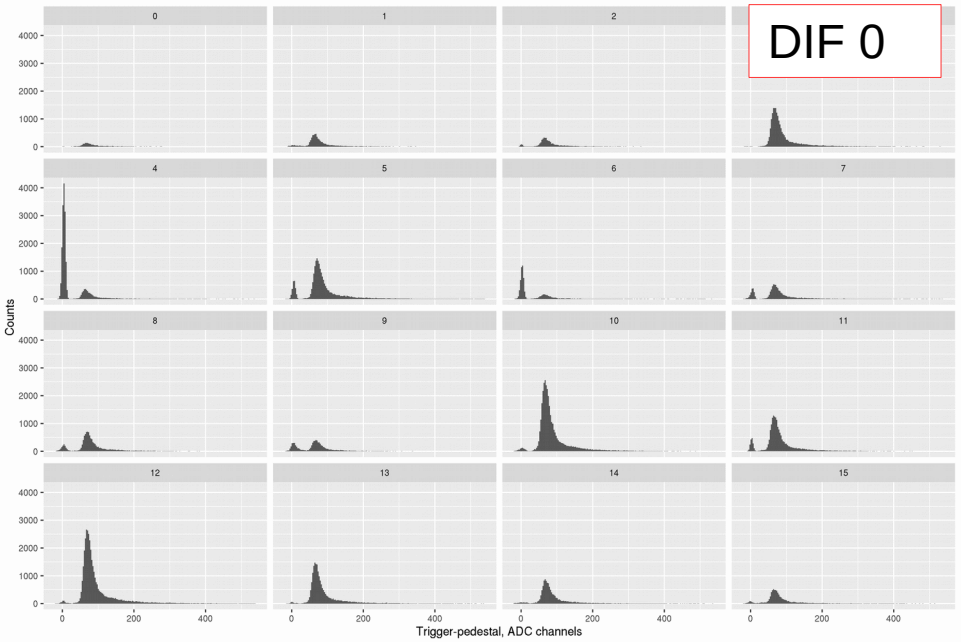




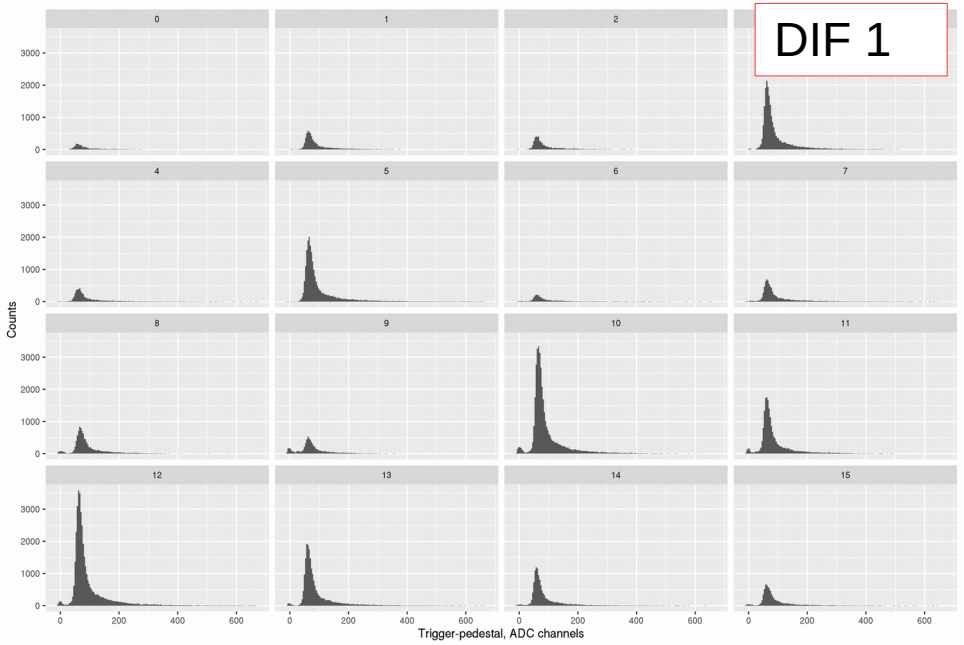
Running conditions

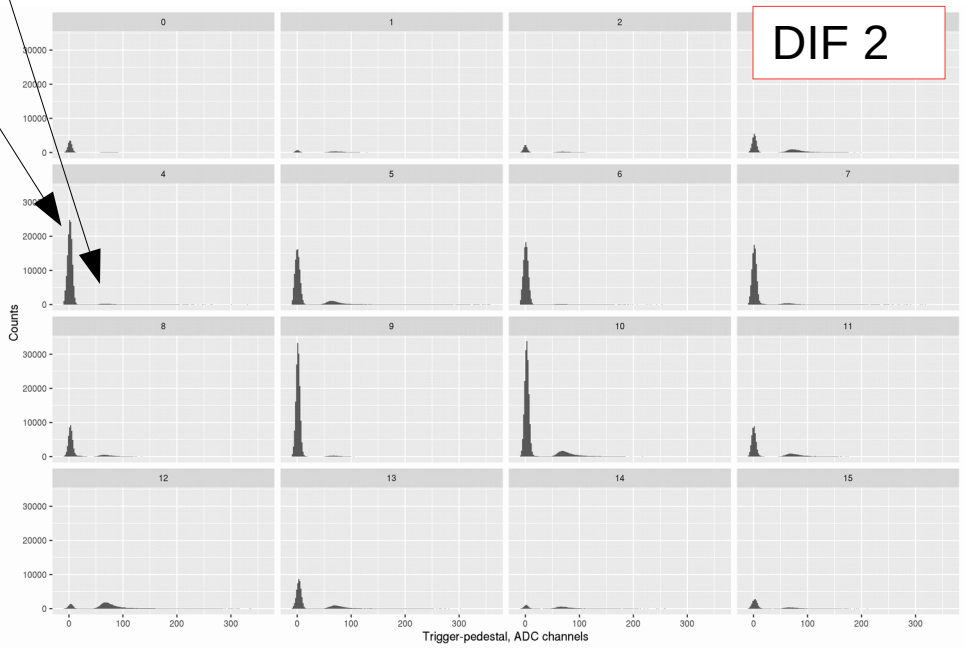
Nice MIP signals

DIF2 always had the largest fraction of noise hits at zero (after pedestal subtraction).



Noise MIP

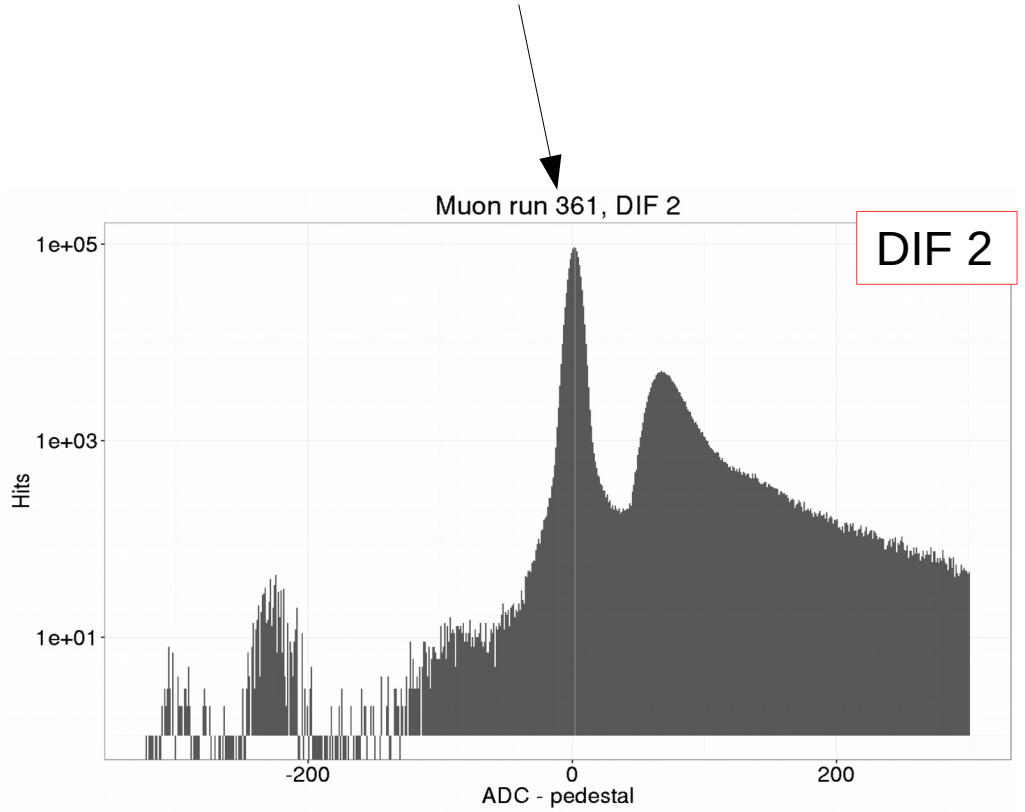


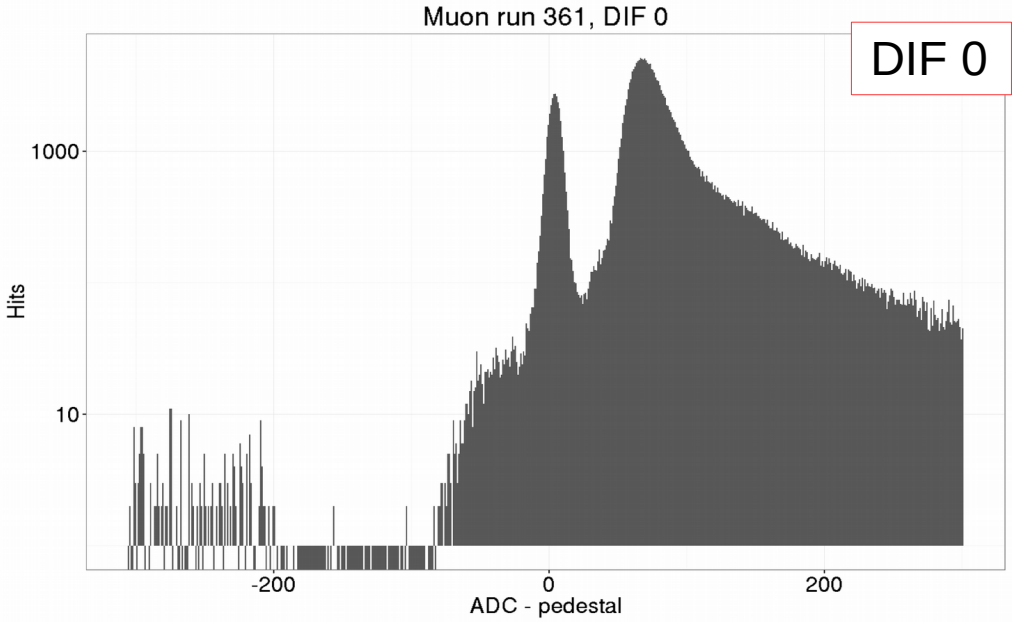


Running conditions, noise in DIF 2

(ADC – pedestal) in DIF 2 and DIF 0 for comparison (DIF 1 is even better), all channels combined, log Y-scale.

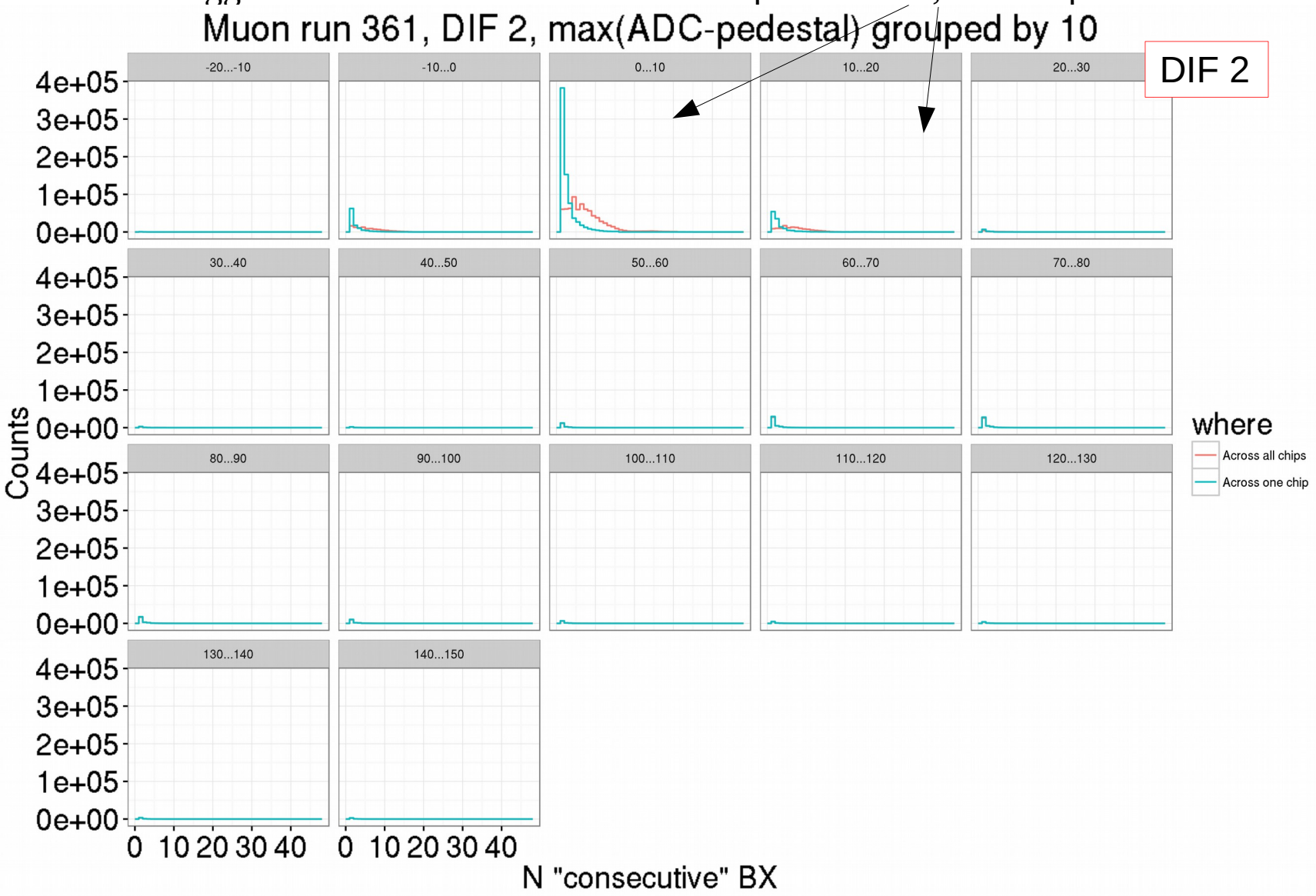
Where peak at zero comes from?





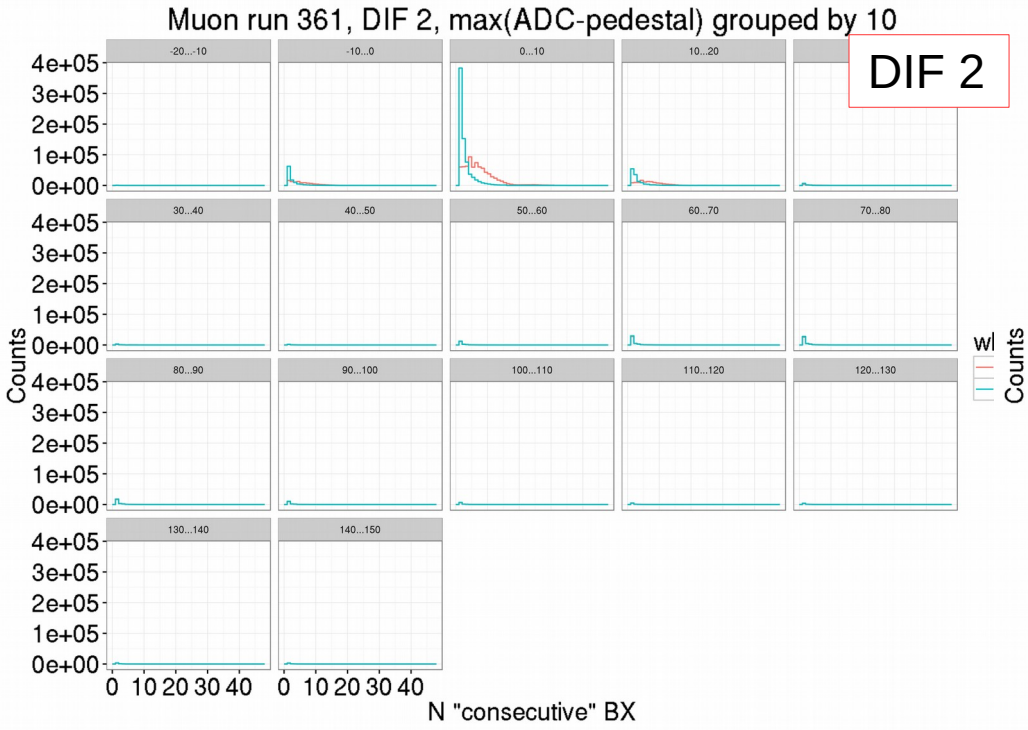
Running conditions, noise in DIF 2

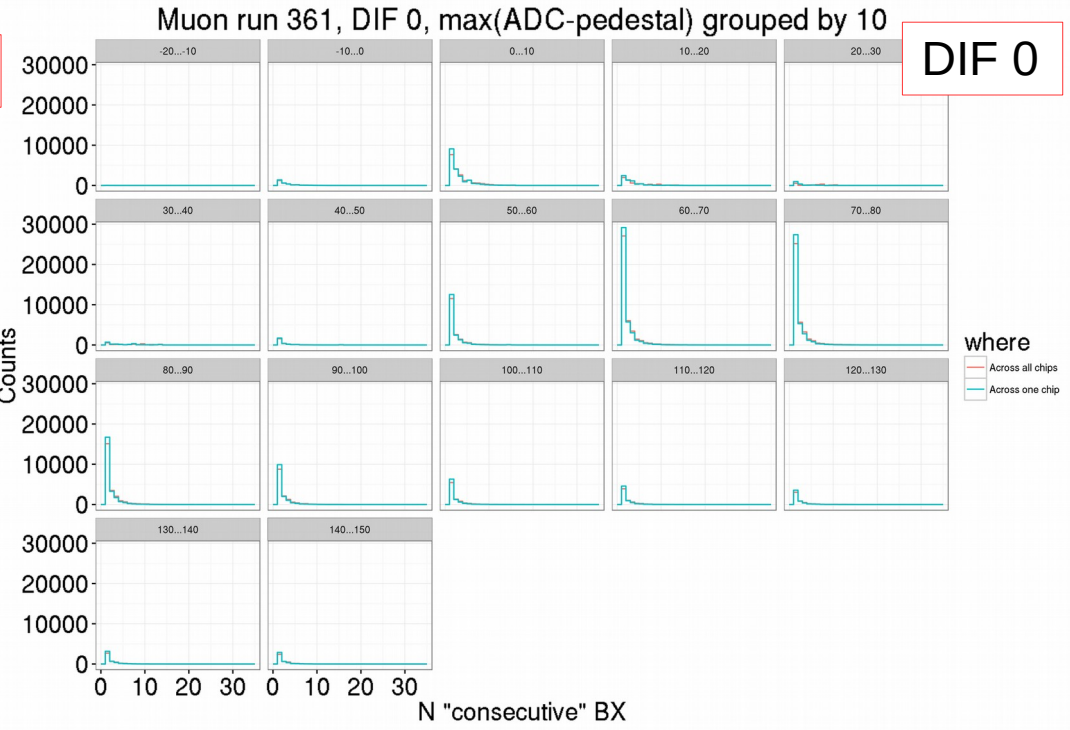
Max.A = Maximal triggered (ADC-pedestal) is selected in event, events are grouped according to Max.A / 10, ie. -20..-10, -10..0, 0..10, … . Here, N “consecutive” BX is plotted in every group. BX, BX+1, BX+2, … clustering is done either across all chips (when BX's from all chips are combined, red) or across single chip only, blue. If there is a deviation between red and blue, the chips are not independent and retrigger in common. This is the case for peak at zero, and the peak is due to retriggers.



Running conditions, noise in DIF 2

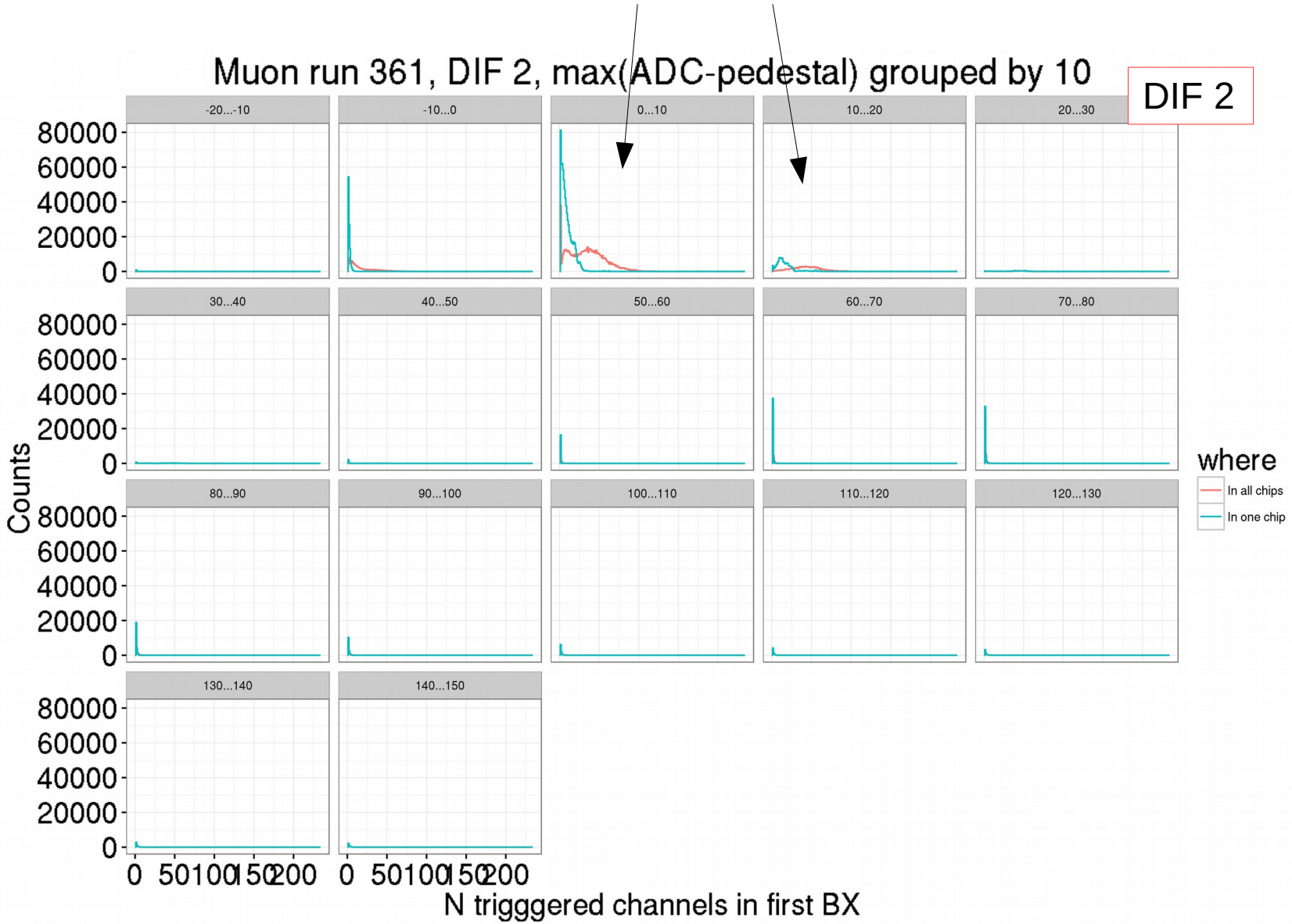
Comparison between DIF2 and DIF0. In cleaner DIF0, retriggers are not yet fully developed (they mainly stay below threshold), so peak at zero is smaller than muon MIPs. When we tried to reduce the threshold from 230 to 220, the peak at zero became dominant in all DIFs, so it was impossible to work.
Conclusion: the reason why triggered thresholds can not be lowered, are retriggers.





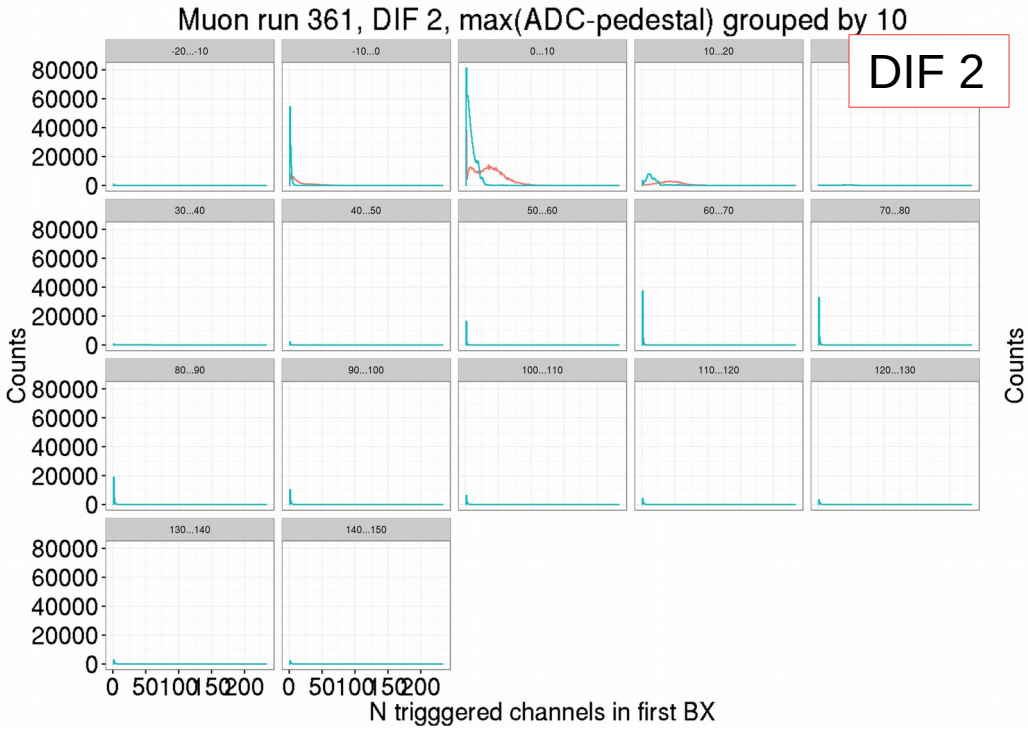
Running conditions, noise in DIF 2

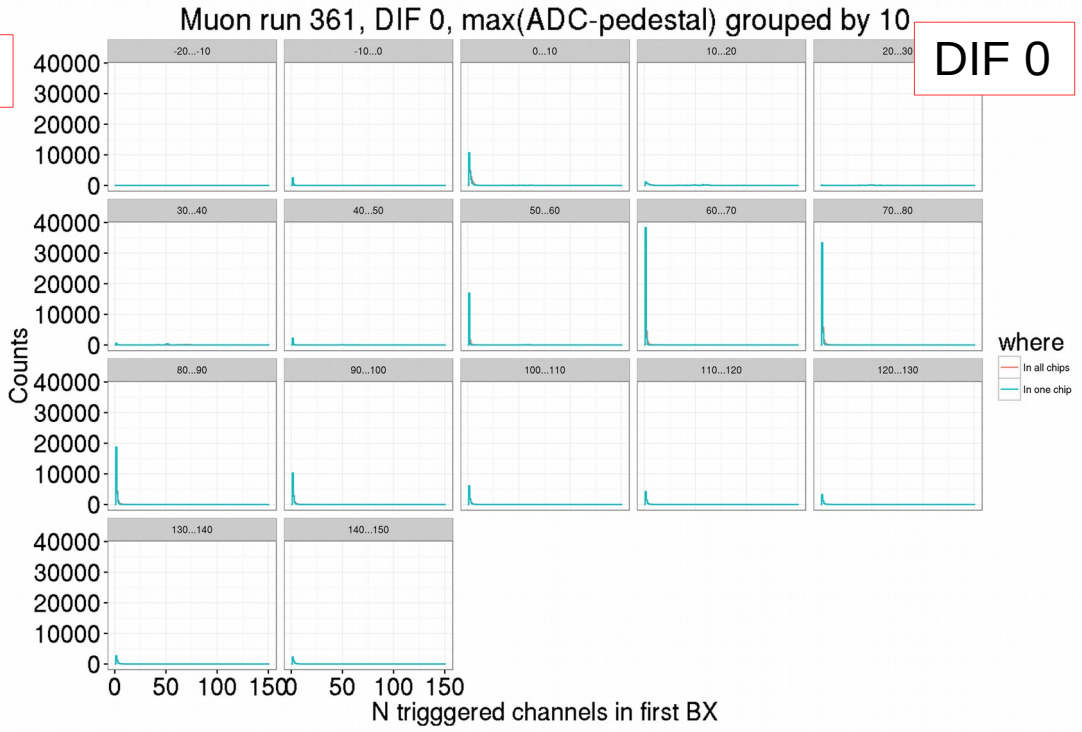
Number of triggered channels in first BX event; again, in bints of Max.A = max(ADC-pedestal) variable which distinguishes noise at zero and MIP. Like before, red is when counting triggered channels across all chips, while blue is when counting inside a single chip. Peak at zero is due to retriggered events with many hits, moreover, a cross-talk between the chips (power lines?) is again clearly visible (red!=blue).



Running conditions, noise in DIF 2

Comparison between DIF2 and DIF0 in N triggered channels. Retriggers in DIF0 are not yet fully developed (mainly, below threshold and invisible).





Running conditions, retriggers

Conclusion:

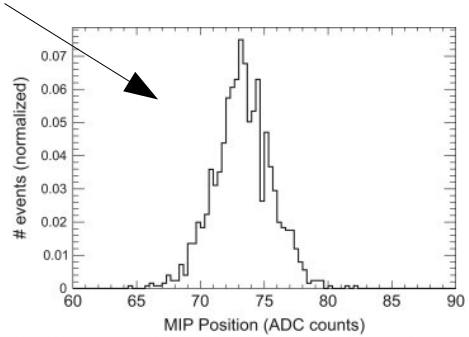
SKIROC has excellent S/N=17..18 (see later). However, retriggers

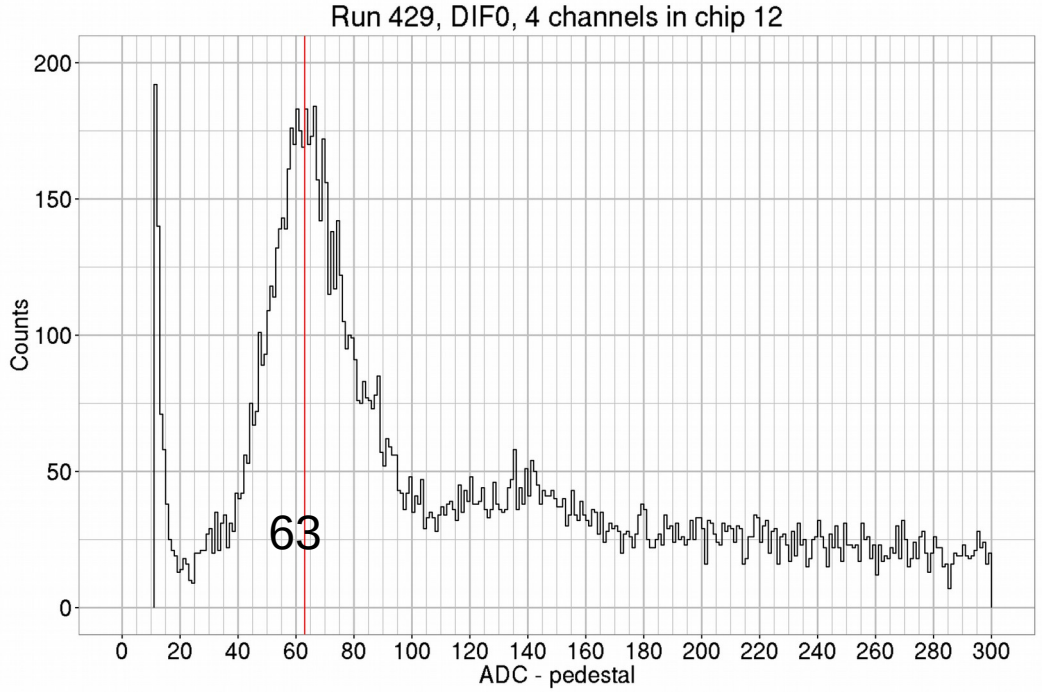
- do not allow to set low trigger thresholds, this is the most critical issue
- introduce dead time in BX+1,+2,…
- fill up SKIROC memory: in relatively “clean” DIF0,1 the retriggers occur after about 25% of events and occupy ≅50% of SKIROC memory.
- when decreasing trigger threshold, peak at zero contains events where chips “talk” to each other during retrigger. This is much less the case after physical events.

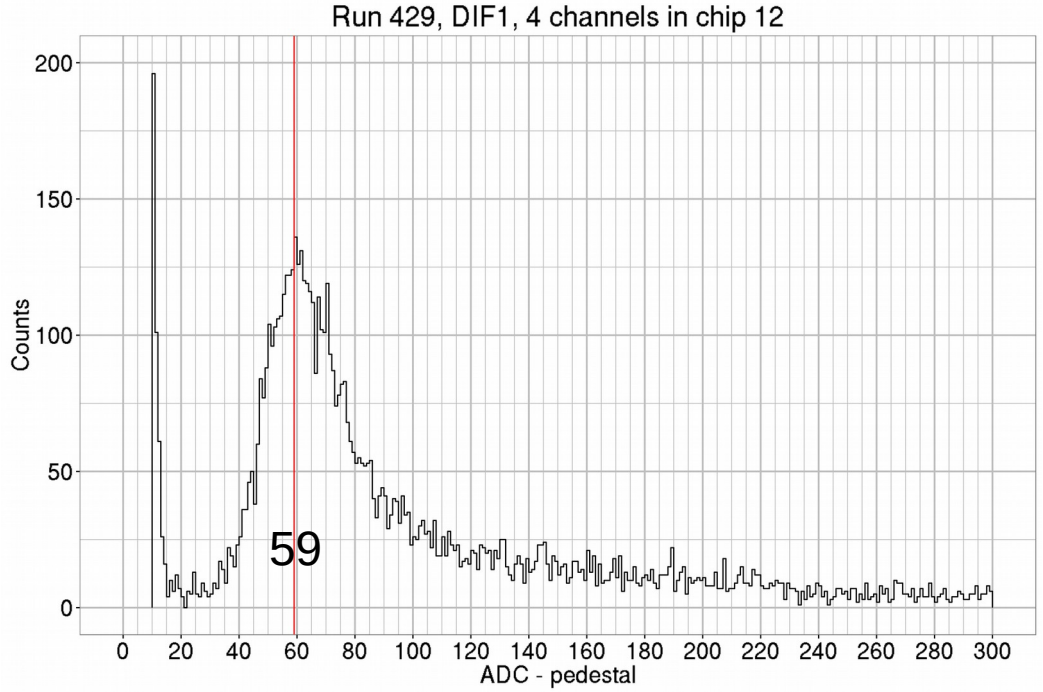
Trigger threshold level

In one run (#429, pions) I've tried to reduce the trigger threshold as much as possible by enabling only 4 central pixels (7,10,16,22) in chip 12 (where beam was centered).
It was possible to run with threshold=200 instead of 230 for DIF 0 and 1. DIF 2 was too noisy.

MIP is rather close to 60 ADC counts, not 73 as in Fig.14 published in NIM A 778, p.78 (2015), analysis from 2012. The latter can be caused by MPV shift due to trigger inefficiency.

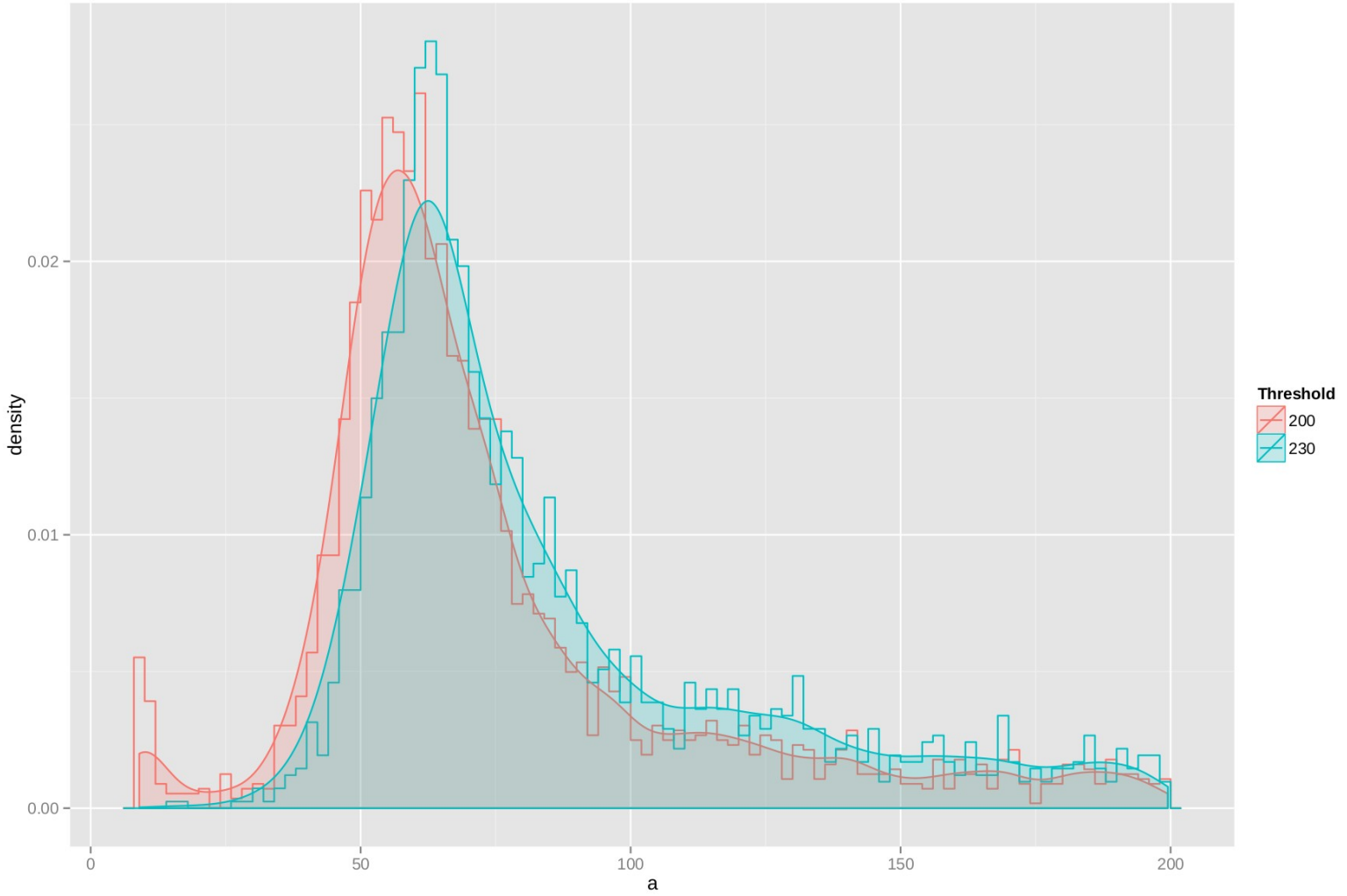






Trigger threshold level

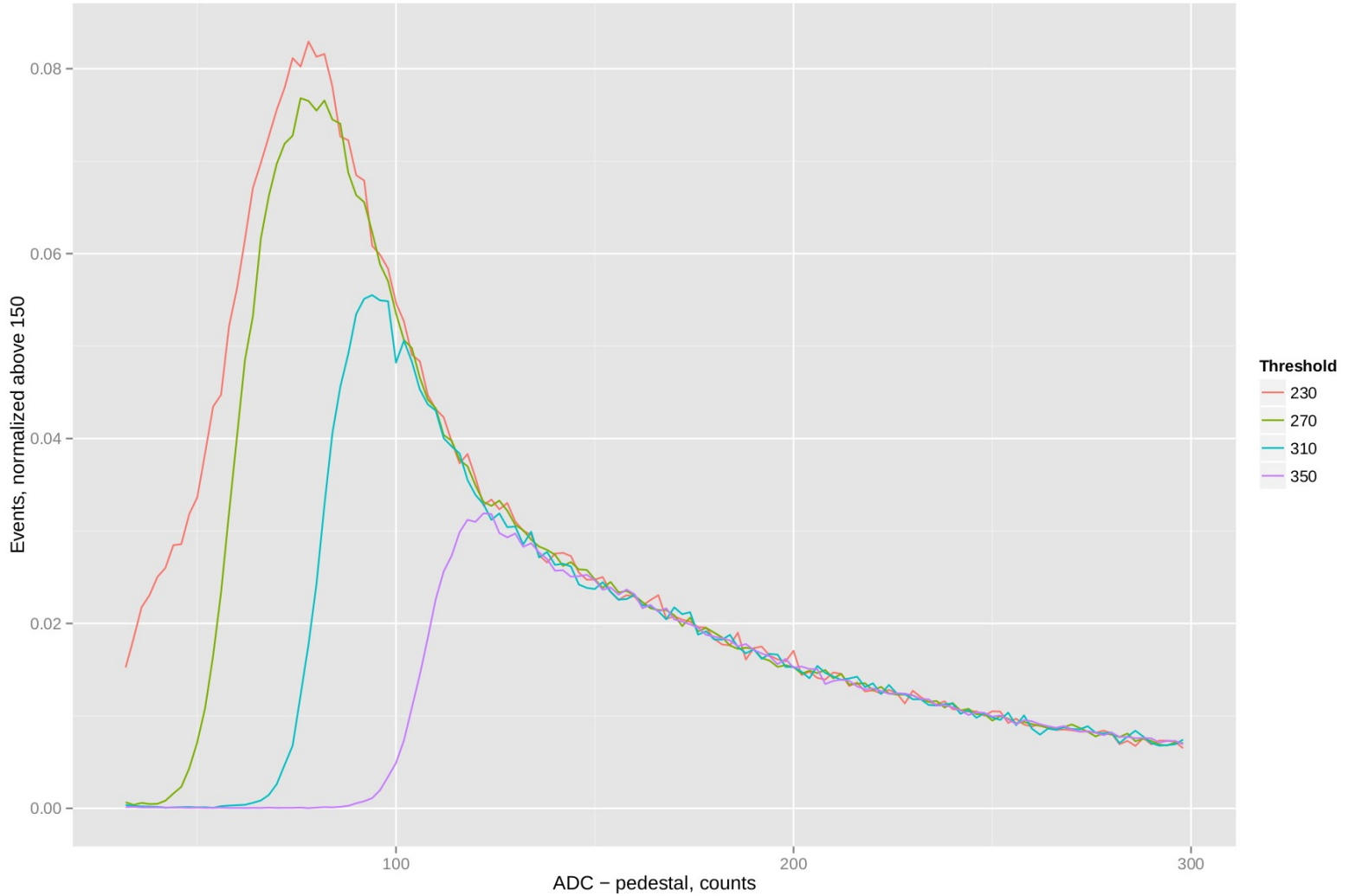
Comparison with the “nominal” trigger threshold 230 (run #423) for DIF1.
Red is normalized sum over the allowed 4 channels in DIF1 @threshold=200,
blue – same 4 channels @ “nominal” threshold 230, from e-log entry 882.



Trigger threshold level

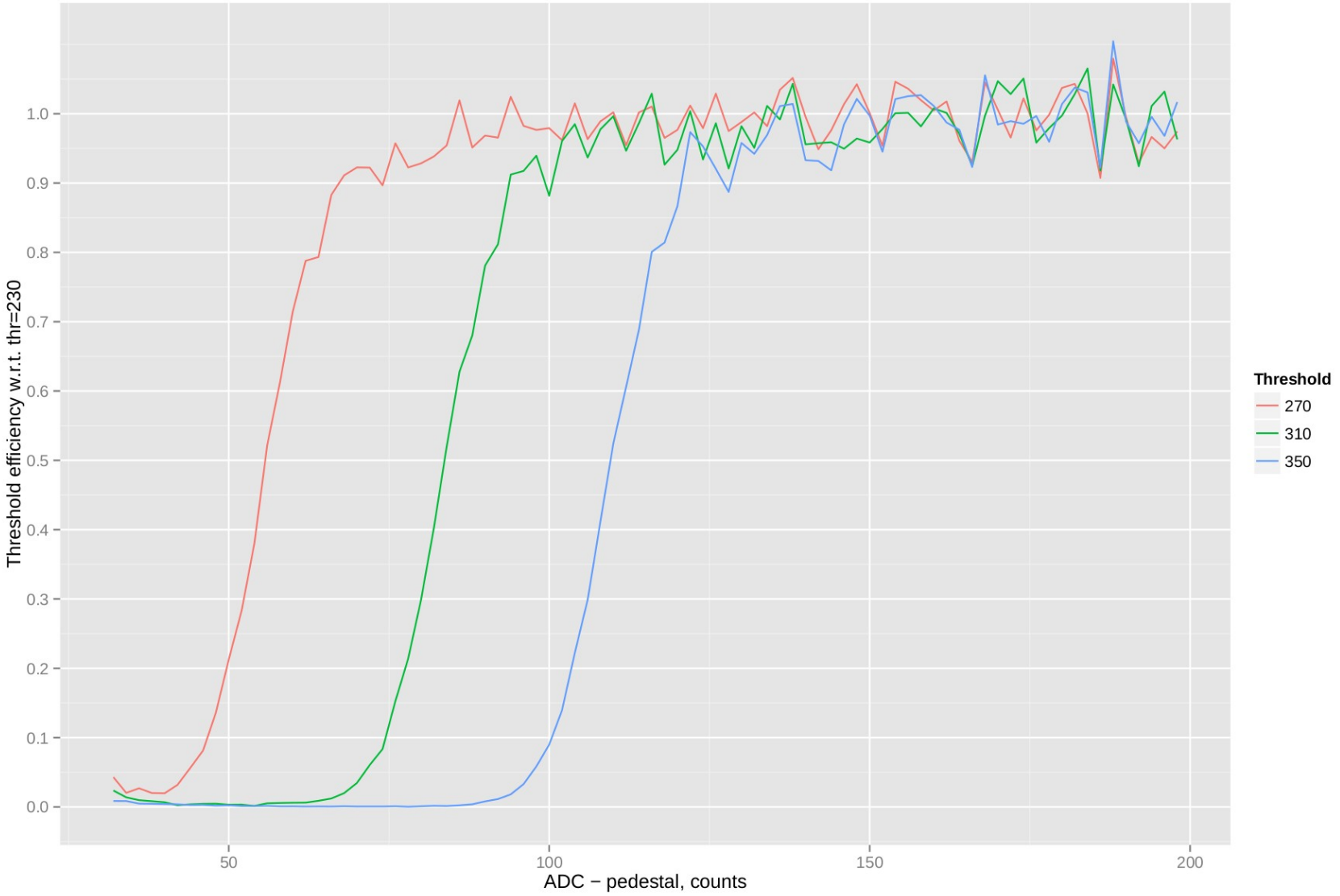
We rotated our setup by 49 degrees to increase signals by 1/cos(49)=1.5. Then, MPV should not be cut anymore. We made trigger threshold scan with the values 230 (nominal), 270, 310 and 350.

Histograms below are for all channels and different thresholds in DIF1, normalized in the interval ADC-pedestal>150 (with 100% efficiency for all chosen thresholds), see e-log entry #933.



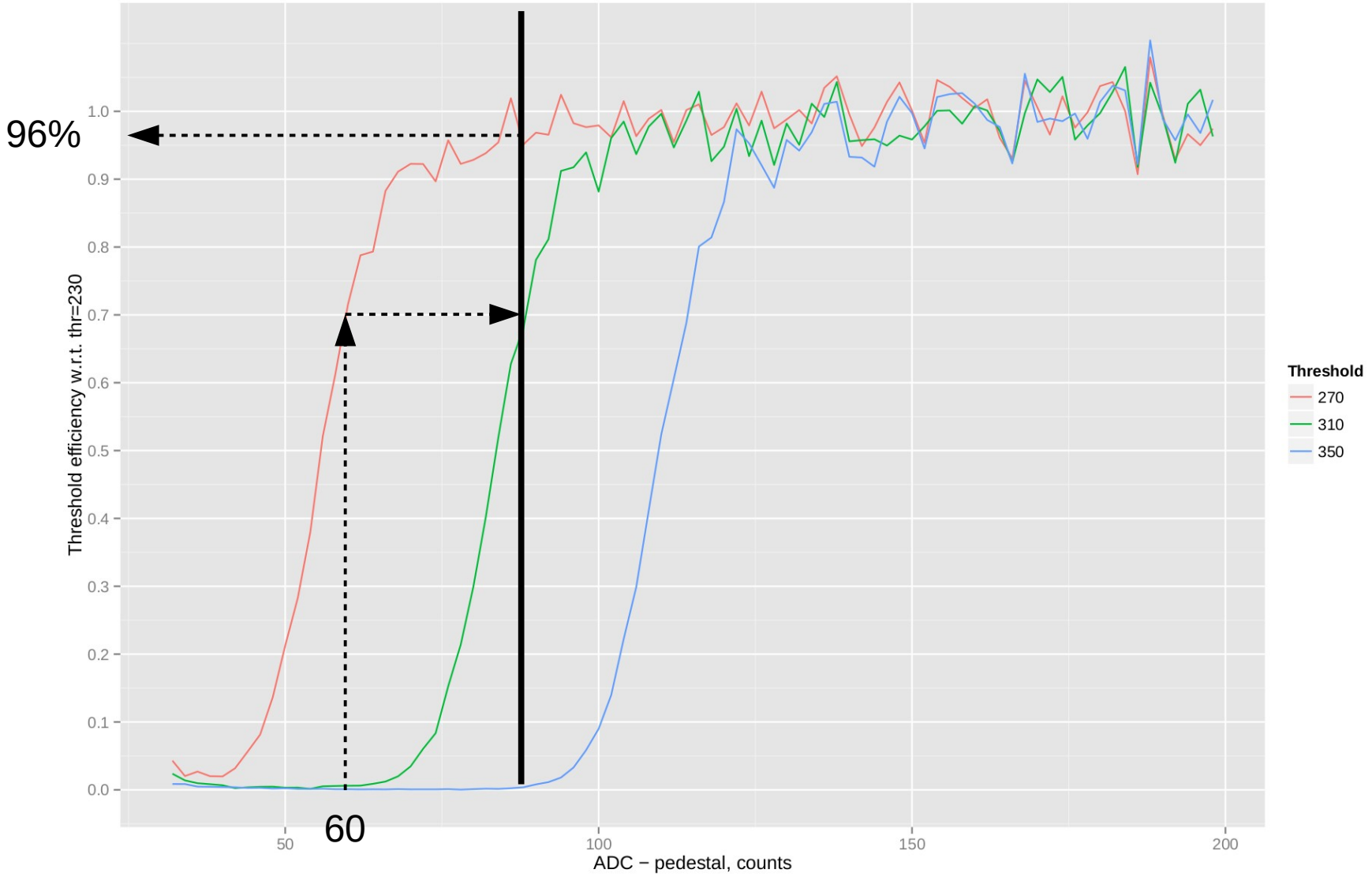
Trigger threshold scan @49° rotated setup

Ratio of the MIP spectra from the previous slide to the one at nominal threshold 230.
Equidistant placement of S-curves differing by delta threshold = n*40 indicates linear scale of trigger threshold in this region.



Trigger threshold scan @49° rotated setup

Assuming linear scale of trigger threshold also for lower signals: imagine a similar S-curve at nominal threshold 230 on the left, then, shift it to the right so it overlays with the first, red curve in the plot below, its intersection with vertical solid line gives the efficiency at MPV=60: eff≅96%,
eff=50% at about 30 ADC counts.
(another example: @threshold=290 for first cosmic tests one year ago: eff≅10% for MPV=60).



Study of bugs and features

To provide input before new SKIROC production.

Known problems without prooven solution (from at least end 2012):
- retriggers (no solution)
- pedestal baseline correlation with large signals (might be improved, not tested)
- S/N better for higher gain
- external trigger (to be solved in new SKIROC production, not tested)

New, from last Nov TB'15:
- triggering in BX+1 under high load, see next talk by Kostya.

Also note:
- Myth: ECAL rates in ILC are low.

In fact, rates in endcaps: up to 40 events / spill (ILD train), and up to 180 in endcap ring,
see H.Tran talk at ILD ECAL meeting in Paris, 2013, https://agenda.linearcollider.org/event/6036/

Why progress is slow?

1) Too complicated system?
- may need debugging tools, up to now emphasis on development but not debugging / improving existing design. debug : development = 2:1

- engineers themselves do not use efficient tools for data analysis

2) Reduced motivation / manpower / budget because of uncertainty with ILC. Synergy with HGCAL might help.

Bug and features: more on retriggers

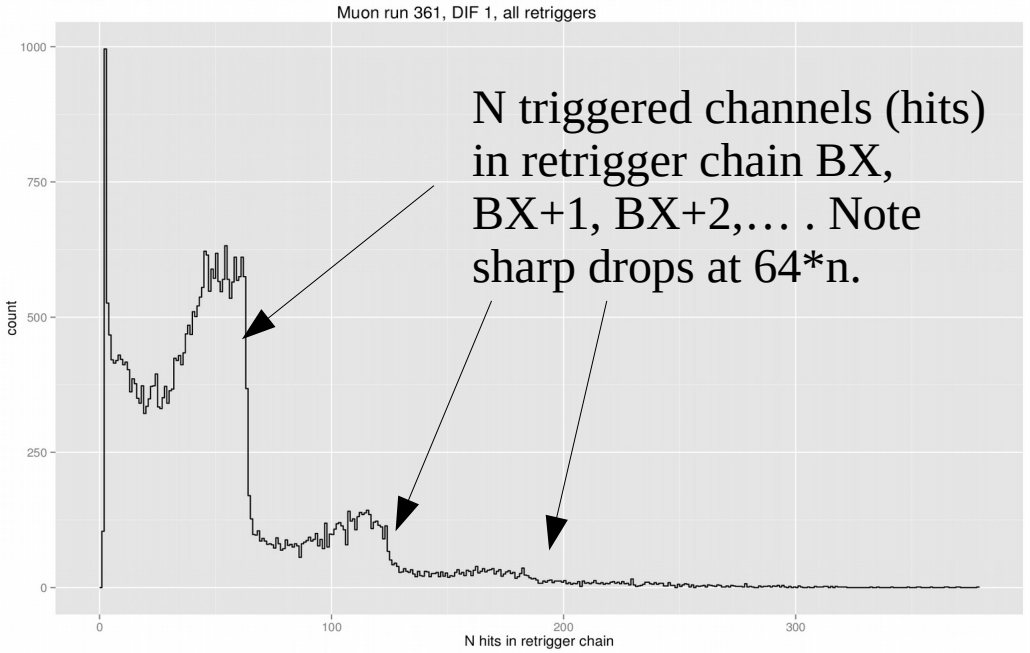
Retrigger chain is one “macro” event lasting about 1 msec (2-3 BX). Retriggers in BX+2 are caused not by triggers in BX+1, but are “programmed” from the beginning in BX. The chip in BX already “knows” whether it will retrigger or not. If yes, all its channels are “excited”.

Pedestals:

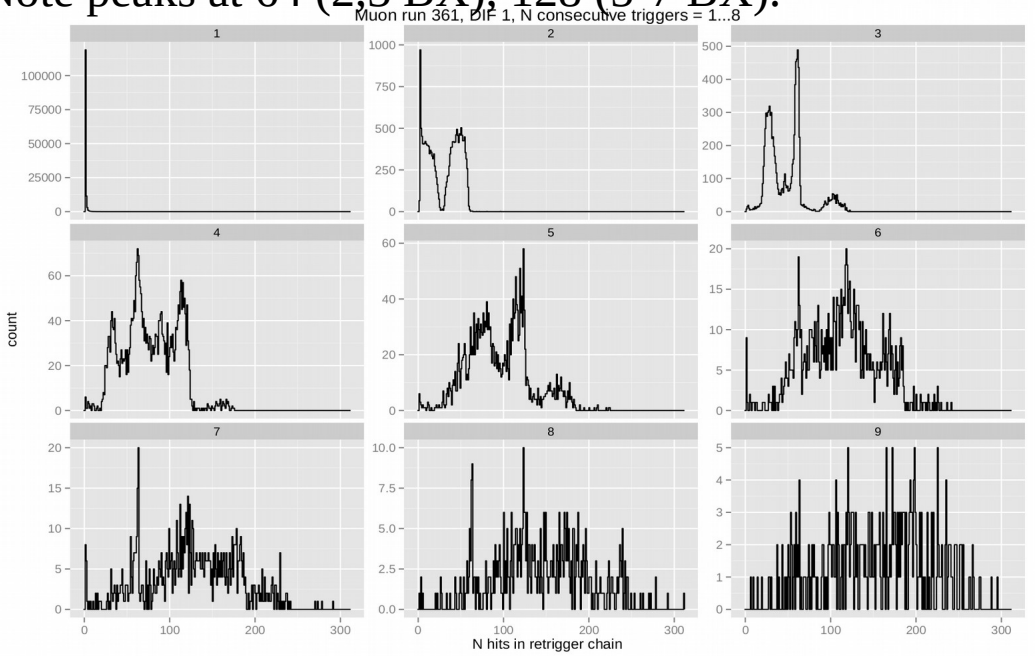
The pedestal positions of all channels in BX are shifted synchronously to the right. As retrigger develops, more and more pedestals move to the nominal positions on the left. When all pedestals arrive at their nominal positions, the retrigger stops.

Triggered channels:

In one of BX+1,+2,… every channel “emits” its “excitation” by triggering. This can be visible or invisible, maximum 64 channels can be triggered in one “macro” event, but not more. Every channel either produces one trigger or nothing. One “macro” event may initiate another one, so that we can see 64*n (n=1,2,3) triggers in total.

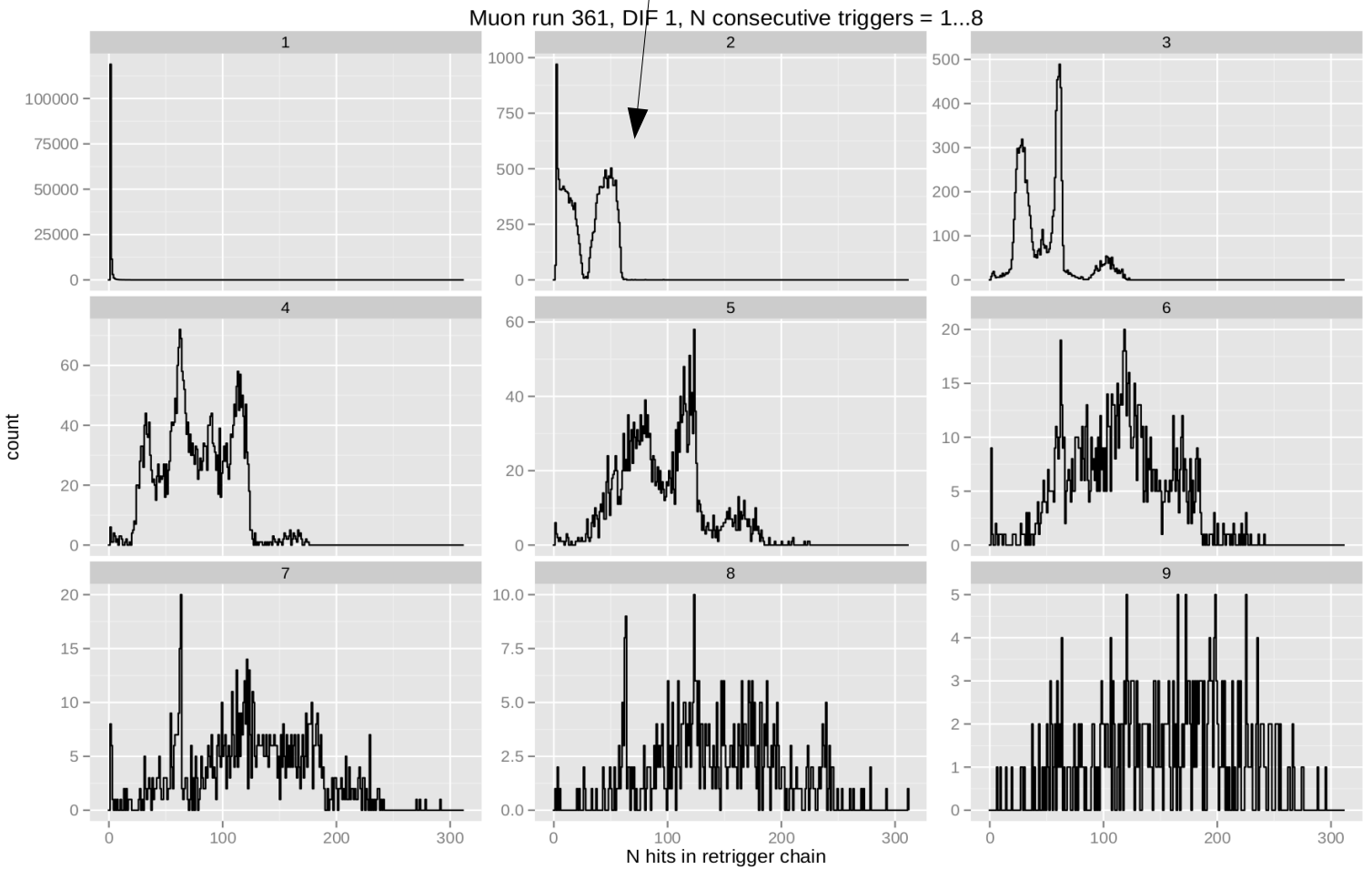


N hits when “macro” event lasts 1,2,…,9 BX.
Note peaks at 64 (2,3 BX), 128 (5-7 BX).



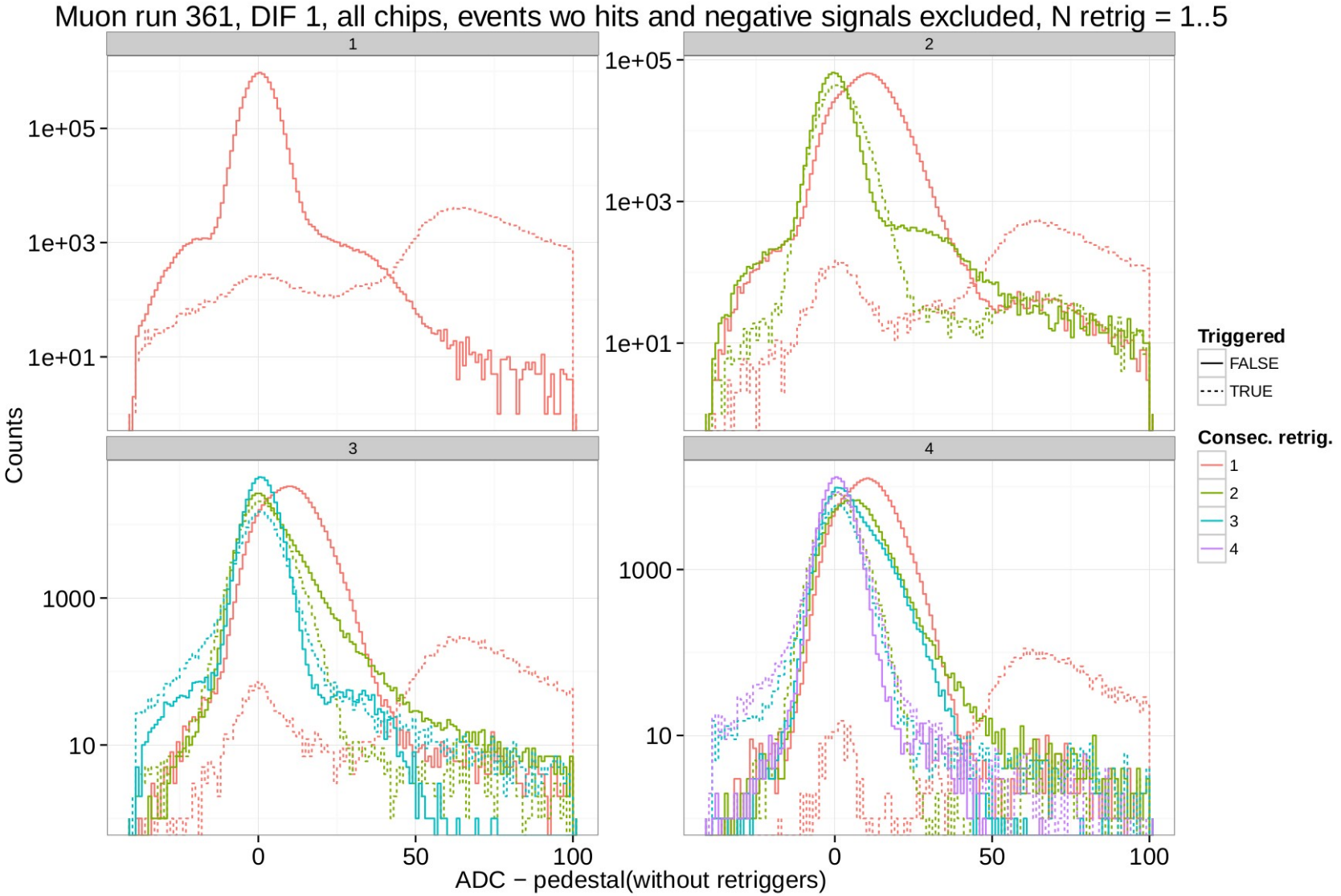
Bug and features: more on retriggers

Why there is no peak at 64 if “macro” event consists of only BX and BX+1?
Possible explanation: because “macro” event lasts longer than 2*BX = 800 nsec. After BX+1, there is still relaxation of “excitons” in BX+2 as usual, but we do not see them, since they all happen to be below trigger threshold (OR64 not fired), so BX+2 is not recorded.
We know that retriggers are very much suppressed by higher trigger thresholds (at 1-2 MIPs), but this activity may always be present in the chip, and may just proceed invisibly.



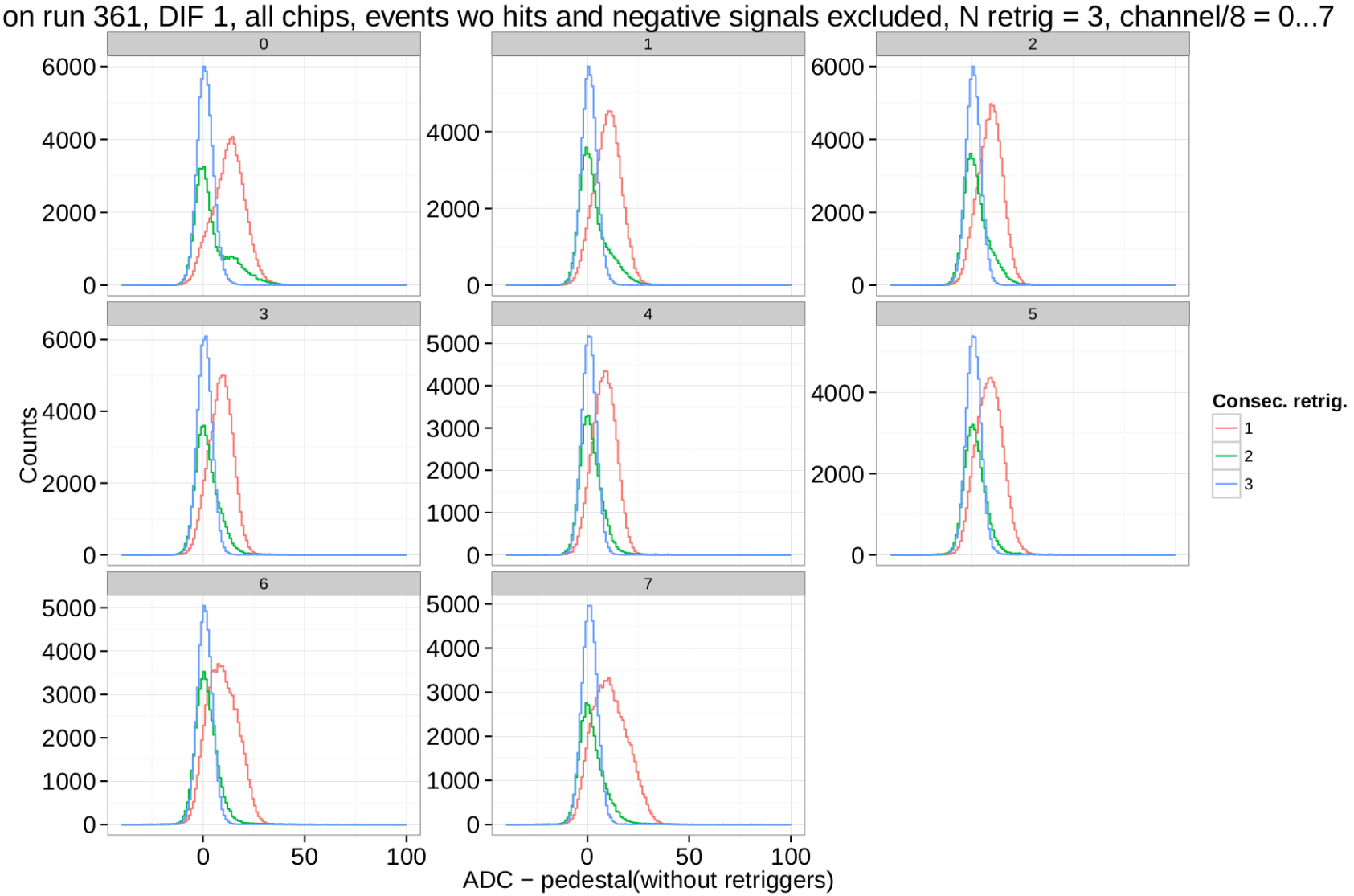
Bug and features: more on retriggers

ADC during retriggers: pedestals are shifted to the right, triggered hits – mostly at zero.
4 plots below: “macro” event = 1 BX (no retrigger), 2, 3, 4 BX.
(ADC – unbiased pedestal) is plotted; unbiased pedestal is taken from no-retrigger BX.
Colors distinguish BX, BX+1, BX+2, BX+3. Solid is for hits, dashed – for pedestals. All SCAs and channels are combined. When all pedestals arrive to their nominal positions, retrigger stops (last BX+n)



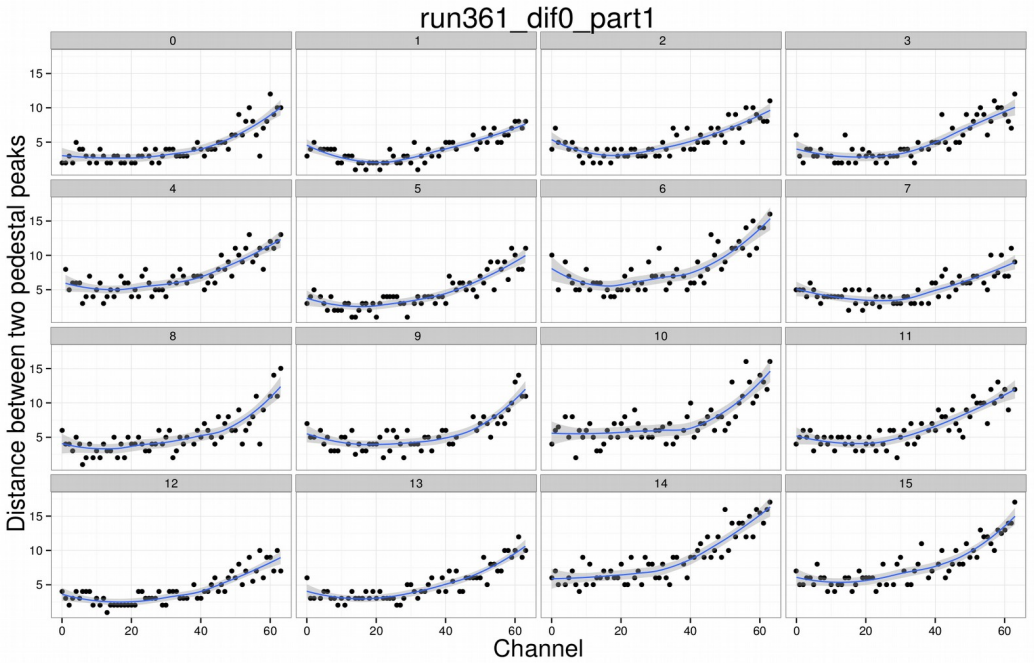
Bug and features: more on retriggers

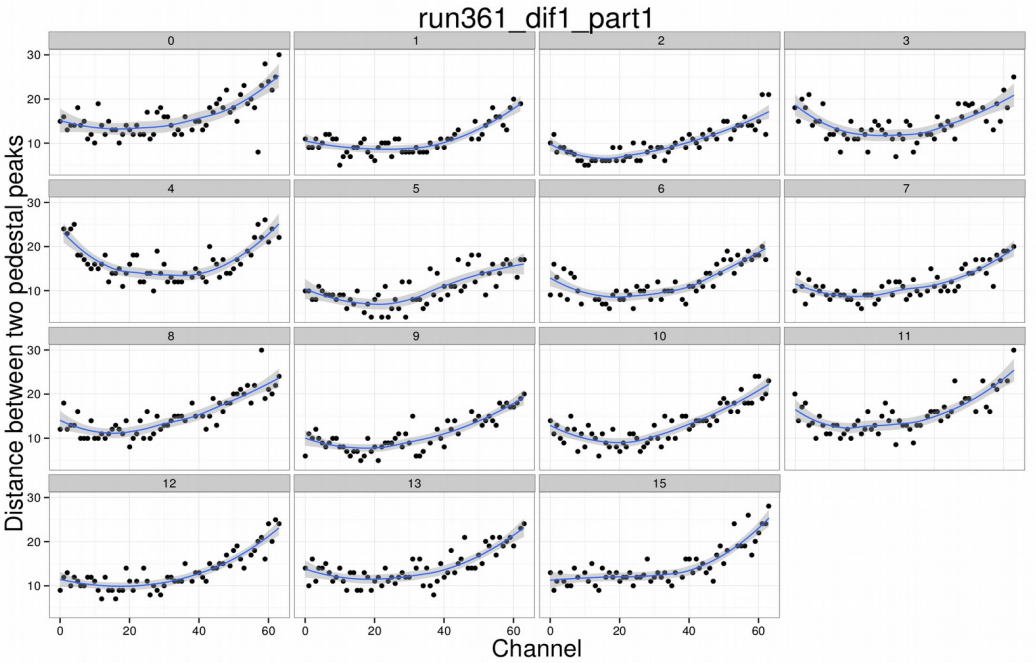
Pedestals only, linear scale, “macro” event=BX,BX+1,BX+2, separately for groups of 8 channels (0..7, 8..15, …, 56..63)

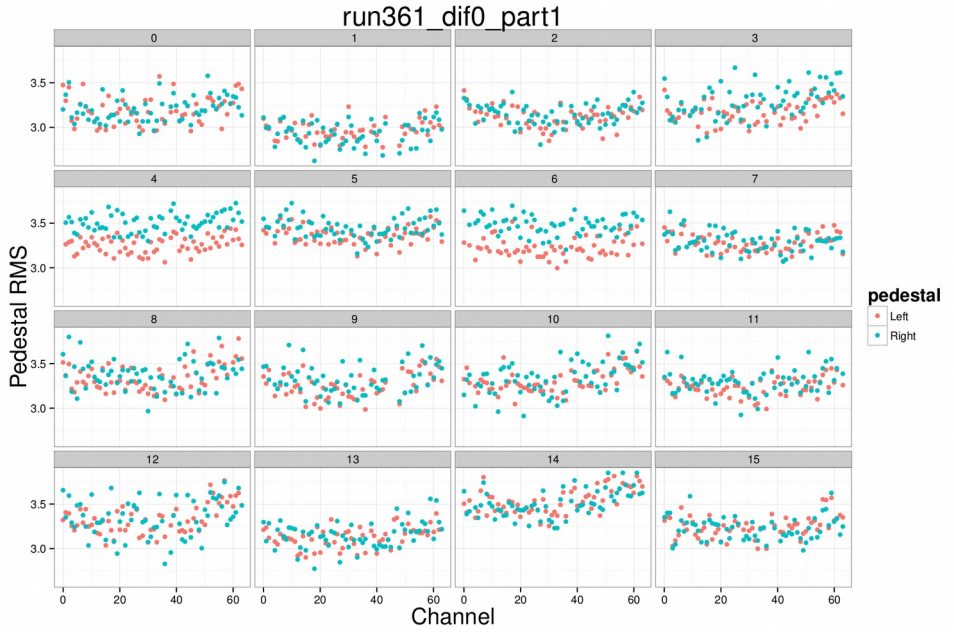


Bug and features: more on retriggers

Pedestal splitting is layer dependent. 2-10 in DIF0,2 (top left for DIF1) and 10-25 in DIF1 (top right). Widths of left, right peaks are about the same (bottom).

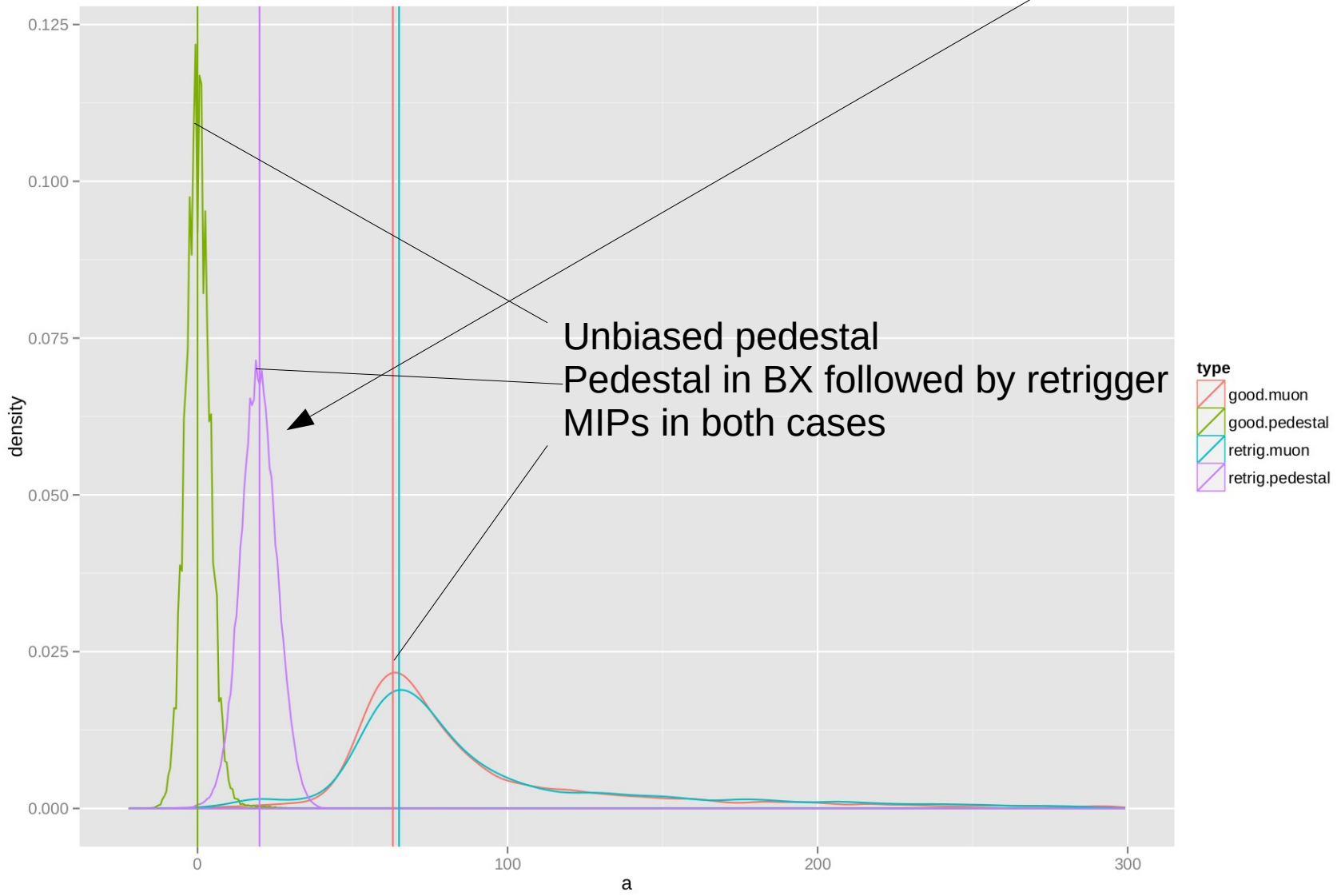






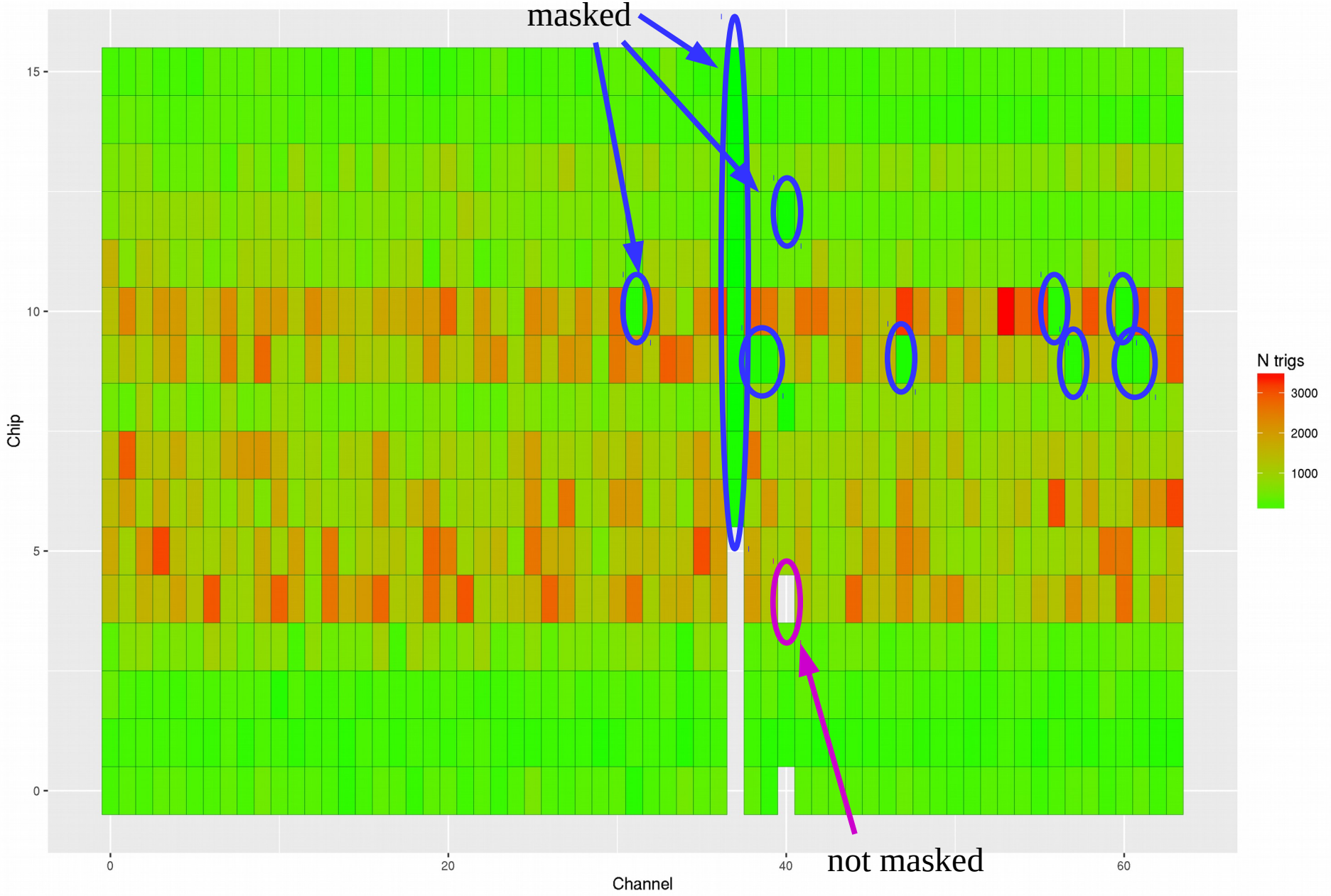
Bug and features: more on retriggers

MIP is not shifted, only pedestal, here for channels 56..63 in DIF1 with maximal pedestal splitting, SCA1, muon run #361.
Average pedestal splitting = 20, MIP splitting <=2.
Right, biased by retriggers pedestals have about the same widths, but their peak is wider here because of variation of pedestal split.



Bugs and features: masking

Configuration masking does not coincide with real masking. Example for DIF2



Bugs and features: masking

Full table of mask mismatches, format: “chip (channel)”, both start from zero

DIF	Masked but has triggers	No triggers though not masked
0	6,7,12 (37)	1,2 (3), 9 (3)
1	12 (23,49), 6,7,11,12 (37)	2 (3)
2	8 (40), 9 (38,39,47,57,60,61), 10 (31,56,60), 12 (40), 6,7,8,9,10,11,12,13,14,15 (37)	4 (40)

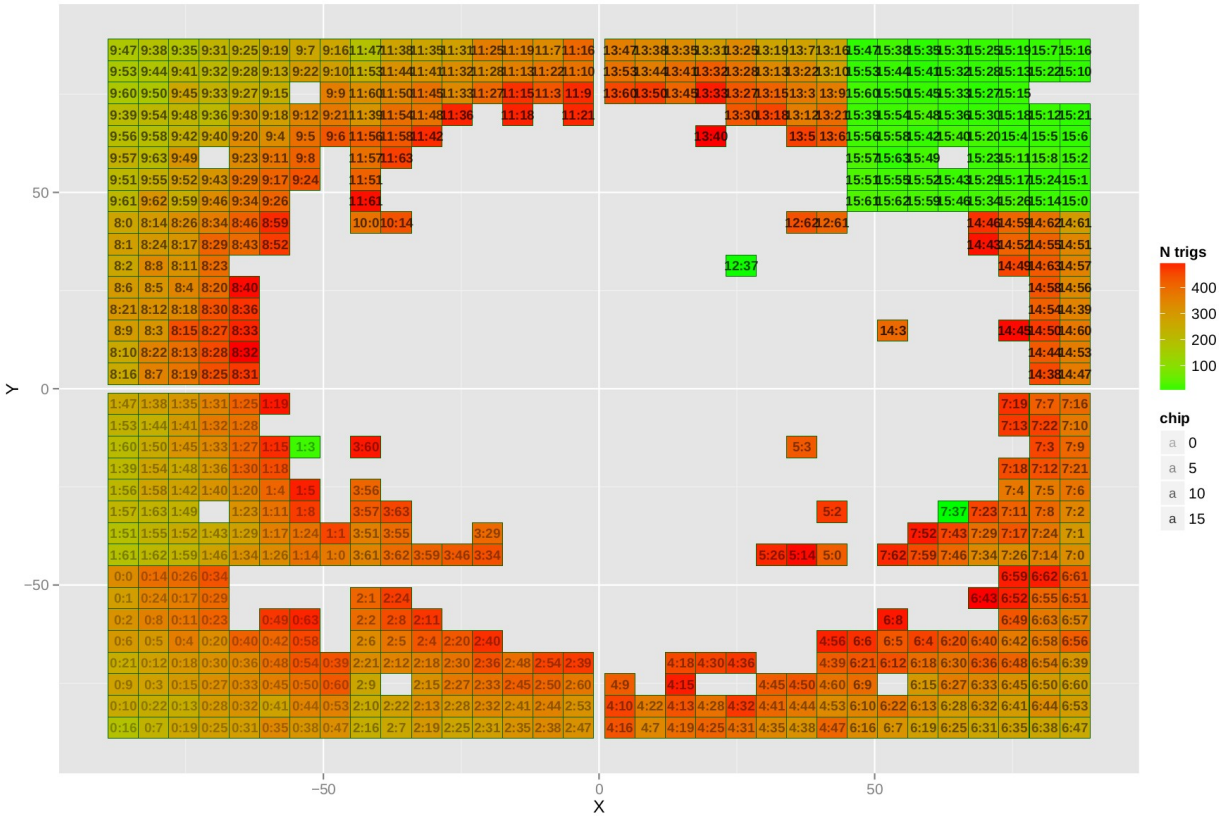
Number of mismatches = 35,
with total supposed number of masked channels = 68

Bugs and features: data corruption

Spill = data taking + readout, data corruption occurs if readout time is not sufficient.

In the first runs 2 Hz spill was set as 490 + 10 msec (do not know why, 10 msec is too low).

Corrupted event rate fluctuated from run to run: eg. #86, 150 GeV electrons – about 30% corrupted events, run #205, 100 GeV e+ – 1.5% (it seems: threshold effect).
Discovered and changed from run 207 on, to 150 + 50 msec, also increased rate to 5 Hz (e-log entry 382).
Then, Taikan discovered that chip #15 was missing in data in all 3 layers, from run 313 on, e-log entry 641.
This was attributed again to data corruption, which jumped to 13% in run 313 (e-log 618).



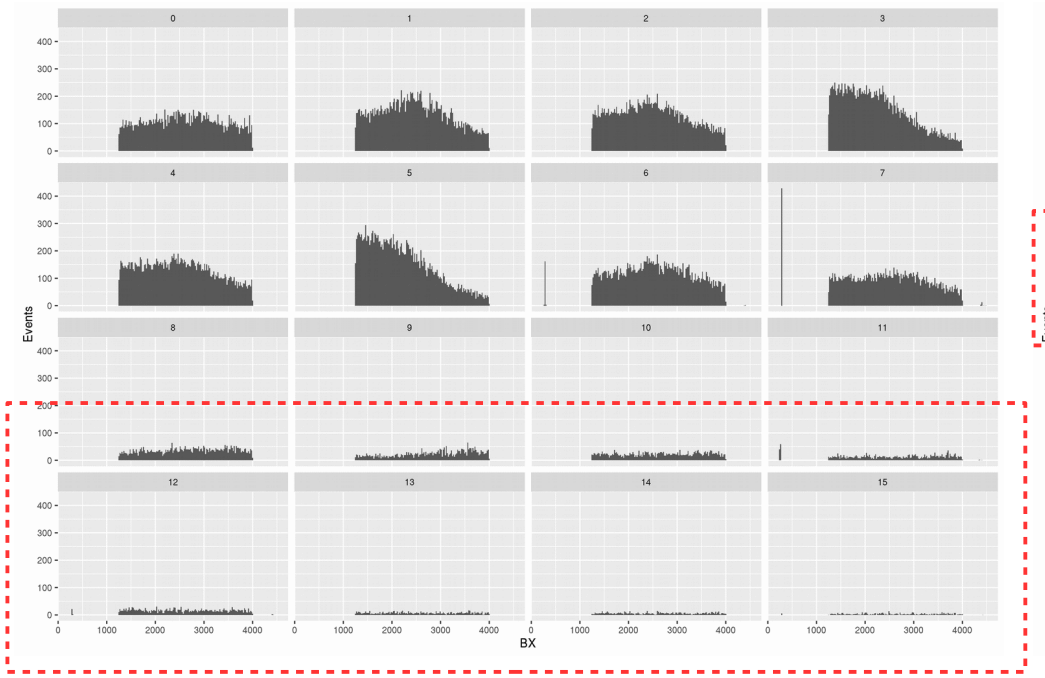
Bugs and features: data corruption

We increased the rate to 10 Hz (eg. with 2.5 + 97.5 msec = data taking + readout time, BX plot for 16 chips below), and data from upper half of chips (8-15) became significantly suppressed.

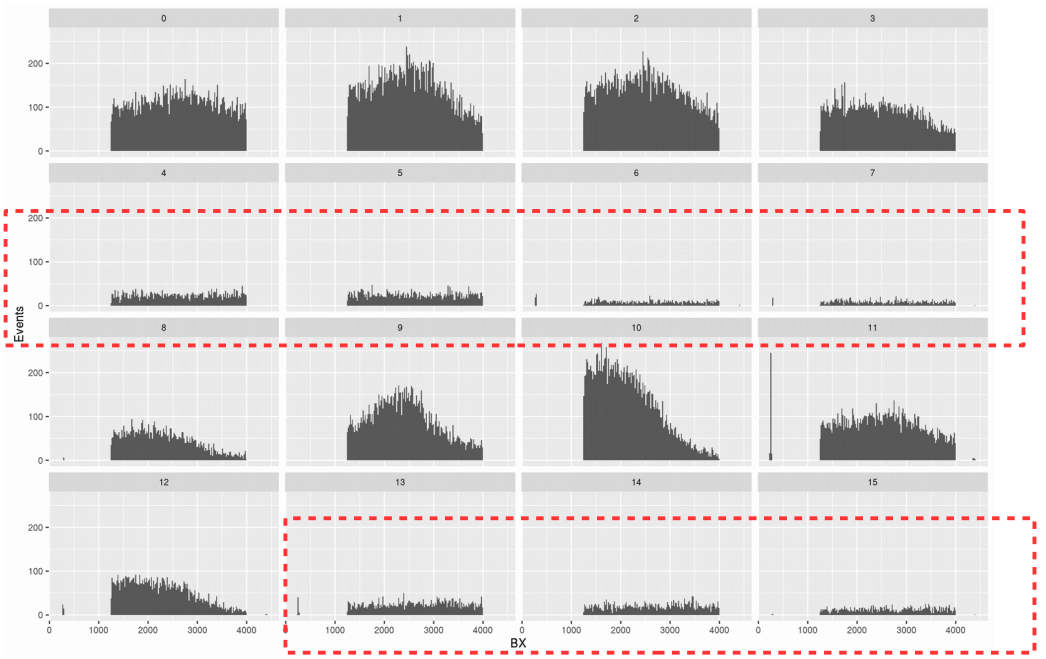
We changed frequency to 4 Hz (run 330, 332 on), everything became normal. In the following, we either used short or long spills: 2.5 + 247.5 or 200 + 50 msec, respectively, @ 4Hz.

In conclusion, “safe” settings: readout (dead) spill time >= 50 msec, rate <= 4 Hz

Run 326, 10 Hz, half of chips missing

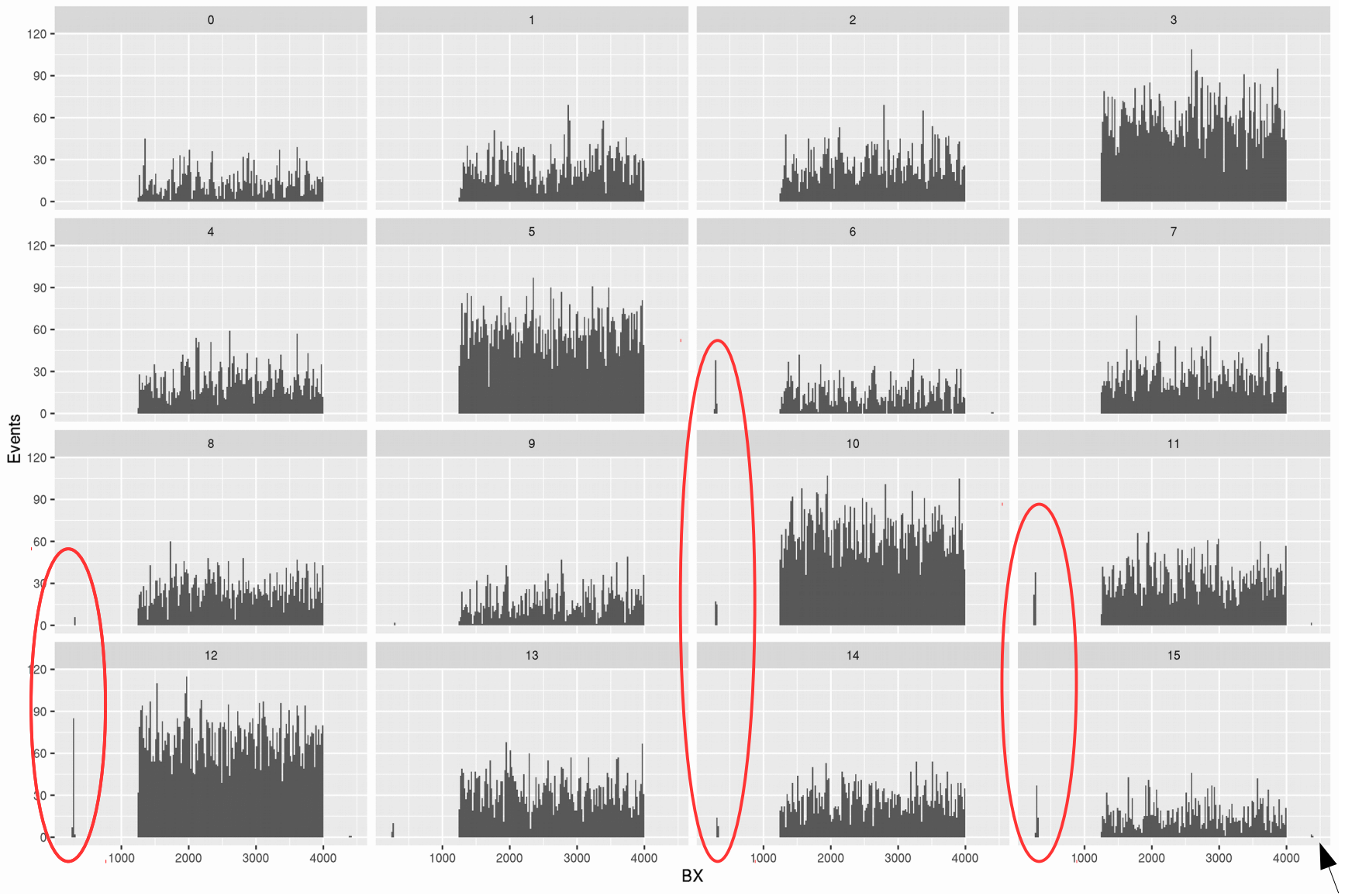


Run 331, 20 Hz



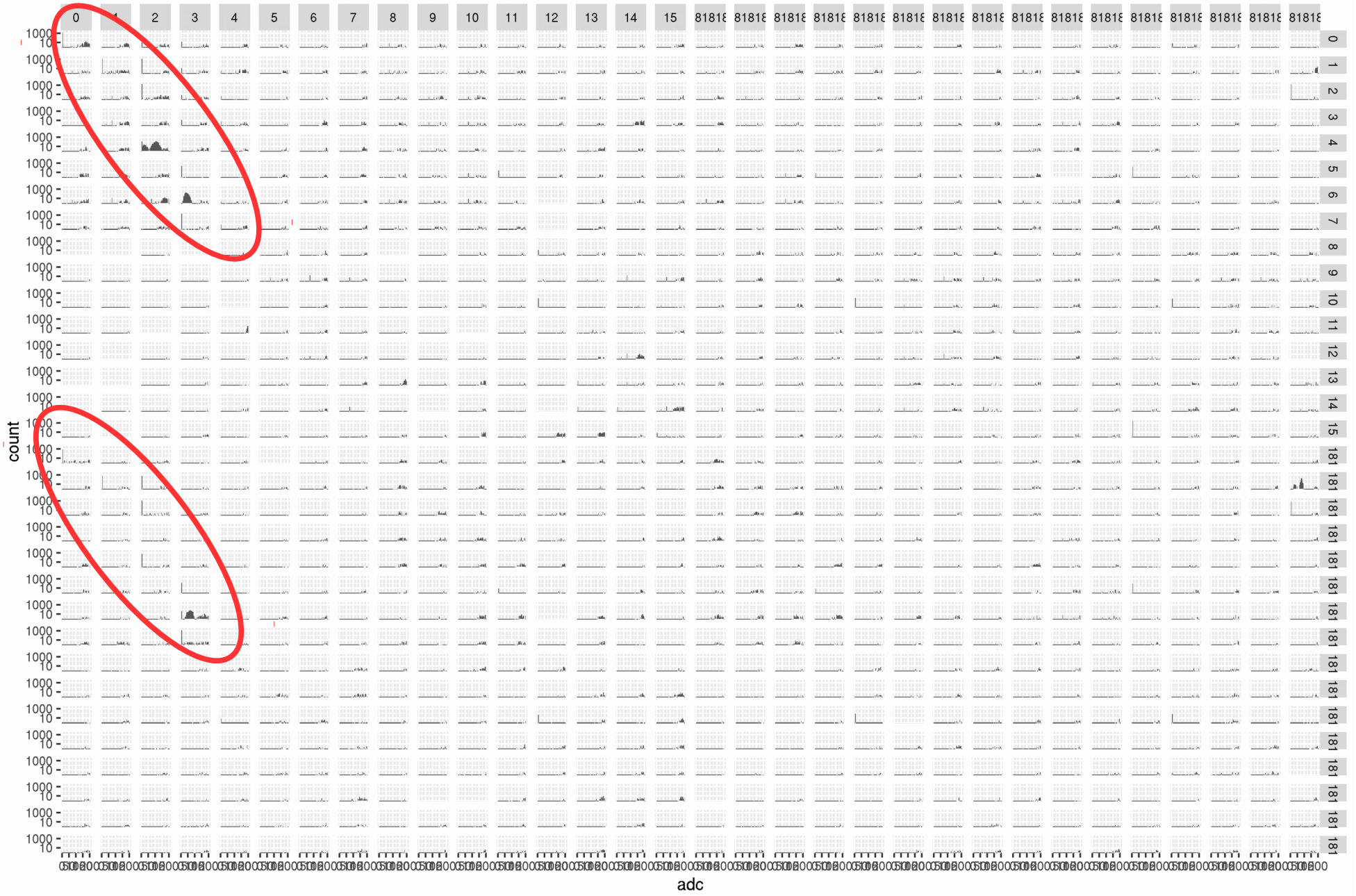
Bugs and features: wrong BX

In short spills (2.5 + 247.5 msec = data taking + readout time) BX should be between 1250 and 4000,
But there are entries at zero and (very little) above 4095. Muon run 414.



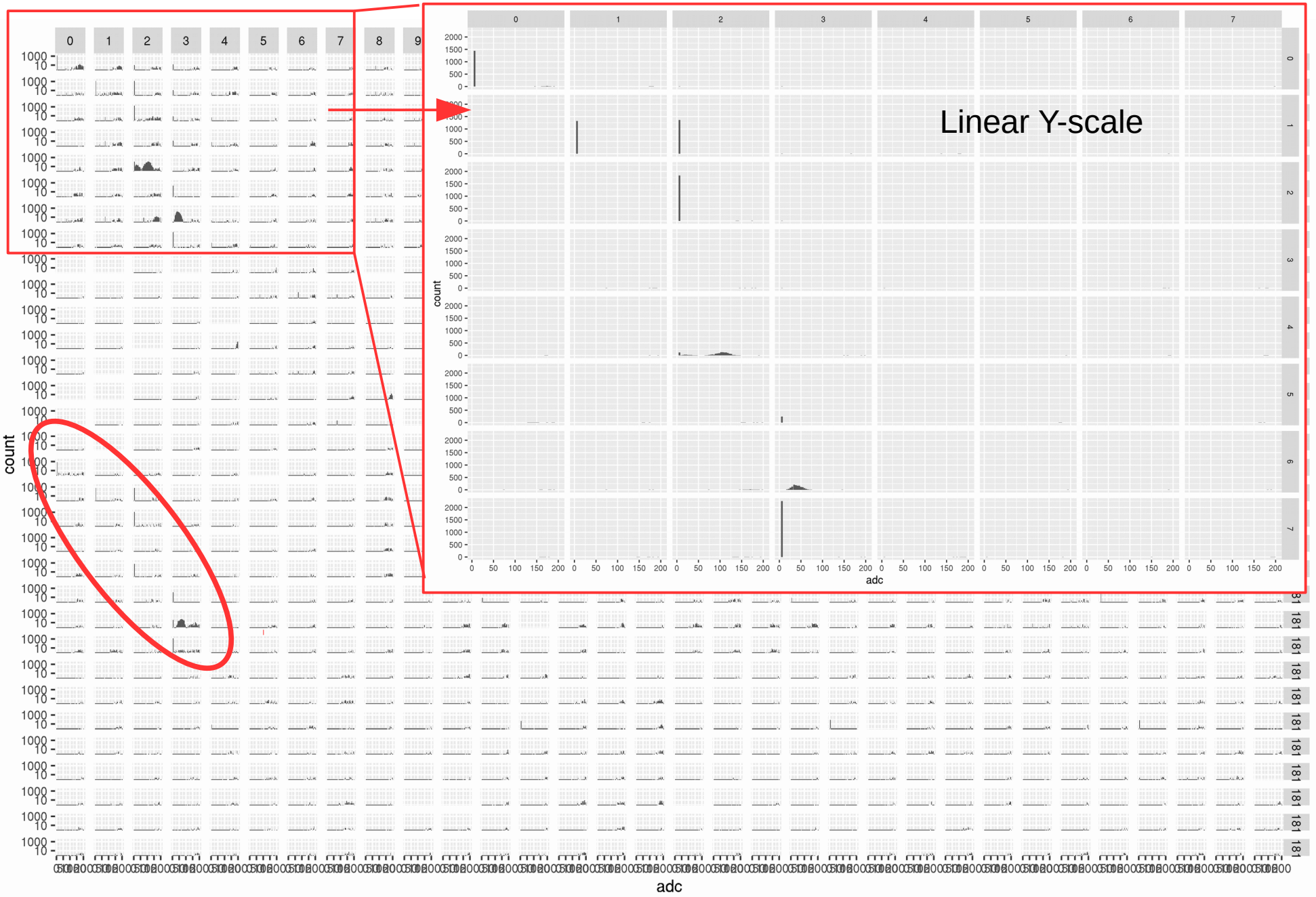
Bugs and features: negative signals

Negative signals sometimes appear below pedestal, in ADC=4 in case of underflow. Note log Y-scale.
DIF 1, muon run 361 as an example.



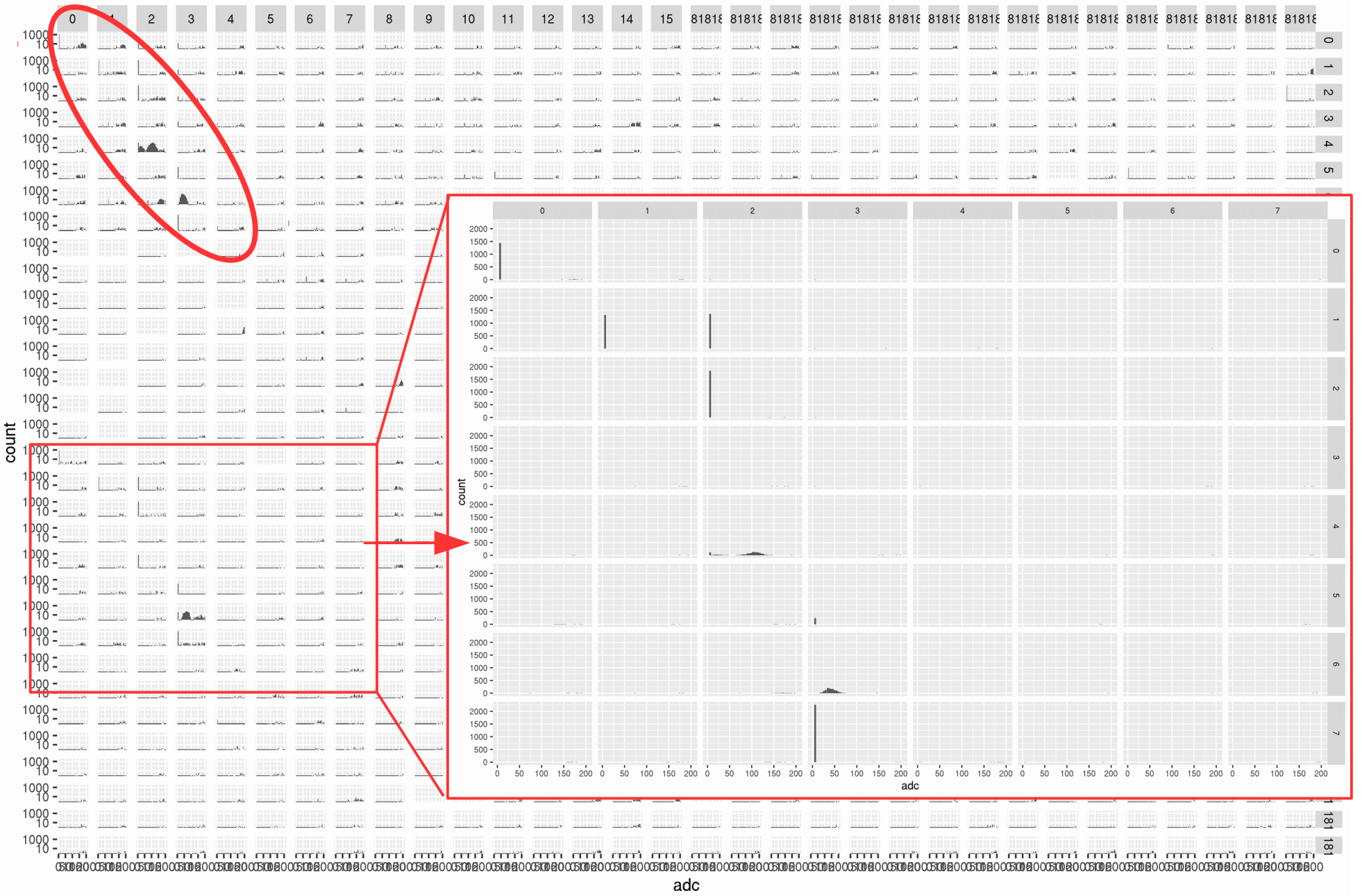
Bugs and features: negative signals

Grouping along two lines in chips 9 and ...



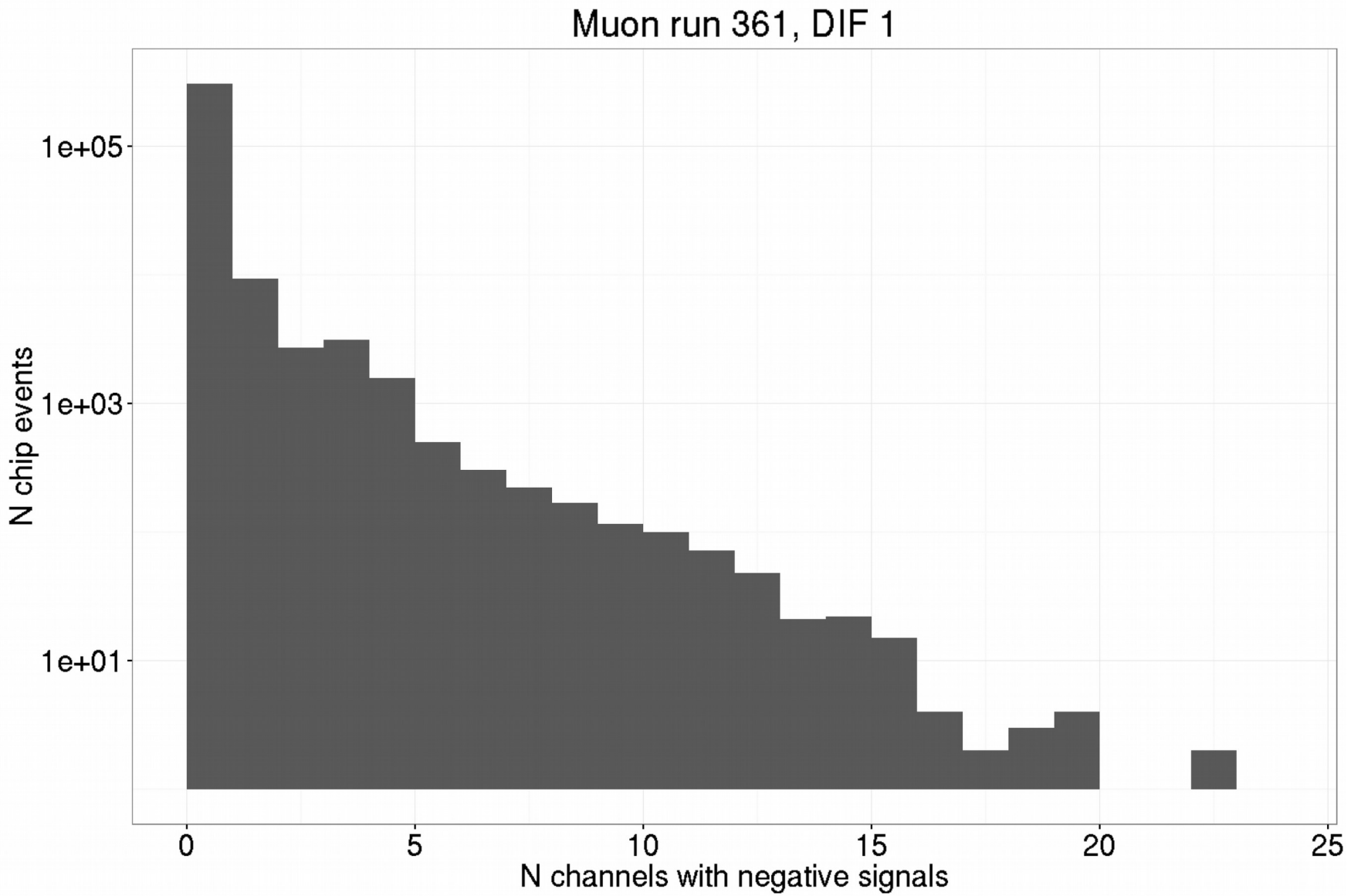
Bugs and features: negative signals

… in chip 1.



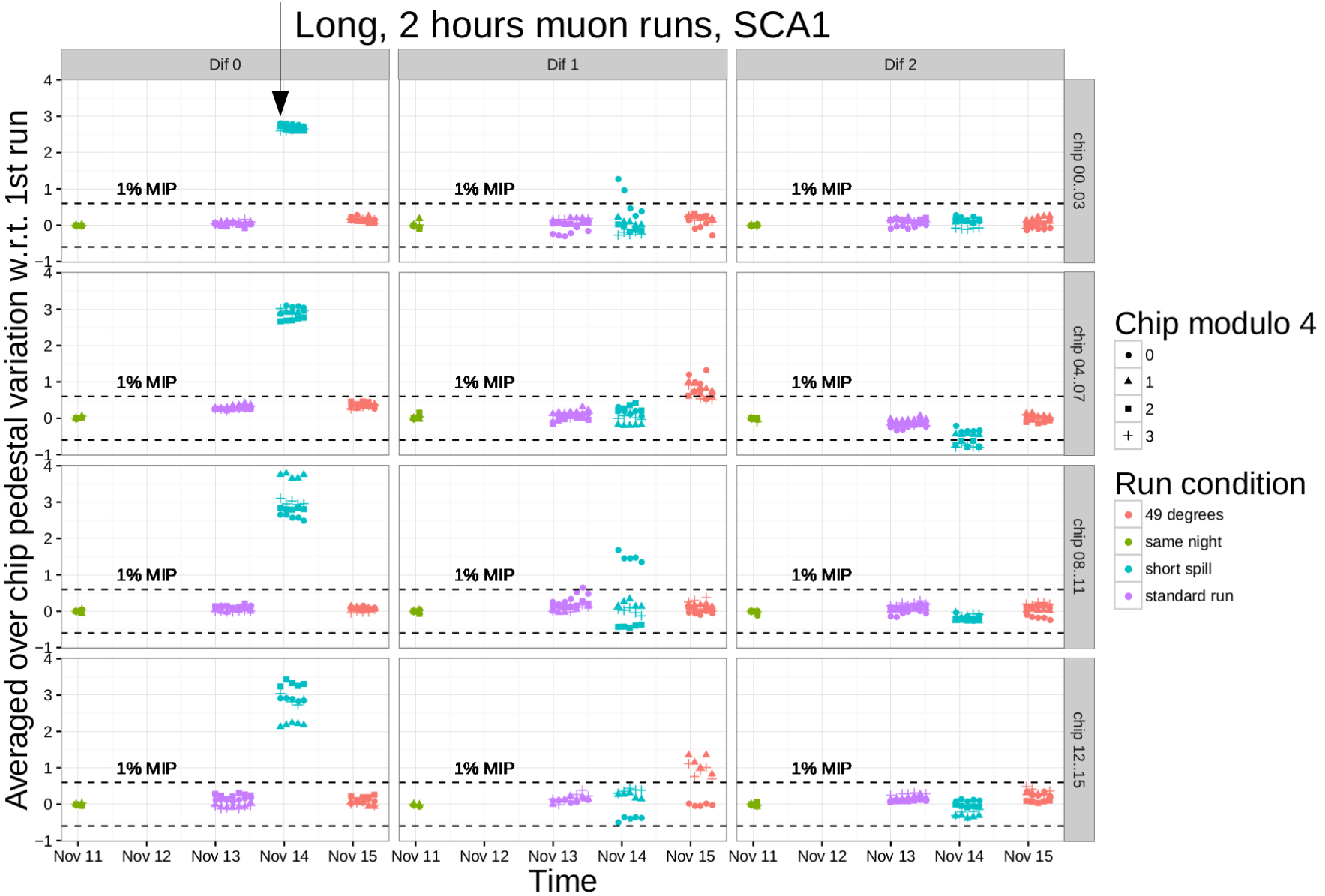
Bugs and features: negative signals

Such negative signals are completely different from the effect of pedestal double peaks due to retriggers (see later). Eg. pedestals shift synchronously in all channels, while only a few (0,1,2,…) channels may get negative signals, see plot below and note log Y-scale.



Pedestal time stability, SCA=1

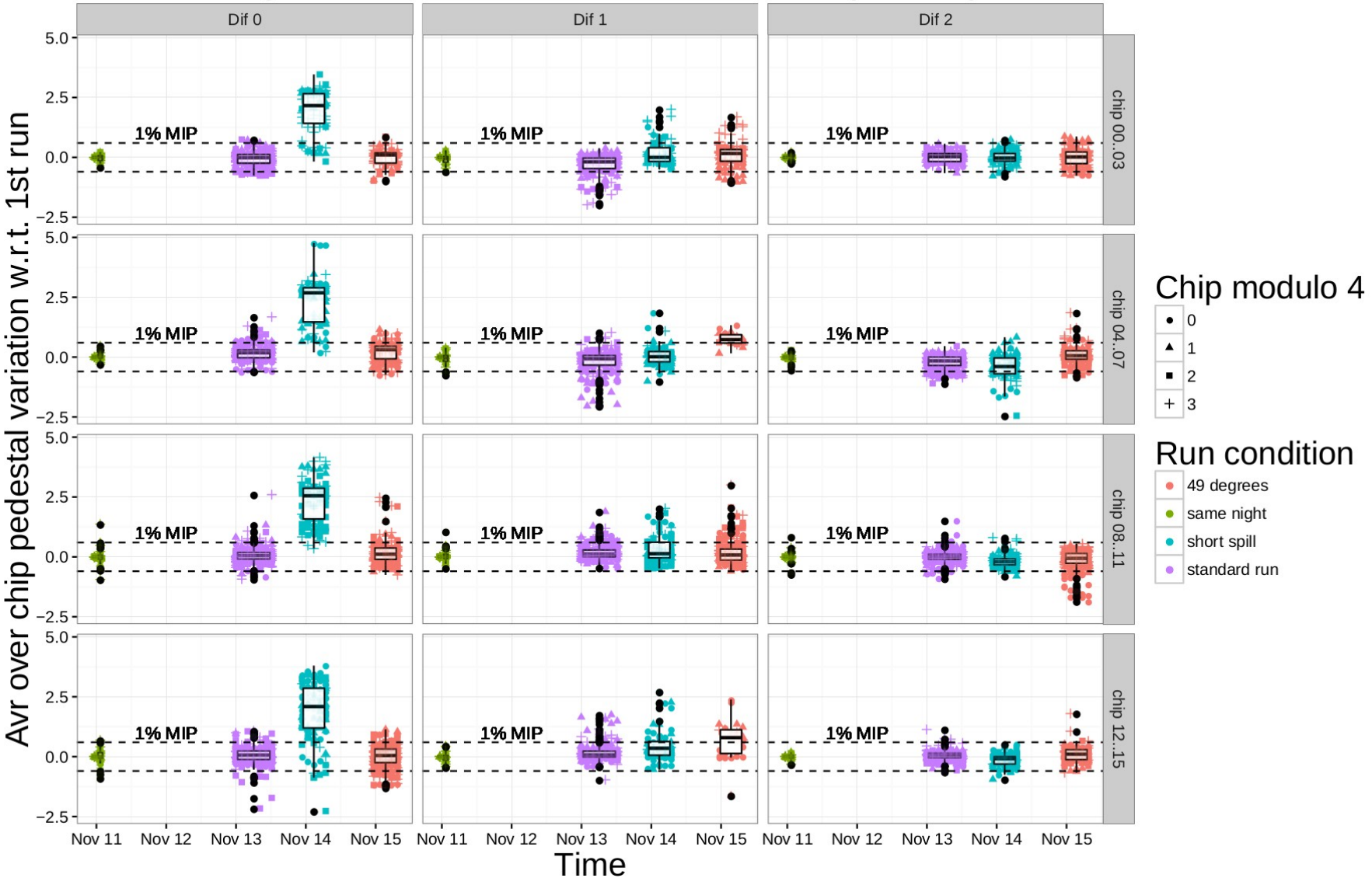
19 muon runs, 2 hours each, mainly taken at night; 64 channels averaged in each chip. Every point is one run and one chip, 19x16x3 = 912 points in total. Evolution of average pedestal position is shown w.r.t. to first run 361. Here, only SCA=1 is selected. Channels #37 (and #45-47 in chips 1,9 w/double peaks) are excluded. Short spills with 2.5 msec data taking (blue): pedestal drift after power ON (stabilization) is still visible, up to 5% * MIP (= 3 ADC) in DIF 0 and layer dependent.



Pedestal time stability, all SCA

Same, but for all SCA. If channel have <25 evts in a given SCA, it is excluded from averaging. Box contains 25%...75% quantiles, lines above and below extend to the last point within 1.5*box height, outliers beyond are shown by black.

Long, 2 hours muon runs, all SCAs separately

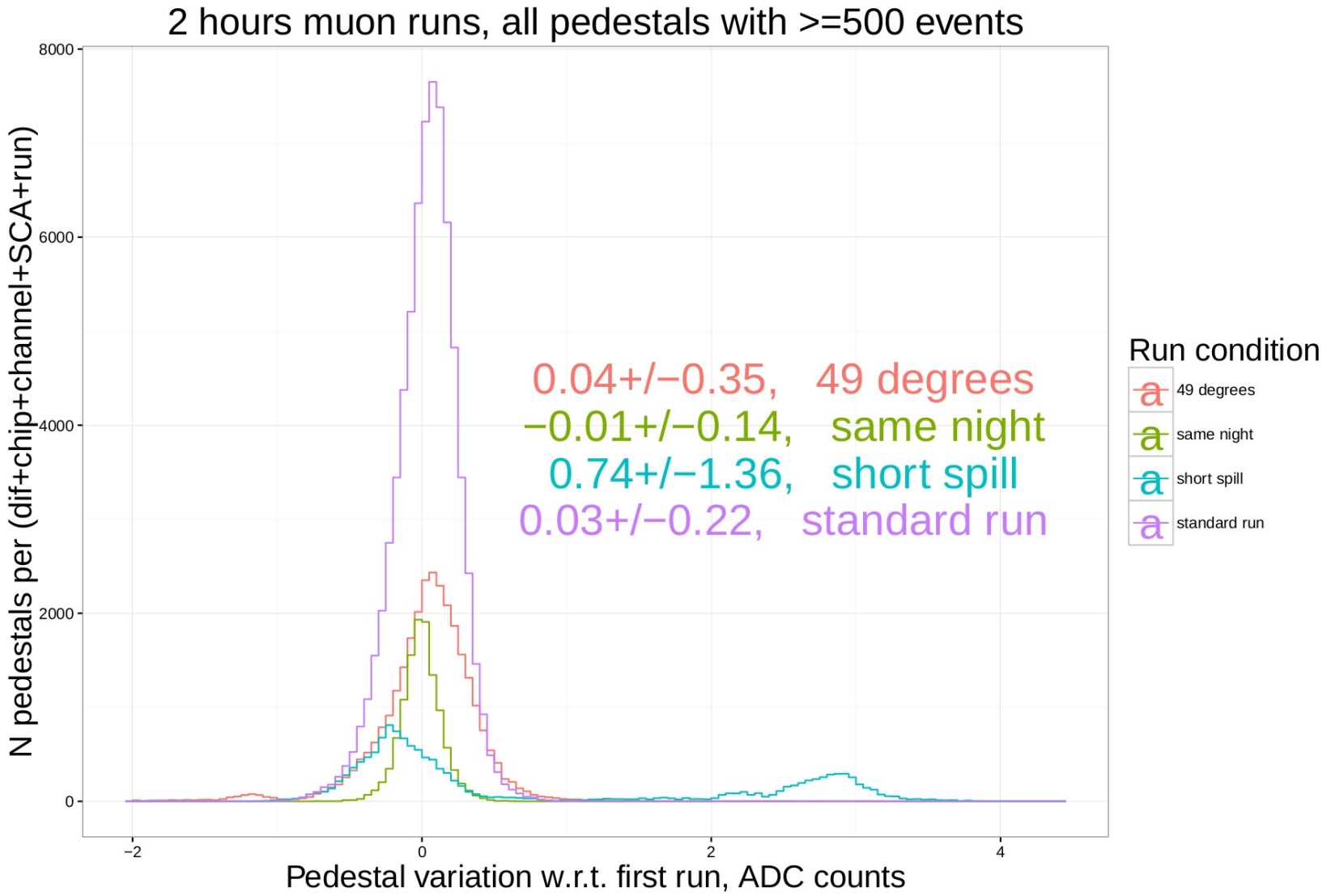


RMS (variation of pedestals averaged over chips)

N evts in ped. spectrum	Without short spill runs	Short spill runs
>=25	0.36 ADC = 0.61% * MIP	1.23 ADC = 2.1% * MIP
>=100	0.45% * MIP	2.1% * MIP

Pedestal time stability, all SCA, all channels

All channels and all their SCAs are shown separately, it is required to have >=500 events in every pedestal spectrum == 1 histogram entry (first SCAs have higher weight because of low muon rate).



Eg. for runs with 49° rotated detector: RMS(ped – ped_in_1st_run) = 0.35 ADC = 0.6% * MIP.
Is it negligible if we want to measure showers with >100 or >1000 MIPs?

How stable should pedestals be?

We aim at 1% ECAL systematics.
Measurement with 1% uncertainty is always very chalenging (N(1% contributions) >> N(10%))

We need to calibrate ECAL using MIPs before installation.

If pedestals vary with time with RMS=0.6%*MIP, does this deteriorate our calibration?
Possibly, not, if we precisely measure pedestals during calibration and if this jitter appears only in pedestals, but the MIP stays constant (offset floats, but slope is constant).

However, we also want to continuously monitor and to verify our calibration at 1% accuracy during the physics run (we'll need time to accumulate statistics for all SCAs), then, if pedestals are not measured continuously (zero suppressed in future SKIROC 3), their jitter will hit us exactly at this level of 0.6%. If pedestals are not known / measured with <<1% accuracy, we can not calibrate continuously.
“Pedestal” runs with random triggers between ILC trains (eg. after every 10^{th} train?) and with the same spills as during physics, could be sufficient?

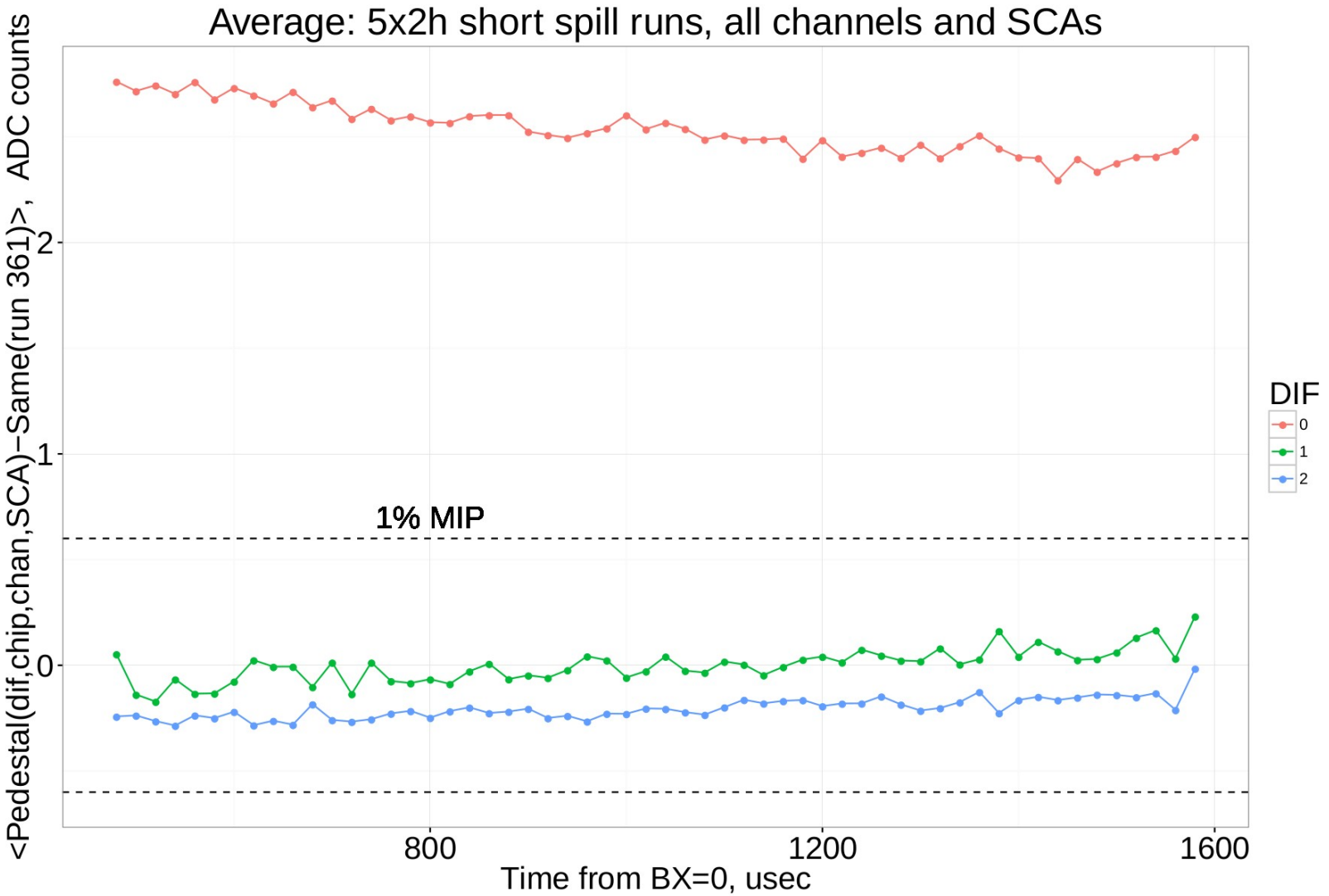
Three other points on pedestals:

2) Binning: MIP=60 ADC at 1.2 pF, but for nominal 6 pF: MIP=12 ADC, so there may be problems to measure peak in 12^{th} ADC bin with <<1% precision.

3) There is about 5% nonlinearity at MIP due to low amplitude and slower trigger. Either it should be calibrated with charge injection in every channel (O(10M)) or per chip or group of chips. Note, there may be technical difficulties in injecting small signals at MIP level.

Pedestal drift after power ON

4) In muon runs with short, 2.5 msec spills, the pedestal drift after power ON (stabilization) is still visible in DIF 0, but only after averaging over 5x2h runs, 1024 channels X all SCAs. Thedrift is very slow. May be a problem for 1% measurement (about O(1 msec) delay is already implemented).

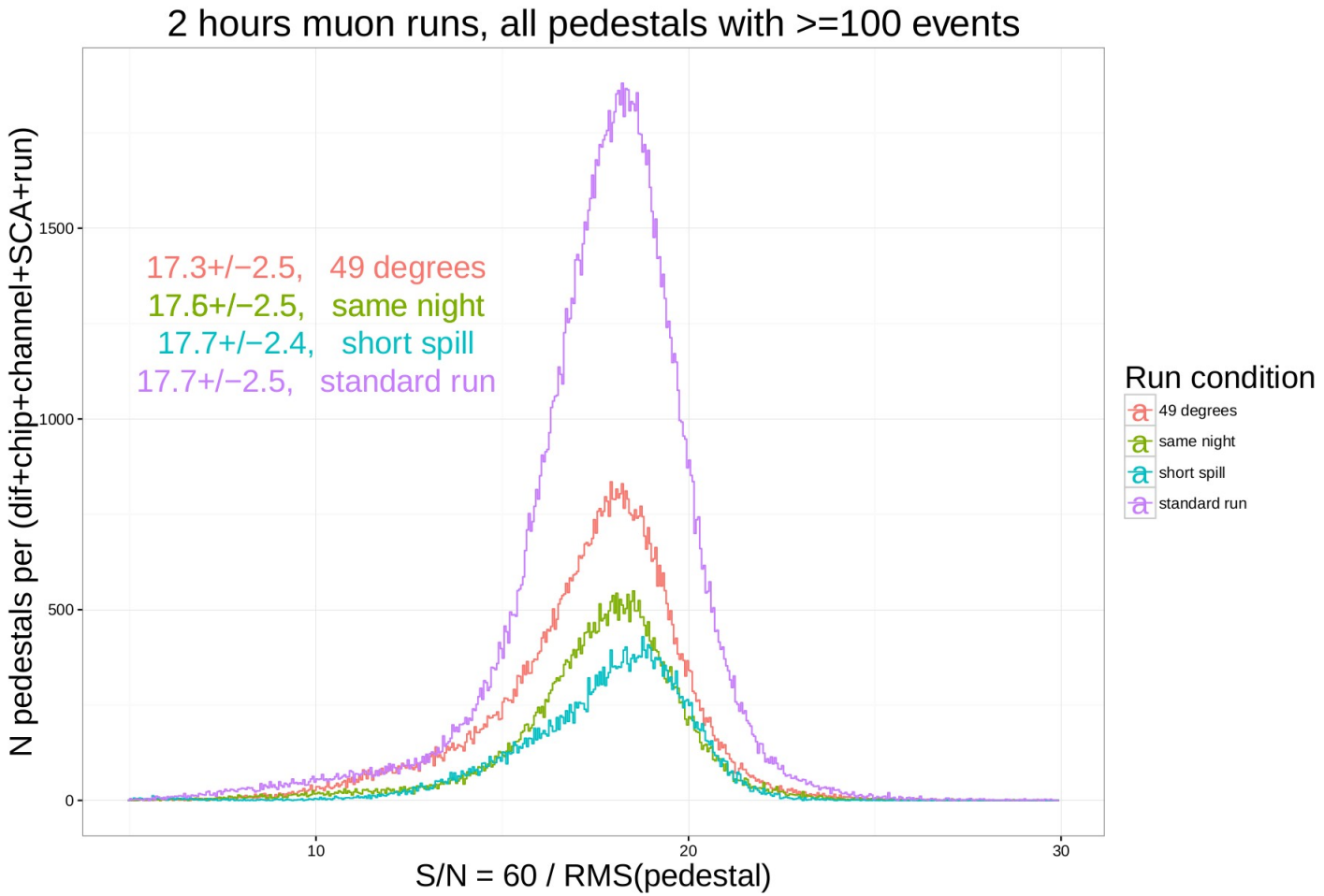


Pedestal widths

Perfect: S(MIP) / RMS(pedestal) =17..18. SKIROC has a very good potential.
Note, even S/N is the same even in short spills with “real” power pulsing and drift effects.

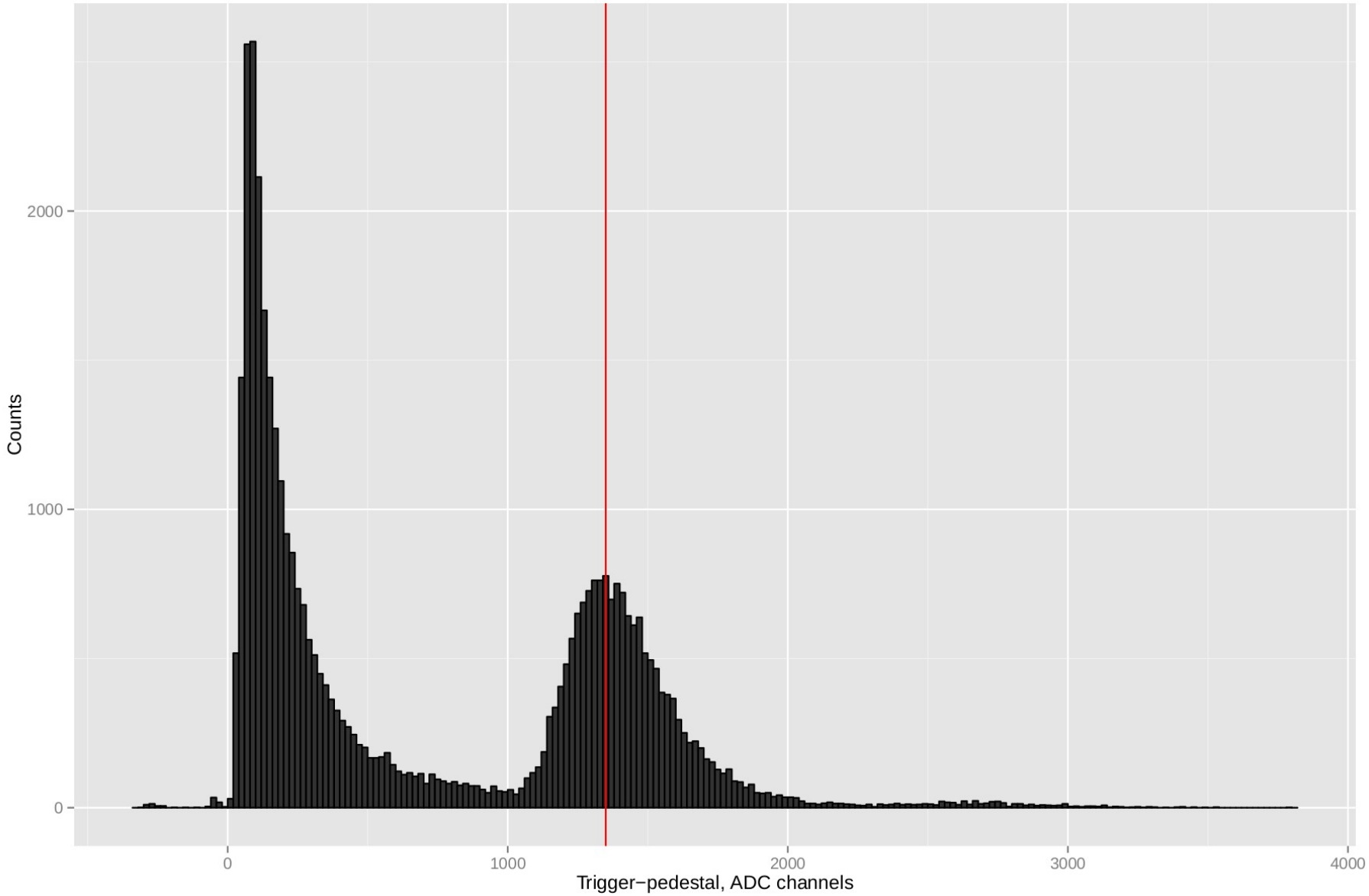
Limiting factors at the moment: surprisingly, *at lower gain S/N degrades*. No measurement with this board, but with FEV8 in 2013: similar S/N at 1.2 pF, while for nominal 6 pF (4 times less gain): about 7..8.

Also, note: we can not set thresholds low regardless of such a good S/N, because of instabilities in a trigger line (retriggers constantly occuring in the chip become visible with low thresholds). This effect does not influence RMS(pedestal).



Setup rotated by 90°

Run #464, a peak at around 1350 is due to particles passing through 5.5 mm of silicon in DIF1.



Plans

- Continue debugging, eg. effect of pedestal baseline correlation with total SKIROC charge was clearly seen online.

- Calibration with muons/ pions (we have large data samples at different energies), taking into account relativistic rise in Bethe-Bloch dE/dx.
Can we demonstrate uniformity of Si <1%? Electronics gain spread measured in FEV8 = a few % (~4%). With cosmic, spread between MIPs was 4-5%.
We'll need a charge injection to every channel to decouple gain variations. Question: what is the uniformity of injection capacitors (injected Q=CU)?

- MIP efficiency: space and time coincidence btw 2 (3) layers, taking into account that 1) one layer may be slightly faster / slower (+/1 BX) than the others and 2) 15 SCAs may become full. Can be repeated for 49^{o} rotated setup (efficiency should be 100%).

- Fractal dimension study in e/pi showers. May be first 2D measurement with data, only transverse granularity is needed.

- e/pi showers: compare with MC the number of hits / energy per layer with different absorber / energy; transverse size (core / tails), invent other transverse variables? correlation between layers; can we distinguish pi0 → gamma gamma component in pi showers using only transverse view?

- Guard ring square events

- saturation in high energy showers

Should be well enough for a paper:
- manily, technology: performance (how suitable for ILD)
efficiency, power pulsing, shower measurements, uniformity, sources of systematics, GR, observed problems,
- physics: fractal dimensions