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Recent ASIC developments for the CLIC vertex detector

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As part of the R&D towards the CLIC vertex detector, many different technologies are being investigated. The current expectation is for a hybrid pixel detector, with the readout ASIC either bump-bonded to slim-edge planar silicon sensors or glued to "active" HV-CMOS sensors. The first generation of capacitively coupled assemblies for CLIC were tested extensively during 2015, and served as input to the design of new devices, created specifically to meet the vertex detector requirements. An overview of the measurements leading up to their design will be presented, along with the final design of both the readout ASIC (CLICpix2) and the HV-CMOS sensor (C3PD). Parallel developments on power-pulsing of the electronics, crucial to achieve the low power budget required at CLIC, will also be presented.

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