FONT meeting

Consensus on fitting and data cuts
+
SIS digitiser saturation levels in ADCs

N. Blaskovic, T. Bromwich, R. Ramjiawan

Fits and cuts to data

Fitting

- Theta → orthogonal fit → clustered or not clustered (importance of error propagation?).
- Scale factor → polyfit (as it is dependent/independent variables) → clustered or not clustered (to account for mover jitter.

Cuts

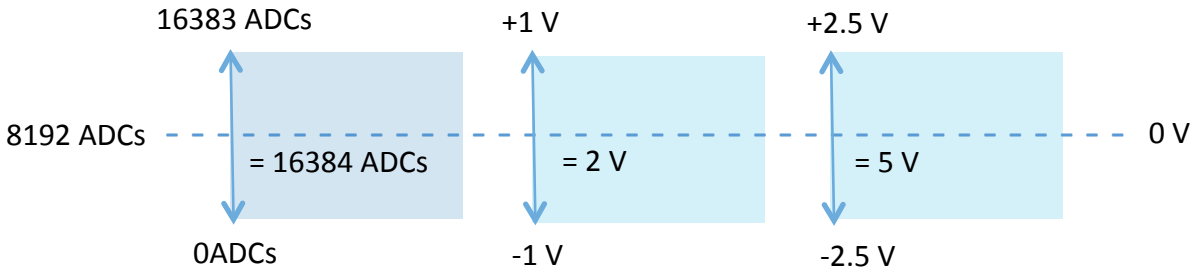
- Check for saturation in just the sample window, remove whole trigger.
- Subtract SIS pedestal.
- Reference threshold cut in the sample window, remove whole trigger.
- 2 x 3-sigma cut on the reference.
- 2 x 3-sigma cut on I/q and Q/q per mover setting (?)

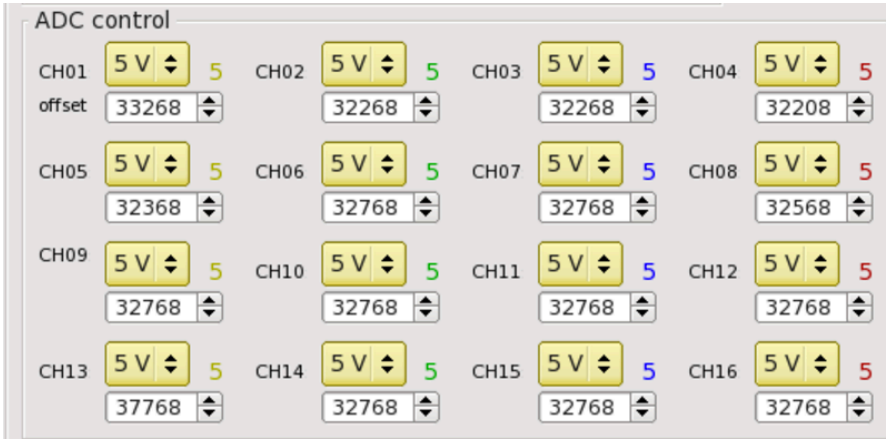
Additional step for jitter

- 2 x 3-sigma cut on I'/q and Q'/q.

Saturation levels in SIS ADC counts

- We believe the processing electronics saturate at approximately ± 0.3 V for the dipole cavity signals.
- 14-bit ADCs on SIS digitiser. ADC count range: 2^{14} = 16384 possible ADC count values.
- The SIS digitiser has default zero offset of 8192 ADC counts. This offset can be set to any value using a digital offset in the ATF DAQ, but is not recorded in the data file.
- The voltage range on each ADC channel of the SIS digitser can be set to 2V or 5V in the ATF DAQ. This setting is recorded in the data header file.





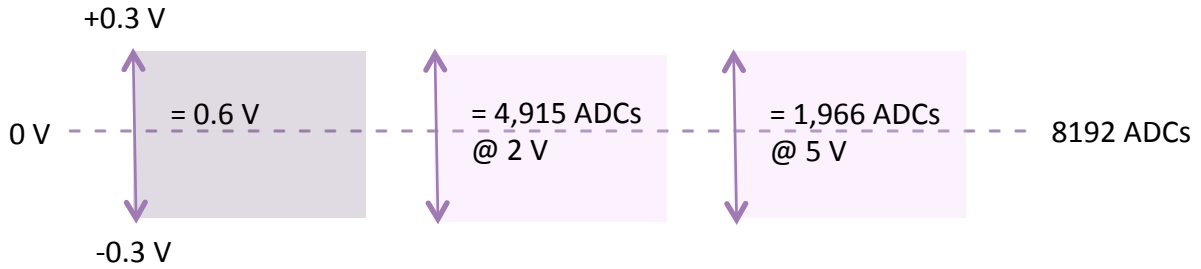
Panel in ATF DAQ to set ADC zero offset and voltage range for each channel of the SIS digitiser

I and Q saturation levels in SIS ADC counts

- Calculate the SIS ADC range that is within the approximate saturation limits of the electronics.

Saturation with 2 V setting: $\frac{16384}{2V} \times 0.6V = 4915$

Saturation with 5 V setting: $\frac{16384}{5V} \times 0.6V = 1966$

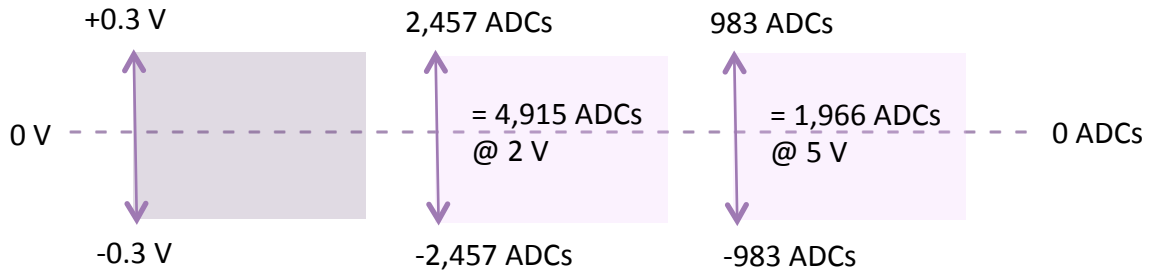


- In practice, the zero offset is usually removed as a first step in analysis.

Within saturation limits, this allows approximately:

± 2,500 ADC counts at 2V

± 1000 ADC counts at 5V



Motivation for reference voltage range

Bench test of limiter/int detector module

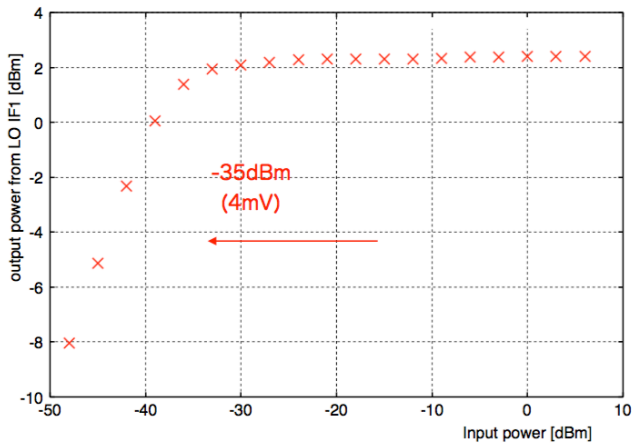
Y.Honda

2006/10/23

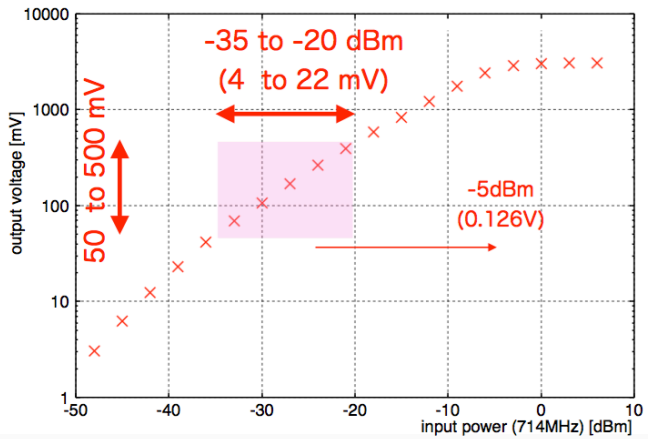
概 要

The limiter/int detector module newly made for IP-BPM was tested in detail. This module produces LO to be used in the phase detector module. Stable output in amplitude and also in phase is needed. We have determined the range of input power to satisfy such requirements.

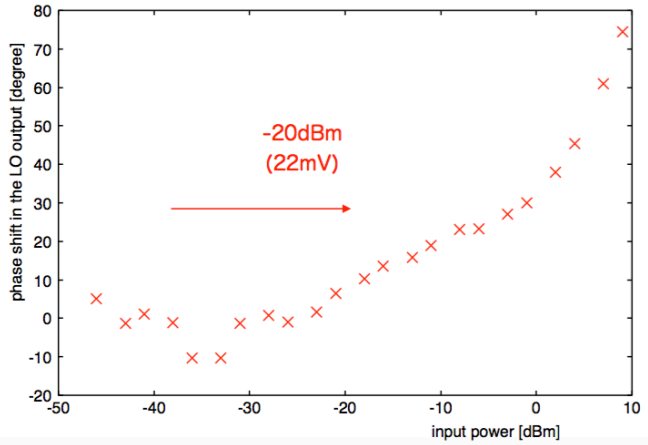
Limiter Output Amplitude



Intensity Detector



Limiter Output Phase



Note by Honda-san:
The performance of the limited detector for the output amplitude and phase, where flat amplitude for the input of greater than –35dBm and zero phase change (or stable phase) for the input of less than –20dBm. Therefore, the input power must be in the range from –35dBm to –20dBm.

Left bottom figure shows the intensity detector performance, where it can work for the input of less than –5dBm. Pink square shows the proper working area of the limited detector.

Tauchi-san's comment:
The note suggested that the intensity detector/monitor should be used for the proper working input signals. That is, the intensity output amplitude must be kept in a range from 50 to 500mV (actually negative output).

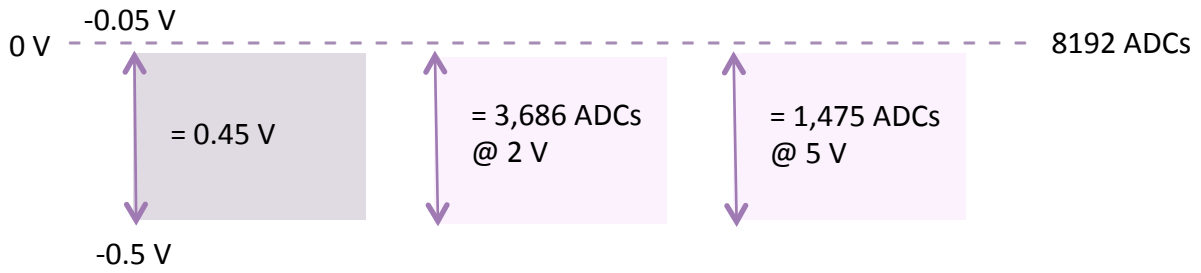
Therefore, the intensity must not be saturated, but it should be within 50 to 500mV. In order to adjust it, a variable attenuator must be put in the input signal as also suggested in the note.

Reference saturation levels in SIS ADC counts

- Calculate the SIS ADC range that is within the approximate saturation limits of the electronics.

Saturation with 2 V setting: $\frac{16384}{2V} \times 0.45V = 3686$

Saturation with 5 V setting: $\frac{16384}{5V} \times 0.45V = 1475$

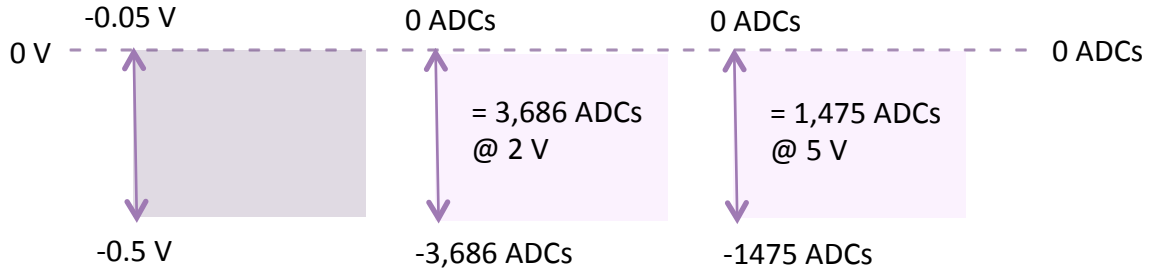


- In practice, the zero offset is usually removed as a first step in analysis.

Within saturation limits, this allows approximately:

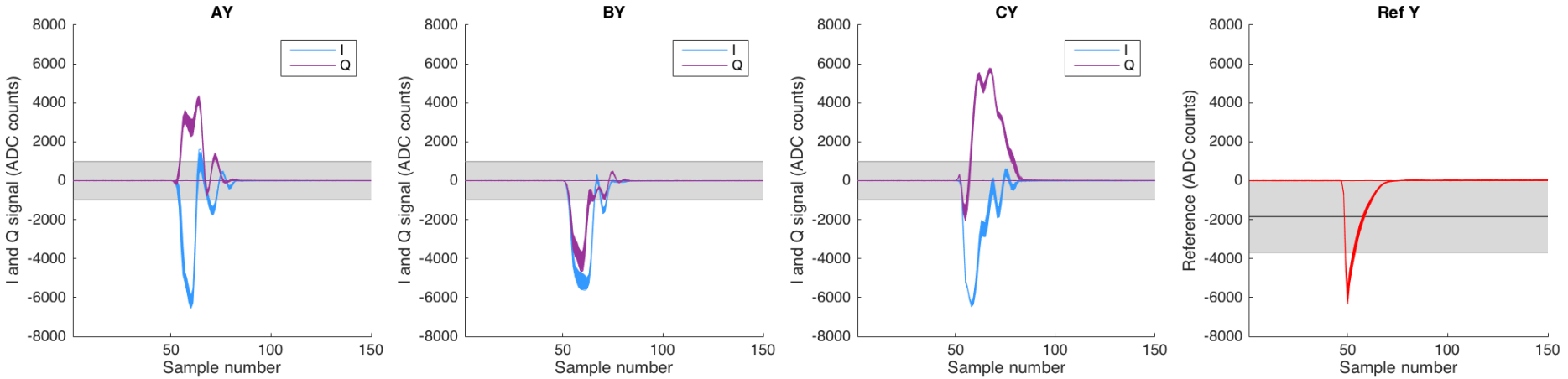
-3686 ADC counts at 2V

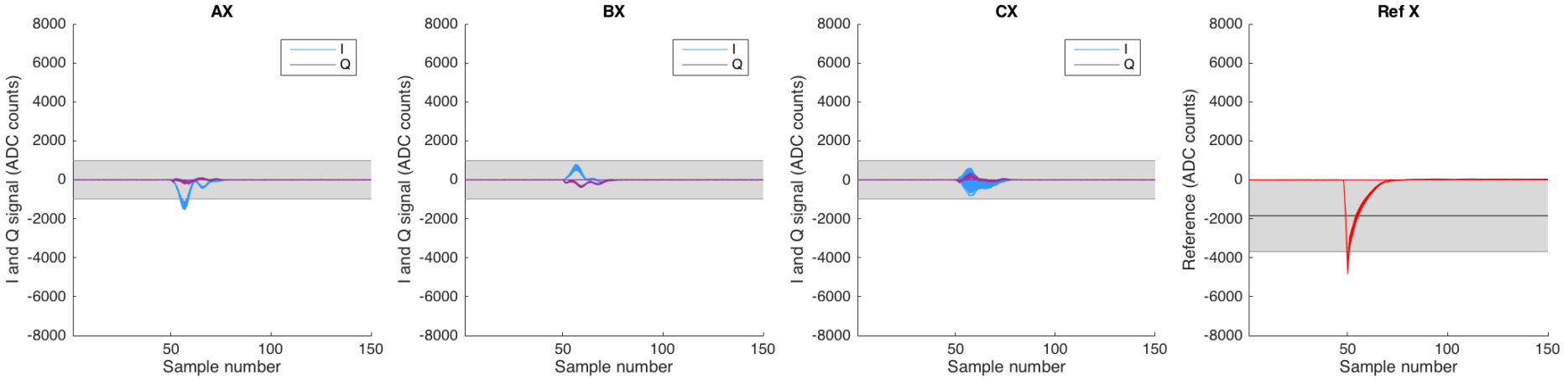
-1475 ADC counts at 5V



Examples of ADC levels

jitRun33_0dB_0.95_ipbpm_160316





Charge ~ 9.1 x 10^{10}

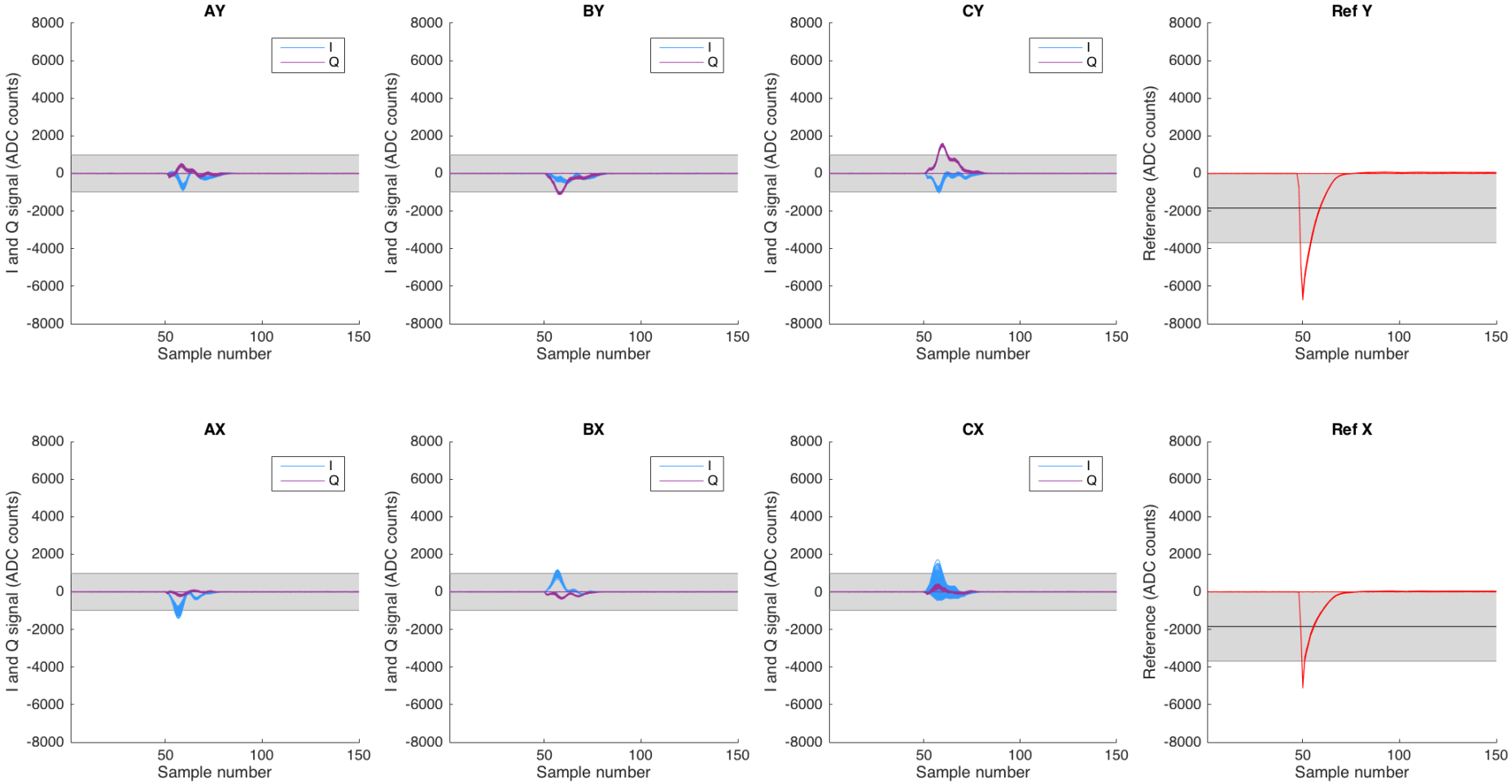
Att Y sig = 0 dB
Att X sig = 20 dB
Att Ref = 50 dB

Y/X chan = 5 V
Ref chan = 2 V

ADC region within the limits of saturating the processing electronics is shaded grey. Everything outside this region may be saturating.

Examples of ADC levels

jitRun3_30dB_ipbpm_160315



Charge ~ 9.8 x 10^{10}

Att Y sig = 30 dB
Att X sig = 20 dB
Att Ref = 50 dB

Y/X chan = 2 V
Ref chan = 2 V

ADC region within the limits of saturating the processing electronics is shaded grey. Everything outside this region may be saturating.