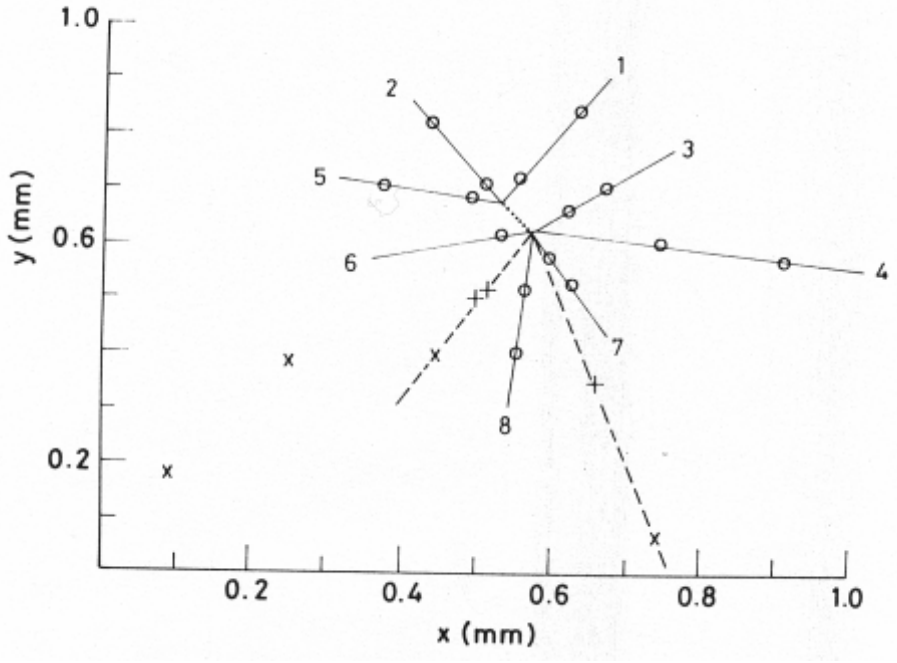
ILC Vertex detectors – Ringberg Castle Post-workshop Summary

Chris Damerell
Rutherford Appleton Lab

- Workshop May 28-31 2006
- Very subjective selection of slides from ~30 talks … [even so, much 'additional material' is included in the body of the talk – can't cover all of this]
- All slides available from http://www.hll.mpg.de/~lca/ringberg/
- Talks:
  - Physics/simulations 8
  - Concepts 3
  - Mechanics 2
  - Pixel technologies (*only* pixels presented: some progress since LCWS 1991!) 9
  - Machine bgd 1
  - Electromagnetic interference 1
  - Proposed 'white paper' on the ILC vertex detector 1
  - Other (ALICE, STAR, SOI(Sucima), EUDET, Castle's history ..)
- ILC Vertex detector 'white paper'
- Moving towards technology selections

- **ACCMOR at Ringberg Castle, 1980**
- **Can you pick out the pioneers of high pressure drift chambers, silicon misrostrip detectors, silicon active target, silicon drift detectors and silicon pixel sensors for use as vertex detectors?**
- **Also, topological vertex reconstruction for flavour ID**


1.0
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y (mm)
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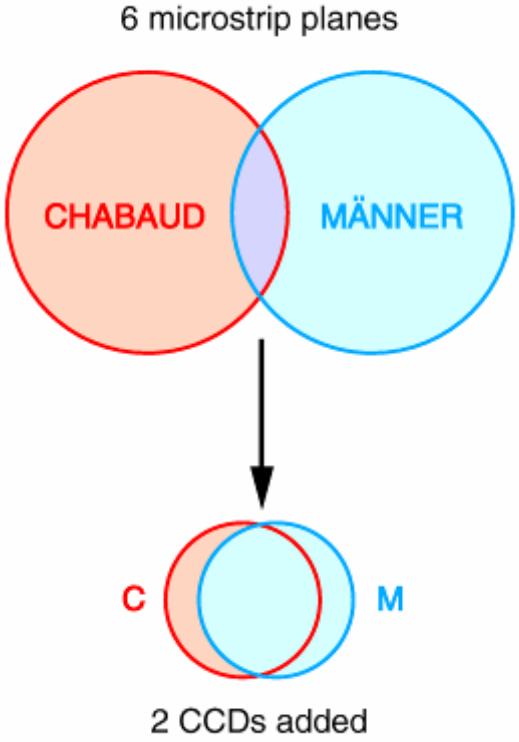

6 microstrip planes
CHABAUD
MÄNNER
C
M
2 CCDs added

Physics and simulations

- **Talks by Marco Battaglia, Thorsten Kuhl, Frank Gaede, Damien Grandjean, Alexei Raspereza, Sonja Hillert**

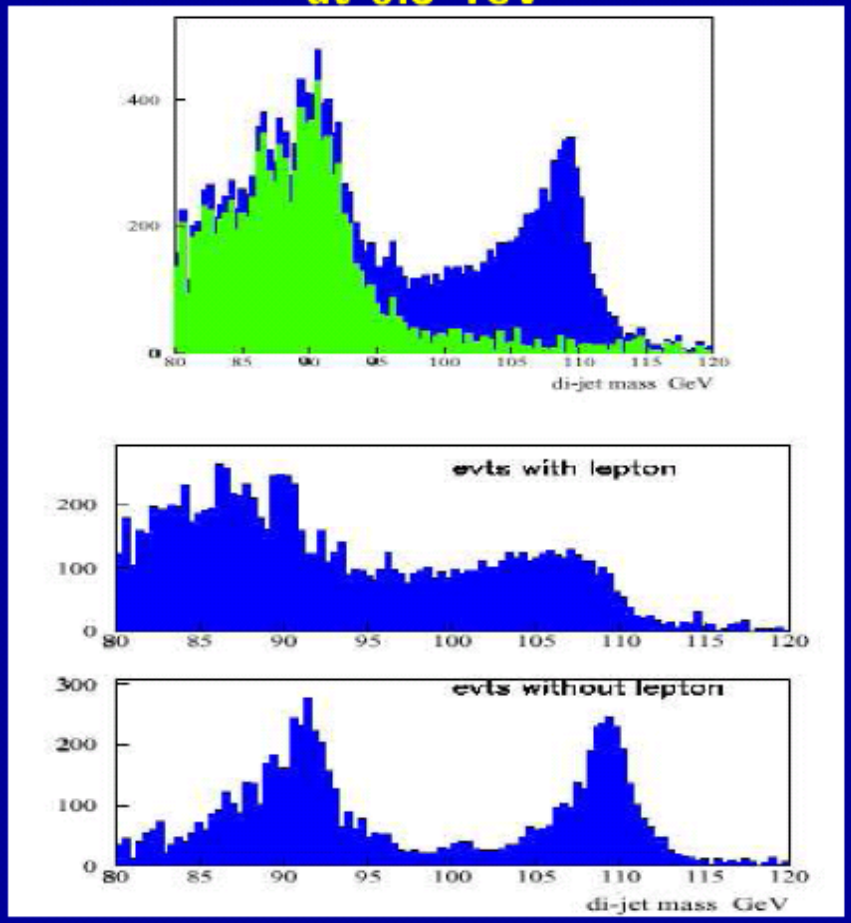
$e^+e^- \to Z^0H^0,\ H^0 \to b\bar{b}$

✧ Detailed study of Higgs couplings to fermions and gauge bosons, requires use of inclusive 4-jet events where $H \to b\bar{b} \to \ell X$ will distort the M_{JJ} invariant mass distribution;

✧ Important to tag secondary leptons in jets to apply corrections and determine b direction from vertexing information in these cases;

✧ Single secondary particle tagging in b jet.

$e^+e^- \to H\nu\bar{\nu}$ and $e^+e^- \to ZZ\nu\bar{\nu}$ at 0.5 TeV



Benchmarking Vertex Charge

$e^+e^- \to Z^0H^0H^0,\ H^0 \to b\bar{b}$

✧ Aid three boson reconstruction by reducing combinatorial with vertex charge determination;

✧ Jet tagging and vertex charge reconstruction in multi jet final state with significant heavy flavour background.

$e^+e^- \to H^+H^-,\ H \to tb$

✧ SUSY loop contributions ($\tilde{t}$, $\tilde{b}$, $\tilde{g}$) may induce sizeable CP asymmetry in heavy Higgs boson decays:

$$\delta CP = \frac{\Gamma(H^- \to b\bar{t}) - \Gamma(H^+ \to t\bar{b})}{\Gamma(H^- \to b\bar{t}) + \Gamma(H^+ \to t\bar{b})}$$

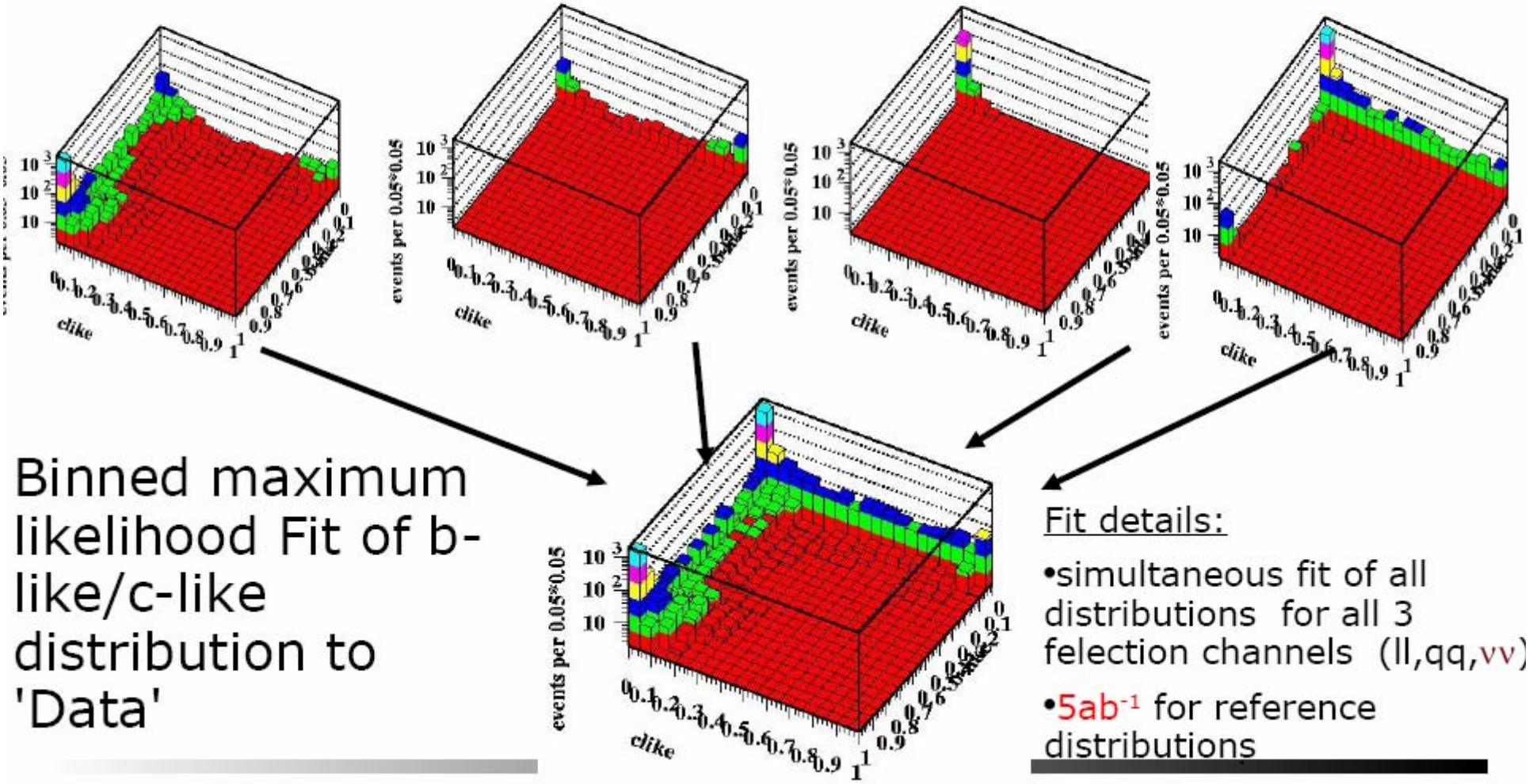
✧ Jet tagging and vertex charge reconstruction in very high jet multiplicity.

- **Marco summarised items from the report of the Physics Benchmark Panel, set up at LCWS 2005. Published March 2006, hep-ex/0603010 v1**

- **Associating leptons with B/D decay vertices and pi-zeroes also (latter by p_t balance) are topics still to be explored, but will provide part of the case for best possible discrimination between secondary and tertiary vertices through the detector volume – easily overlooked**

Braching ratio extraction

$ZH \rightarrow \nu\nu(ll,qq)bb + ZH \rightarrow \nu\nu(ll,qq)cc + HZ \rightarrow \nu\nu(ll,qq)gg$ + background=



Binned maximum likelihood Fit of b-like/c-like distribution to 'Data'

Fit details:

- simultaneous fit of all distributions for all 3 felection channels (ll,qq,νν)
- $5ab^{-1}$ for reference distributions

Comparison with other analyses

	$\Delta(\sigma BR)/(\sigma BR)(bb)$	$\Delta(\sigma BR)/(\sigma BR)(cc)$	$(\sigma BR)/(\sigma BR)(gg)$
This analysis	1,1%	12,1%	8,3%
TDR(Battaglia) *	0,9%	8,0%	5,1%
Snowmass(Brau,Potter)	1,6%	19,0%	10,4%

- A lot of these anaysis were done scaling 1 or 2 channels
- TDR analysis:
  - Error 50% larger
  - But selection much more efficient in qqnn and qqll
  - Difference: optimistic jet-based flavor tag parametrisation based on monojets: no jet-jet confusion, no gluon splitting ...
- Snowmass (Brau/Potter)
  - Flavor tag a bit better (1.2cm inner radius)
  - Similar analysis using only qqqq and qqll
  - Cuts for flavor separation instead 2-dim fit
- J-C Brient (direct measurement from recoil events): error in binominal error treatment, extraction should be redo.

Conclusion

- Results for flavor tagging
- Detector:
  - Most important: innermost layer
- Flavor tag:
  - B-Tag robust (LEP Btagger as good as „Tesla“)
  - C-Tag is the benchmark!
- Use realsistic and comparable physics and tools
- Several analysis for higgs Branching ratios/jet flavour tagging done
  - Differences are well understood
  - Mostly differences in analysis technics
- No Beam related background studied (the biggest difference between different detector concepts ?)
- 5 year develoment (Hawkins, Xella, Wing, de Groot, Raspereza, Desch, Kuhl...)

- **This important work is just about to be published**
- **It was the most thorough physics analysis based on the simulation/reconstruction code developed for the TESLA TDR (Brahms and Simdet, with NN combination of ZVTOP and ALEPH code for flavour ID)**
- **Urgent need to re-open the door for such studies for the three concepts and different vertex detector options**
- **Getting close, with help of LCIO for code sharing. See following talks by Gaede, Grandjean, Raspereza and Hillert – a loosely coordinated international team effort**

Proposal for an LCIO vertex class

EVENT::Vertex

+ ~ Vertex()
+ *getMomentum() : const float**
+ *getMass() : float*
+ *getCharge() : float*
+ *getPosition() : const float**
+ *getCovMatrix() : const FloatVec&*
+ *getChi2() : float*
+ *getProbability() : float*
+ *getPreviousVertex() : Vertex**
+ *getParameters() : const FloatVec&*
+ *getTracks() : const TrackVec&*
+ *addTrack(track : Track*) : void*

EVENT::ReconstructedParticle

+ ~ ReconstructedParticle()
+ *getType() : int*
+ *isCompound() : bool*
+ *getMomentum() : const double**
+ *getEnergy() : double*
+ *getCovMatrix() : const FloatVec&*
+ *getMass() : double*
+ *getCharge() : float*
+ *getReferencePoint() : const float**
+ *getParticleIDs() : const ParticleIDVec&*
+ *getParticleIDUsed() : ParticleID**
+ *getGoodnessOfPID() : float*
+ *getParticles() : const ReconstructedParticleVec&*
+ *getClusters() : const ClusterVec&*
+ *getTracks() : const TrackVec&*
+ *addParticleID(pid : ParticleID*) : void*
+ *addParticle(particle : ReconstructedParticle*) : void*
+ *addCluster(cluster : Cluster*) : void*
+ *addTrack(track : Track*) : void*

- original LCIO idea:
  use ReconstructedParticle also for compound objects like jets and vertices
- LCFI proposes dedicated vertex class
- need to optimize to avoid overlap and
- redundancy with ReconstructedParticle

http://forum.linearcollider.org

Summary

- the VTX detector is now becoming to be treated properly in the ILC software framework:
  - improved full simulation in Mokka
  - vertex detector raw data classes in LCIO
  - a vertex class for LCIO under development
  - proper digitization and reconstruction code in Marlin (talks: M. Bataglia, A. Raspereza)
- still lacking: GEAR API and xml description of VTX

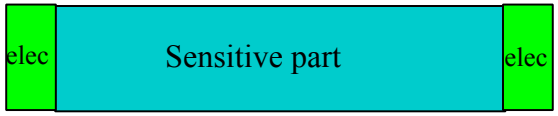
your input is needed !

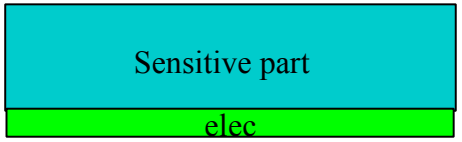
- Outlook:
  - have implementation of MokkaGear for VTX to automatically create xml description

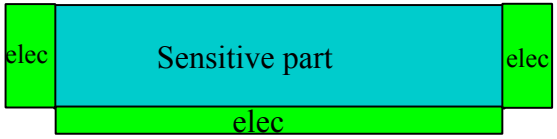
go to the software portal for more information:
http://ilcsoft.desy.de

- LCIO is now the *de facto* persistency and data model for ILC software
- Original idea of the LCIO group was to include vertices in the 'reconstructed particle' class, as they do for jets
- However, vertices have particular attributes (parent and daughter vertices, decay directions wrt their parents, etc) which make it more natural to create a new vertex class
- The driving motivation is to produce the most user-friendly code, as opposed to a black box, opaque to all except a few specialists
- Class LCEvent contains collections of objects of the different data types, including (if this proposal is agreed) vertex objects (one PV, and some numbers of secondary and tertiary vertices in decay chains, mostly associated with specific jets in the event)

Goals and requirements of the simulation

- Optimised the VTX design
  - Number of layers
  - Acceptance
  - Material budget
  - Physic study capabilities
- Simple modification of the geometry by any users
  - Using a configuration file
- Consider all technologies
  - CCD 

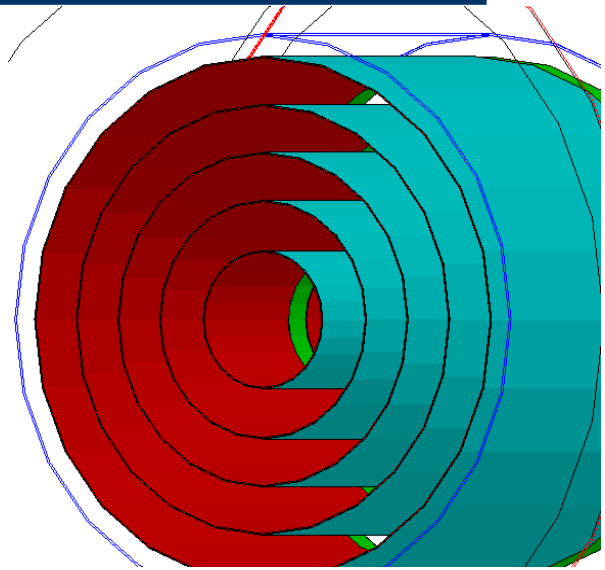
  - CMOS 

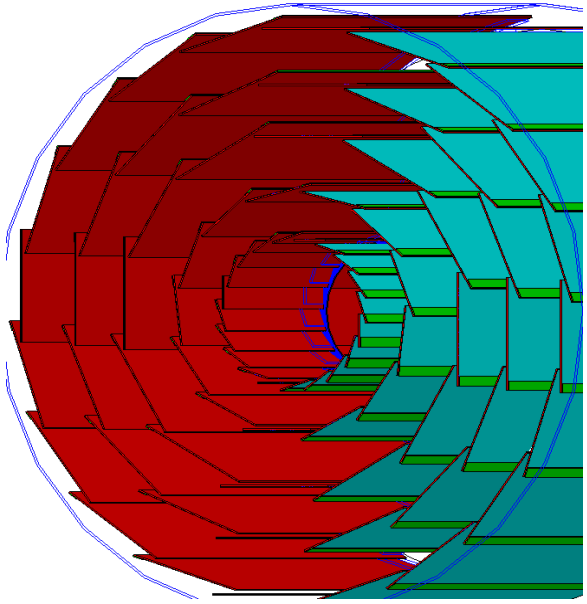
  - DEPFET 

    - Differences between technologies from the simulation point of view :
      - **Readout and control electronic location**
      - **Cryostat needed or not**
      - **Cooling system**
      - **Ladder mechanical support**

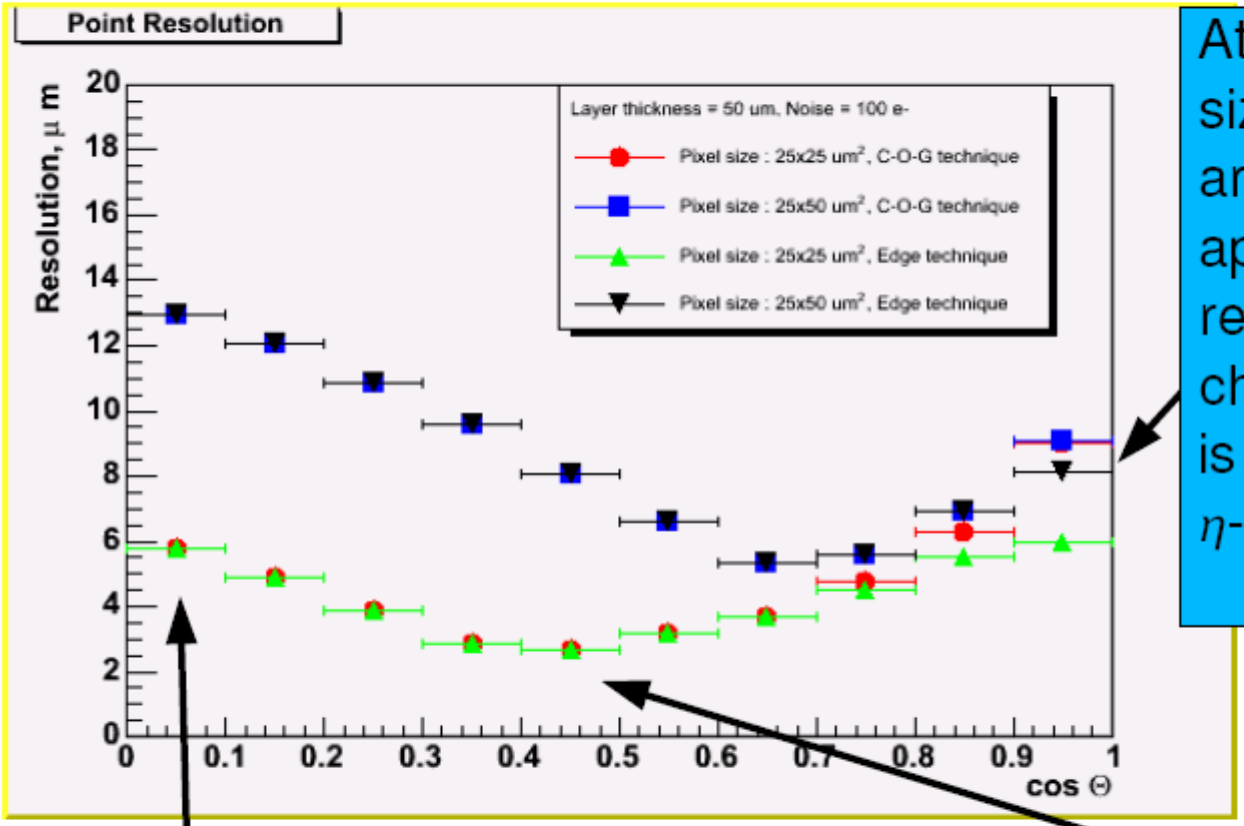
First flexible geometry version /1

- Implementation of a realistic geometry
  - Old version: VXD00
    - Layer designed with cylinder of materials
      - Too far from reality
      - Can't be used for design optimization
  - New version: VXD01 (available from Mokka 05.02 release)
    - Layers designed with ladders
      - Realistic material budget
      - All technologies can be considered





Point Resolution in Z



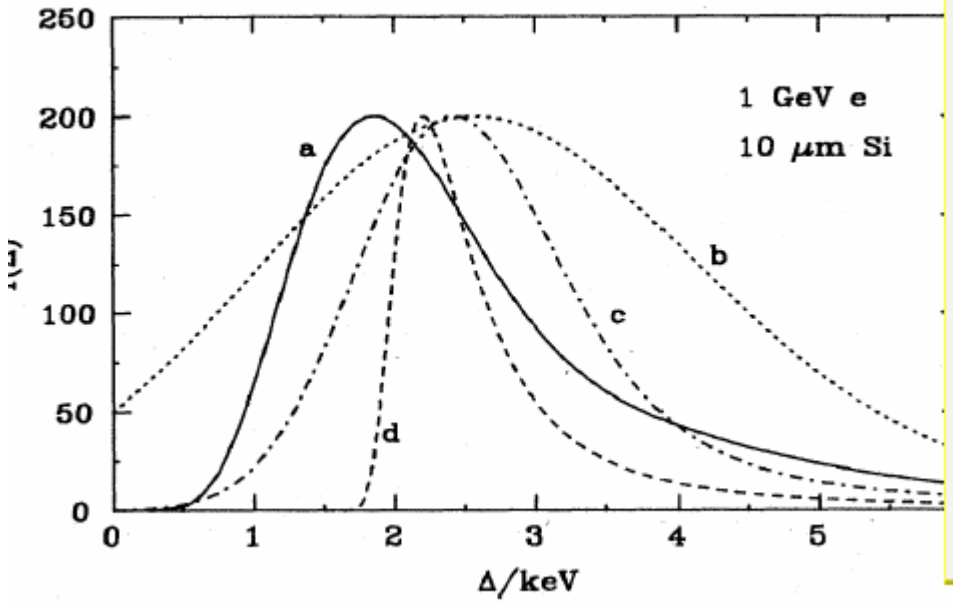
At shallow angles cluster size gets extremely large and simple centre-of-gravity approach yeilds poor resolution due to inter-pixel charge fluctuations. Resolution is improved by means of η-algorithm (edge-technique)

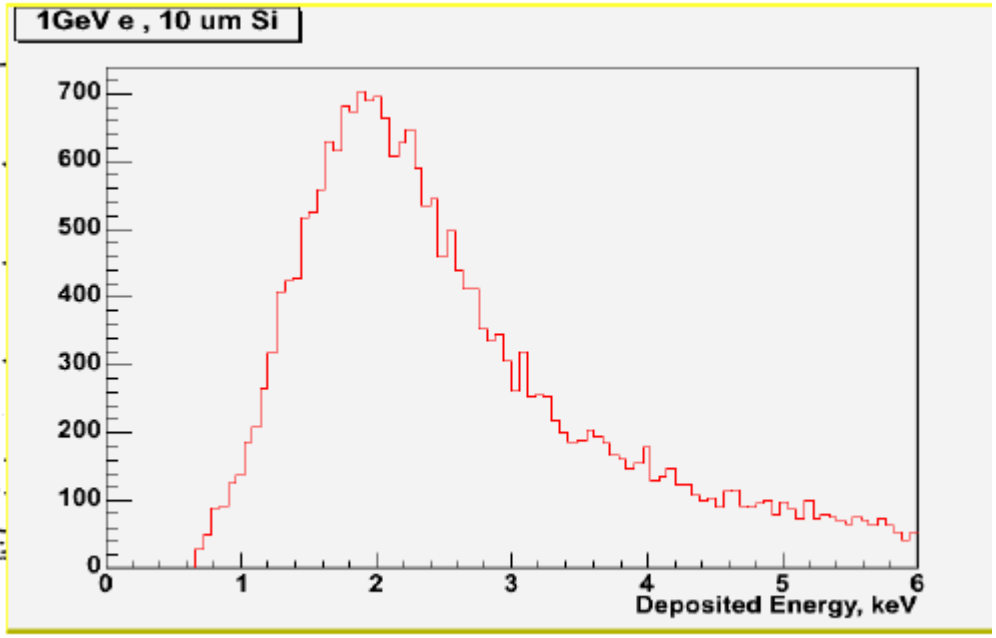
In many cases at normal incidence only one row is fired : resolution is limited by pixel size

When track is inclined more than one row is fired -> resolution gets better

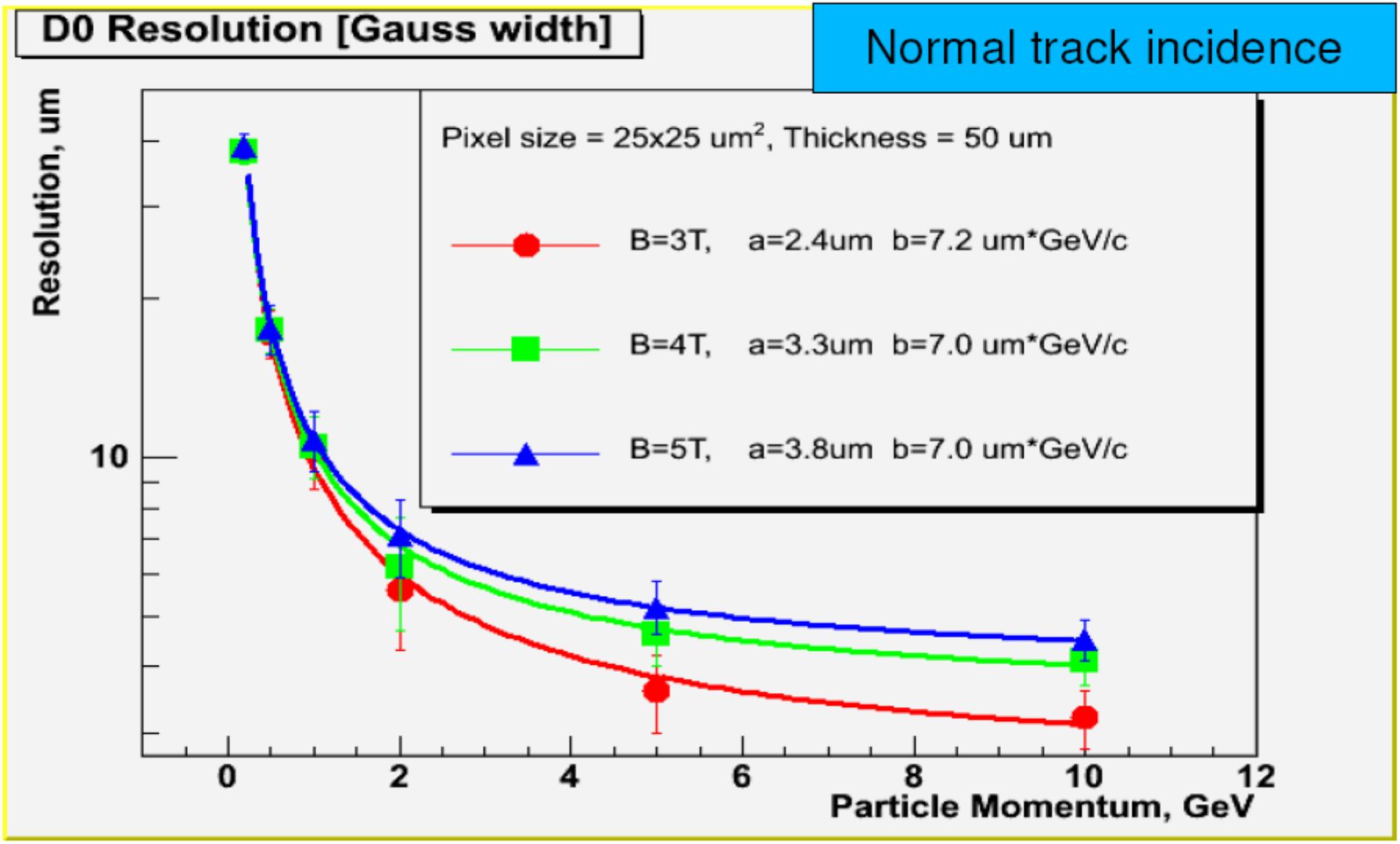
Is G4 Simulation of E_{loss} Fluctuations @ Short Flight Distances reliable?

H.Bichsel Rev. Modern Physics 60-3 (1998) plot a)	G4 Simulations





IP Resolution [Gauss Width]

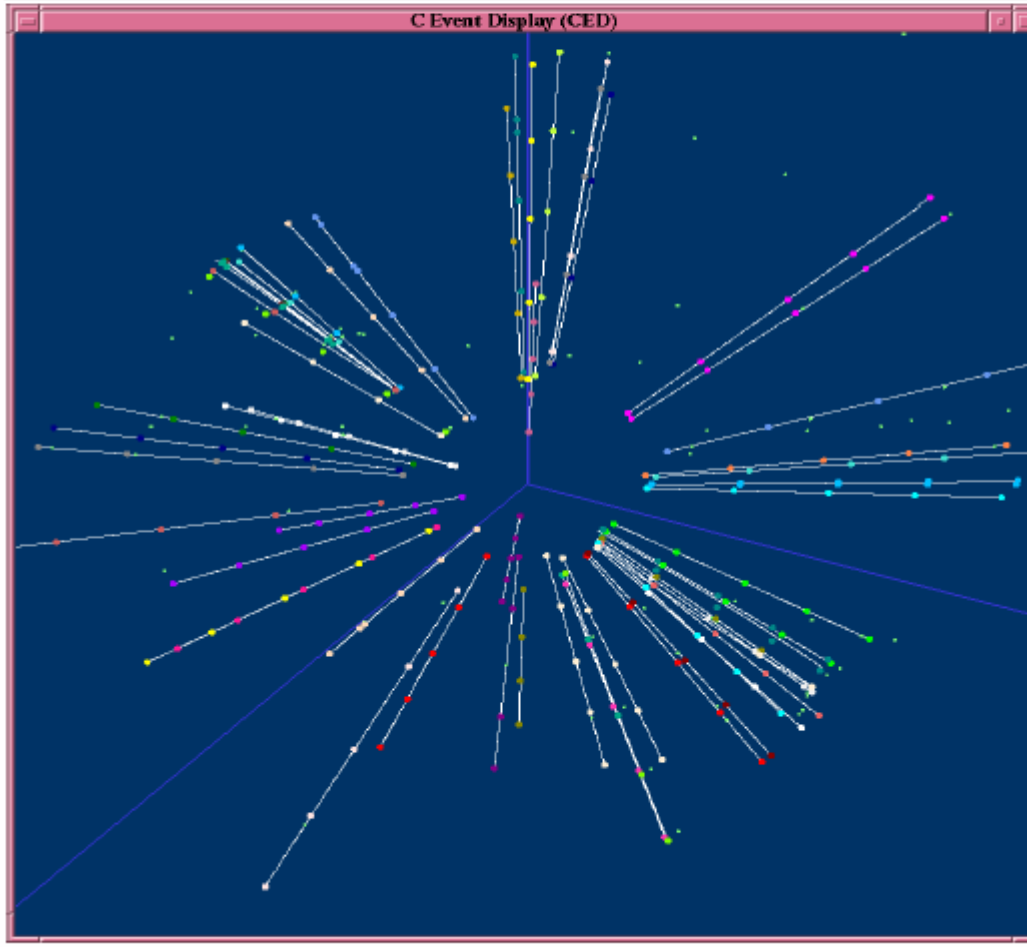


Stand-alone Pattern Recognition in VXD

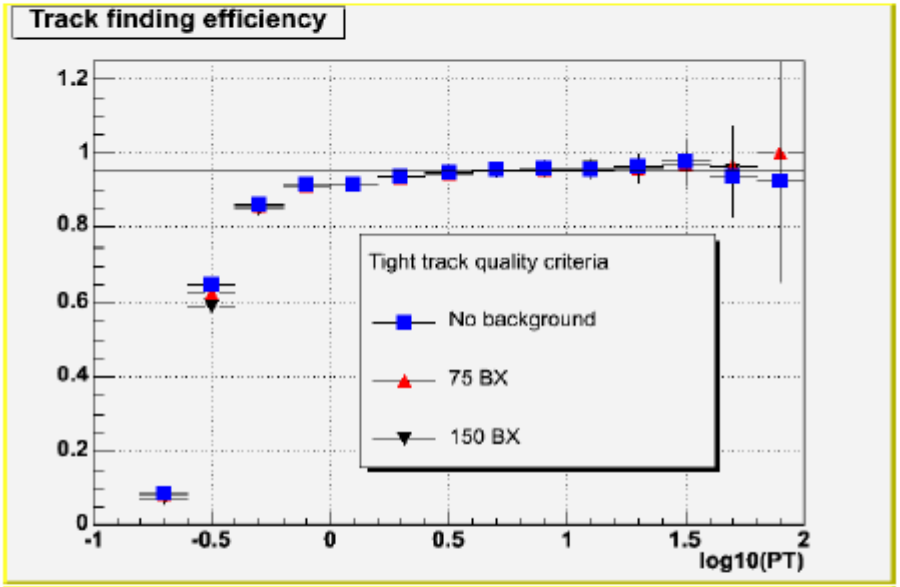
Algorithm features:

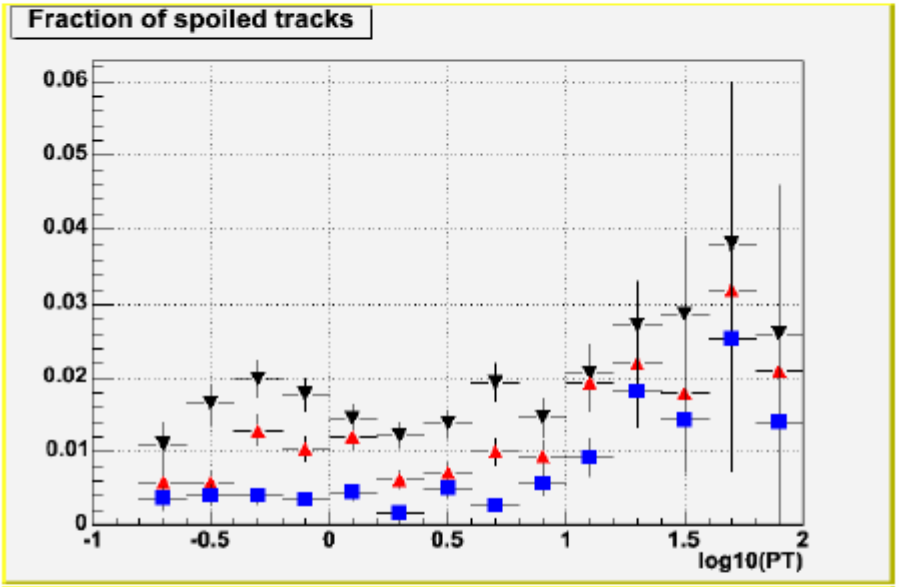
- Starts with finding triplets in the outer layers
- Inward search for additional hits
- Good χ^2 of helix fit – main criterion to accept track candidates
- Additional loose cuts against fake tracks composed of background hits:
  - D_0, Z_0 < 10mm
  - P_T > 100 MeV
  - # hits in track candidate > 3

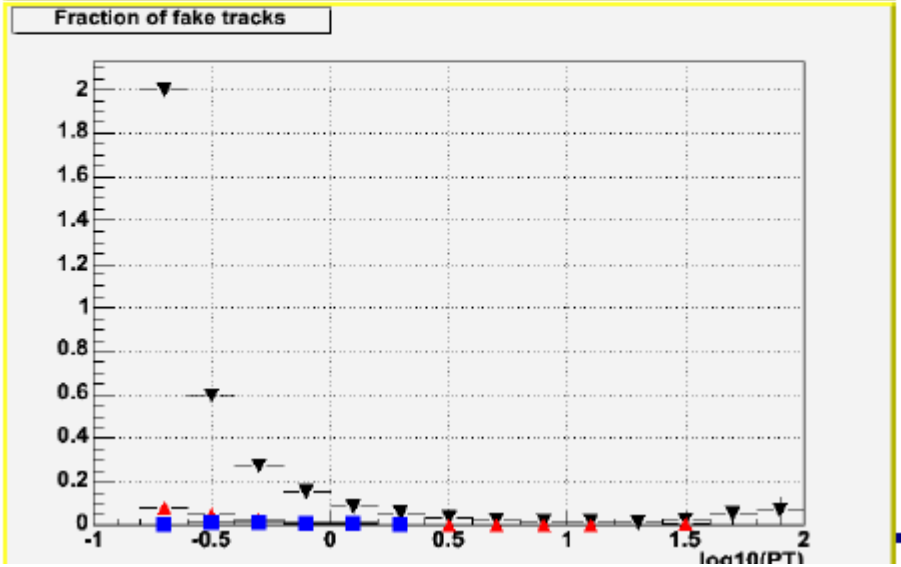
$t\bar{t} \Rightarrow$ 6jet event @ $\sqrt{s}$ = 500 GeV

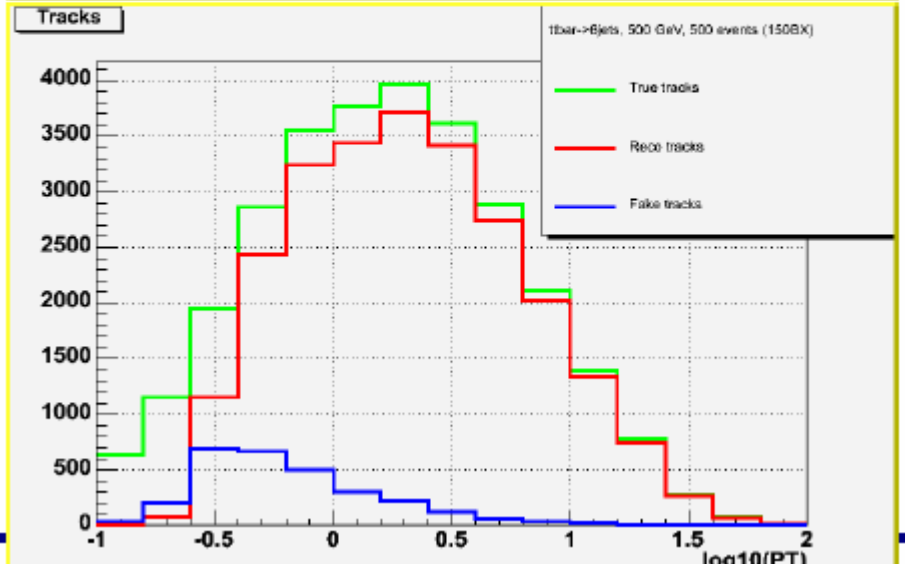


Pattern Recognition Performance in Presence of Backgrounds

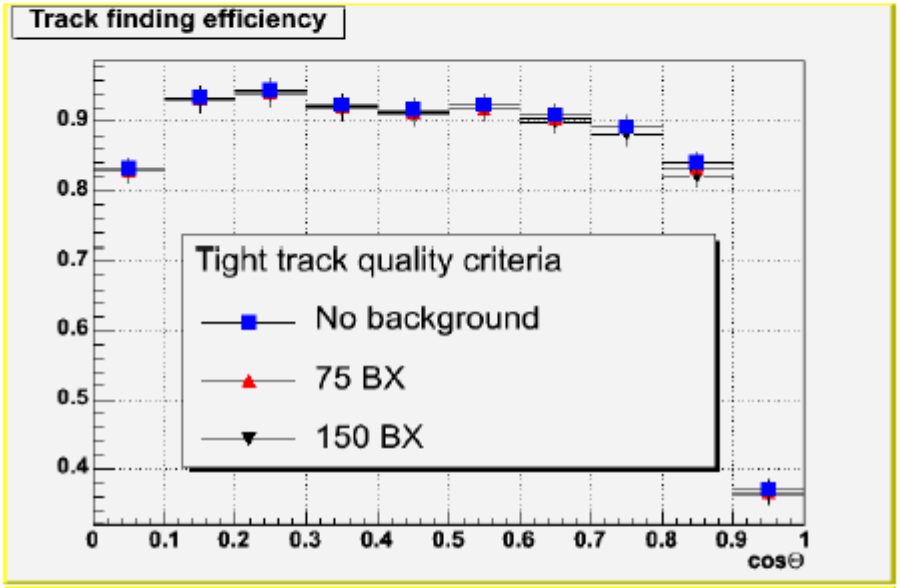


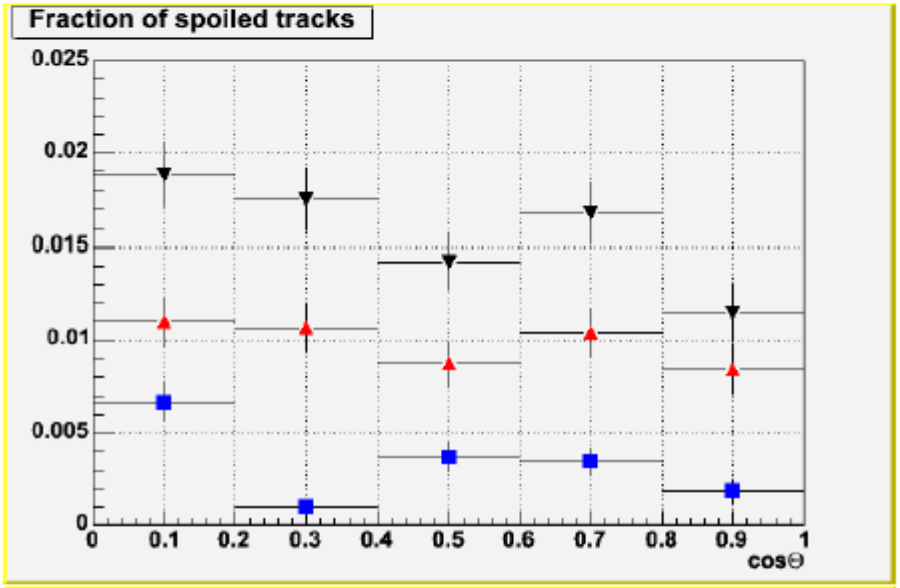


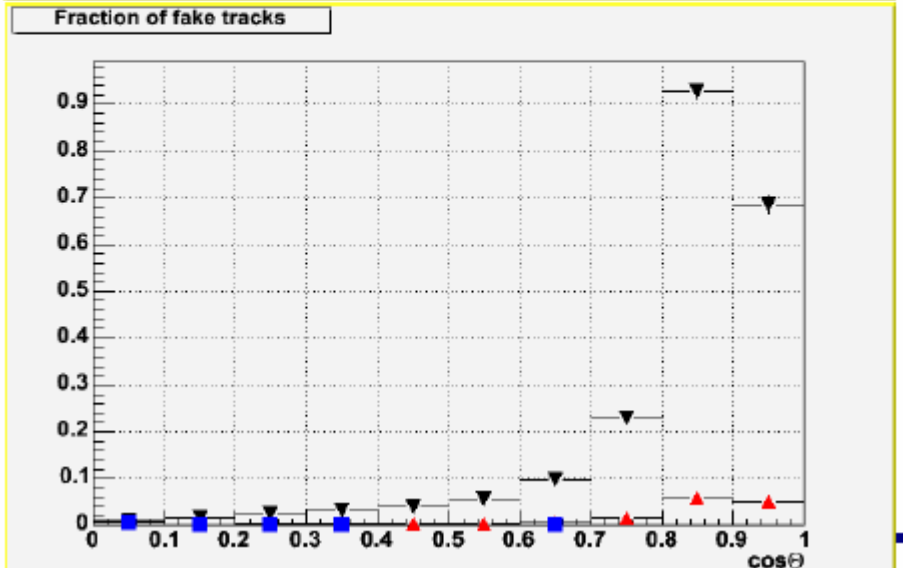


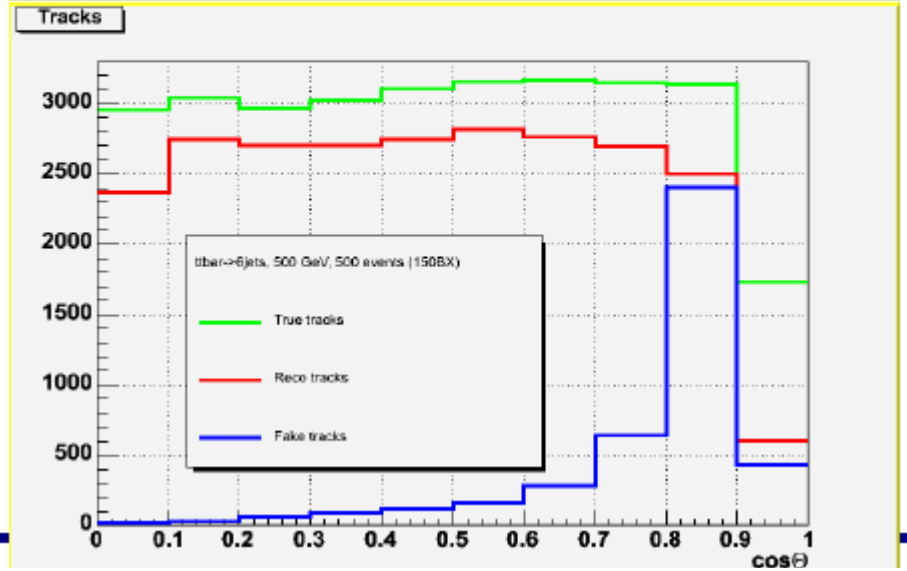


Pattern Recognition Performance in Presence of Backgrounds



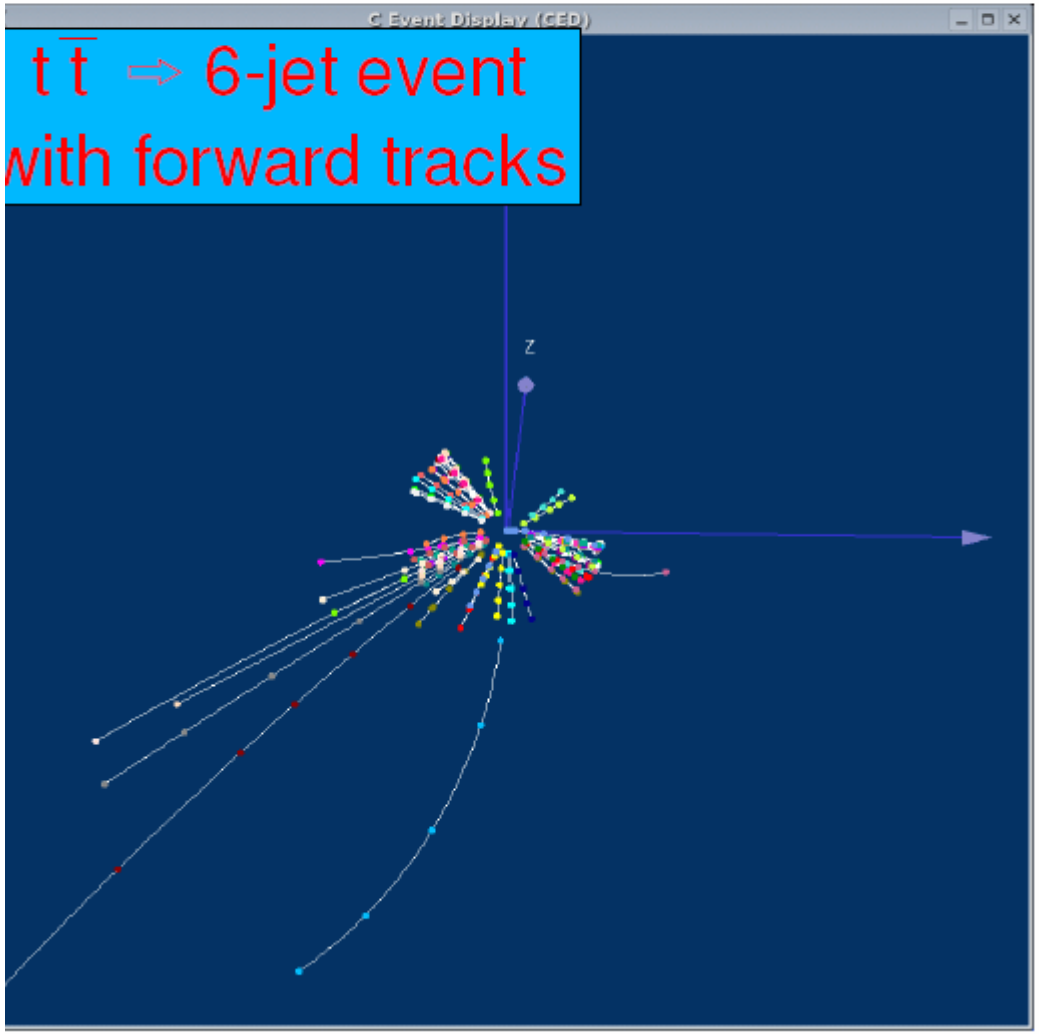


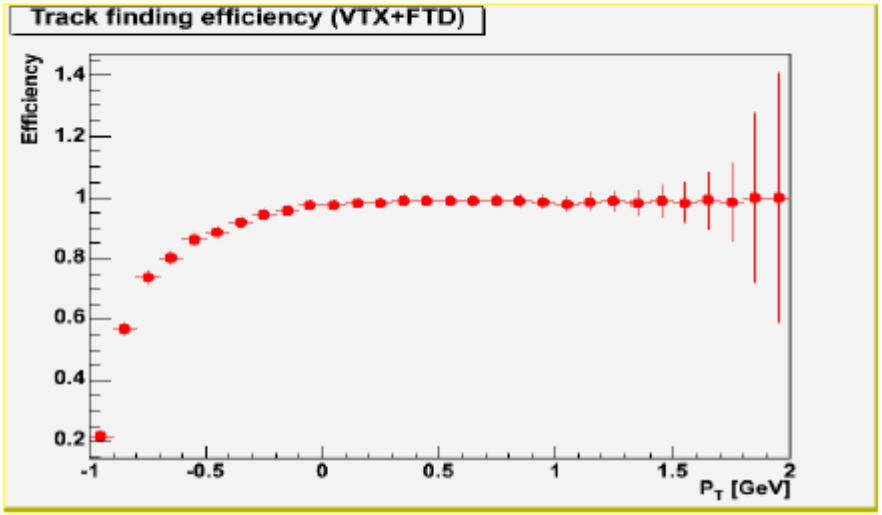


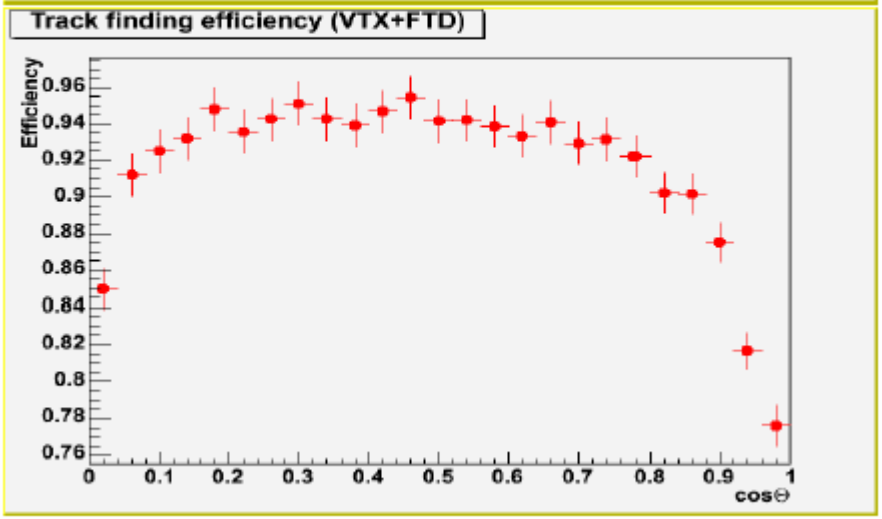


Current Developments

- Since recently pattern recognition includes also tracking in FTD

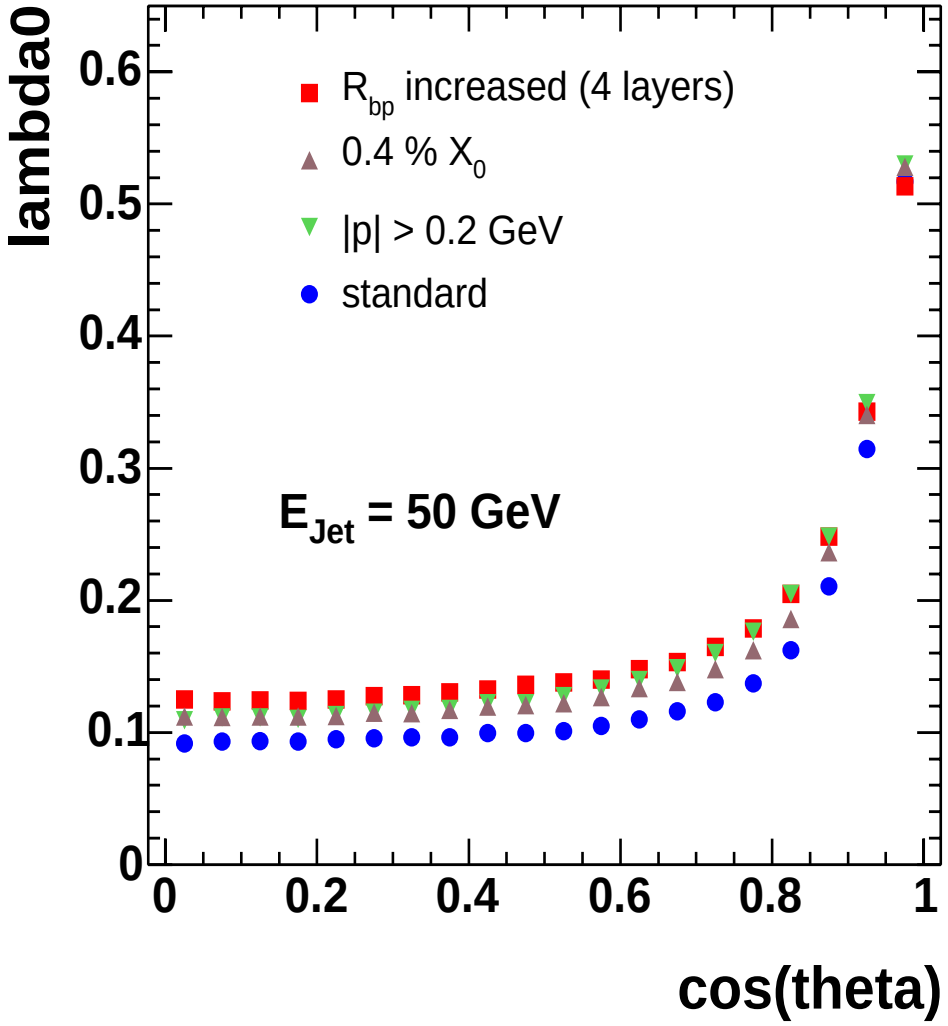






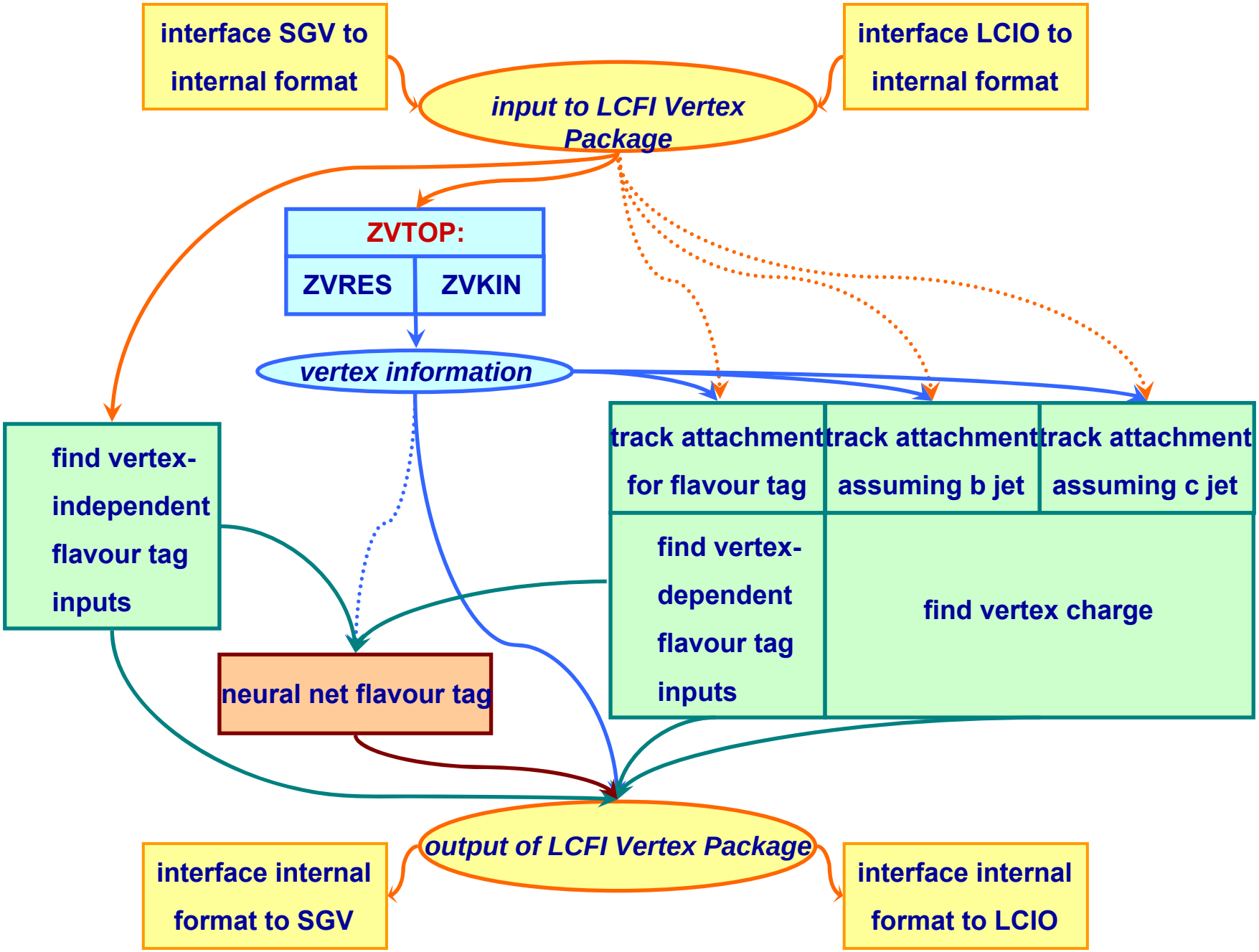
- DEPFET-based detector shows mild degradation in spatial resolution with B field, due to increasing Lorentz angle
- G4 is OK even for thin silicon sensors (surprise?)
- Standalone VXD track finding gets into trouble for p_t below ~ 300 Mev/c and cos(θ) above 0.8. (poor trk finding effic and many fake trks) This agrees with earlier study by Nick Sinev
- However, promising first look combined VXD + FTD tracking, in LDC
- Argues for thin VXD layers (search area proportional to thickness, for low mom trks) and for an FTD with considerably enhanced performance (additional thin pixel layers to smaller angles?)
- Why work so hard on VXD, but then throw in a FTD one happens to find on the ATLAS shelf? This was identified as a 'missing topic' by the Detector R&D Panel last year. Good to see it getting attention!

Sensitivity to other parameters



- since vertex charge performance is sensitive to multiple scattering need to keep layer thickness small (target 0.1 % X_0)
- also strong dependence on momentum cut (track selection) – this depends critically on tracking performance:
  - track finding capability
  - background rates
  - linking across subdetector boundaries

- should push all these parameters to their limits, as all these effects will eventually add up in the real detector


interface SGV to internal format
interface LCIO to internal format
input to LCFI Vertex Package
ZVTOP:
ZVRES
ZVKIN
vertex information
find vertex-independent flavour tag inputs
track attachment for flavour tag
track attachment assuming b jet
track attachment assuming c jet
find vertex-dependent flavour tag inputs
find vertex charge
neural net flavour tag
output of LCFI Vertex Package
interface internal format to SGV
interface internal format to LCIO

The ZVTOP vertex finder

D. Jackson,

NIM A 388 (1997) 247

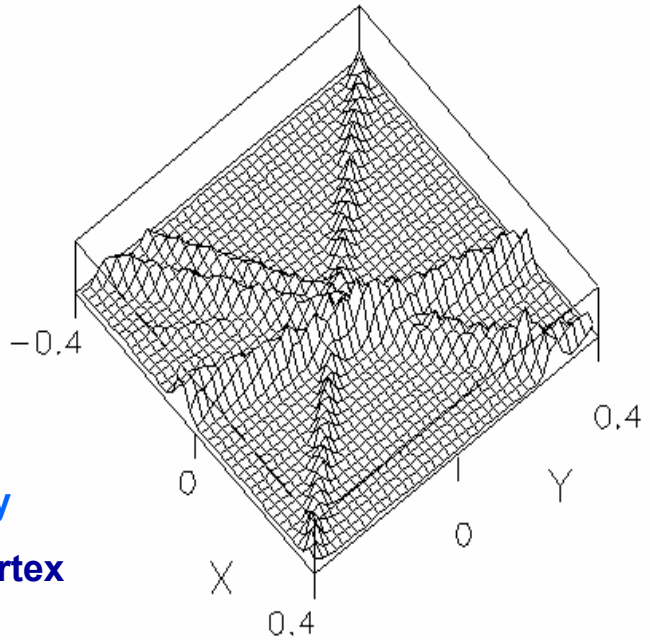
two branches: ZVRES and ZVKIN (also known as ghost track algorithm)

The ZVRES algorithm:

- tracks approximated as Gaussian ´probability tubes´

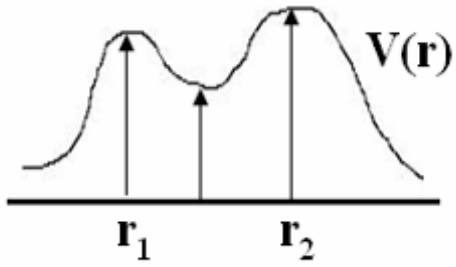
- from these, a ´vertex function´ is obtained:

$$V(\mathbf{r}) = \sum_{i=0}^{N} f_i(\mathbf{r}) - \frac{\sum_{i=0}^{N} f_i^2(\mathbf{r})}{\sum_{i=0}^{N} f_i(\mathbf{r})}$$



- 3D-space searched for maxima in the vertex function that satisfy resolubility criterion; track can be contained in > 1 candidate vertex

- iterative cuts on χ^2 of vertex fit and maximisation of vertex function results in unambiguous assignment of tracks to vertices

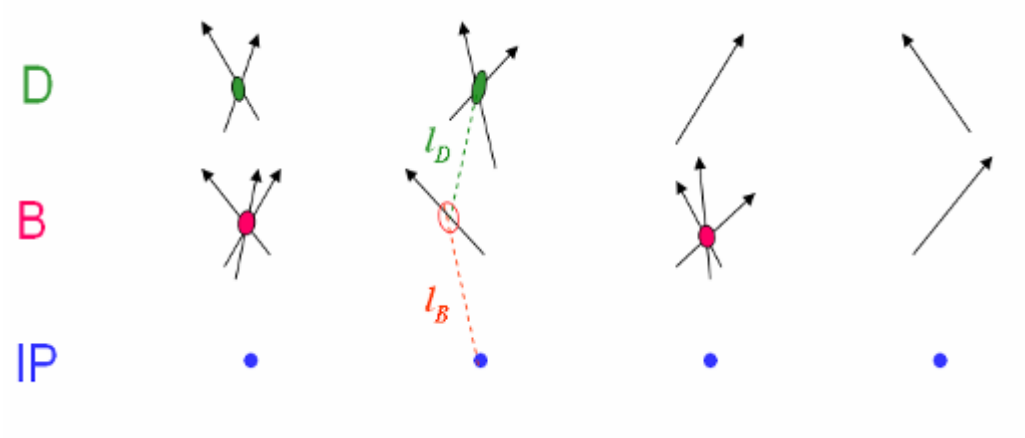


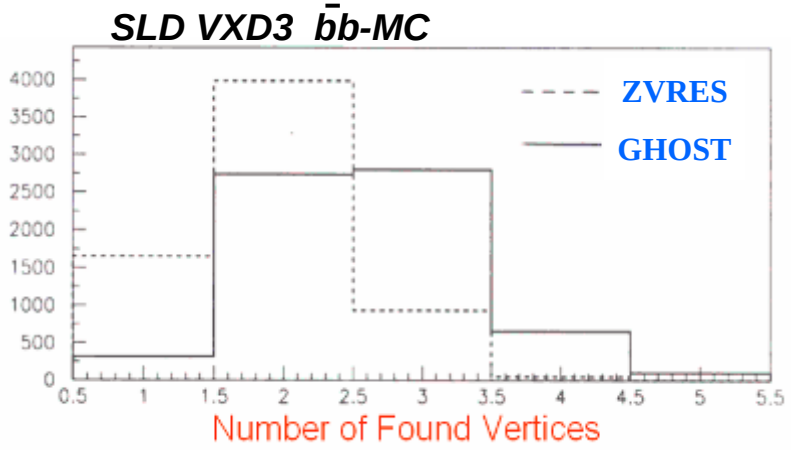
- has been shown to work in various environments differing in energy range, detectors used and physics extracted

- very general algorithm that can cope with arbitrary multi-prong decay topologies

The ZVKIN (ghost track) algorithm

- more specialised algorithm to extend coverage to b-jets in which one or both secondary and tertiary vertex are 1-pronged and / or in which the B is very short-lived;
- algorithm relies on the fact that IP, B- and D-decay vertex lie on an approximately straight line due to the boost of the B hadron





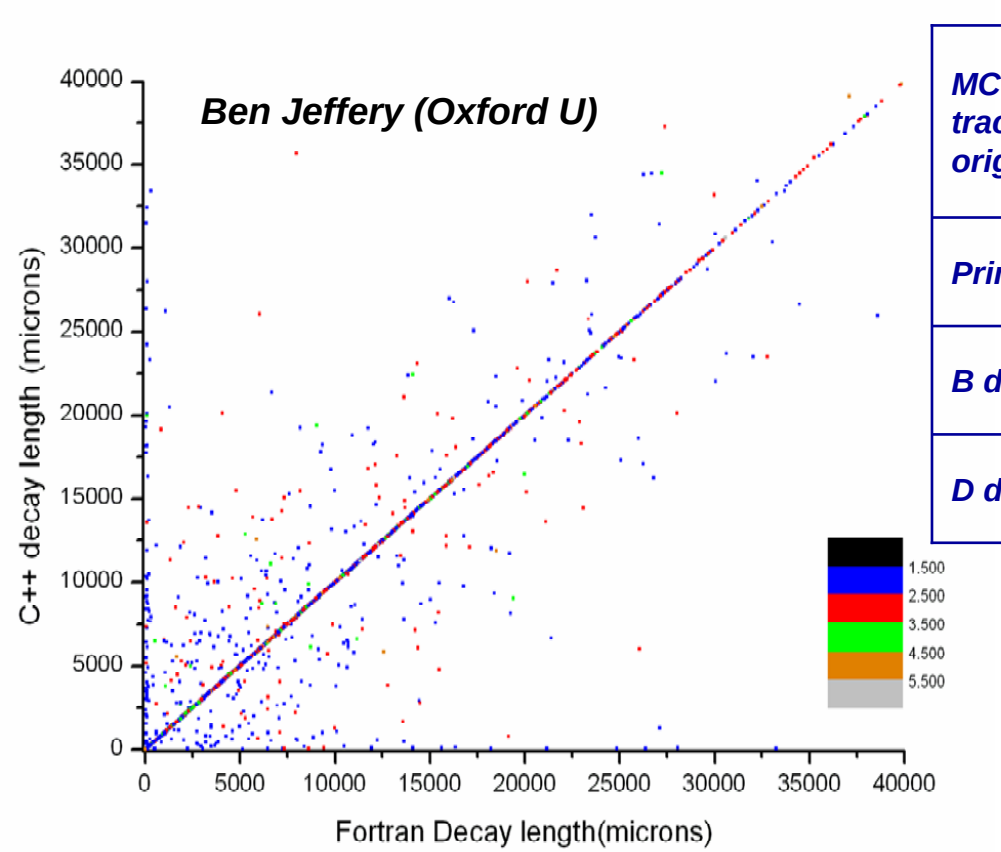
- should improve flavour tagging capabilities

Status of C++ ZVTOP development

- **ZVRES branch: coding completed, validation ongoing**

  left: comparison of decay length reconstructed by C++ to the FORTRAN value

  right: comparison of C++ reconstructed to true track origin (iso = isolated tracks from ZVTOP)



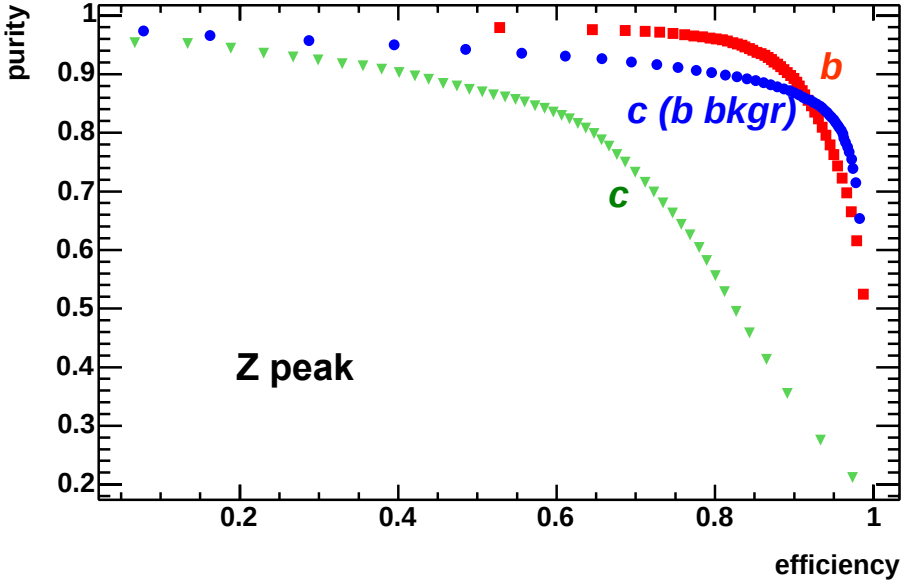
MC track origin	*2 vertices*			*3 vertices*			
	pri	*sec*	*iso*	*pri*	*sec*	*ter*	*iso*
Primary	98.6	0.4	1.1	98.1	1.1	0.0	0.8
B decay	8.8	75.6	15.6	2.3	90.1	3.7	3.9
D decay	2.1	80.5	17.4	0.5	17.8	77.4	4.4

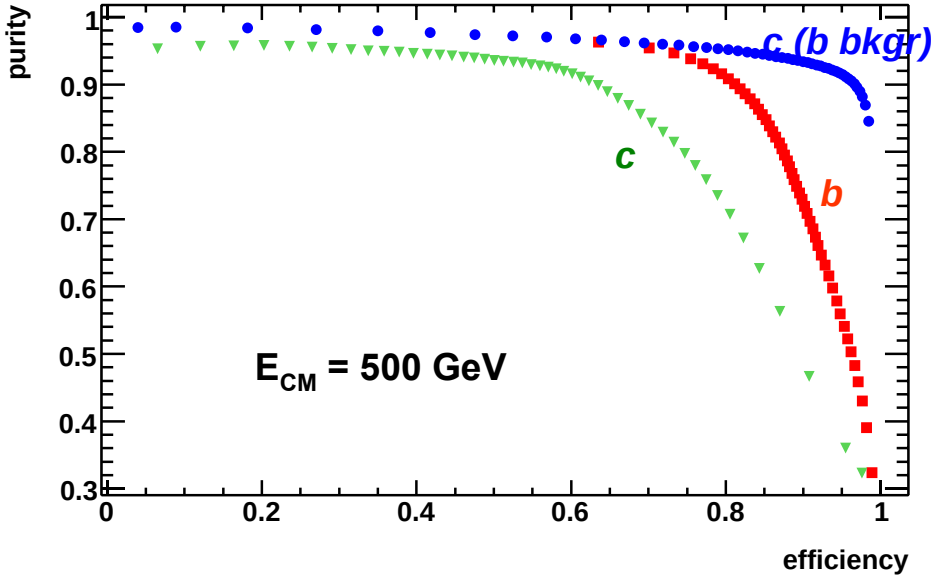
Mark Grimes (Bristol U)

- **coding of ZVKIN branch ongoing, determination of ghost track direction complete**

Towards completion of the Vertex Package

- test of full chain of C++ ZVTOP with FORTRAN flavour tag and vertex charge imminent
- pure FORTRAN results (from SGV) show below:





- C++ code for calculation of inputs for flavour tag being written
- Vertex charge reconstruction for c-jets under development

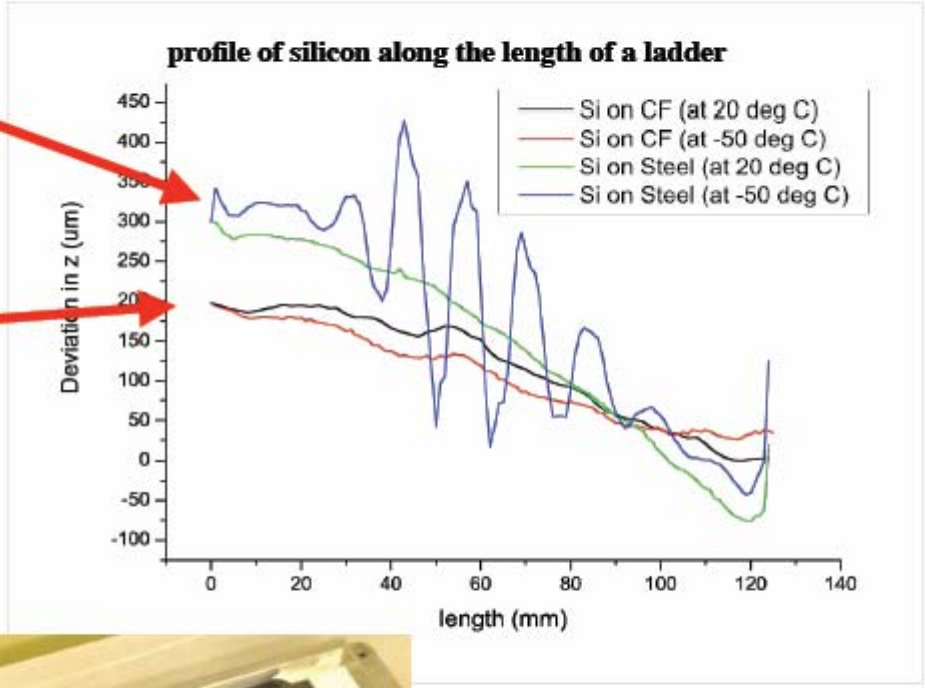
- These tools are eagerly awaited. Small but dedicated team is coming close to delivering the goods …
- These tools will permit detailed quantitative studies of the physics impact of many of the currently debated vertex detector parameters (inner layer radius, layer thickness, pixel size, geometry options, readout speed, …)
- [Some issues, such as radiation hardness and resistance to EMI, will be settled independently]
- Evaluation of 'luminosity factors' for sensitive physics channels will extend the study pioneered at Snowmass
- These studies will also influence the design of FTD (crucial), SIT (is it needed?) and possibly the central tracker (both the silicon and TPC options)
- Highly efficient reconstruction of low momentum tracks from jets of all angles, curved so as to miss the SIT and TPC or main Si tracker, is necessary for *adequate particle flow performance* as well as vertex charge determination

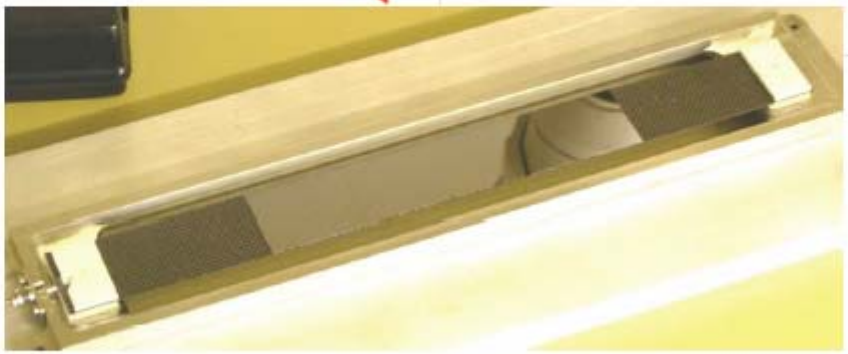
Mechanics

- **Talks by Joel Goldstein and Bill Cooper**

Thin Substrates

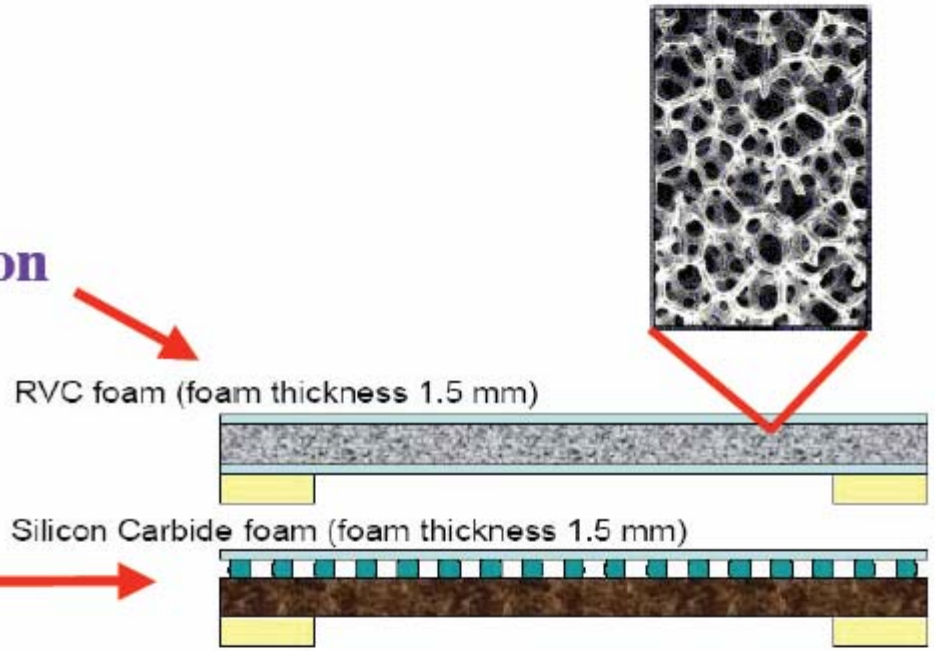
- **Beryllium**
  - **CTE mismatch too large**
- **Carbon fibre**
  - **0.09% X_0 prototype**
- **Ceramics**
  - **Fragile**



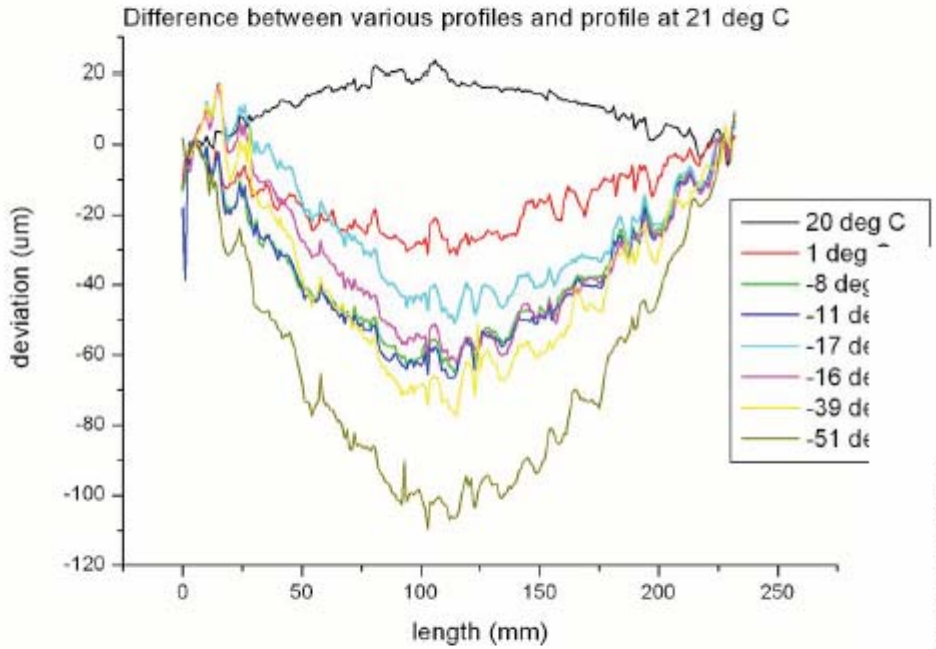


Rigid Structures: Foams

- **3% RVC Sandwich**
  - **0.09% X_0**
  - **Working on glue application**
- **8% Silicon Carbide**
  - **0.14% X0**
  - **3-4% believed possible**

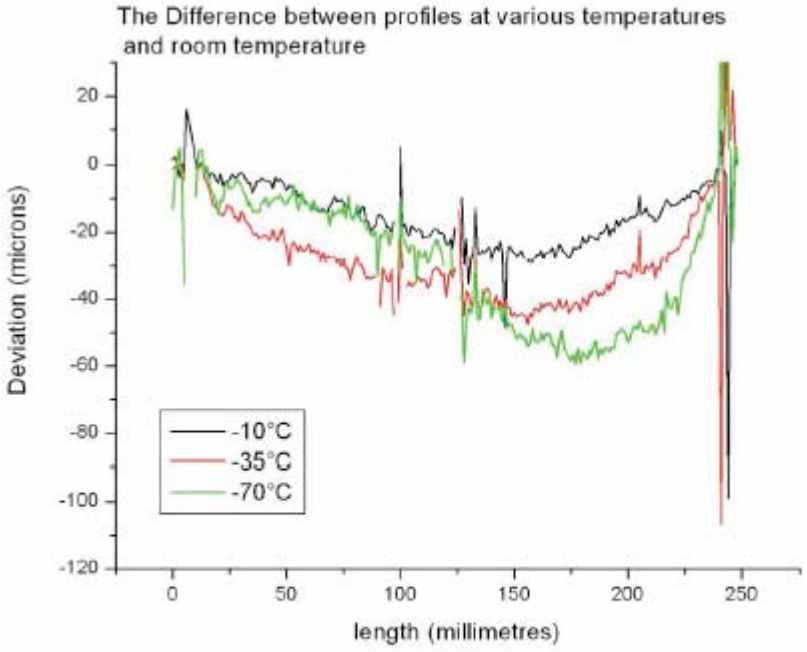


SiC Foam Results



Thin glue layer

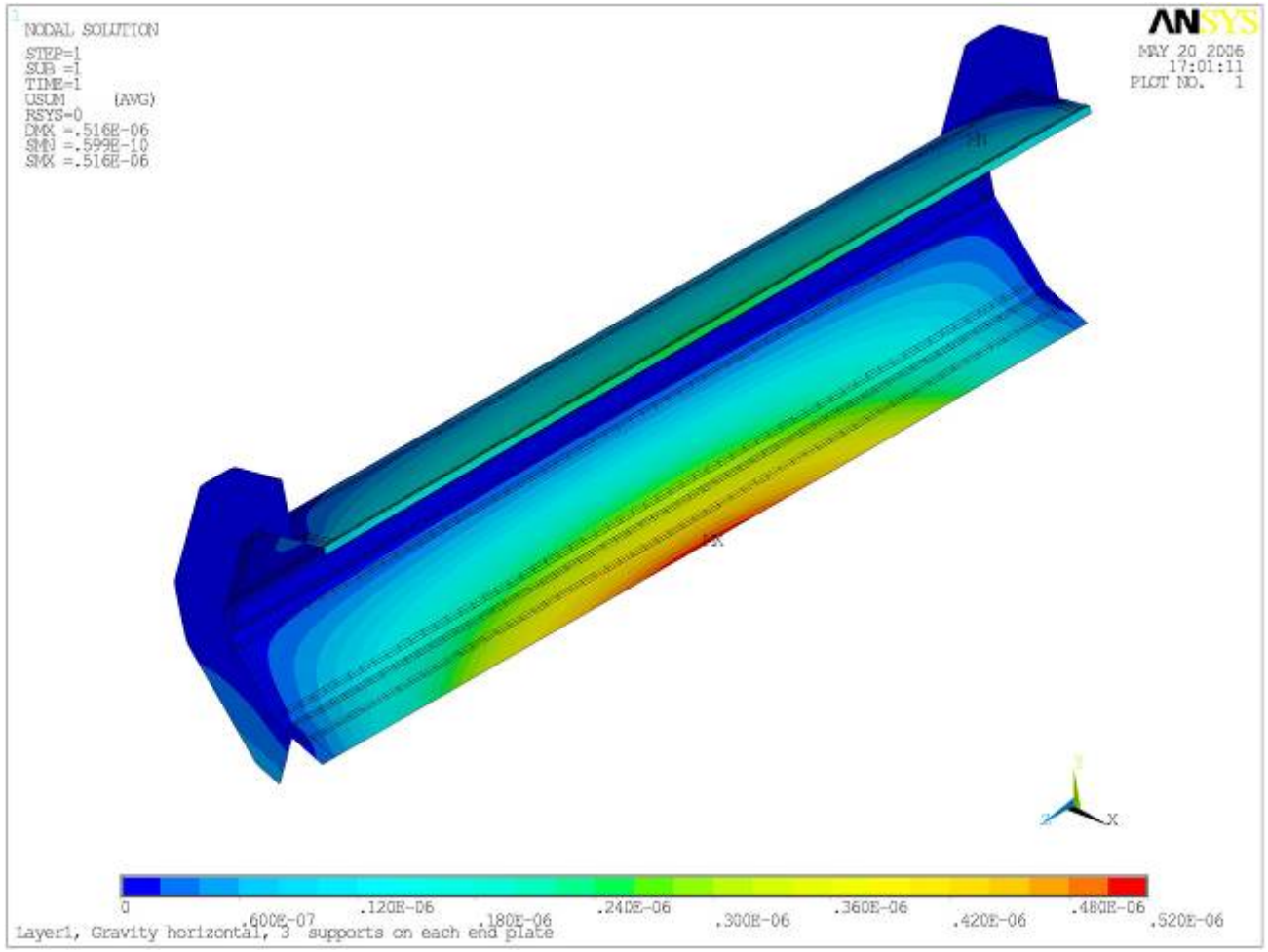
Glue "pillars"



- SLD (VXD2 and VXD3) got some of us into the ladder 'groove'
- A ladder is a handlable item, convenient for adding components (bump-bonded or wire-bonded) and for standalone testing before assembly
- It can provide full-area support for very thin (hence flexible and delicate) sensors
- If mounted appropriately, it can have the advantage of benign behaviour in event of electrical failure/ powering off. This feature may be unimportant if low-CTE substrates are acceptable (to be determined)
    - In this case, mechanical linking after assembly (small glued parts, etc) may improve mechanical stability (reduced susceptibility to bowing and vibration), and allow a reduced material budget, particularly in end-support regions
- May achieve situation where endplate thickness is dominated by electrical components (for some but not all detector options)
- However, there is new creative thinking which goes in a different direction …

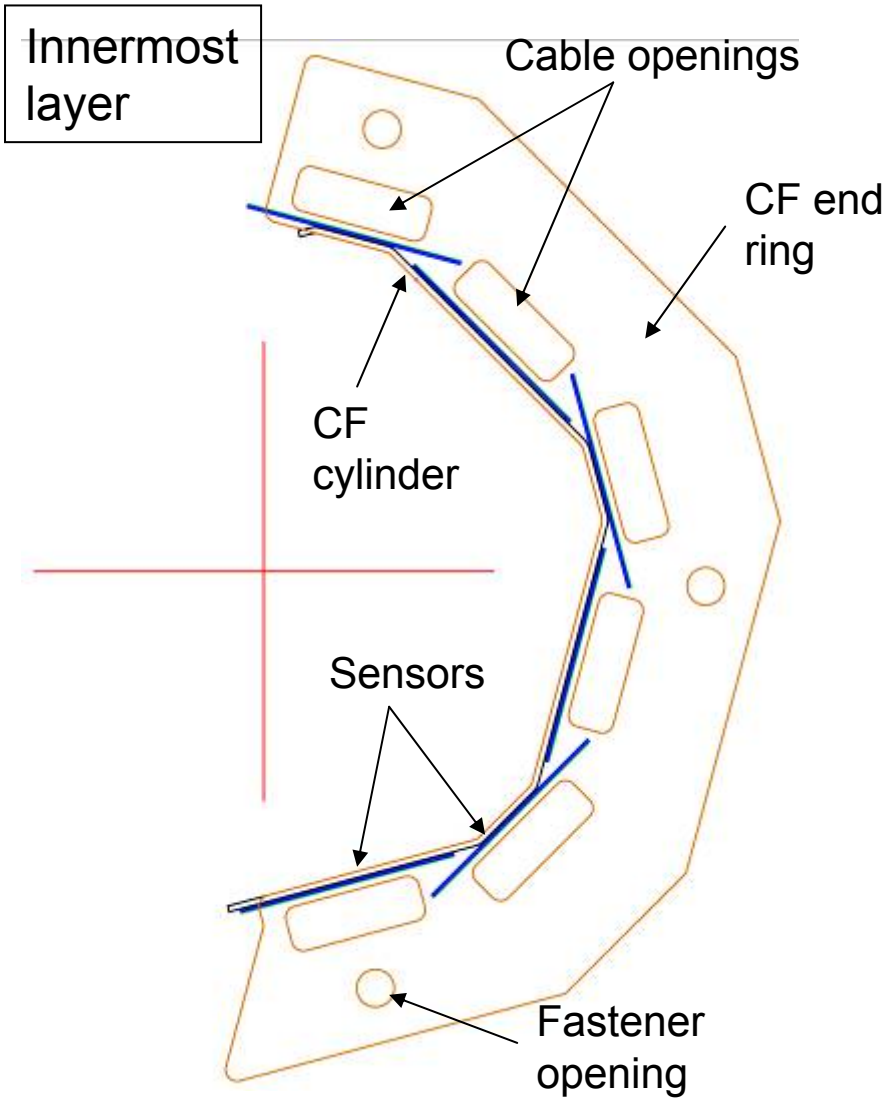
SiD Half Barrel (Innermost Barrel)

- Deflection with gravity acting horizontally = 0.5 μm
- Suggests a split at equator works better
  - A surprise to some of us
- The good results suggest



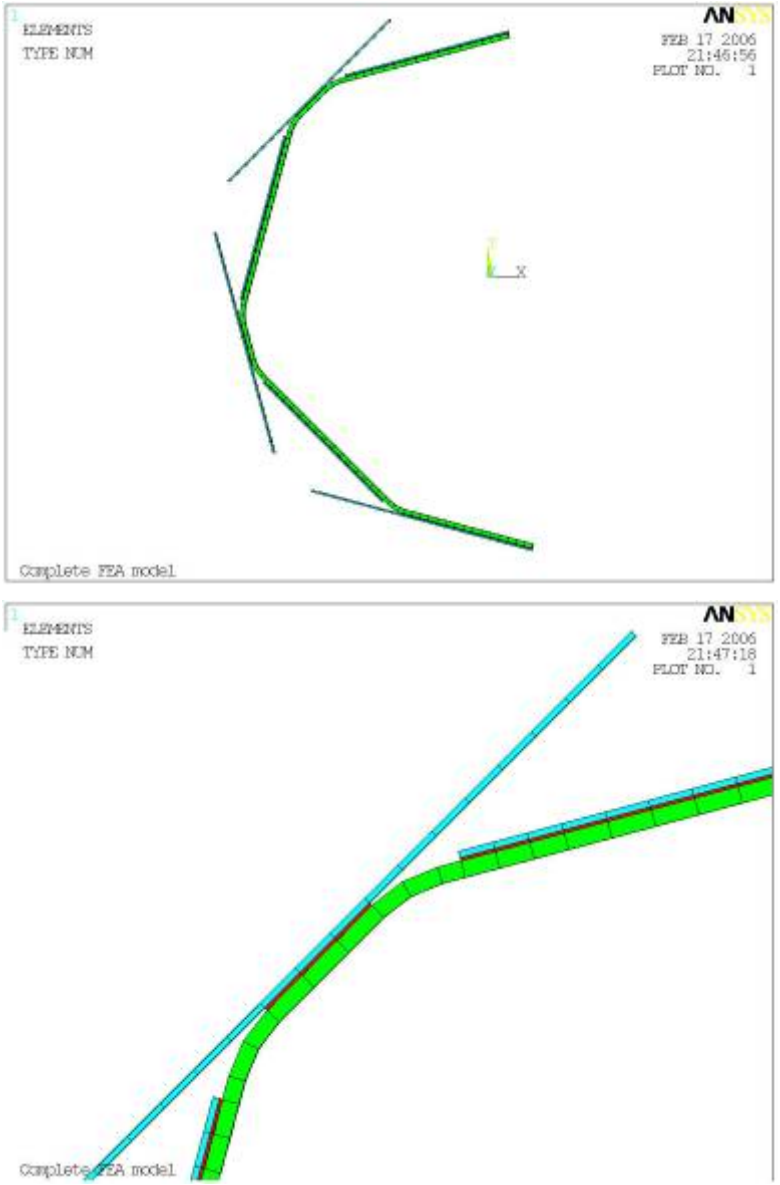
Barrel Layers

- Sensors are supported from and glued to a carbon fiber (CF) shell.
- Each barrel layer includes a CF end ring, which controls out-of-round distortions.
- Openings provide cable, optical fiber, and dry gas passages.
- Other openings to reduce mass and adjust gas flow would be added.
- End membranes connect one layer to the next to form a half-barrel.
- To control material, the use of fasteners has been limited.
  - Three fasteners per end ring



Finite Element Analysis (FEA)

- An initial model was developed by Colin Daly (University of Washington) to represent the barrel 1 carbon fiber (CF) support structure, sensors, and epoxy which holds sensors in place.
- All sensors are on the outer surface of the carbon fiber (CF).
- A & B layers have been placed leaving 0.54 mm from the edge of an A-layer sensor to the surface of a B-layer sensor.
- All barrel 1 sensors are shown 9.6 mm wide (9.1 mm active).
- B-layer sensors overhang CF ~3.3 mm.



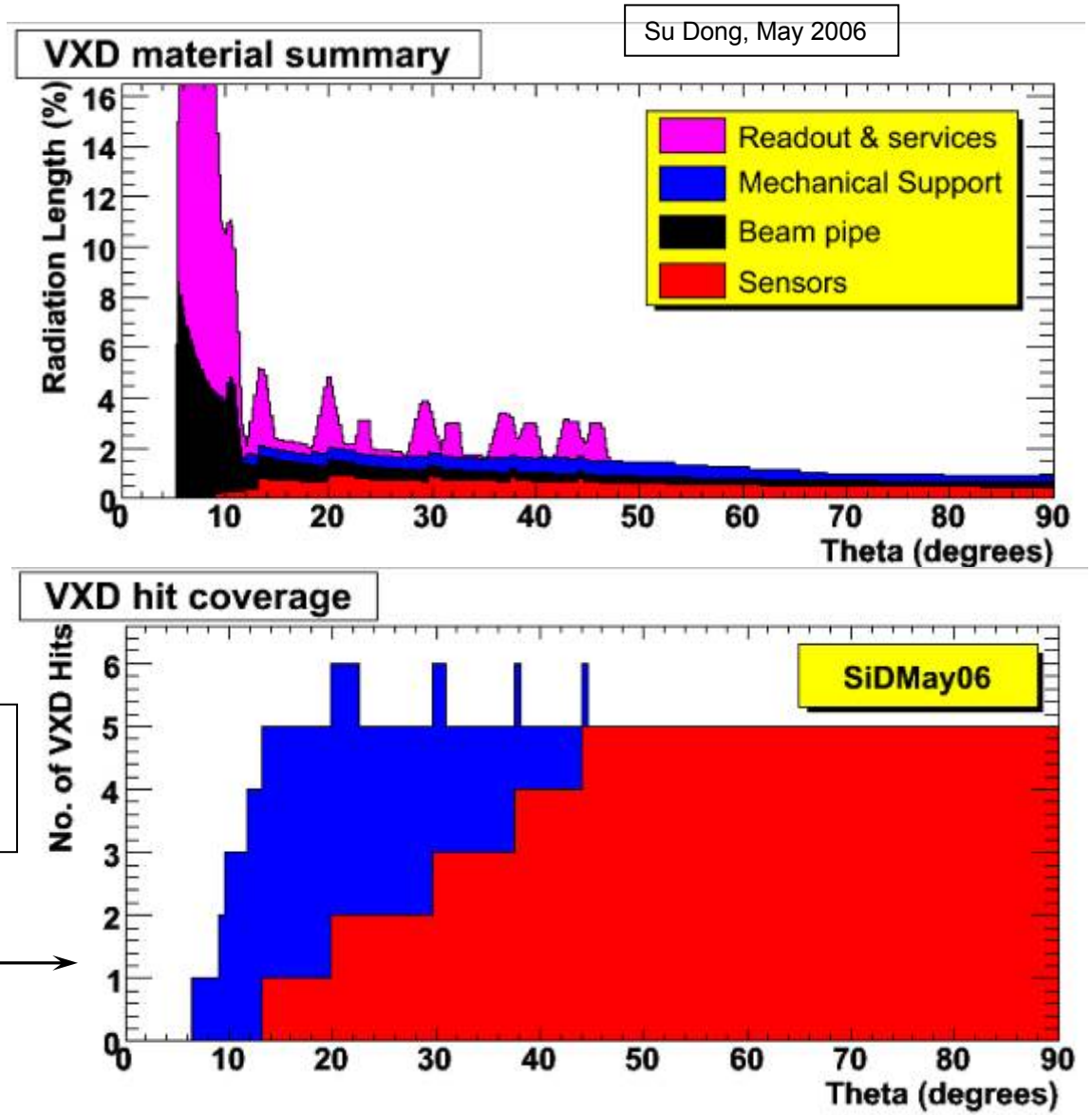
VXD Material

- Assumptions (partial):
  - 100 μm sensor thickness
  - 50 μm epoxy
  - 260 μm CF with ¾ of area removed
  - 400 μm beam pipe wall (central region)
  - 25 μm Ti beam pipe liner

For more information, see http://www-sid.slac.stanford.edu/vertexing/material/material-may06.htm

Barrel layers only

Barrels plus disks



cm

- **Shell structure has clear advantages, but some possible disadvantages**
  - **Bump-bonding to sensors (if required). Not entirely excluded, but …**
  - **Possible mechanical distortions if a sensor is switched off (regardless of the operating temp)**

- **For all VXD mechanical R&D with novel materials, micro-creep needs to be investigated (HIPed Beryllium has a track record for telescope and gyroscope mounts, as well as proven stability at SLD)**

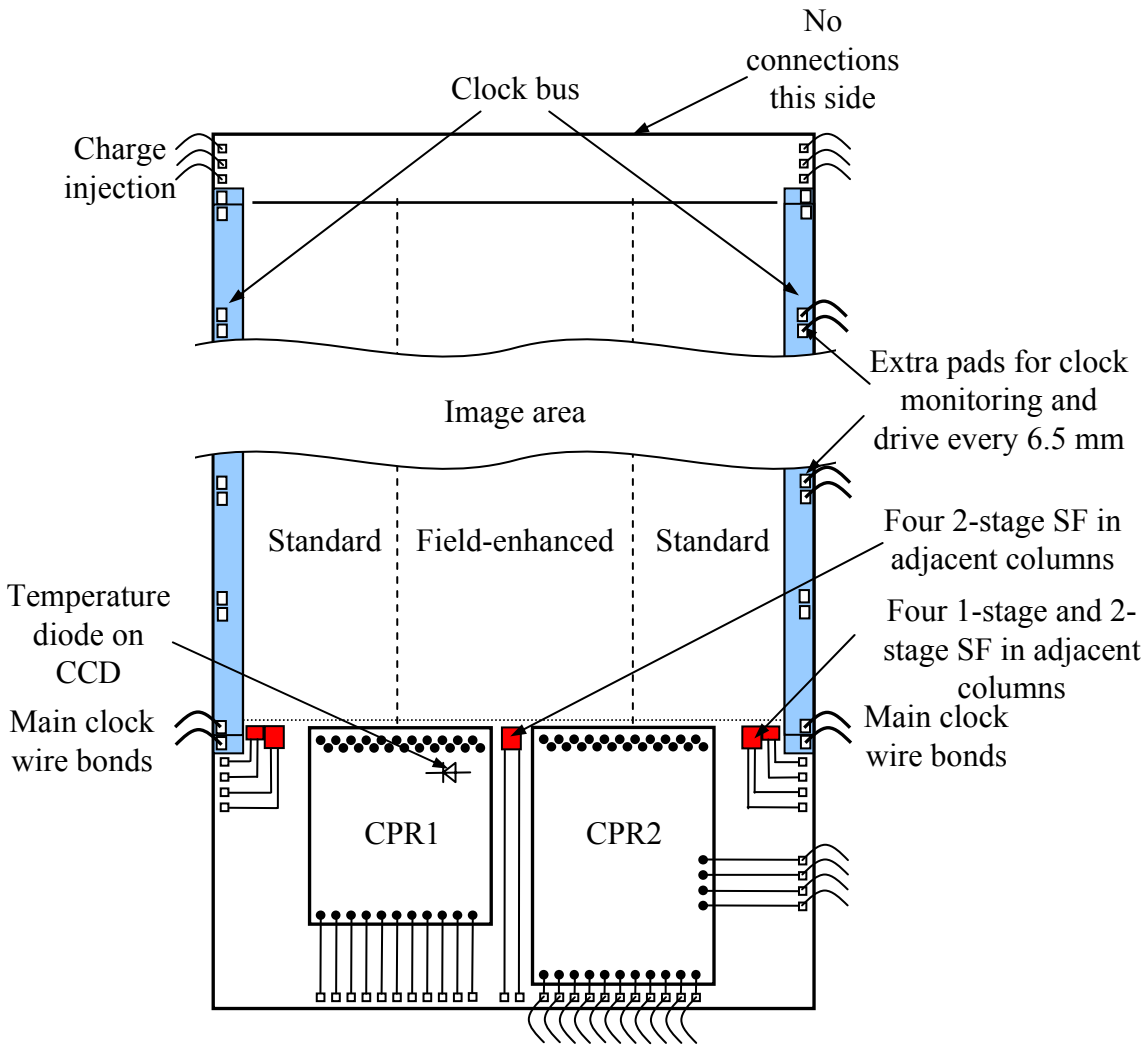
- **Short barrels plus end-disk detectors provide 3-hit coverage to cos(θ) = 0.98 cf 0.96 for long barrels. What will be the relative quality of the measurements?**

- **Eventual decision between long barrels and short barrels/disks will emerge from detailed studies. Tradeoffs between 'vertex-quality' layers and 'tracking-quality' FTD layers depend on many open questions, starting with the chosen detector technologies. How much material do they impose at ladder ends?**

Pixel Technologies

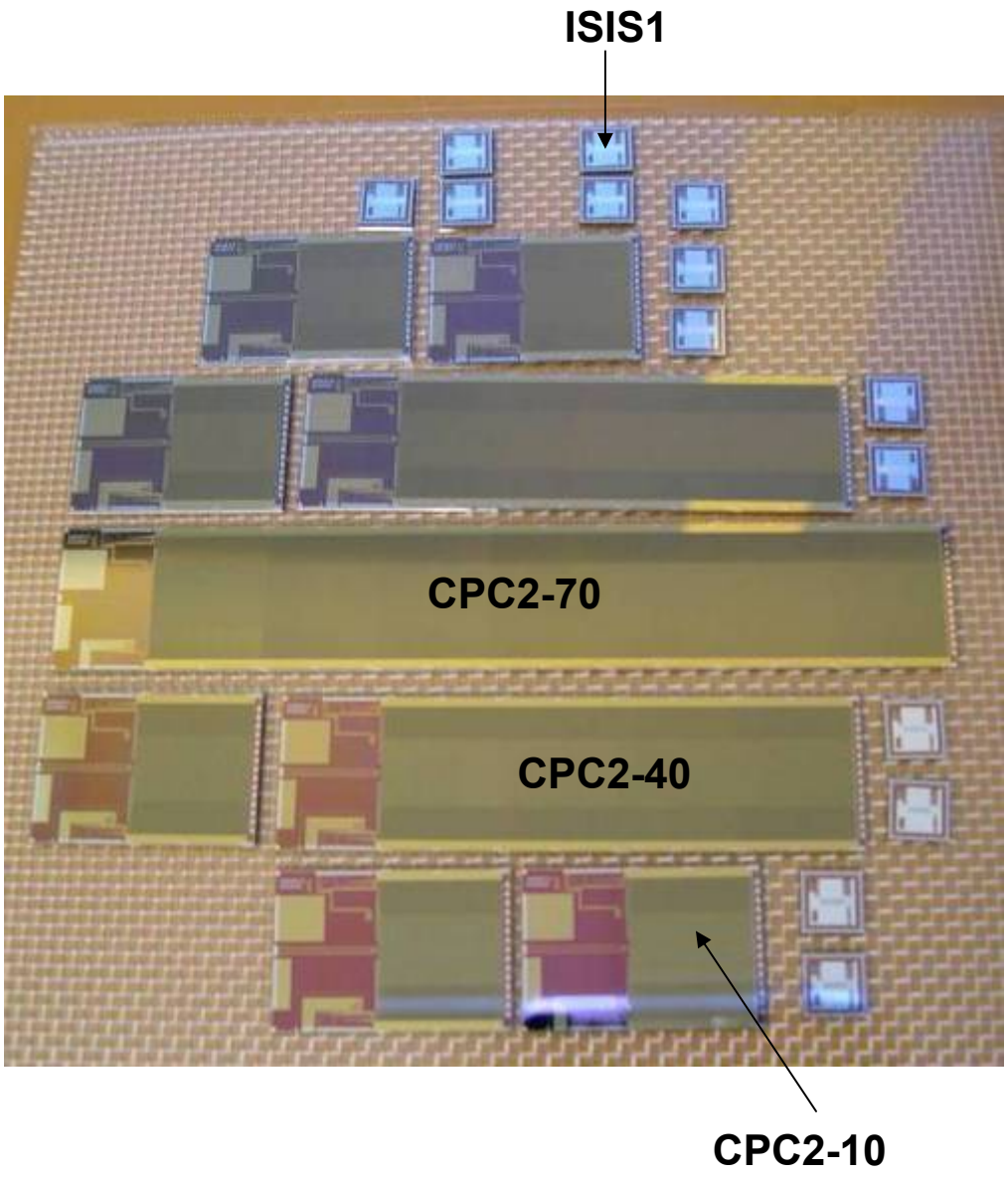
- Talks on:
  - CPCCD and ISIS (Konstantin Stefanov)
  - DEPFET (Rainer Richter and Hans Krueger)
  - MAPS (Marc Winter, Devis Contorato, Valerio Re)
  - FPCCD (Yasuhiro Sugimoto and Tadashi Nagamine)
  - 3D integrated sensors (Ray Yarema)
  - Macropixels not represented

Next Generation CPCCD : CPC2



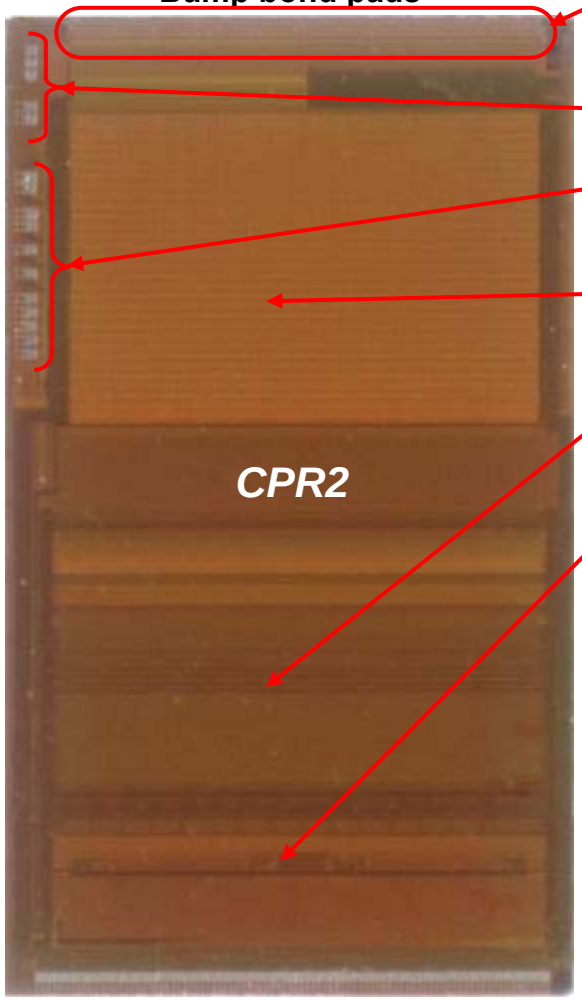
- **Three different chip sizes with common design:**
  - ❖ **CPC2-70 : 92 mm × 15 mm image area**
  - ❖ **CPC2-40 : 53 mm long**
  - ❖ **CPC2-10 : 13 mm long**
- **Compatible with CPR1 and CPR2**
- **Two charge transport sections**
- **Choice of epitaxial layers for different depletion depth: 100 Ω.cm (25 μm thick) and 1.5 kΩ.cm (50 μm thick)**
- **Baseline design allows few MHz operation for the largest size CPC2**

CPC2 + ISIS1 Wafer



- 5” wafers
- One CPC2-70 : 105 mm × 17 mm total chip size
- Two CPC2-40 per wafer
- 6 CPC2-10 per wafer
- 14 In-situ Storage Image Sensors (ISIS1)
- 3 wafers delivered

Next Generation CPCCD Readout Chip – CPR2



Voltage and charge amplifiers 125 channels each

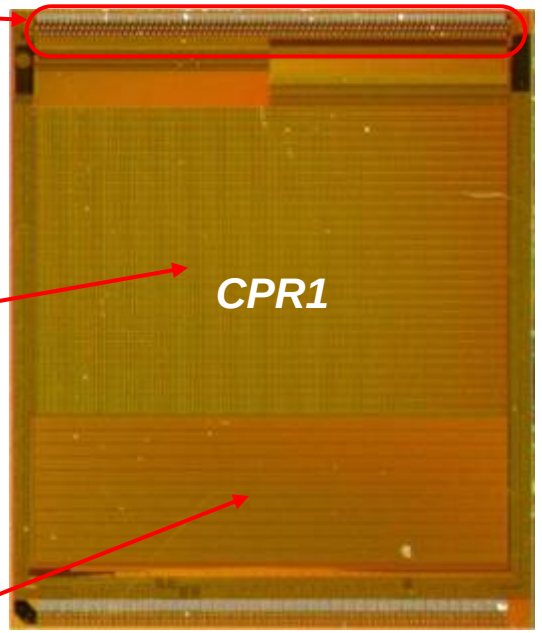
Analogue test I/O

Digital test I/O

5-bit flash ADCs on 20 µm pitch

Cluster finding logic (2×2 kernel)

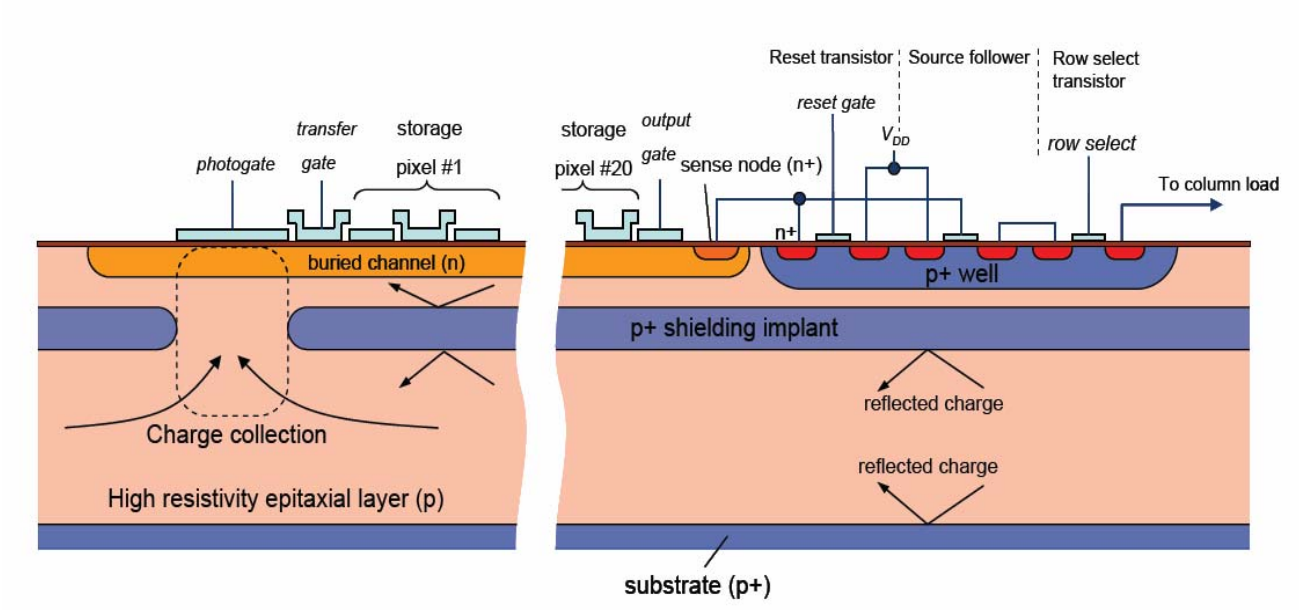
Sparse readout circuitry



- CPR2 designed for CPC2
- Results from CPR1 taken into account
- Numerous test features
- Size : 6 mm × 9.5 mm
- 0.25 µm CMOS process (IBM)
- Manufactured and delivered February 2005

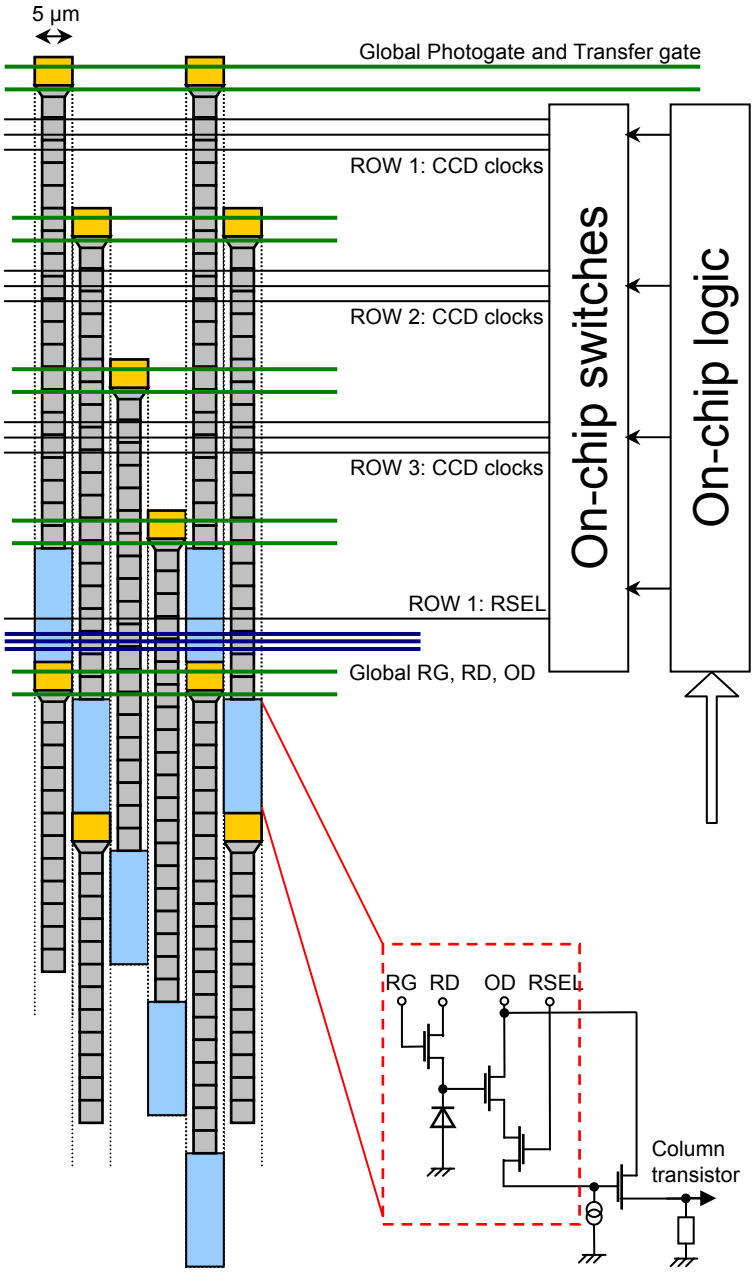
Steve Thomas, RAL

In-situ Storage Image Sensor (ISIS)



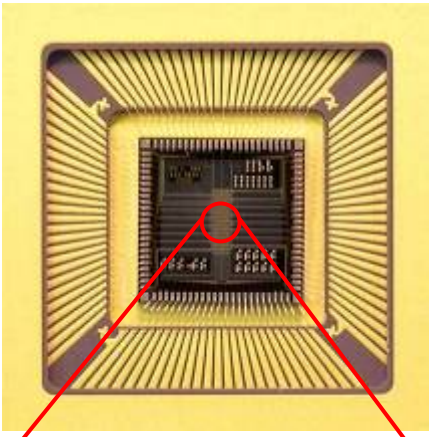
- **Beam-related RF pickup is a concern for all sensors converting charge into voltage during the bunch train;**
- **The In-situ Storage Image Sensor (ISIS) eliminates this source of EMI:**
  - **Charge collected under a photogate;**
  - **Charge is transferred to 20-pixel storage CCD in situ, 20 times during the 1 ms-long train;**
  - **Conversion to voltage and readout in the 200 ms-long quiet period after the train, RF pickup is avoided;**
  - **1 MHz column-parallel readout is sufficient;**

In-situ Storage Image Sensor (ISIS)

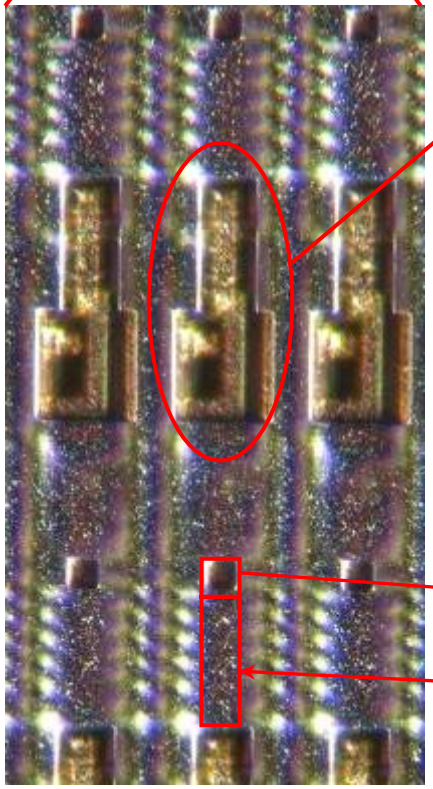


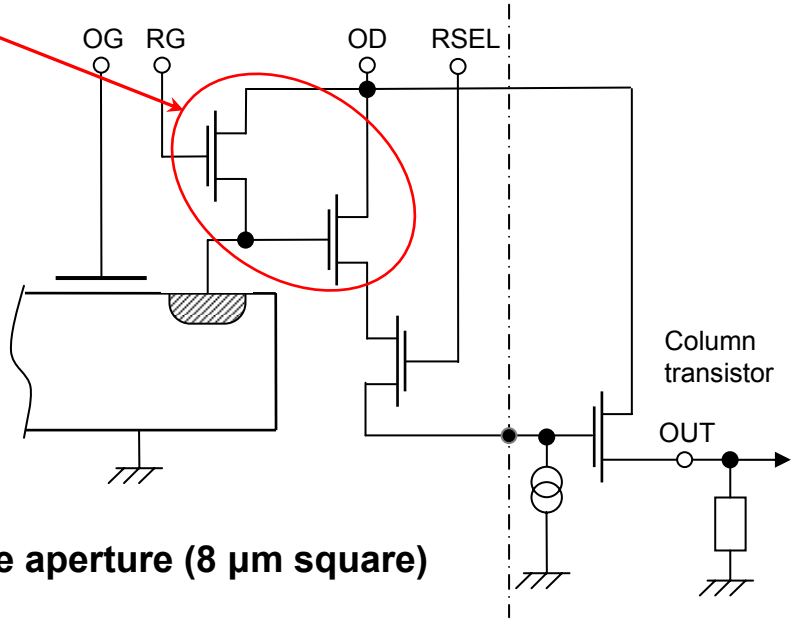
- **Additional ISIS advantages:**
  - ❖ **~100 times more radiation hard than CCDs – less charge transfers**
  - ❖ **Easier to drive because of the low clock frequency: 20 kHz during capture, 1 MHz during readout**
- **ISIS combines CCDs, active pixel transistors and edge electronics in one device: specialised process**
- **Development and design of ISIS is more ambitious goal than CPCCD**
- **"Proof of principle" device (ISIS1) designed and manufactured by e2V Technologies**

The ISIS1 Cell



- 16×16 array of ISIS cells with 5-pixel buried channel CCD storage register each;
- Cell pitch 40 μm × 160 μm, no edge logic (pure CCD process)
- Chip size ≈ 6.5 mm × 6.5 mm



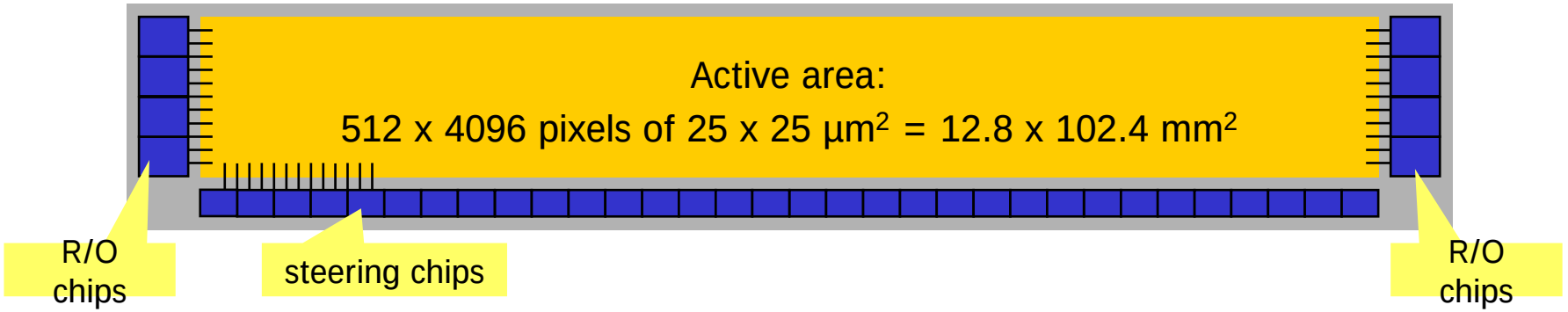


- **For CPCCD, several concerns:**
  - **storage capacitors at ladder ends could be challenging**
    - **New ideas for reduced capacitance CCDs**
    - **Possible operation close to room temperature would allow 'supercapacitors'**
  - **Readout does use true CDS, but voltage sensing during the train could still be dangerous**

- **For ISIS, LCFI collab is investigating which manufacturer has the process 'most likely to succeed'**

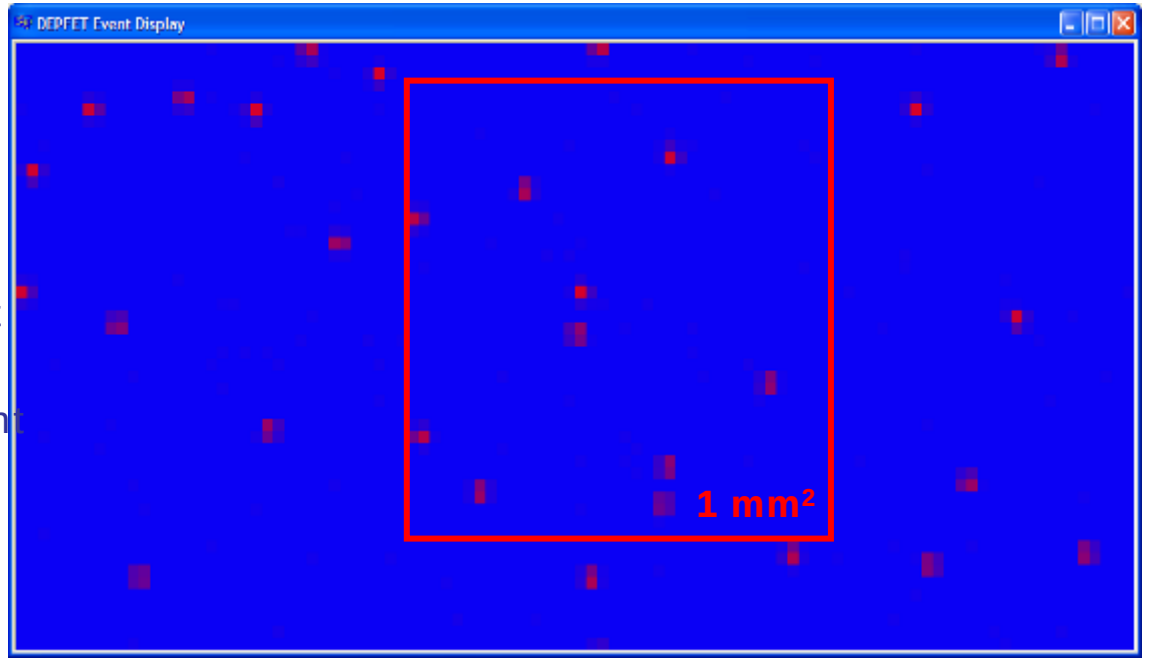
ILC DEPFET Module (Layer 1)

- Modules have active area ~**13 x 100 mm2**
- They are read out on **both sides**.



- "Poor mans" occupancy simulation:
  - Assume signal width of 10µm
  - Read **10 frames** per train
    i.e. 10 x 2048 rows in 1ms
    or one row in 50ns (two rows at a time @ **20MHz**)
  - Expect ~10 tracks / mm² / event

- Pattern recognition should not be a problem!



Module Concept/Power Consumption

Total power consumption of the vtx-d in the active region (TDR design, 25 µm pixel)

DEPFET matrix only:

1st layer : 2 rows active, 30 µA · 5V · 650 · 2 · 8 = 1.6 W

2nd .. 5th layer: 1 row active, 30 µA · 5V · 1100 · 1 · 112 = 18.5 W

Steering chips: assuming 0.15 mW for an inactive, 300 mW for an active channel

1st layer : [(4998 · 0.15 mW)+(2 · 300mW)] · 8 = 10.8 W

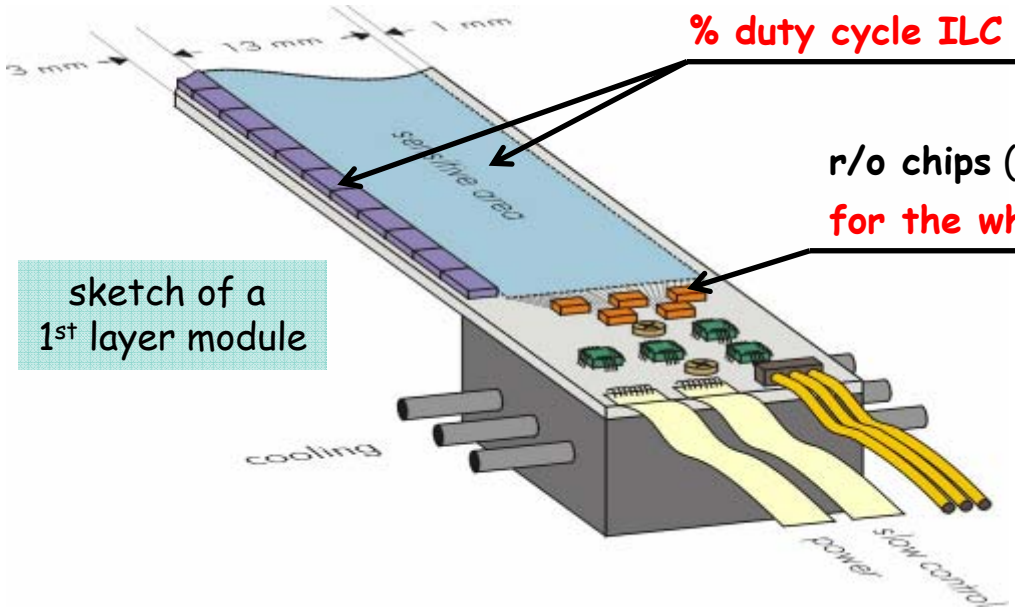
2nd ..5th layer: [(6249 · 0.15 mW)+(1 · 300mW)] · 112 = 138.6 W

Σ active region ≈ 170 W

% duty cycle ILC 1/200 → ≈ 0.9 W

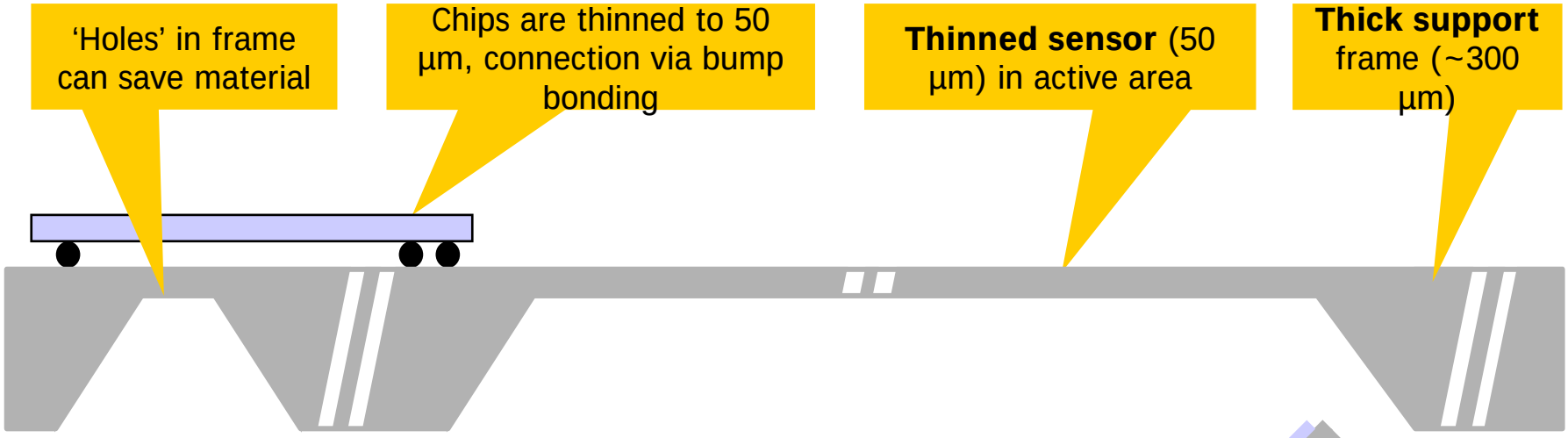
r/o chips (current version):2.8 mW/chn.

for the whole vtx-d: ≈ 2W



sketch of a 1st layer module

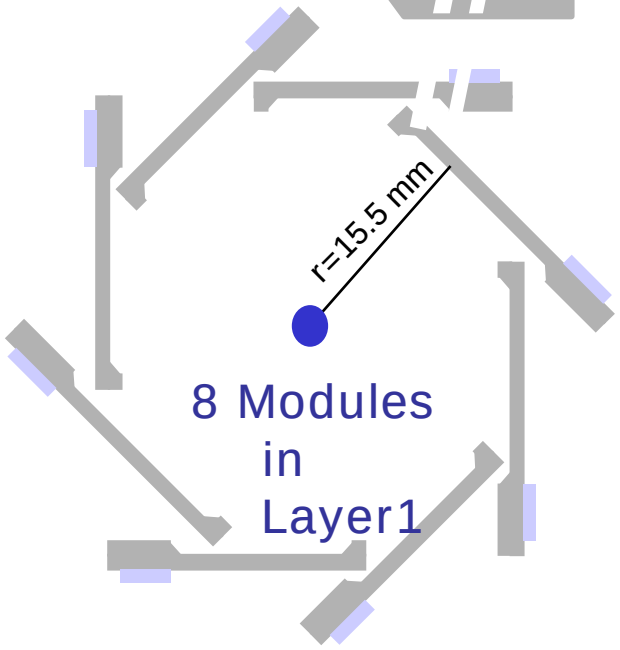
Possible Geometry of Layer 1 (all-silicon module)



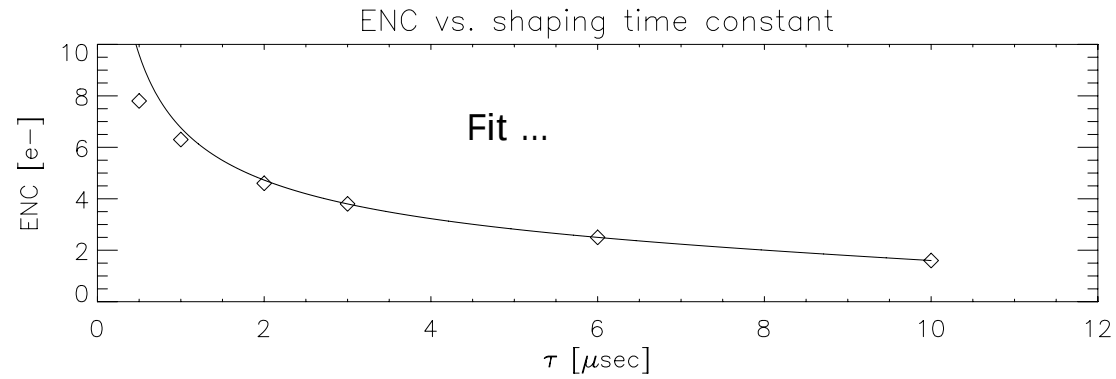
Cross section of a module

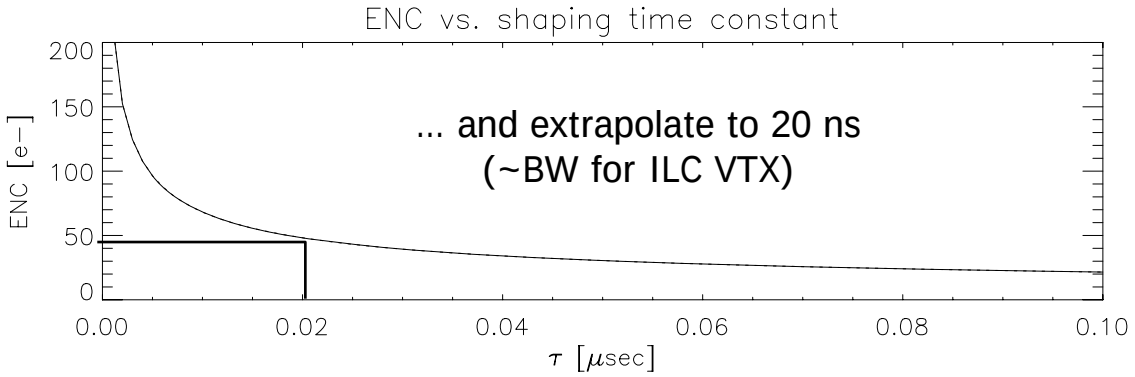
Estimation of material budget:

pixel area:	13x100 mm², 50µm:	0.05% X_0
steering chips:	2x100 mm², 50µm:	0.01% X_0
bump bonds:		?
frame w. holes:	4x100 mm², 50% of 300µm:	0.05% X_0
total:		0.11 % X_0



Noise vs. shaping time τ



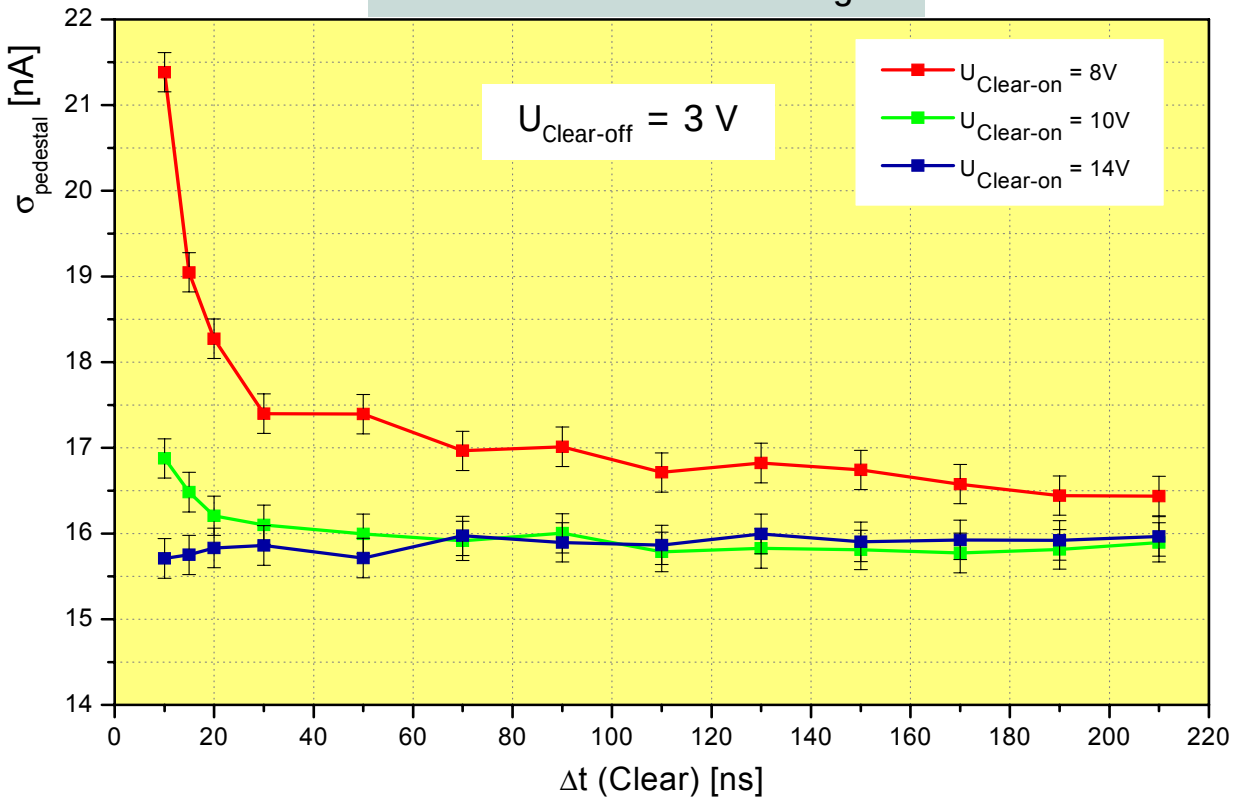


$$ENC = \sqrt{\underbrace{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau}}_{\text{Therm. noise}} + \underbrace{2\pi a_f C_{tot}^2 A_2}_{\text{1/f}} + \underbrace{q I_L A_3 \tau}_{I_L}}$$

Fast Clearing

Study clear efficiency for short clear pulses

Device with common clear gate



Complete clear in only 10-20 ns @ ΔV_{clear} = 11-7 V

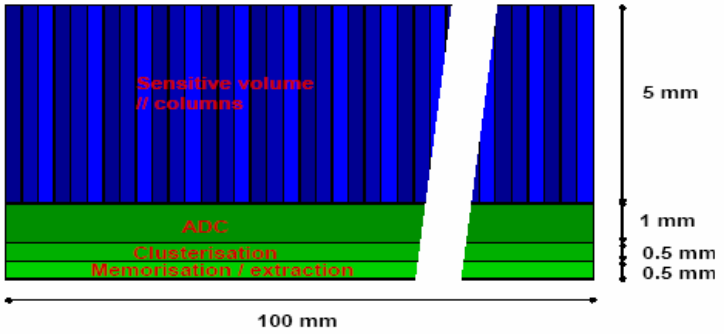
- **Achieving a rad-hard process for switching the CLEAR pulse:**
  - **requires operation with much-reduced clear voltage**
  - **design being modified to achieve this**

- **Window frame:**
  - **creates undesirable regions of high material budget**
  - **mechanical stiffness may not be as great as desired**
  - **considering changing to a uniform substrate for mechanical support**

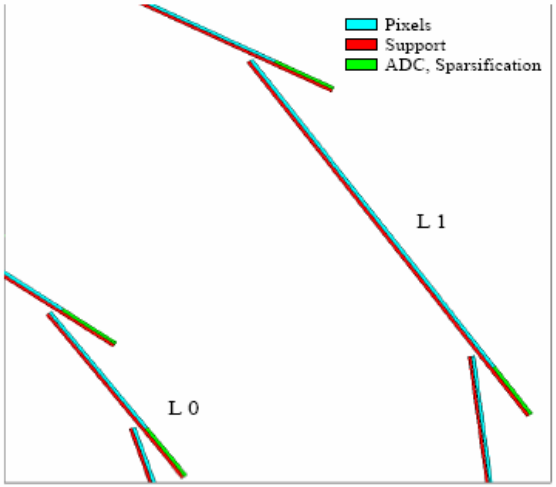
- **20 MHz operation with true CDS (sample/clear/sample within 50 ns) is challenging, but may be achievable**

Consequences on Inner Layer Design

- $\lesssim$ 25 μs in L0:
  columns of 256 pixels (20 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 5 mm depth
- $\sim$ 50 μs in L1:
  columns of 512 pixels (25 μm pitch) $\perp$ beam axes
  read out in // at $\sim$ 10 MHz $\longrightarrow$ 13 mm depth



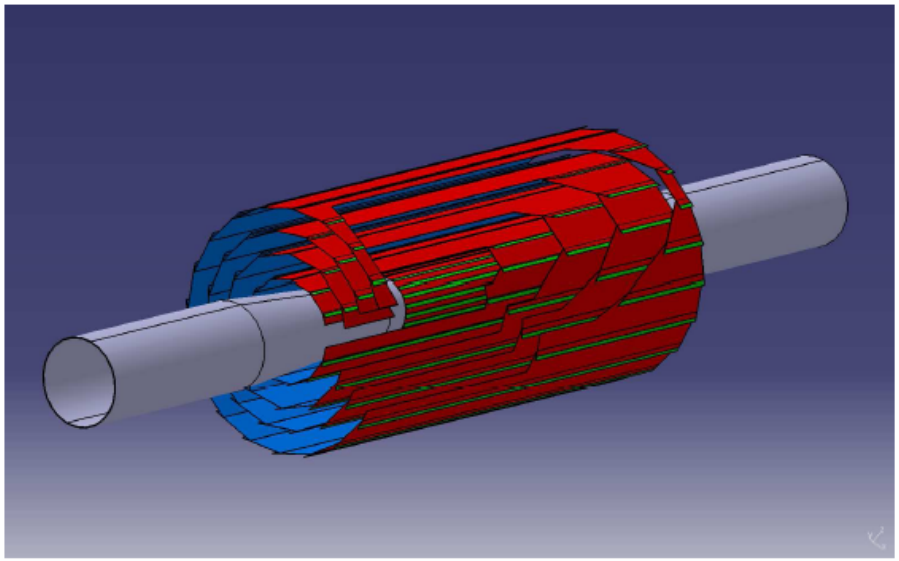
- $\lesssim$ 2 mm wide side band hosting ADC, sparsification, ...
  $\hookrightarrow$ effect on material budget SMALL :
  b increases by $\sim$ 5 – 10 %
- Option with discriminator instead of ADC :
  $\sim$ 1 mm wide side band $\Rightarrow$ effect on $\mathrm{b} < 5$ %



Basic Vertex Detector Design features

- Geometry : 5 cylindrical layers (R = 15 – 60 mm), $\|cos\theta\| \leq$ 0.90 – 0.96
- L0 and L1 : fast col. // architecture
- L2, L3 and L4 : multi-memory pixel architecture (?)
- Pixel pitch varied from 20 μm (L0) to 40 μm (L4) by 5 μm steps $\rightarrow$ minimise P_{diss}

Layer	Radius (mm)	Pitch (μm)	$t_{r.o.}$ (μs)	N_{lad}	N_{pix} (10^6)	P_{diss}^{inst} (W)	P_{diss}^{mean} (W)
L0	15	20	25	20	25	$<$100	$<$5
L1	$\leq$ 25	25	50	$\leq$26	$\leq$ 65	$<$130	$<$7
L2	37	30	$<$200	24	75	$<$100	$<$5
L3	48	35	$<$200	32	70	$<$110	$<$6
L4	60	40	$<$200	40	70	$<$125	$<$6
Total				142	**305**	$<$565	**$<$3–30**



- Ultra thin layers: $\lesssim$ 0.2 % X_0/layer (extrapolated from STAR-HFT; 35 μm thick sensors)
- Very low P_{diss}^{mean}: $<<$ 100 W (exact value depends on duty cycle)
- Fake hit rate $\lesssim 10^{-5} \rightarrow$ whole detector $\cong$ 100 MB/s (mainly from $e^{\pm}_{BS}$)

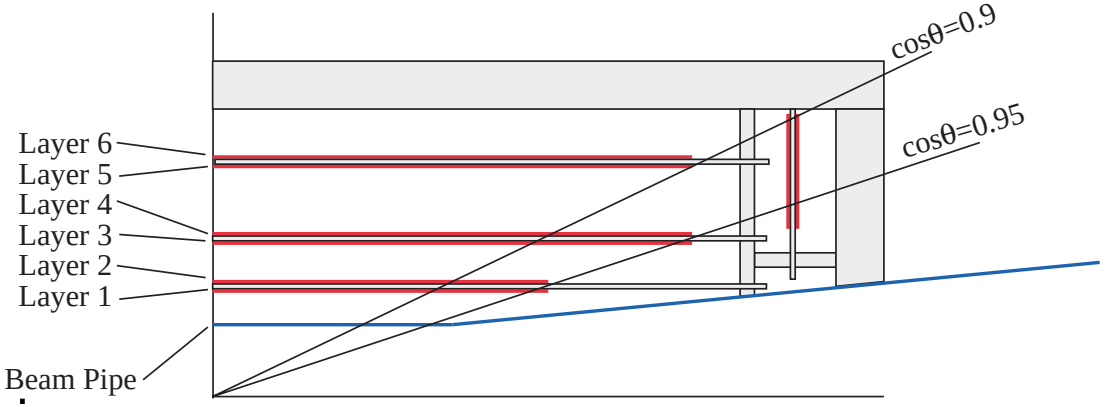
- **Better described as a 'row-parallel' architecture. Columns are usually defined to be parallel to the long axis of the sensors (beam direction). 'Column parallel readout' is outside the sensitive volume; 'row parallel readout' is distributed throughout this volume**

- **Query relaxing of parameters that present technical problems:**
  - **Layer thickness [search area for pattern recognition (track finding) scales with thickness, and low momentum fake tracks are a problem]**
  - **Pixel size [B/D SV/TV separation is as important for long-lived as for short-lived Bs – nobody yet made a vertex detector that was adequately precise!]**
  - **In-pixel CDS [If this is based on a rolling shutter, it is more appropriately labelled PDS for Pseudo-CDS – vulnerable to baseline drift and pickup]**
  - **Fewer than 6-bit ADCs [need to be able to reject clusters with high energy-loss fluctuations]**

- **How can 5-bit ADC plus sparsification be fitted in 1/3 of length needed by LCFI? Maybe assumes 0.25 μm → 0.065 μm design rules; is this realistic for stitched devices 10 cm long, in forseeable future?**

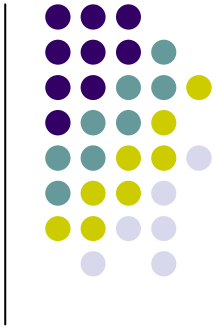
Evaluation Model

- VTX in GLD baseline design
  - Sensor; Fine Pixel CCD (FPCCD)
  - Accumulate 1 train and readout between trains
  - Background rejection by cluster shape
    → T. Nagamine's talk
  - Three doublets = 6 layers in the barrel region plus one doublet in the forward region
  - Layer thickness; 80μm Si equivalent / layer
  - Three options of the inner radius



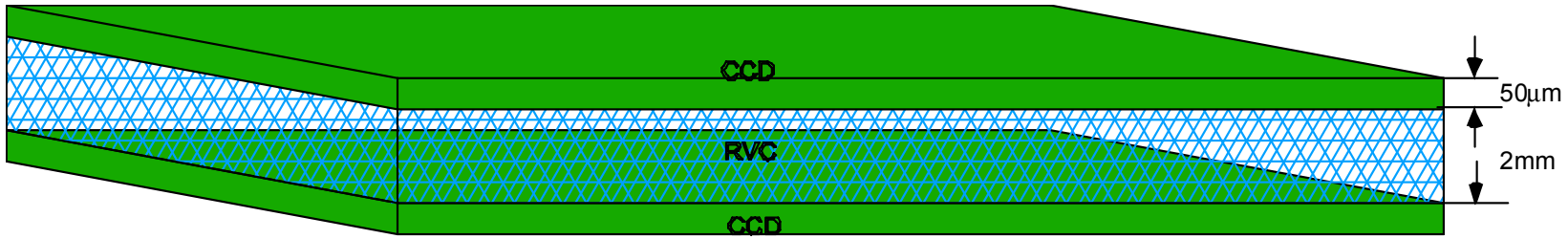
Configuration	$R_{Beam\ Pipe}$	R_{VTX-1}	Z_{VTX-1}
Baseline	15 mm	**20 mm**	65 mm
Small R	13 mm	**17 mm**	55 mm
Large R	19 mm	**24 mm**	75 mm

Summary



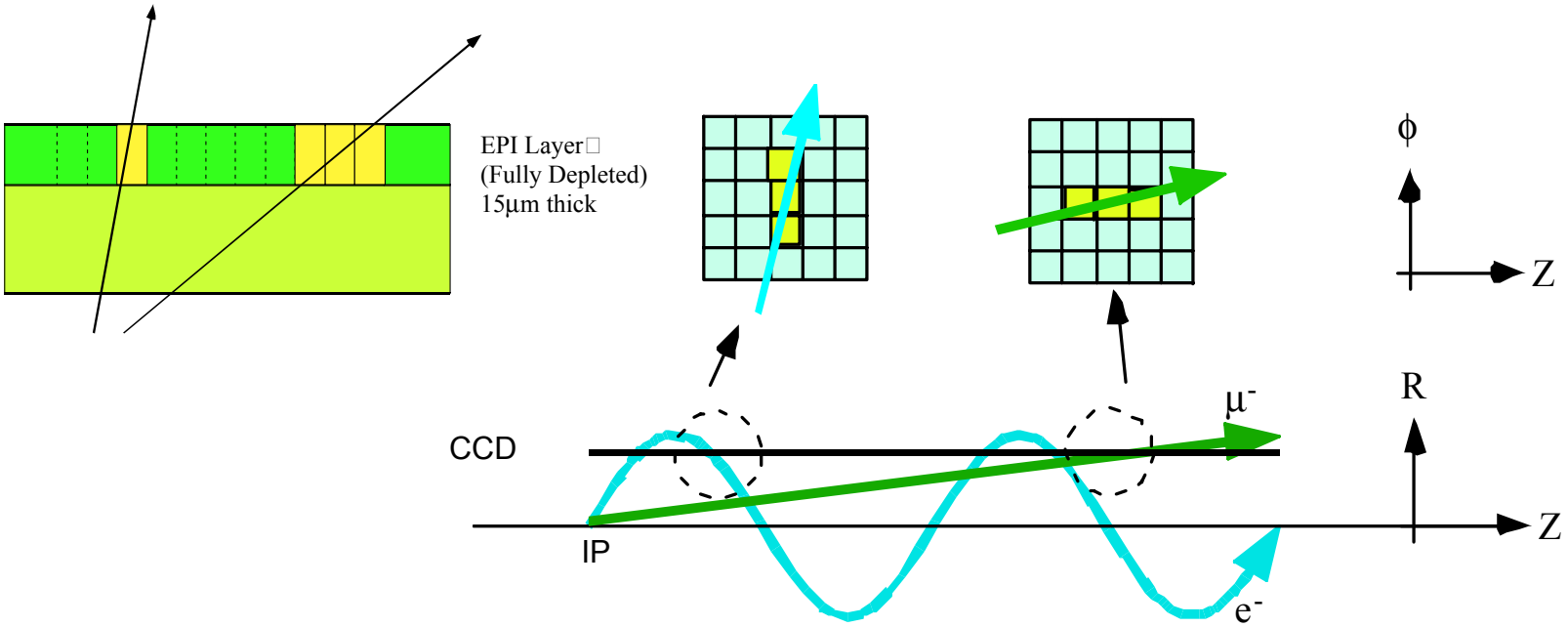
- GLD has a tracking system with powerful pattern recognition capability. So, GLD VTX can cope with higher hit density.
- Due to weaker solenoid field, GLD VTX will have slightly larger inner radius (B-dependence of R_{in} is weaker than $1/B^{1/2}$)
  - 17mm for nominal option at 500GeV
  - 20mm for Andrei's high luminosity option at 1TeV ← Baseline
  - 24mm for original high luminosity option at 500GeV
- Nevertheless, the GLD tracking system can achieve the performance goals of impact parameter resolution (except for original high luminosity option) and momentum resolution
- Difference in physics output between 3 detector concepts due to difference of the VTX inner radius seems very small.
- Detailed **engineering design** to minimize the material budget would be important : $\sigma_{MS} \sim R_{in} \times \theta_{MS} \sim \sqrt{x / X_0 B}$
- **Optimization** of the GLD VTX design is not complete yet, and has to be continued

Ladder Structure



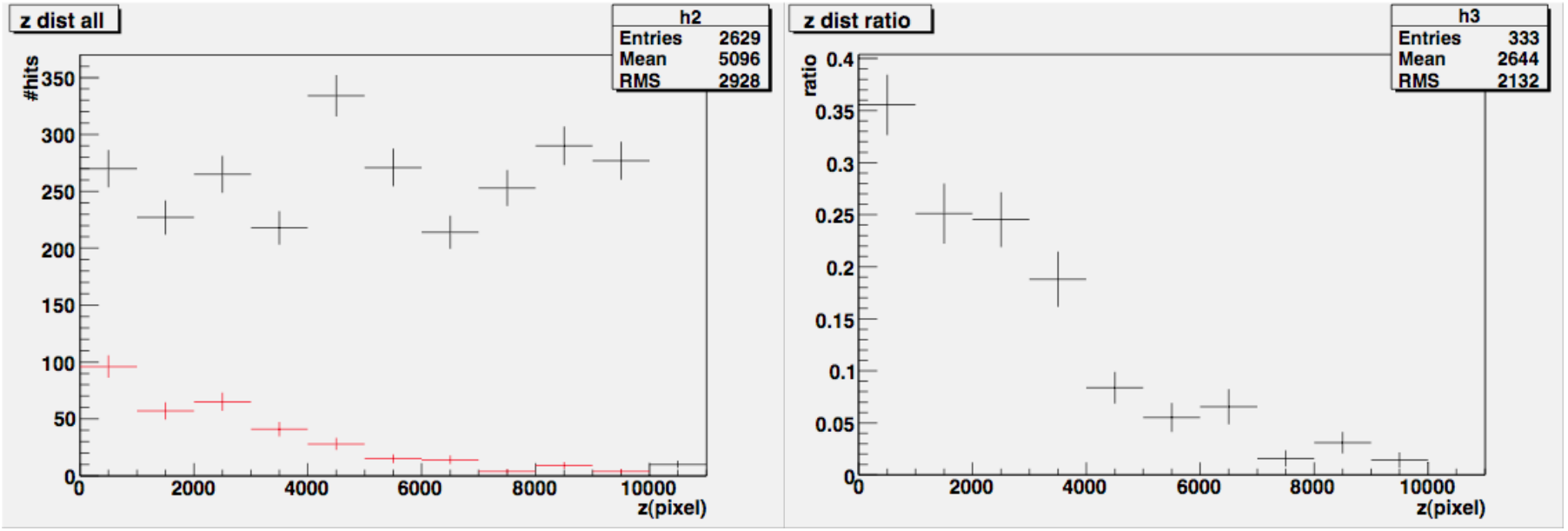
- 2 FPCCD on both side of Support Structure
- RVC will be used for main support structure.

Cluster Shapes for Low P_T and High P_T tracks



- Pair Background (e^+e^-) : Lower P_T (blue line)
- Most particles in Interaction : Higher P_T (green line)

Hit Efficiency for Pair Background

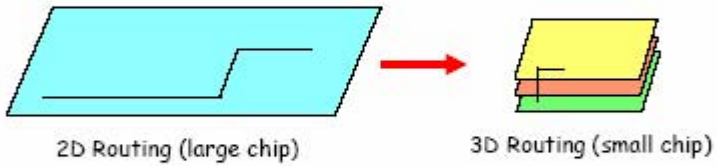


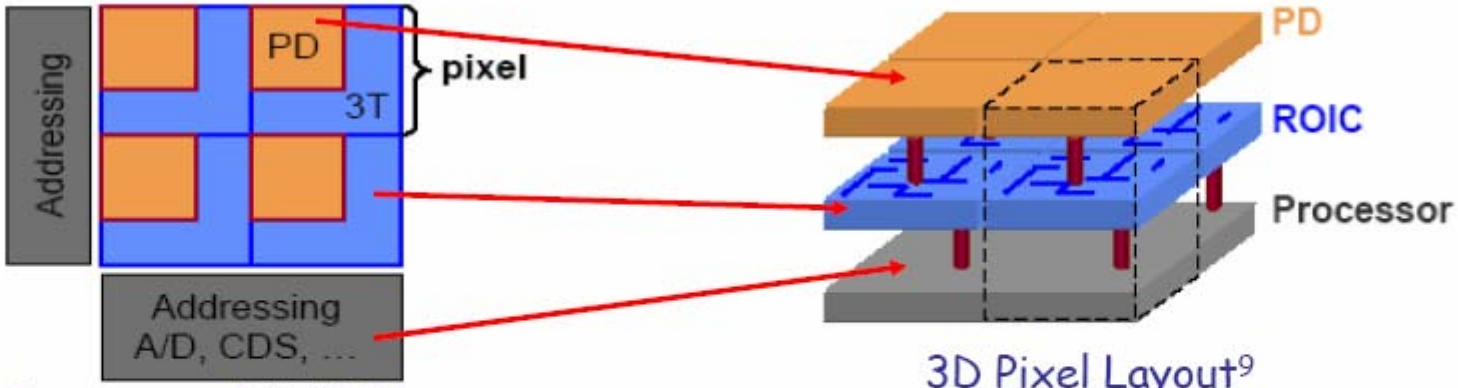
- Layer 1
- Left: all hits (black) and accepted (red) ▪
- Right: efficiency

- This is the technology closest to reality
- Unlikely to be overtaken soon – could well provide one of the ILC startup vertex detectors
- May remain the technology of choice (minimal power dissipation and potentially minimal thickness), depending on background levels encountered as the machine luminosity improves
- Only this and the ISIS are robust regarding EM pickup during the bunch train. Experience at ILC will decide whether this is a soluble problem for other technologies
- Modest level of fake tracks at low p_t can surely be cleaned up by the FTD

What are the Advantages?

- Going 3D reduces trace length
  - Reduces R, L, C
  - Improves speed
  - Reduces interconnect power, crosstalk
- Reduces chip size
- Processing for each layer can be optimized
- MAPS as an example
  - 100% diode fill factor
  - Four-side abuttable devices

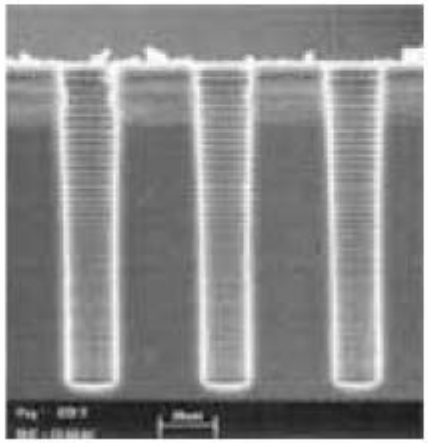




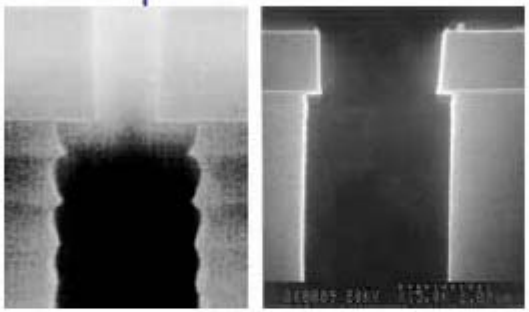
Conventional MAPS Layout[9]

3D Pixel Layout[9]

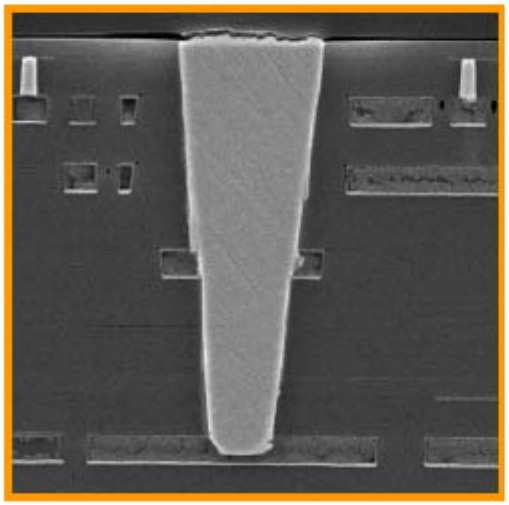
Via Formation



SEM of 3 vias made with Bosch process [7]

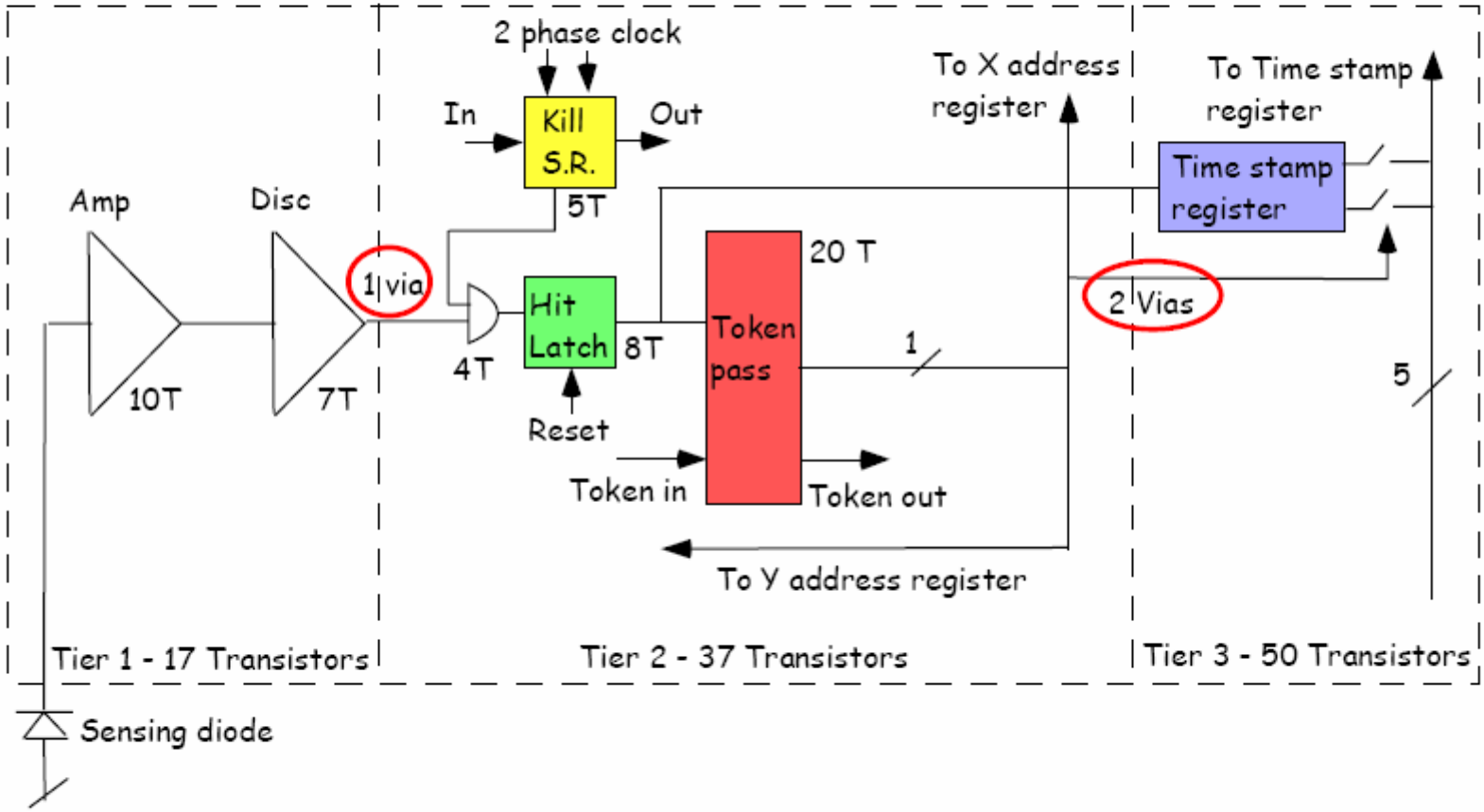


Close-up of walls with/without Scallops in Bosch process [7]



Tapered wall using high density plasma oxide etch (MIT Lincoln Labs)

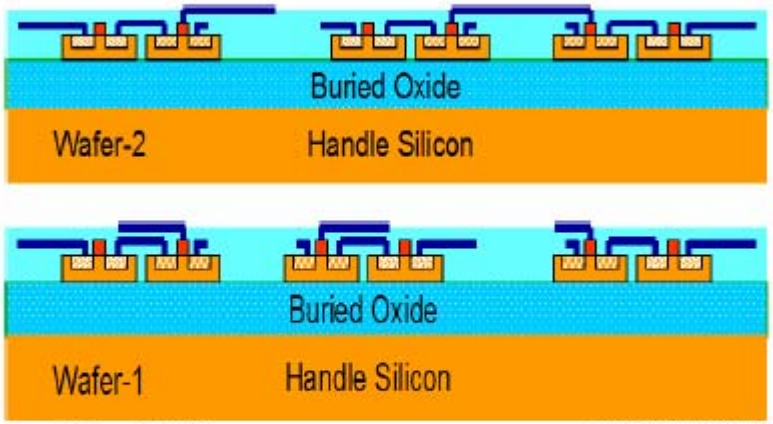
Pixel Cell Block Diagram



Process flow for 3D Chip

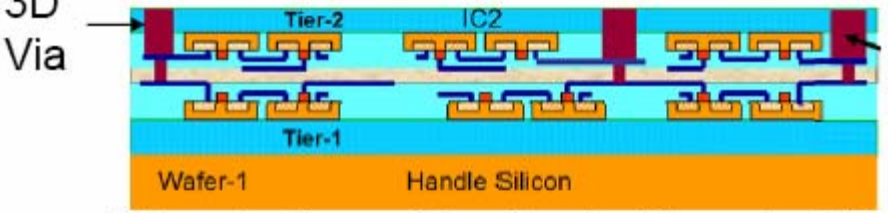
- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers

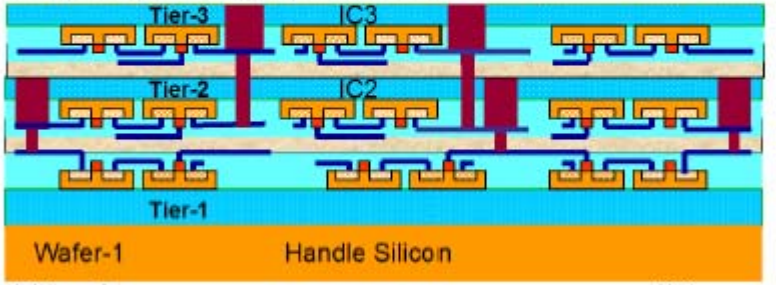


2) Invert, align, and bond wafer 2 to wafer 1

3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten



4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3



- **This is the most adventurous technology, but in time may become a standard. It has long been a dream …**

- **Origins of Z-plane technology:**
  - **Focal plane architecture: an overview, W.S. Chan, Proc SPIE 217 (1980) 2. Listed the challenges of 'vertical integration'**

- **Being liberated into the 3rd dimension is potentially very interesting, but being constrained (in case of parallel processing of all pixels) to the available pixel area can severely restrict functionality**

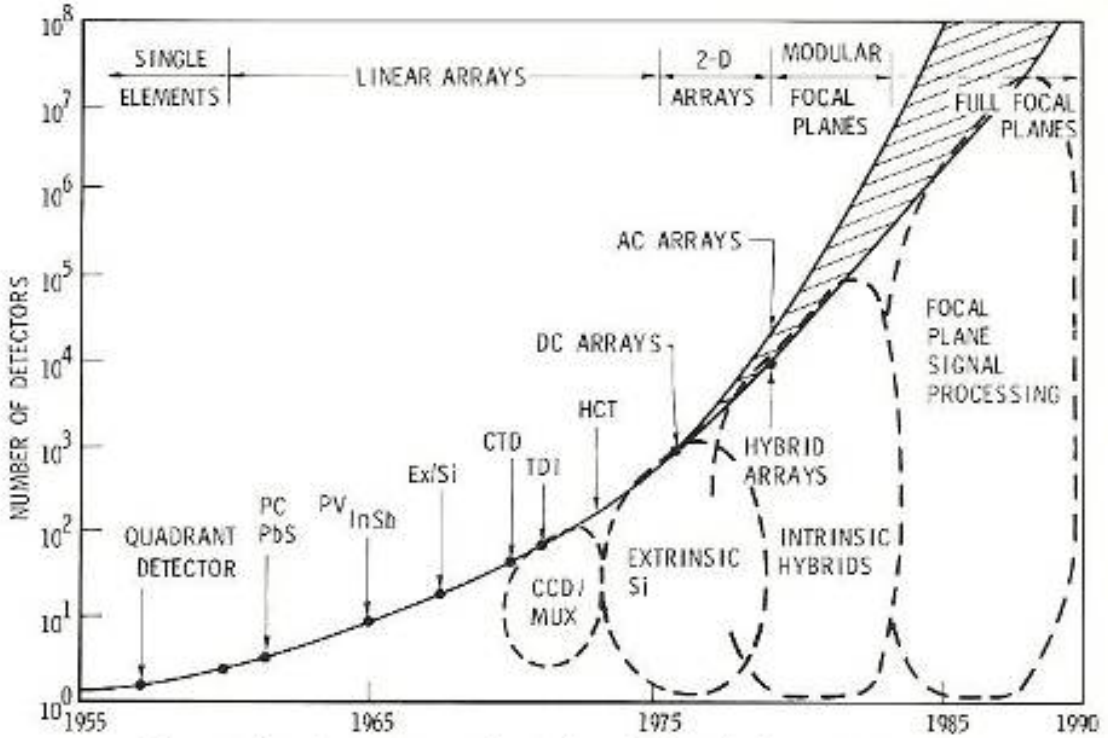
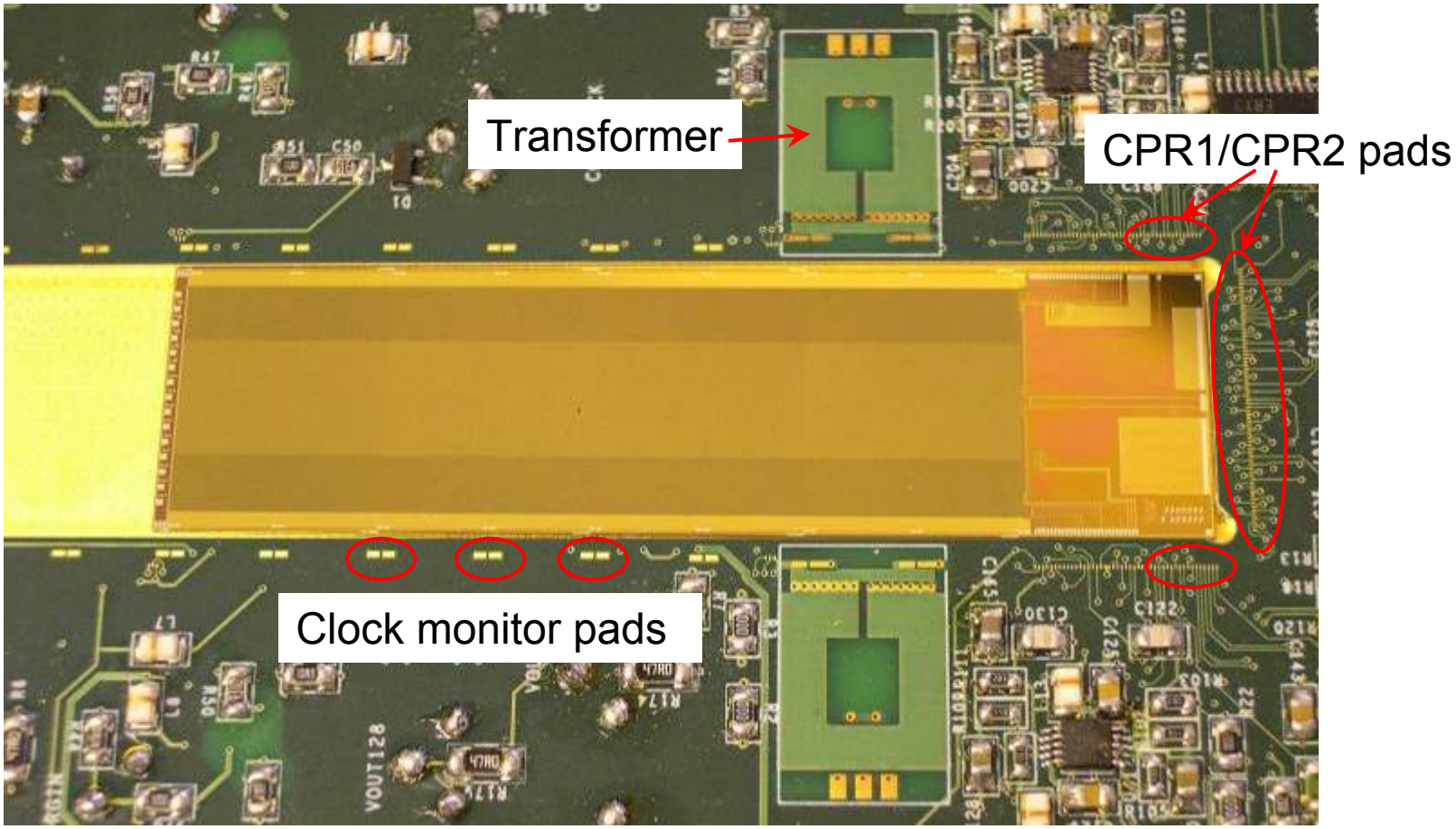


Figure 4. Progress and trends in focal plane technology

- Small pixels (15μm x 15 μm) chosen to avoid need for ADCs – but binary readout has some disadvantages in principle (calibration, radiation-induced and other time-dependent effects, δ-electrons which pull cluster centroid)
- Need shaping time ~100 ns, but sample only every 30 μs without CDS, for >10^9 pixels – daring)
- Same concerns as most others, regarding EMI sensitivity, but more so …
- All functionality (and power) moved into the active volume. Probably OK – pulsed power on analogue front-end. Readout looks relatively comfortable, as regards time required (<< 100 ms) and power dissipation
- Mechanical stability of a 3-tier structure with *all* tiers very thin. Any experience?
- 5 k x 1 k possible? Don't be too worried about yield, specially if each tier can be tested before assembly
- This is the 'new kid on the block', and may have good answers to these concerns. Even if timescale proves to be very challenging, could provide an important upgrade path

CPC2-40 in MB4.0

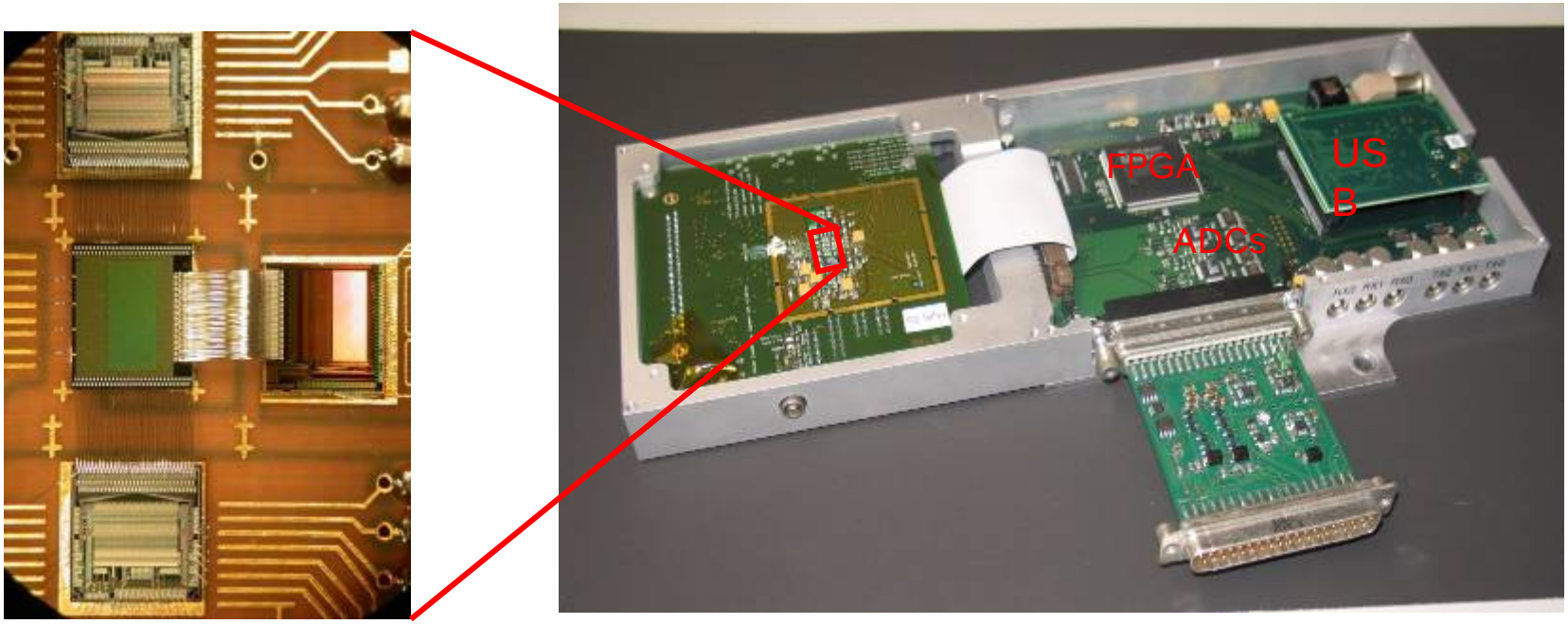


Johan Fopma, Oxford U

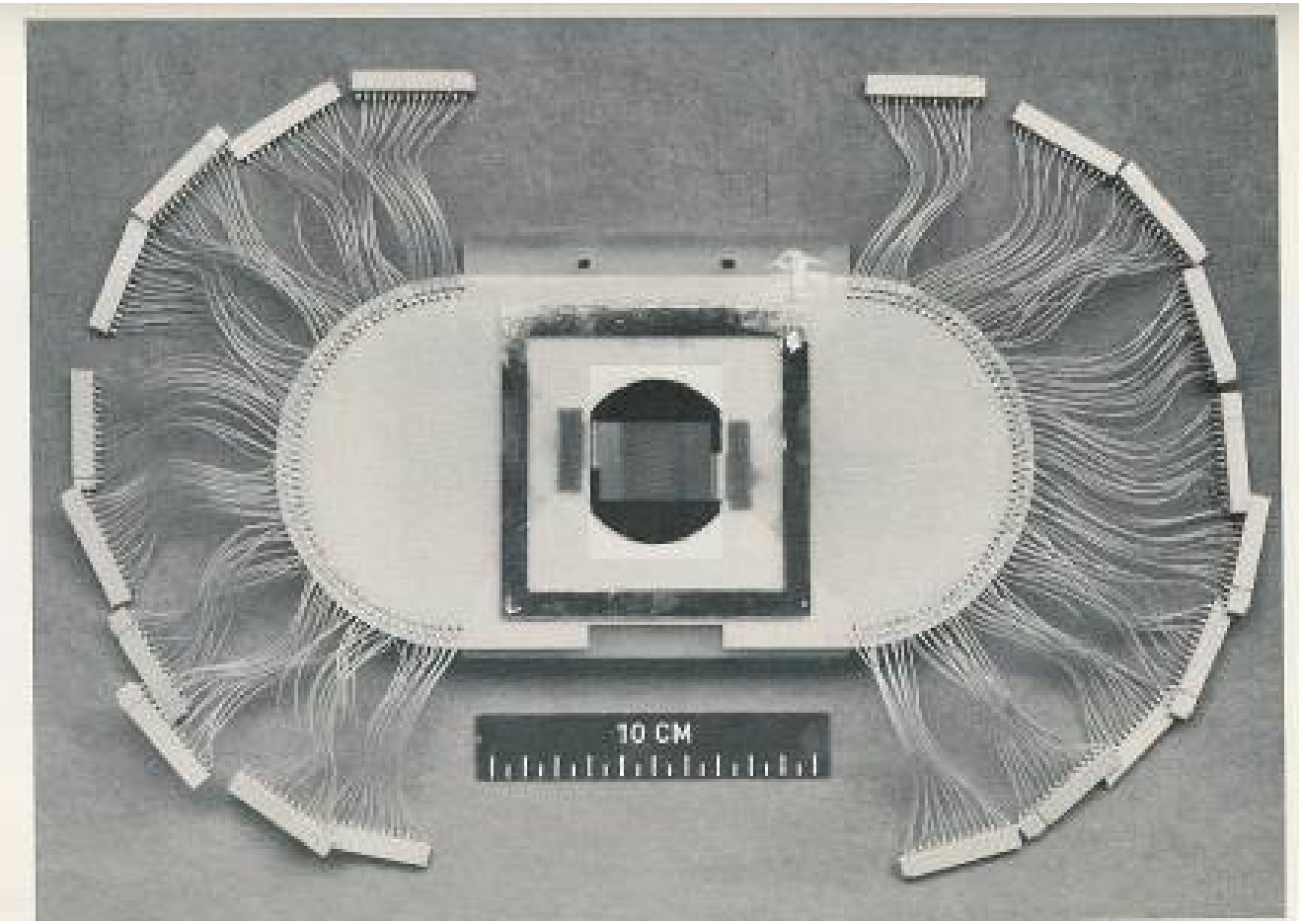
Test boards for every technology are still miles away from ladders to be assembled into an ILC detector. So much to do by 2010/2012 …

Prototype System

- DEPFET module
  - Hybrid PCB with 128 x 64 pixel matrix, 450 µm substrate
  - One CURO 2 r/o + two SWITCHER 2 steering chips
  - FPGA board with fast ADC and SRAM
  - USB 2.0 interface



- We all have a long way to go to reach ‘ladders in test beams’
- Reminiscent of the transition from fixed target to collider detectors, starting nearly 30 years ago …
- We succeeded then, at SLC and LEP, and surely will again!

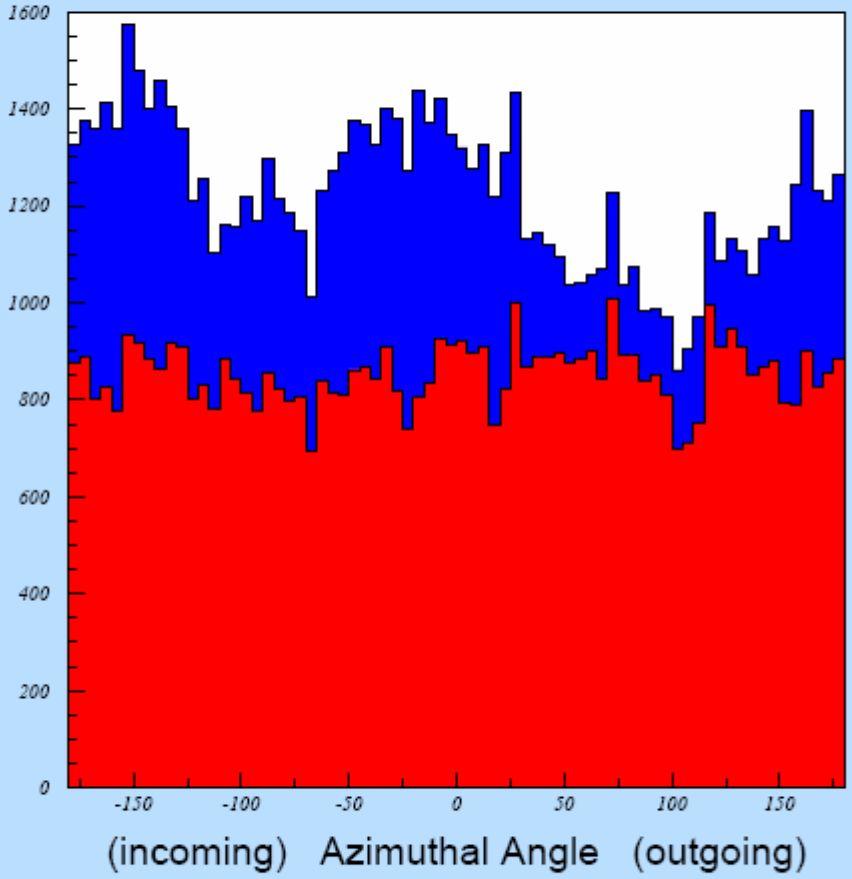


Detector backgrounds

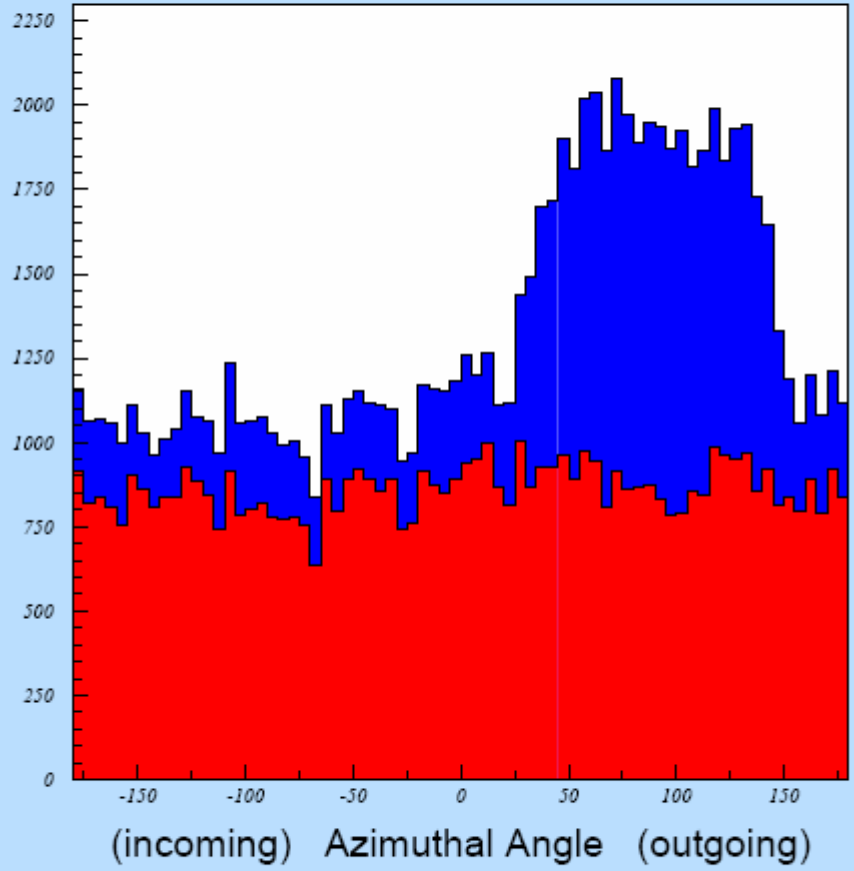
- **Talk by Adrian Vogel**

VTX Hits – phi Distribution

Separation of immediate hits (red) and backscatterers (blue)



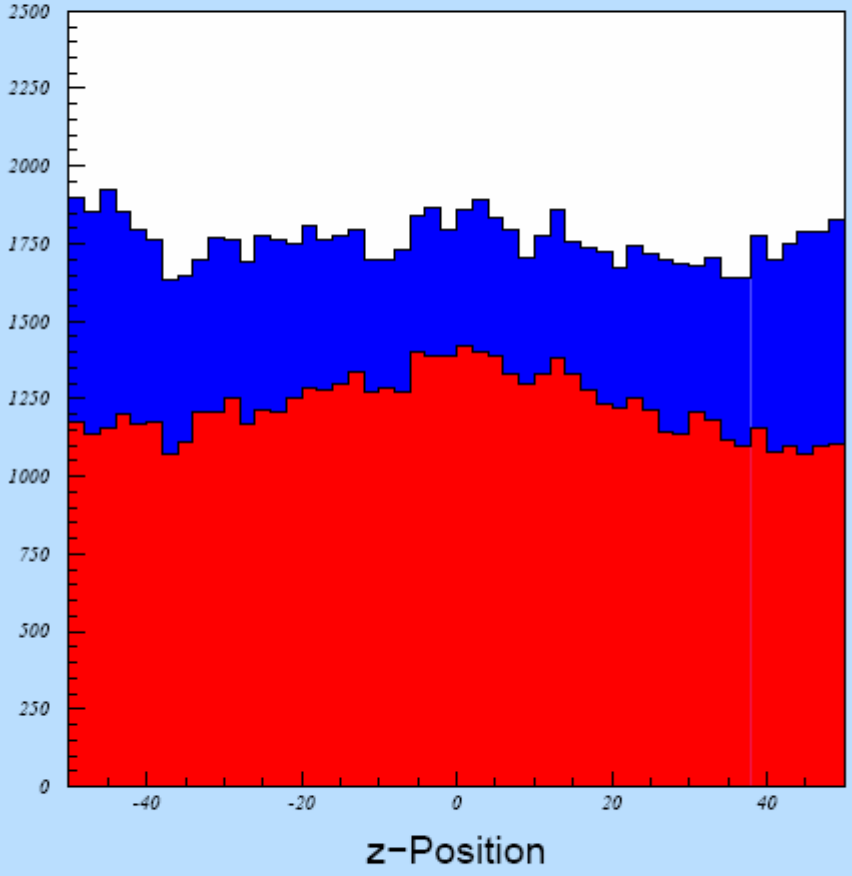
Layer 1, 2 mrad



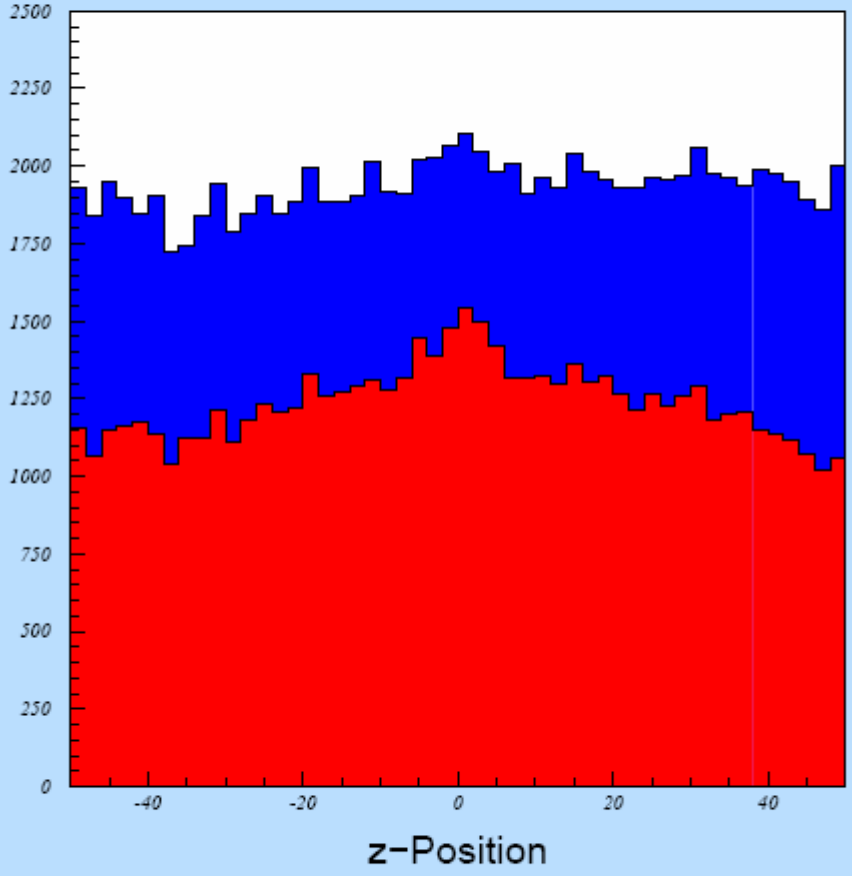
Layer 1, 20 mrad, DID

VTX Hits – z Distribution

Separation of immediate hits (red) and backscatterers (blue)



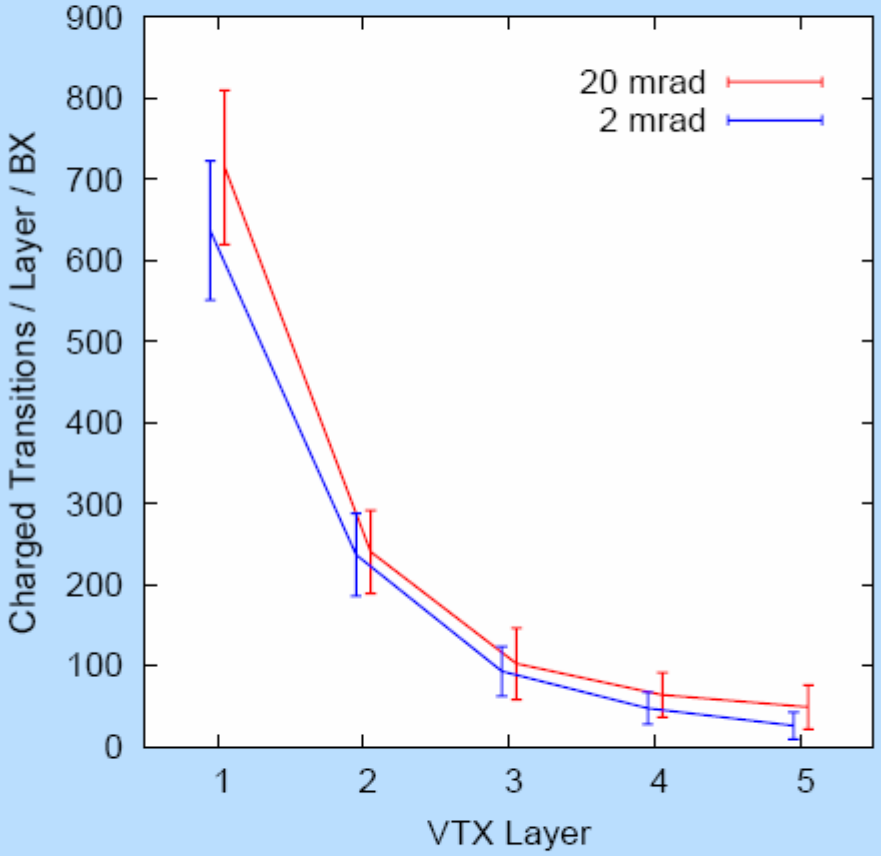
Layer 1, 2 mrad



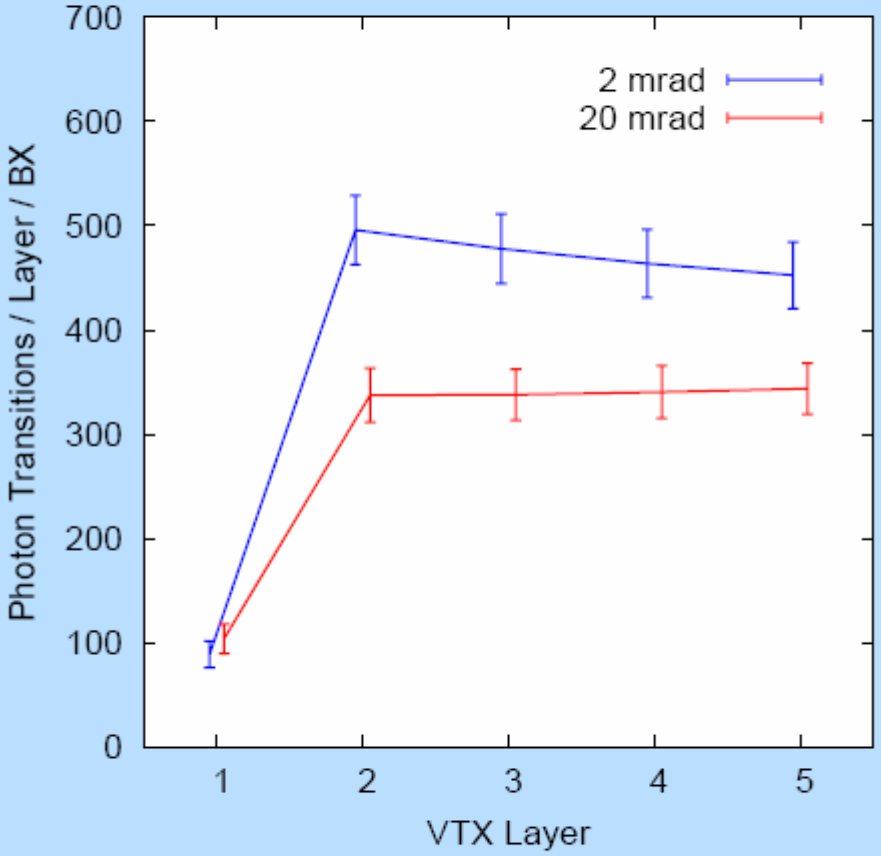
Layer 1, 20 mrad, DID

VTX Transitions – EM Particles

Particles passing through the VTX layers

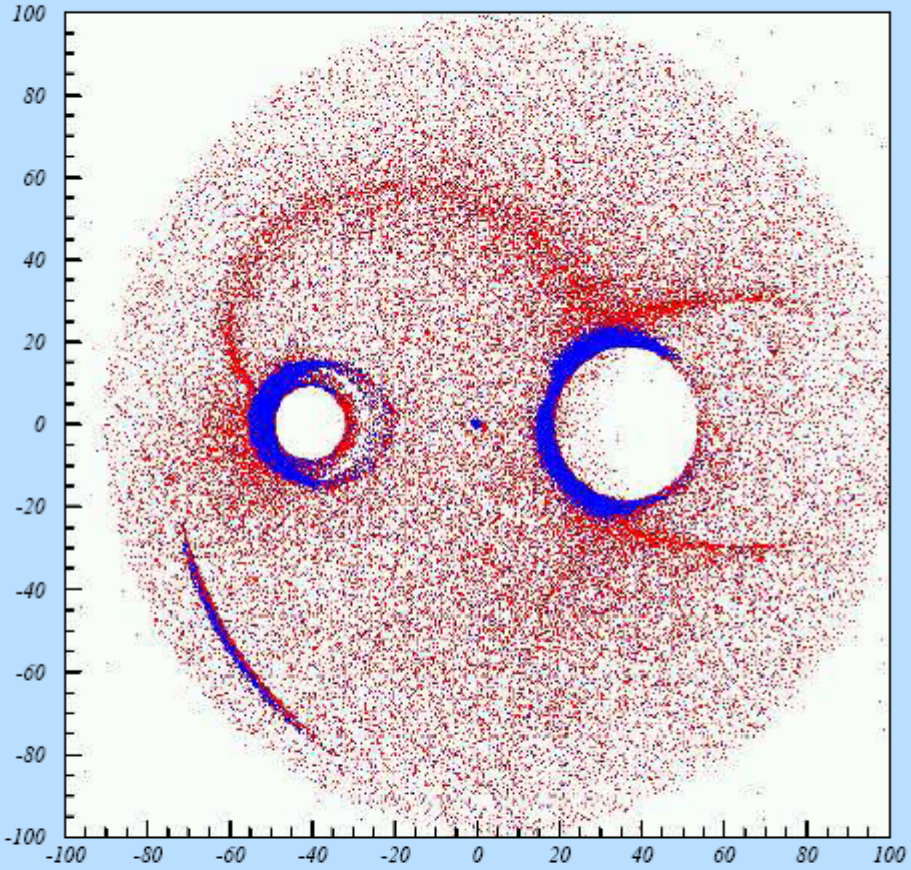


Charged (e^+e^-)

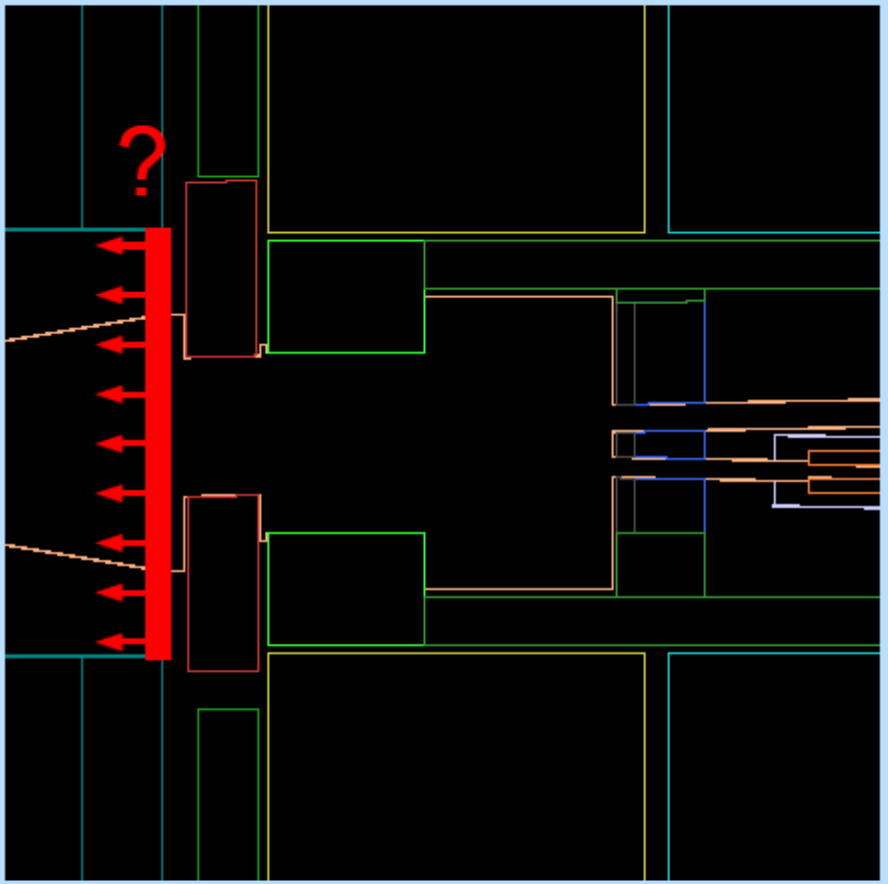


Photons

Backscattering Sources



Origins of electrons (red) and positrons (blue) which . . .



. . . go through this surface in front of the LumiCal

- **Backscatter rates are sensitive to the DID configuration**
- **However, at one time it seemed that backscatter electrons could be reduced to a relatively low level by the graphite block in front of the quad/collimator faces**
- **What happened?**

Beam-related and other RF pickup

- SLD problems now believed (with confidence, following Snowmass 2005) due to 'the elephant' (Steve Smith), namely the mirror current pulse (~ kA) induced on the inner wall of the beampipe - a 'pancake' that accompanies every bunch

- How can it induce external signals? Easily! Cables of BPMs and beamsize monitors provide channels down which RF power will flow. Imperfections in these cables (imperfectly made connectors, 'nicks' in braid during post-installation work, imperfectly closed boxes at the remote ends) provide escape routes for RF radiation

- Seen by Nick Sinev as a delta-pulse on a simple antenna – so not a case of wakefields in the FF cavity (much weaker and longer duration)

- Suggest a 2-pronged strategy:

- *Sensor development*
  - Follow standard industrial procedures to characterise response of sensors to external RF, injected by cables and in form of radiation in a calibrated RF-anechoic chamber
  - Use these results in feedback to the sensor development (just as studies of ionising radiation effects are used to develop sufficiently rad-hard sensors)
  - When collaborations need to select their preferred vertex detector option, use these results, along with the other performance parameters, to reach a balanced decision

❑ *ILC Commissioning*

- **Near agreement that this should be carried out in a relatively open environment (within a blockhouse) with the detector off-beamline, as was done at SLC) [beware of cost-cutting suggestions to commission the machine with the detector in situ!)**

- **Should be possible to include in the machine commissioning a vigilant evaluation of all RF leakage, and fix problems such as badly made connectors, damaged cable screens, loosely screwed cover plates, dirty gaskets on BPM monitor boxes, whatever**

- **For investigation within the IR blockhouse, maybe some highly directional antennas**

- **New idea from Brian Hawes (Oxford U). Instead of highly directional antennas, how about wide-aperture microwave antennas/amplifiers with excellent timing precision (~ 1 ns)? A number of them, stuck to the walls, could pin down the source of RF leakage, as long as a few have line-of-sight visibility to the source. Cheaper and more convenient than directional antennas with remote controlled pointing?**
  [Novel technique being developed to locate people in collapsed buildings, from cellphone transmissions]

ILC vertex detector 'white paper'

Action lines:

- ❖ sensor technologies
- ❖ software tools
- ❖ mechanics/integration issues
- ❖ optimization (physics driven, detector concept *constrained*)

Complemented by:

- ❖ decision making process
- ❖ financial issues (?)
- ❖ inventory of facilities, dedicated and accessible

Potential Editors:

L. Andricek

M. Battaglia

Bill Cooper

T. Greenshaw

+

M. Caccia & advisors (Chris Damerell,…)

Moving towards technology selections

- Suggest that ILC vertex detector community continues to develop as a 'self-organising' structure
- Our previous phone meetings, this workshop, the proposed white paper, suggestions of future workshops every ~2 years, are encouraging
- As well as 'ladders in test beams', where we will learn about:
  - Readout rate
  - Precision in track position measurements
  - Min-I tracking efficiency
  - Actual material budget achieved
- we will need measurements of:
  - Mechanical stability of prototype gas-cooled structures, including vibration and micro-creep (for different geometry options)
  - Radiation hardness
  - Tolerance levels for EMI
- Should we then (2010-2012?) consider a sort of 'mini-ITRP' to make an in-depth investigation of the results, followed by a recommendation to the experiment collaborations, based on a careful evaluation of all performance parameters?
- Those collaborations would as usual weigh this technical recommendation against other factors, in arriving at their decisions