Asian Module R&D
Status & Plan 2016

@LCTPC collaboration meeting
ECFA LCW2016@Santander

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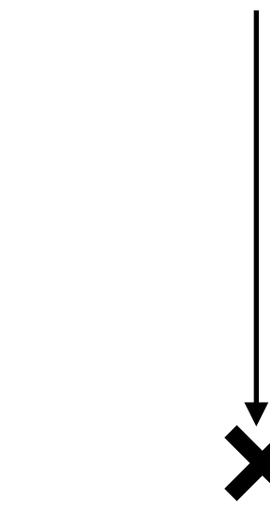
on behalf of LCTPC-Asia/Japan

History of Asian module R&D

2006: JSPS "Gakujyutsu Sousei" start
"Basic concept"
2007: Pre-Prototype study of LP1 module
PCB design @Tsinghua
2008: LP1 Asian module

2009: LP1 module@testbeam w/ Altro RO
without Gate -> Large Distortion
2010: Beam test w/ old gate
Discharge/damage RO electronics
2011 modification of GEM JSPS"Tokusui" start
design field shaper
2012 Beam test w/ field shaper no gate
wire gate
2013 Fujikura Gate type0(3cmx3cm round hole)

2014 Fujikura Gate type3(honeycomb)
2015 type4(module size)



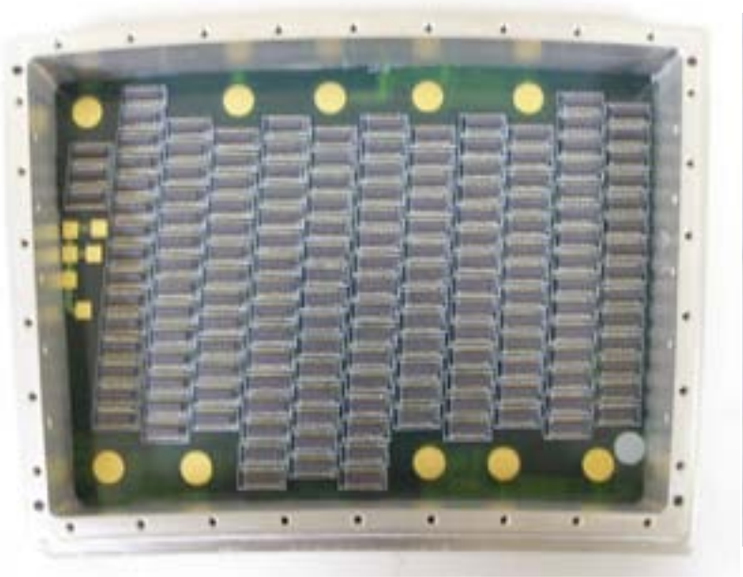
Conceptual design of asian module

Minimize insensitive regions(module boundary, GEM frame)

pointing IP

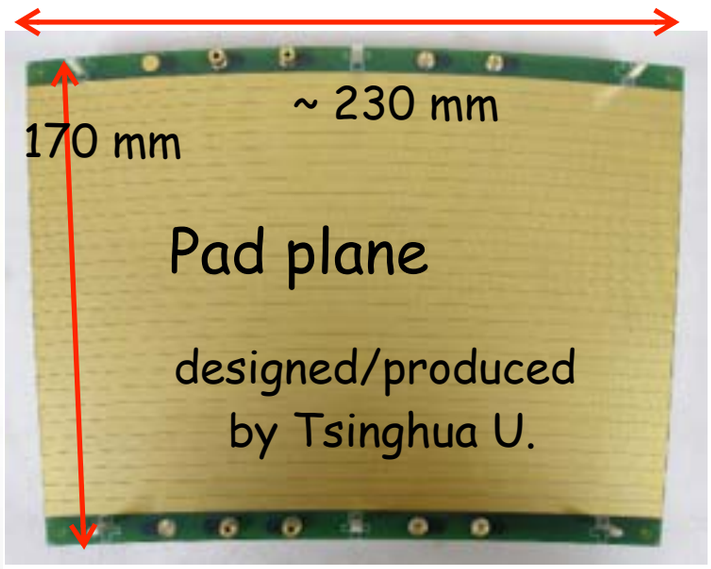
no side frame

not proved yet !



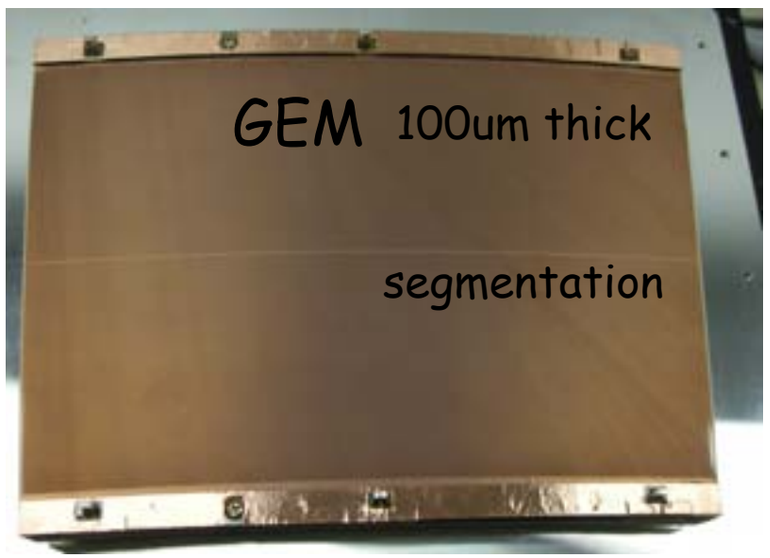
Bunch of tiny connectors
(40 pins) 161 connectors

all other space for HV supply
+ Back Frame



28 pad raws (176/192 pads/raw)
~1.2(w) x 5.4(h) mm^2
staggered every each layer

Total 5,152 ch/module



Double GEM (100um thick)
for simpler structure

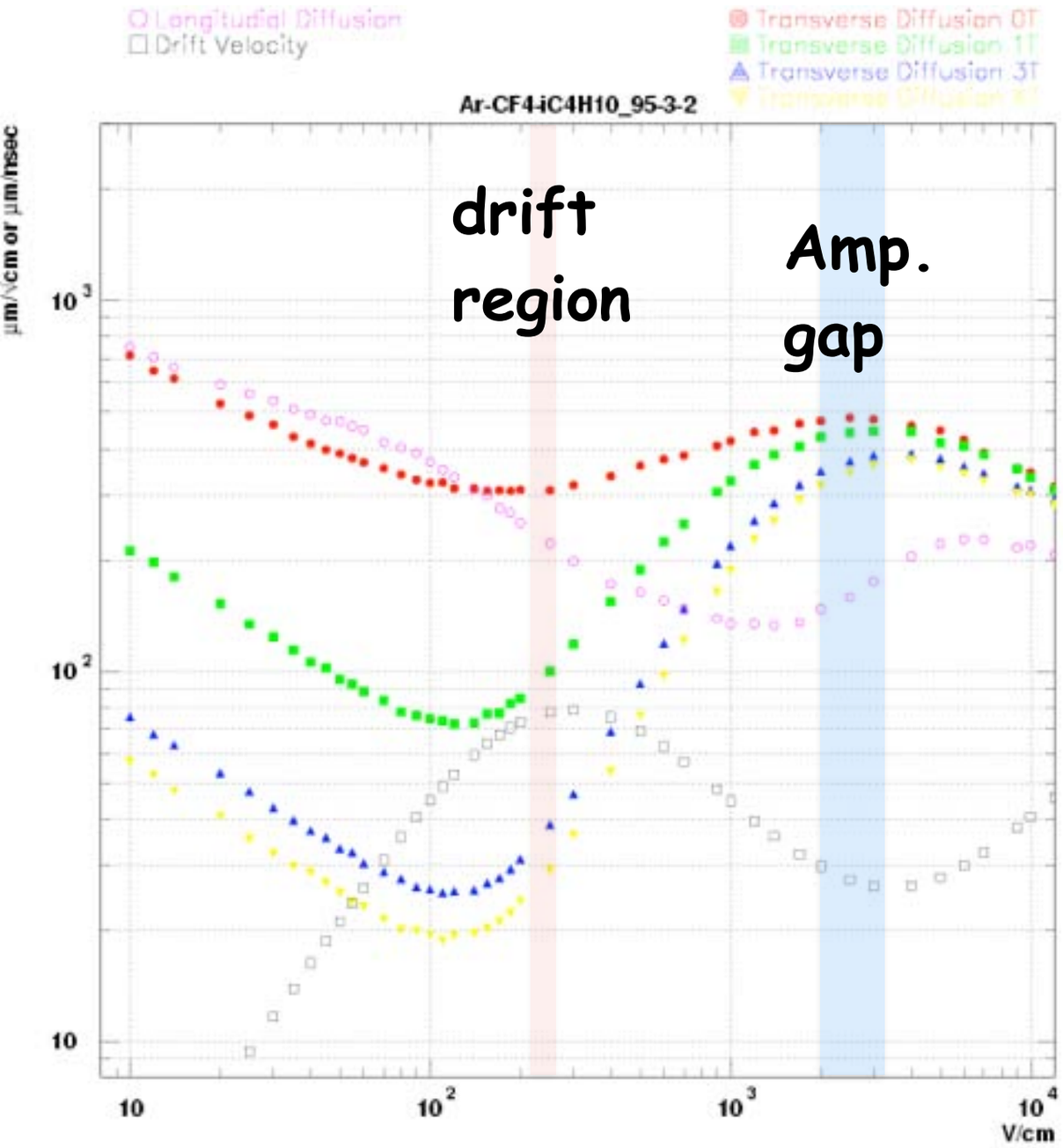
GEM electrode is divided in the middle of R

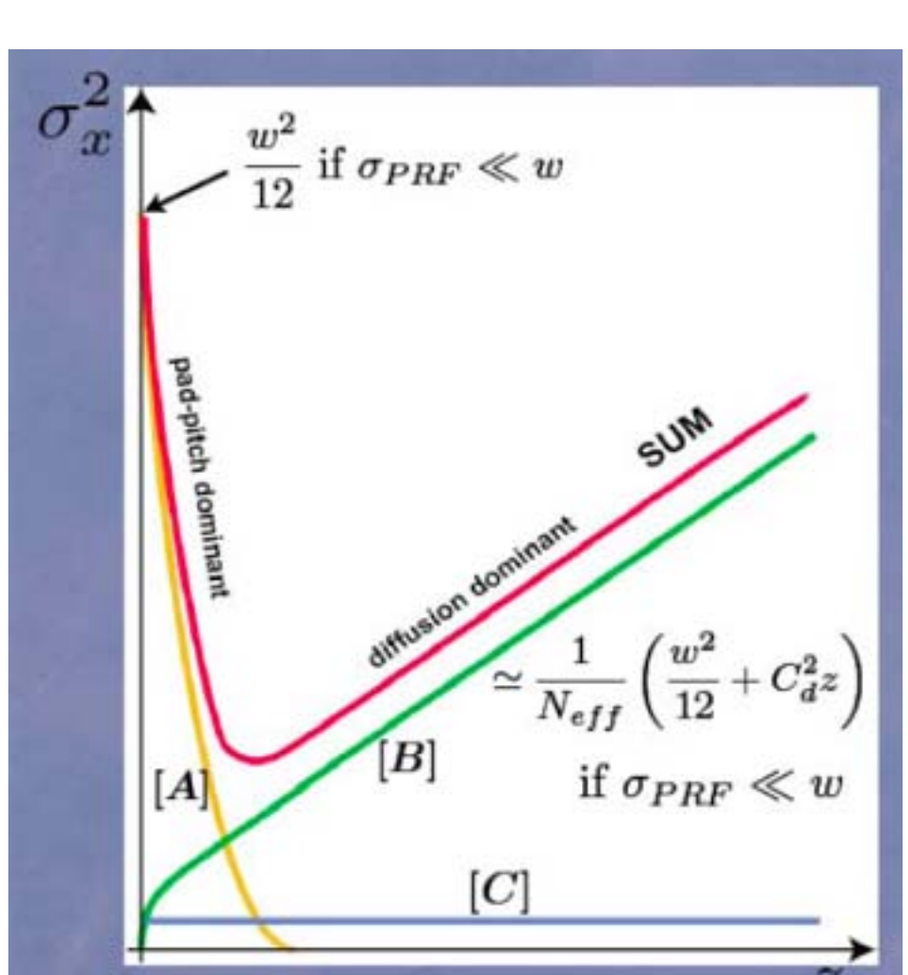
Gate GEM is assumed above GEM structure

Pad size

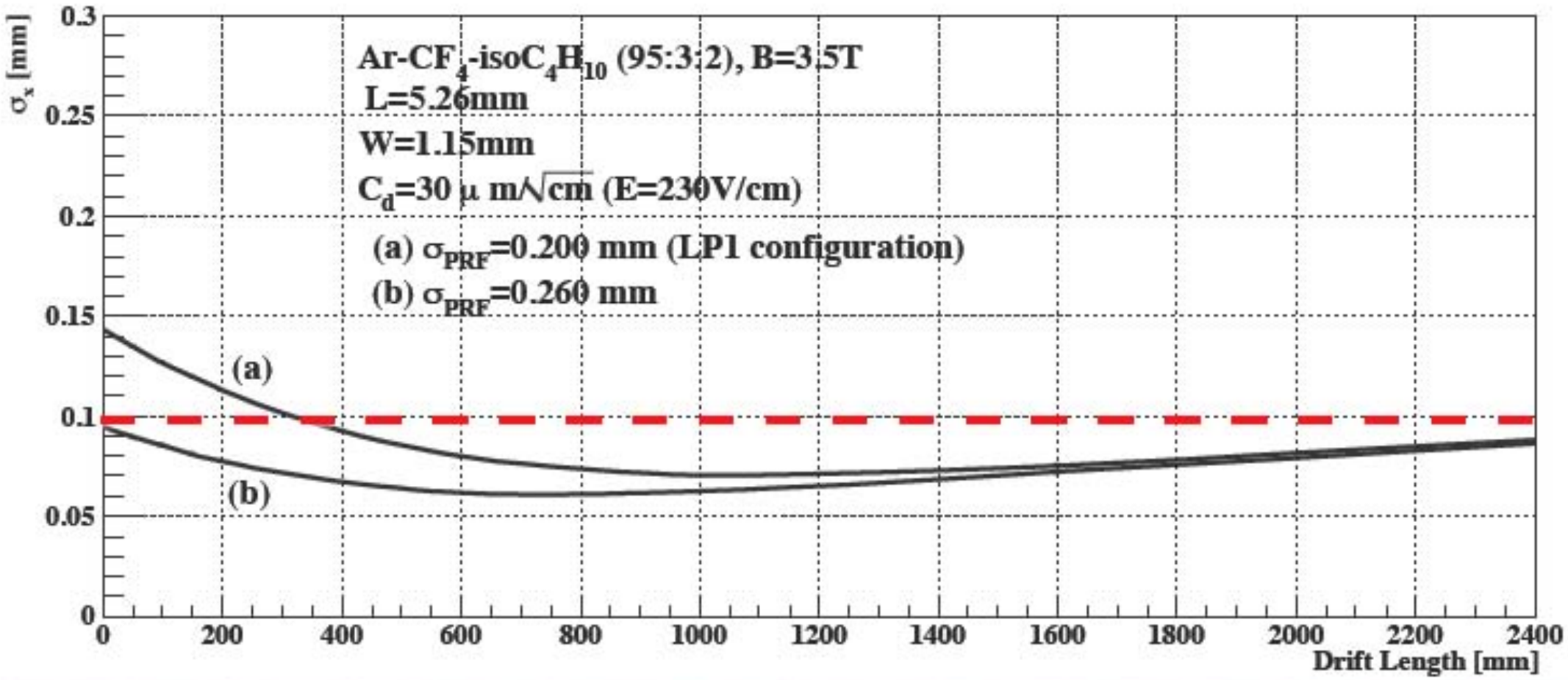
We have a reason to choose 1mm pad width for GEM

Optimum pad width is 3~4 times of diffusion @ amp. region(PRF)
in order to avoid hode scope effect





Extrapolation to the ILD-TPC



The expect perfo
satisfied with th

In order to achieve 100um res. all over the drift volume,
we have to have more diff.@amp region or narrower pad

What we have to do/complete before 2017

LOI ?

technology choice?

Priority module w/ Gate :

-> we have to show we can achieve target performance with gate.

GEM : stable and durable

Cooling method:

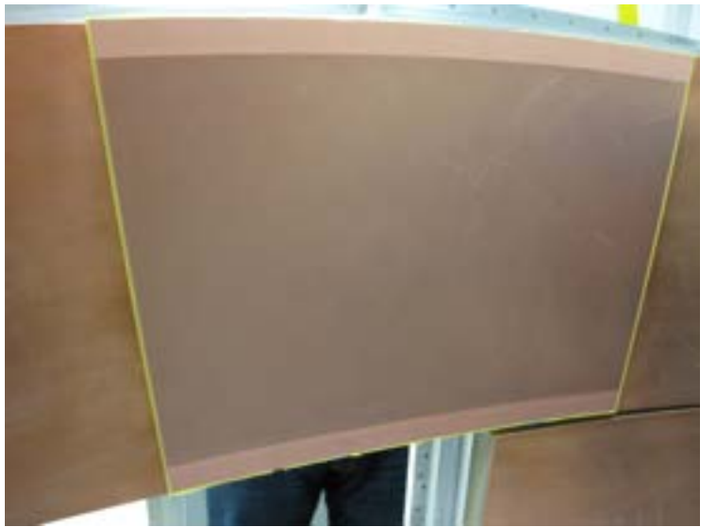
Module boundary:

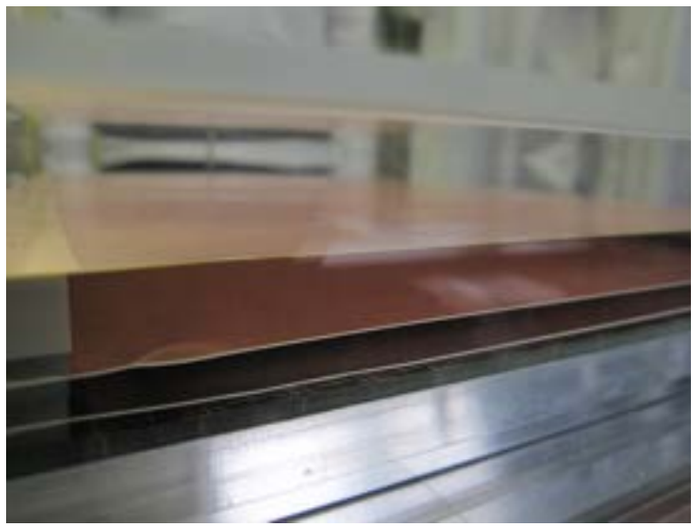
Module structure:

As our budget @2016 is extremely limited
no new investment is possible

Gate on the module

2010 Beamtest
mount to LP1
-> Discharge !!



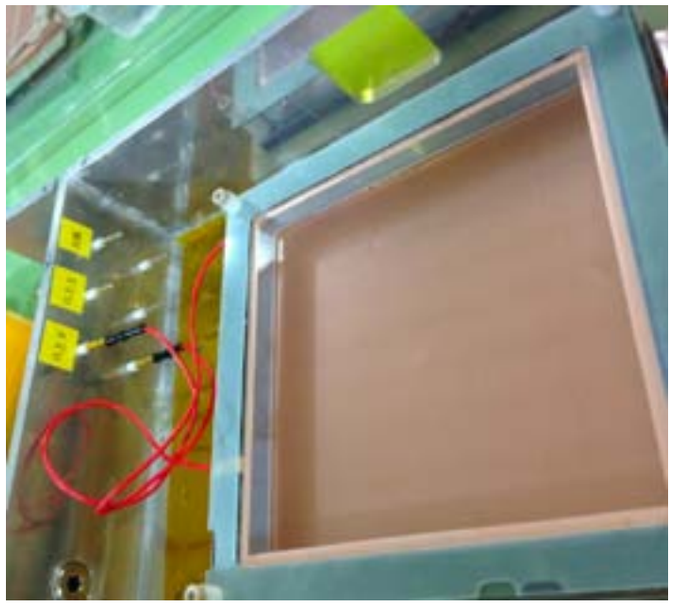


test chamber

2008 Scienergy
90um hole 140um pitch 14um
Transmission ~50%

2013 Fujikura type0
300um hole 330um pitch

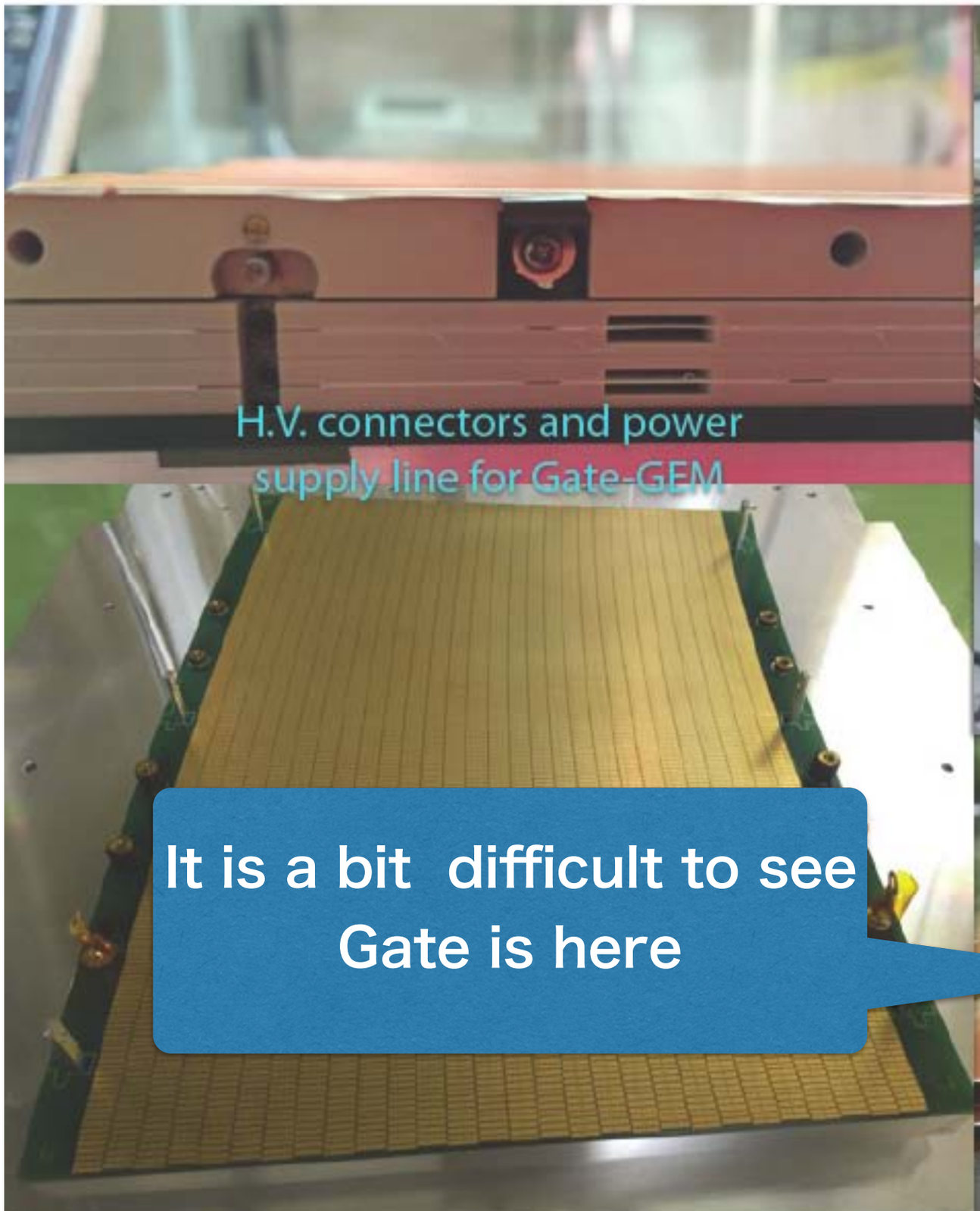
2014 Fujikura type3
300um hole 330um pitch
honeycomb

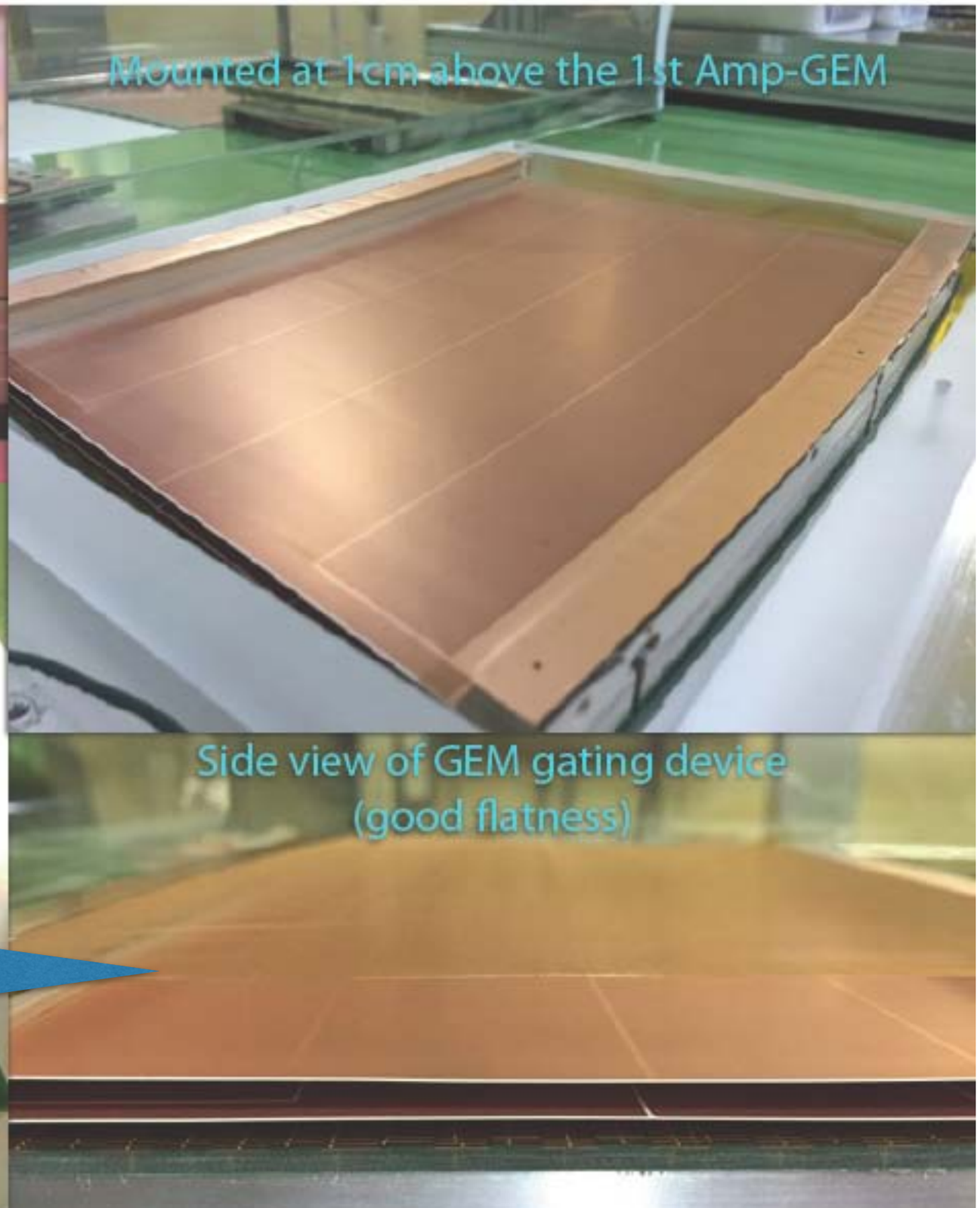


2015 Fujikura type4(same as type3)
300um hole 330um pitch module size
B=0T 55Fe test, laser test

2016 beamtest with type4
performance test

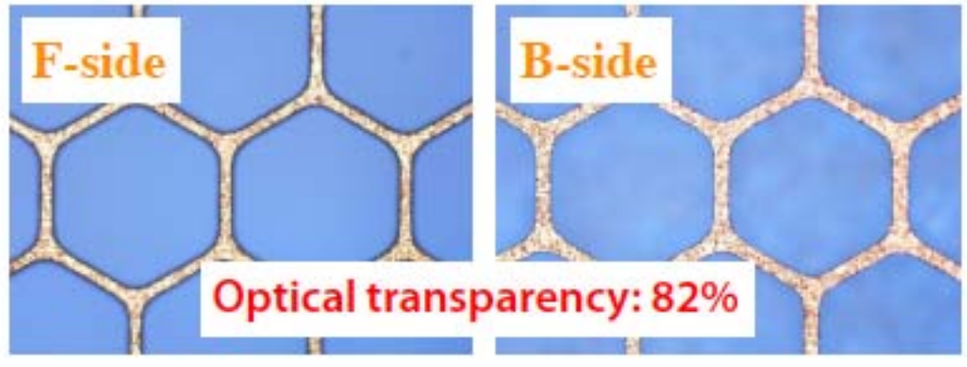
Integration of module-sized Gate-GEM





Gate performance

Type3 : 330um pitch 30um rim
10cm x 10cm



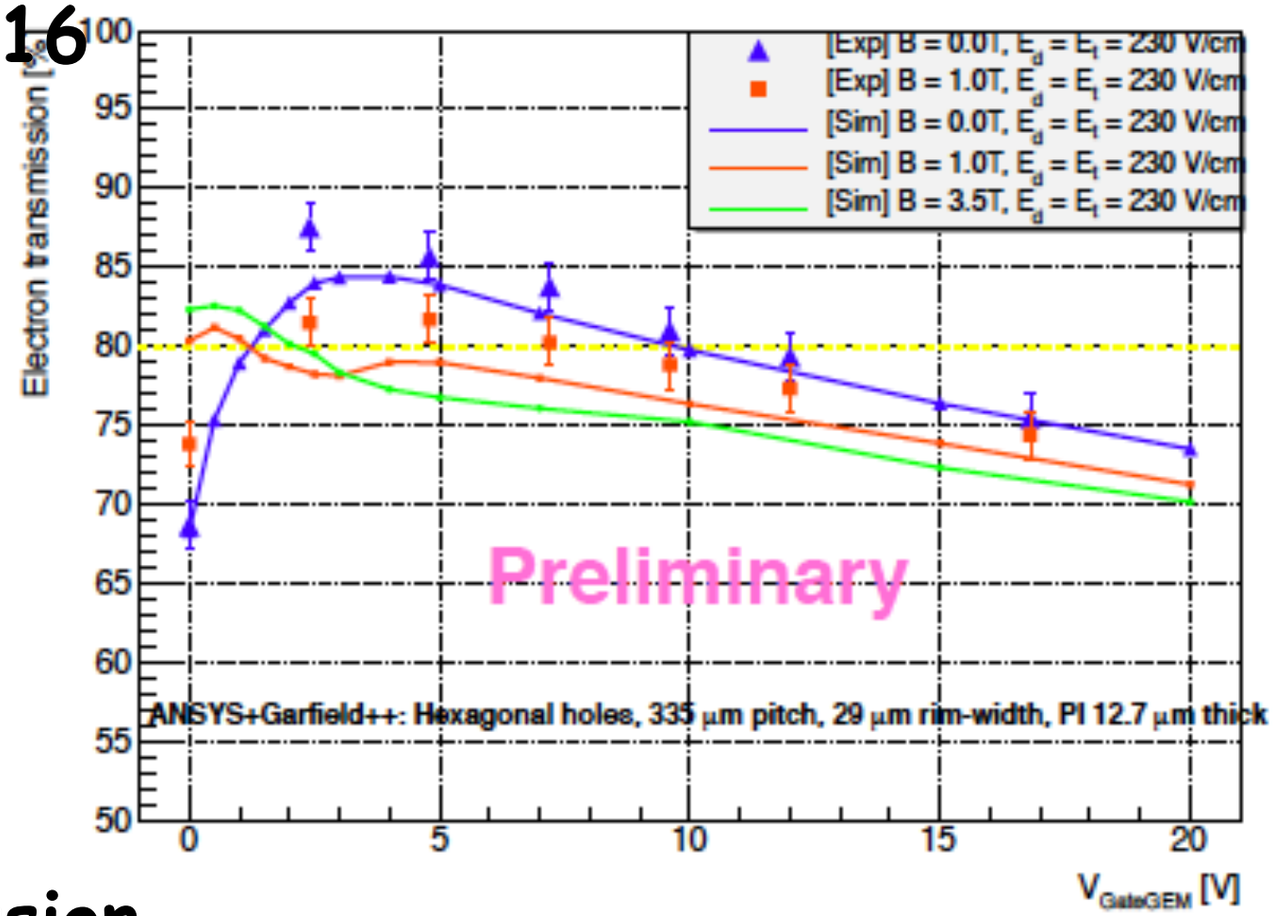
Electron transmission
has been measured @0/1T

80% expected at ILC condition

influence to space information
will be checked at beam@2016

ion blocking ability
not planned yet

Exp vs Sim (Fujikura Type 3)



Detail is discussed at Gate session

GEM on the module

Scienergy : 100um thick LCP GEM double stack

reason: simpler than triple stack at the beginning

reputation: we may have frequent micro discharge.

study by KEK/Kindai -> no difference from CERN GEM

RIKEN (tamagawa) found thickness uniformity is not so good

for LCP (10% diff.)

gain may change locally up to ~100%(?) diff.

overall gain adjustment needs more attention

depend on spec. of each sheet

Study of each GEM sheet property at KEK

gain survey allover the module for each GEM stack
as a function of VGEM setting
and monitor discharge rate.

-> fix proper operation condition for the next beam test

future GEM ?

glass GEM : single GEM provide enough gain
size, diffusion,

GEM sheet design

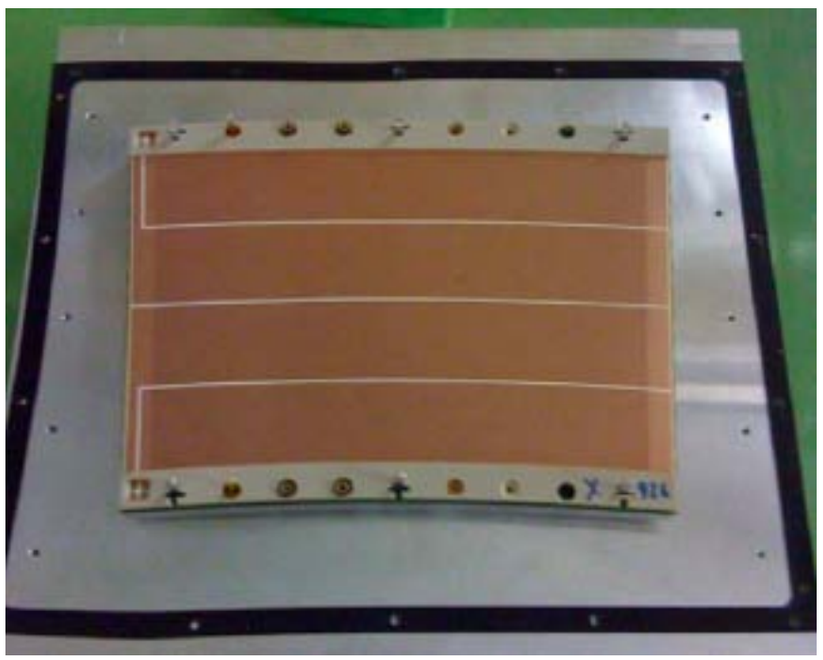
segmentation 2

-> observe frequent trip

gap 300um

-> gap was too short

one segment trip -> discharge@gap



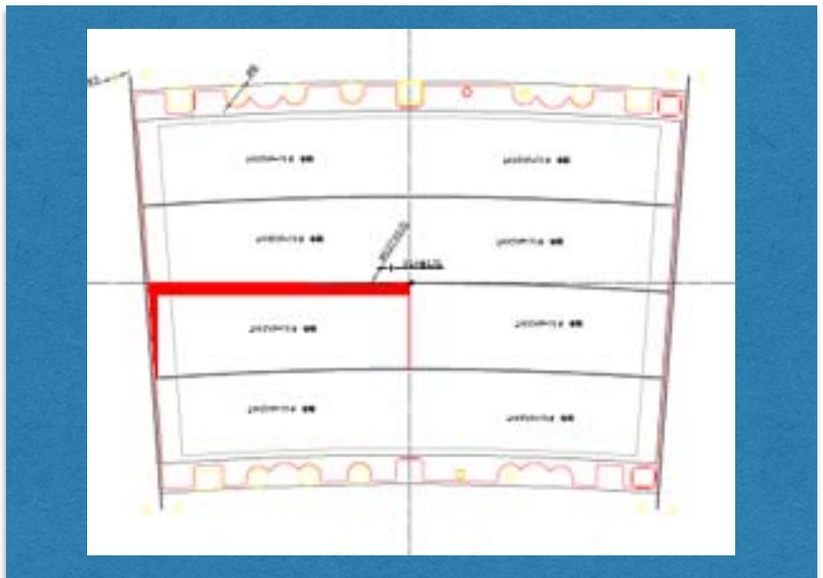
segmentation 4

-> improve? but many discharge

gap 1mm

-> HV OK but

-> this gap provide another distortion



no segmentation@front/ 4 segments@back

-> distortion became smaller

gap 500um

GEM sheet design

Segmentation : necessary, 4 segments be better !?

HV supply : dead space ?

contradiction to side support less structure

gap between segments needs 500 um ?

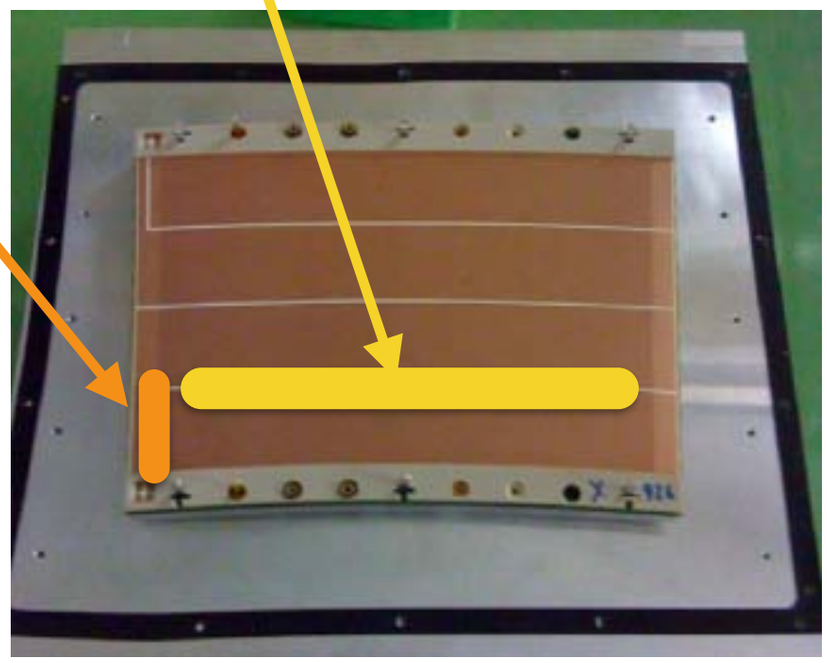
300um was too narrow for occasional HV trip

Gap on GEM sheet effect though Gate will cover GEMs;

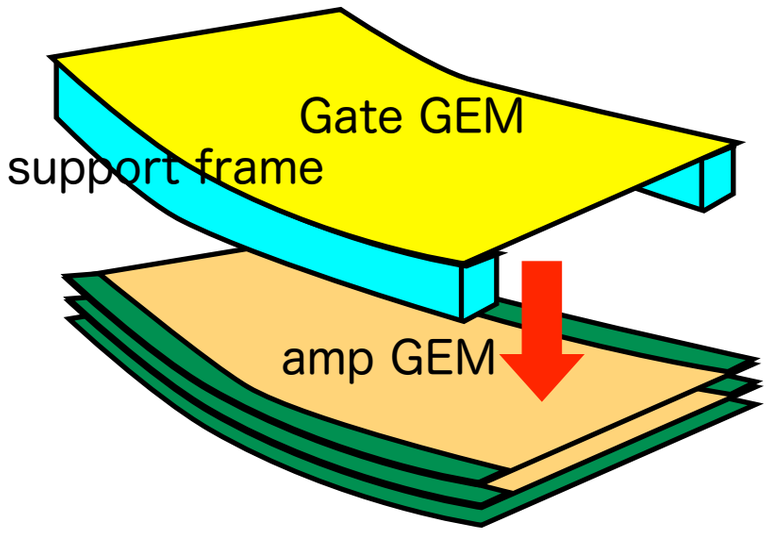
distortion must be local effect at Gate transfer region

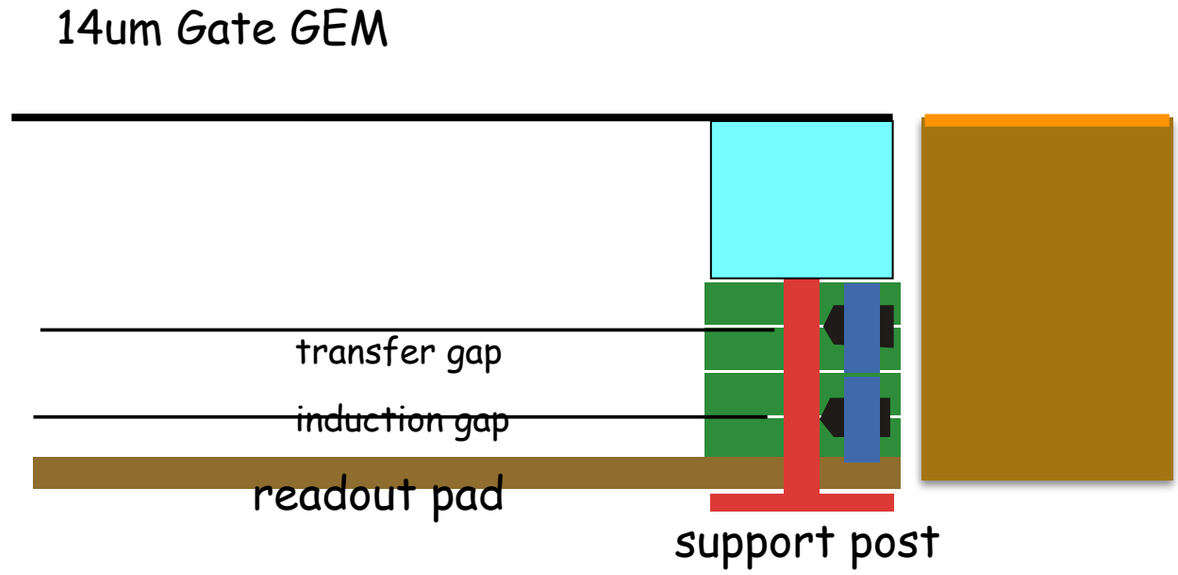
correctable for these region

uncorrectable



GEM stretching method





tension of GEM is applied against post

post metal

too much room for adjustment

difficult to align GEM on the place

We gave up Fit-in method as its concept was not proved

We don't have alternative option yet.

NEXT module

though we don't have budget

Upper structure

Gate GEM

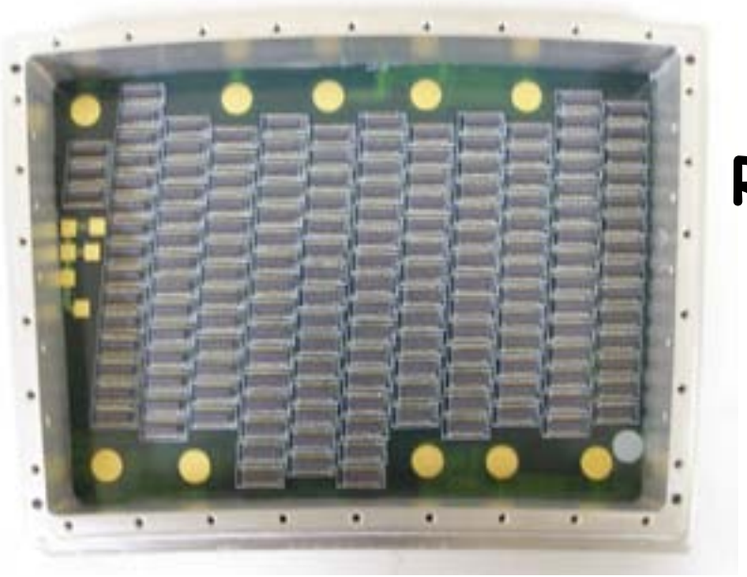
GEM Amplification

how do we mount ?

PCB

Readable channel is 60% of LP1

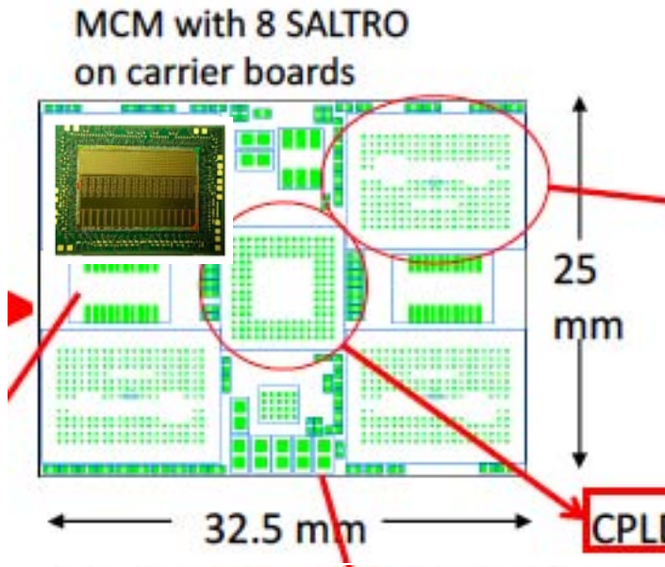
how do we read ?

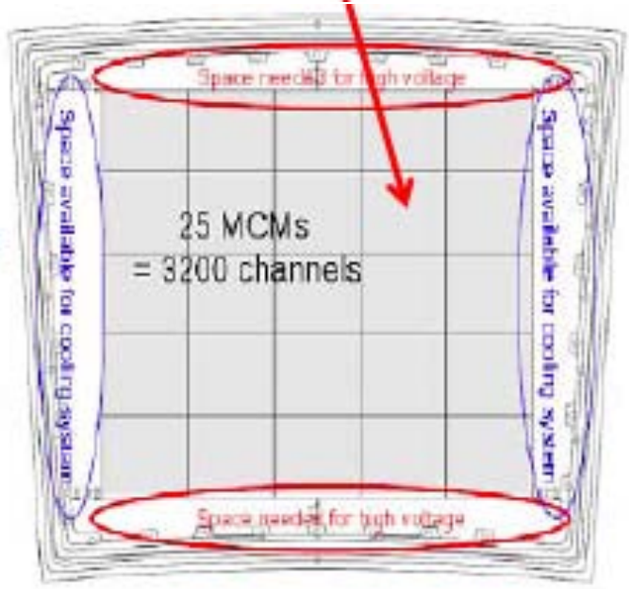


Lower structure

RO electronics/cooling/HV

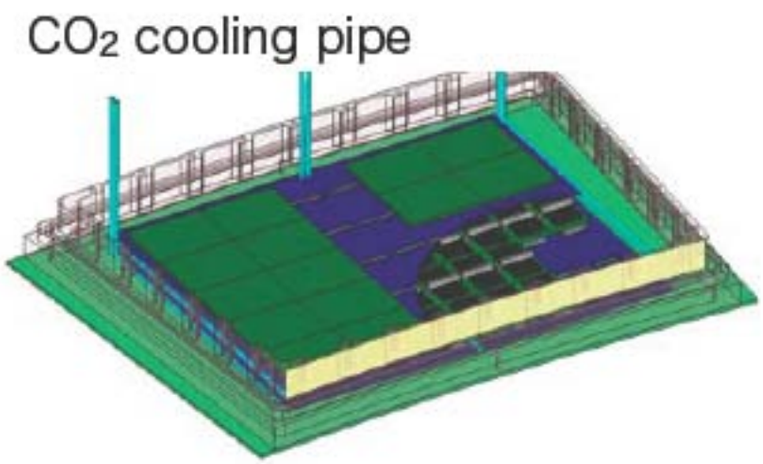
how do we cool ?

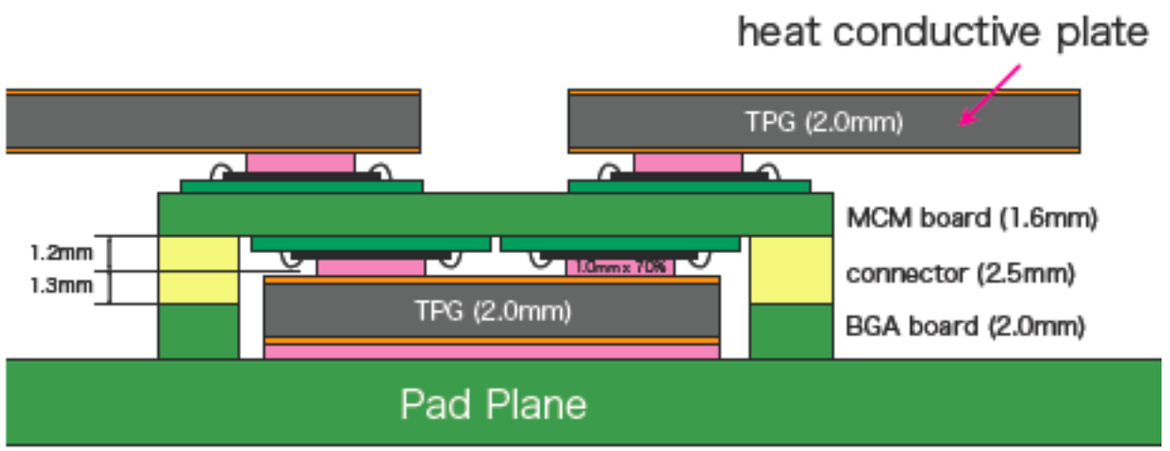




Lower structure　　Readout electronics (Leif)

Paul already demonstrated the case;cooling pipe running over all chip
Is this applicable to sAltro16 ?

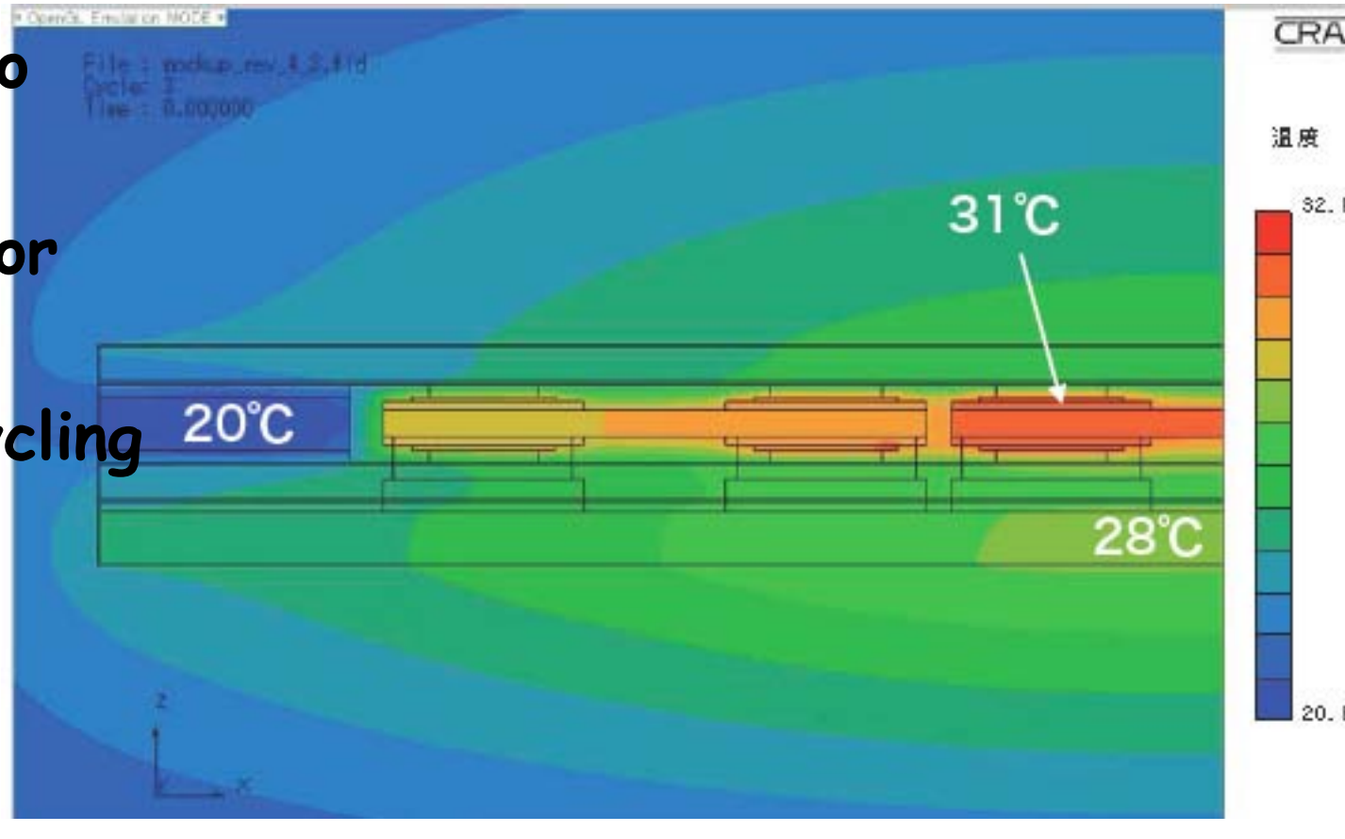




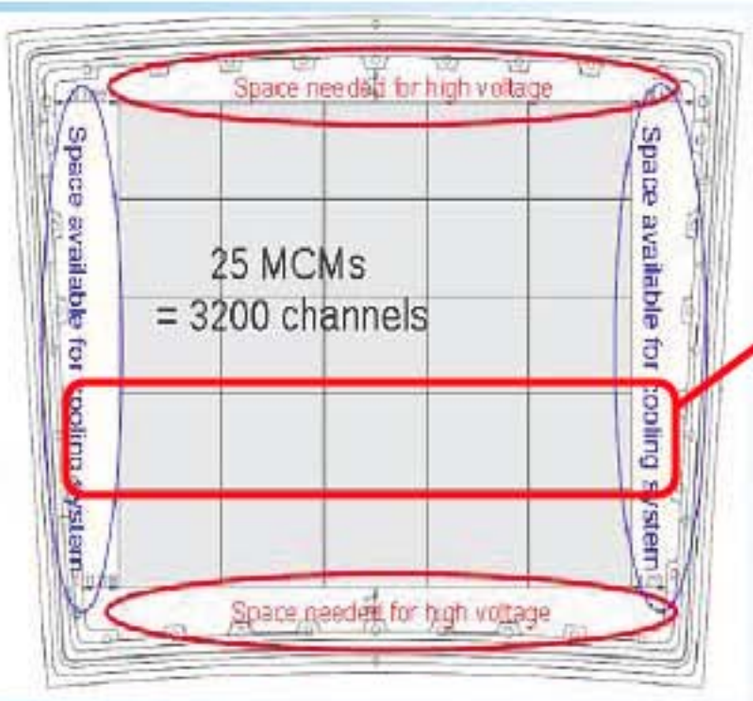
Cooling scheme is studied by Takahiro

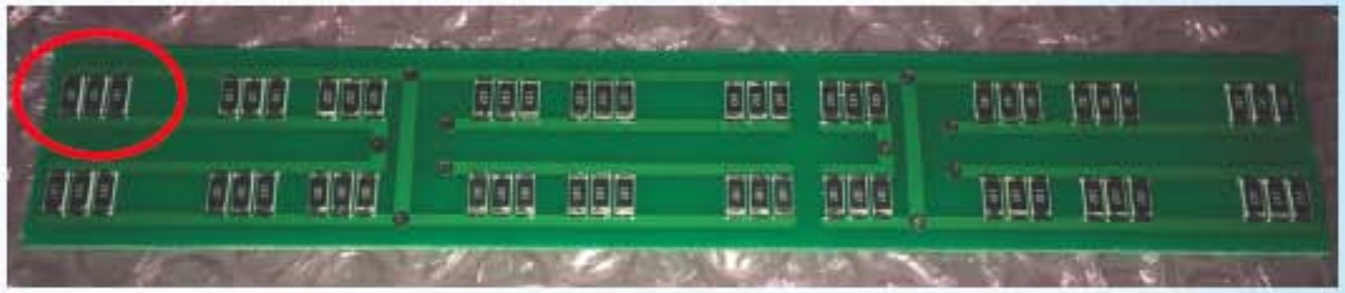
simulation using TPG as heat conductor
non-negligible temp. gradient
w/o power cycling
heat flow through connector

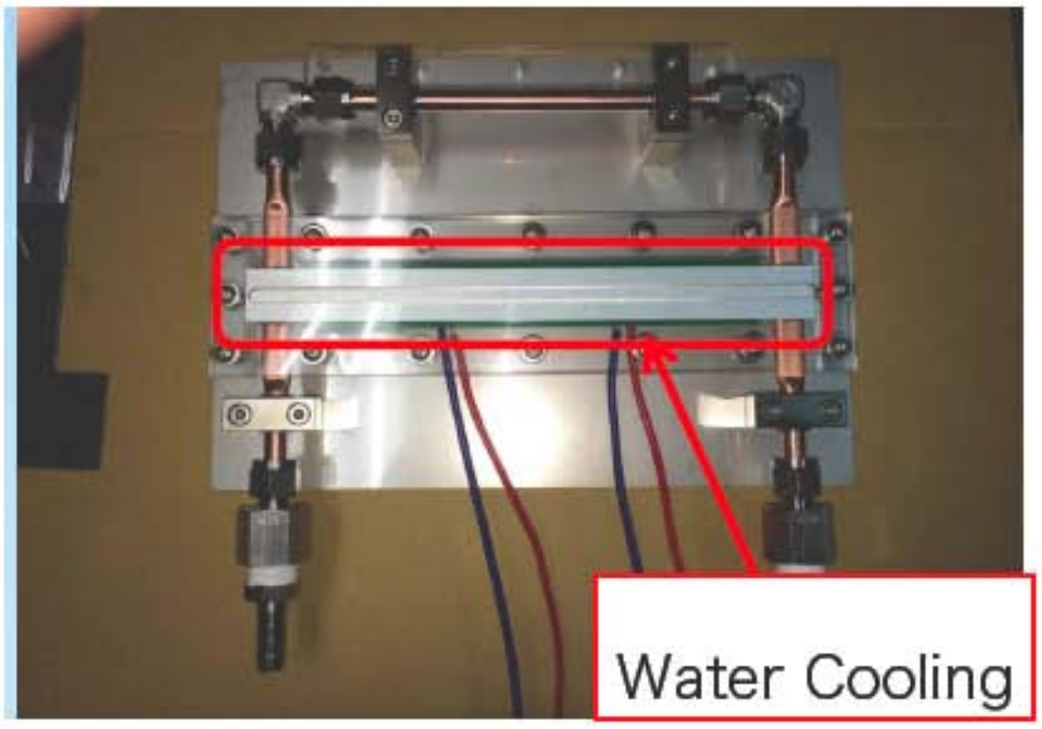
Mockup study will be started

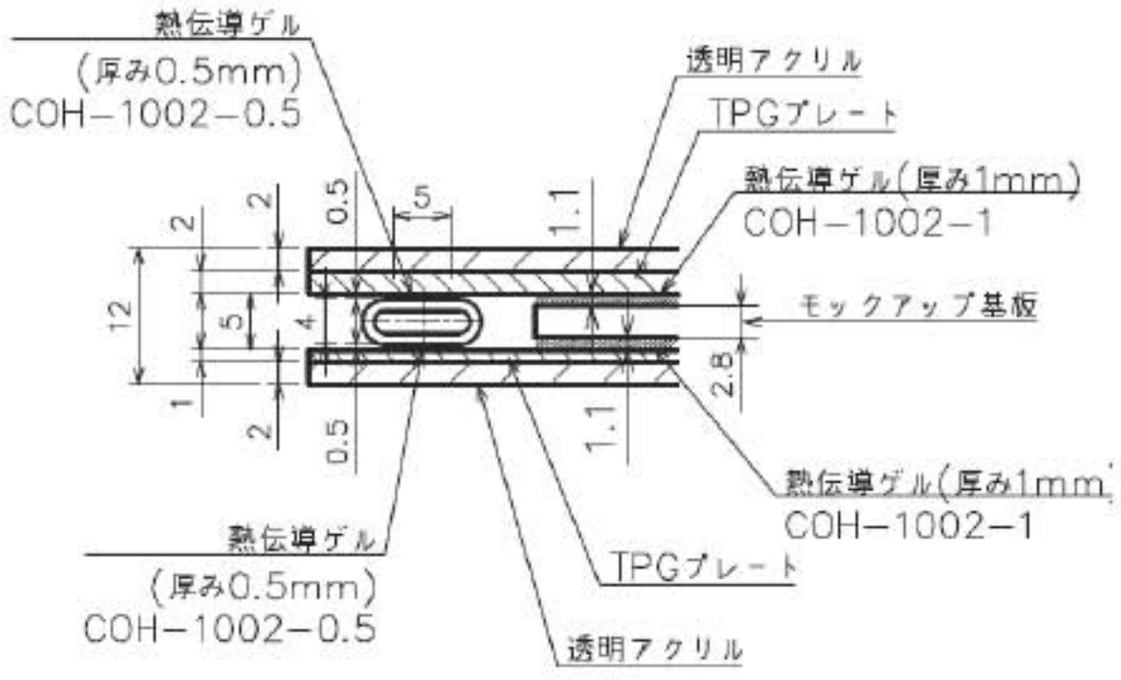


Mockup test under water cooling setup



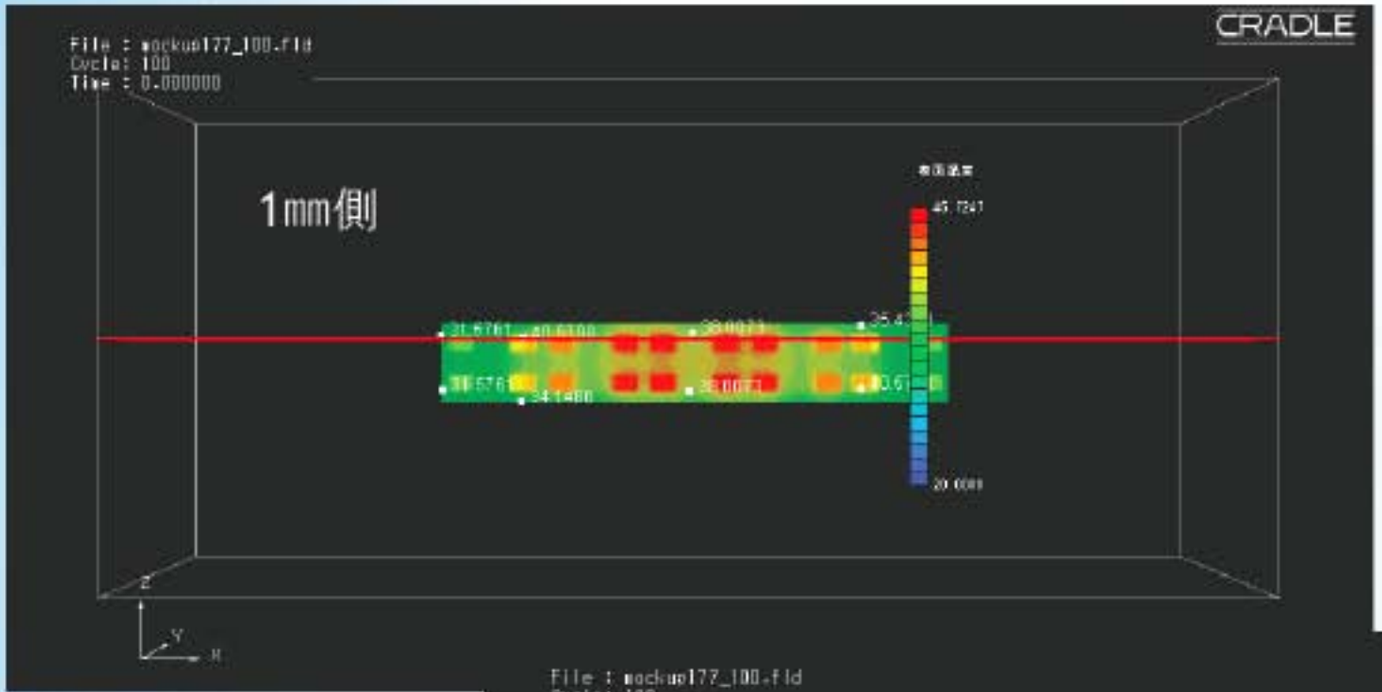






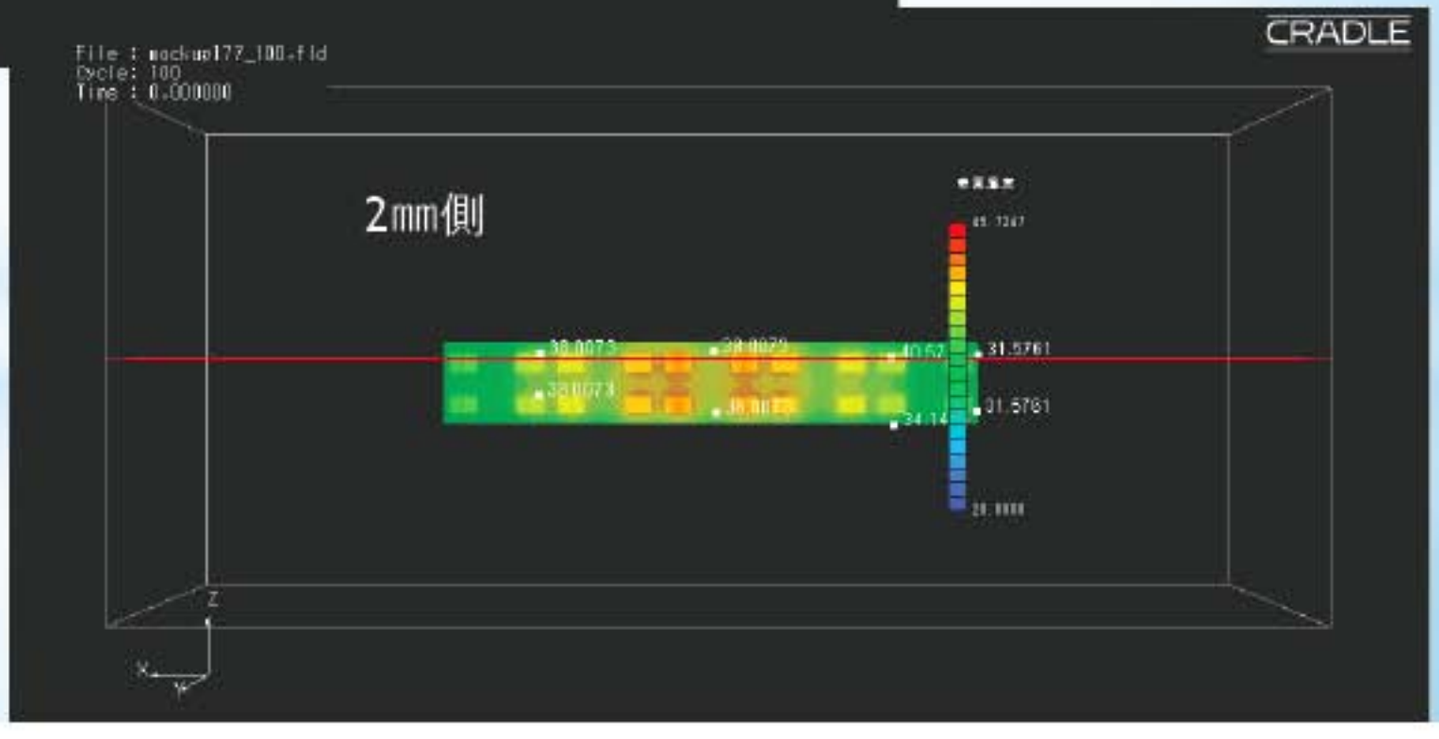
Mockup test under water cooling setup

*電源17.7Vにおけるシミュレーション



・モックアップ
基板上の様子

最高温度45.7247℃
基板上温度勾配　約8℃



Study with CO2 cooling is also going

How do we define the next module ?

Integration of module upper structure and lower(RO) electronics

a demonstration of LP module : important aspect

not necessary for each module

how this work connect to the design for LOI

to technology choice

Schedule of 2016

Nov. 2016

Beam test : module with Gate + Altro RO

demonstration of basic performance of GEM+Gate system

Laser test : basic property of module

module design for sAltro16 integration including cooling

towards the final module design -

inter-module distortion

Summary

Basic performance test of the Gate integrated module
 at Beam is expected Nov.2016
module-size Gate is ready(old structure)
 is processing (Field shaper type)
Demonstration of realistic performance
 Gate related study is also going.

For the next module, we continue study of cooling.

discussion/simulation of the final module is necessary