Gating device

LCTPC collaboration meeting
ECFA LCW2016@Santander

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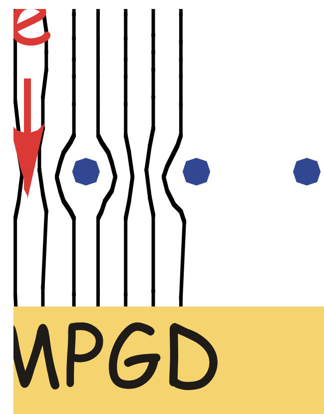
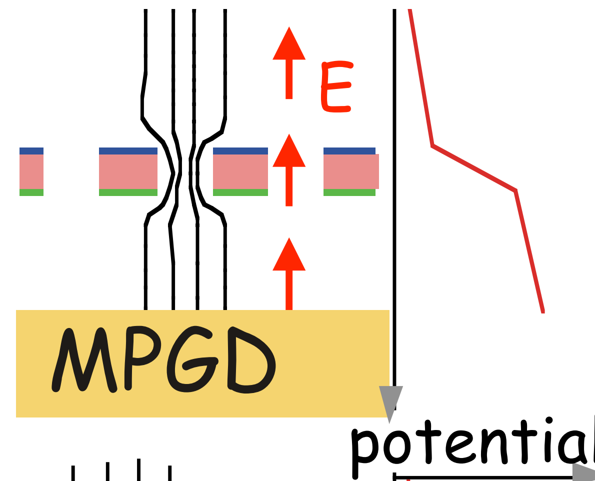
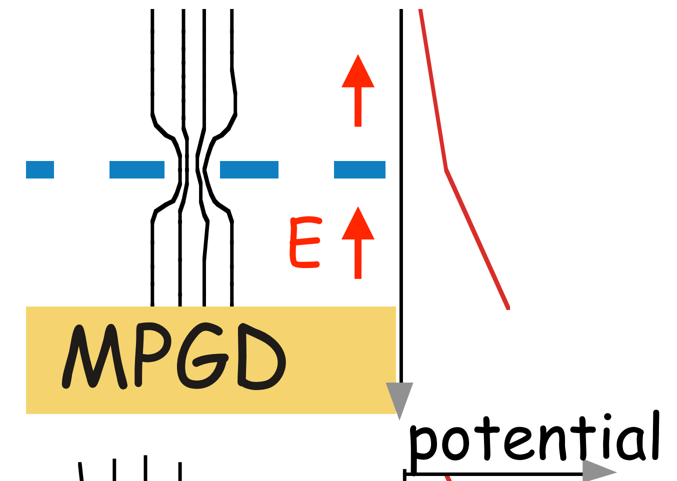
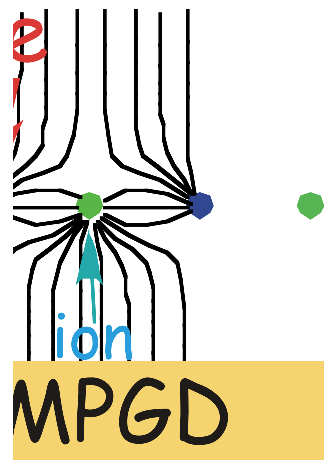
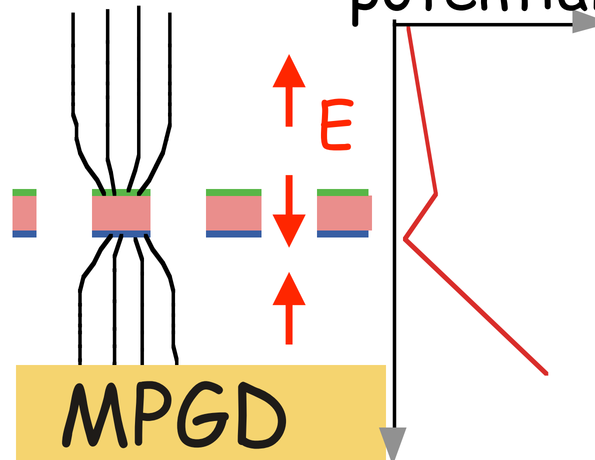
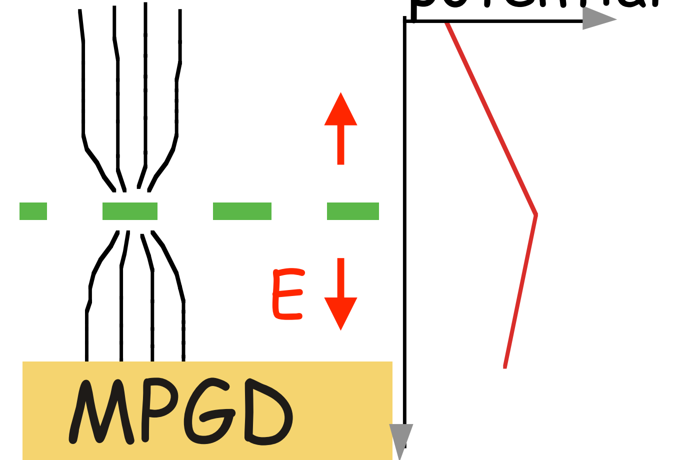
Gate candidate

How can we achieve "Gating" for TPC?

	Traditional wire method	GEM method	micro mesh method
Gate Open			
Gate Close			

Wire :

wire spacing would be large enough
to deteriorate resolution by ExB
wire sp
need sti
Local ch

GEM :

Electron transmission is in question
collection/extraction efficeincy

Micro mesh :

need thin mesh
for higher transmission
esh pitch ~O(50um)

er change of E field
@ drift region

Graphene is also proposed as gating device!!
RD51

fall-back option : wire Gate

Performance has been established at old the past experiments

But Simulation expect small degradation of performance
at high B field 3.5T.

Integration with MPGD module is not so easy
Wire gate was produced on rigid field shaper frame
though it doesn't have open-close mechanism

Some tests are done using laser but
it's difficult to evaluate wire gate without B field

No schedule for beam test.

Status of GEM gate

2. Laser drilling process

Type0

■ Results

Item	Gating foil
Hole size	302µm
Hole pitch	330µm
Rim width : F-side	14µm
Rim width : B-side	28um
Insulator thickness	25µm (&12.5µm)
size	10mm x 10mm
Processing time	6 min (Only Laser)
Optical aperture ratio	75.8%

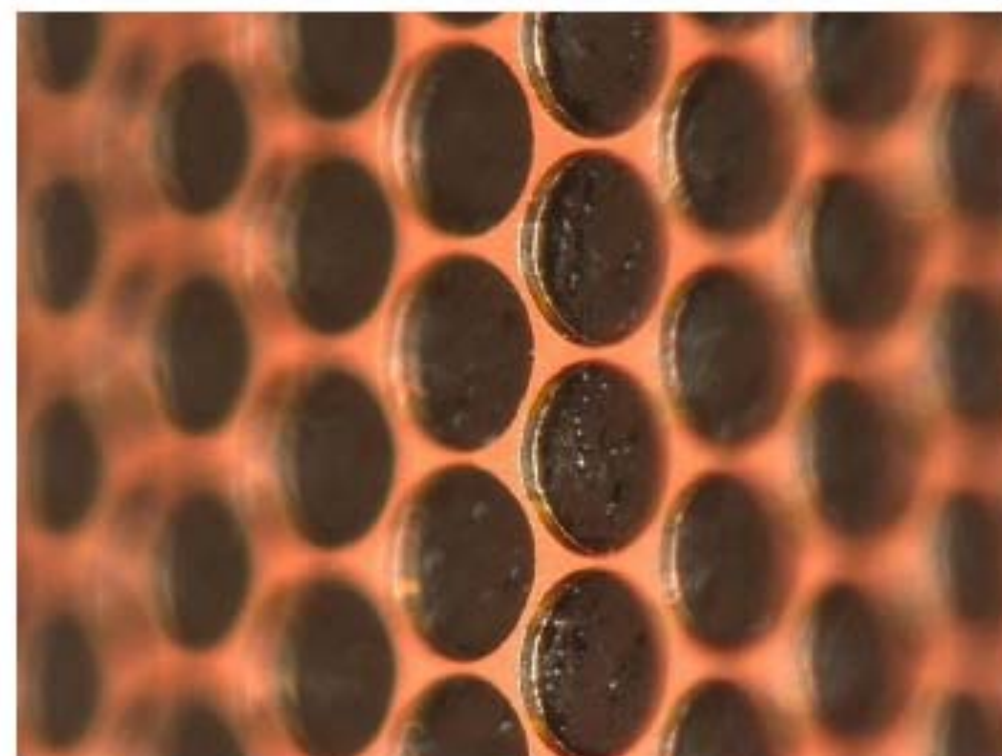


Fig 8. Surface of F-side

- Minimum rim width is 28µm. (Under 35µm)
- The rim didn't break and maintained the fine structure. (Fig.8)
- Copper removed from the polyimide on the F-side rim width 10µm.
  The limiting width of the rim by Laser drilling process is 25µm.
- Optical aperture ratio was 75%. (Under 80%)
- Processing time of 10mm x 10mm was 6min.
  In case of 170mm x 220mm, the processing time is about 2,240min...

Laser drilling process - Problem

2. Laser drilling process

- Circle structure Gating foil couldn't reach optical aperture ratio 80%.
- The Laser machine for FPC products is optimized to circle processing.

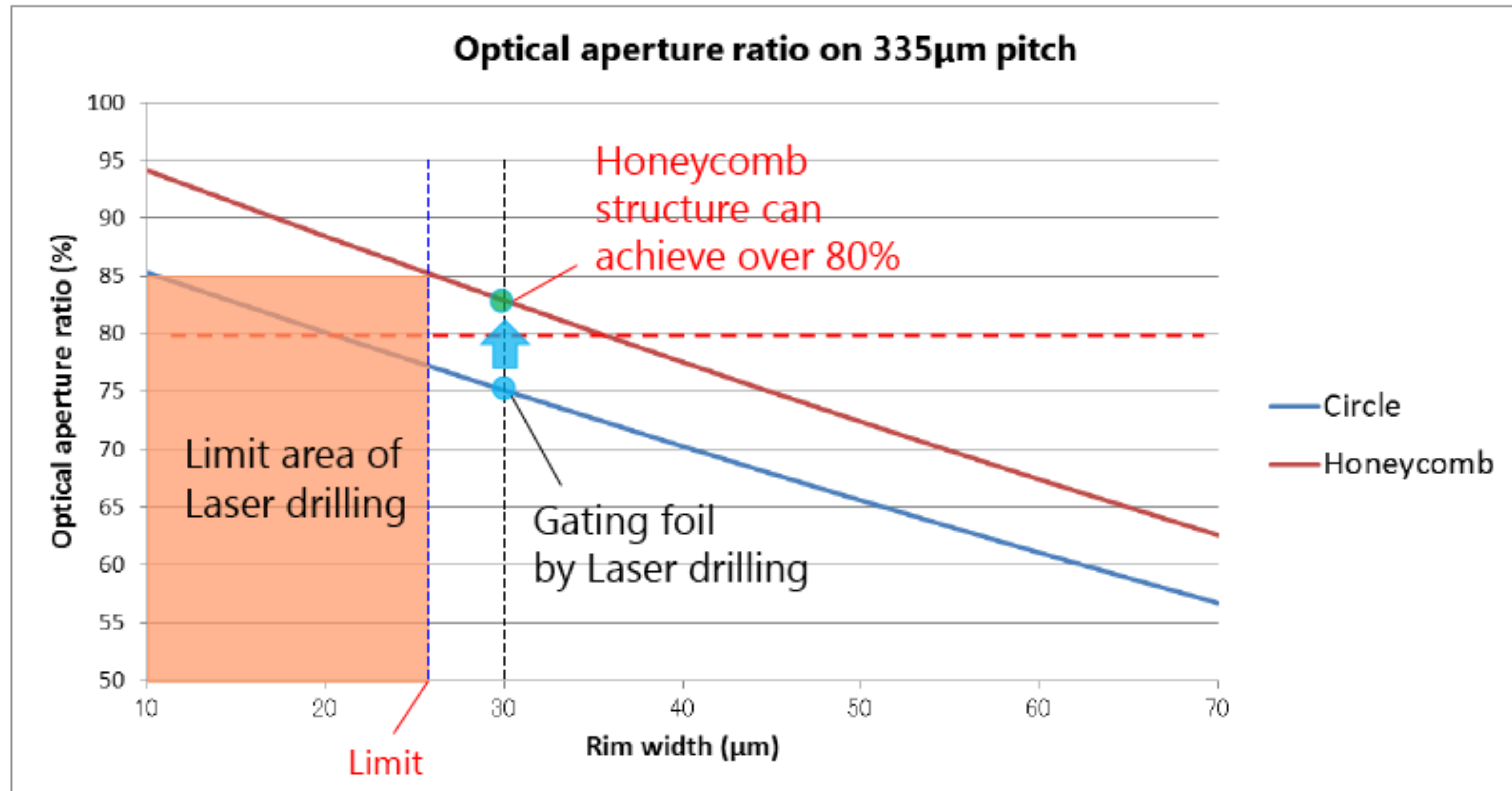


Fig 9. Relationship between Rim size and Optical aperture ratio on 335μm hole pitch

Laser drilling process isn't suitable for the Gating foil processing

Single mask process without Ni-plating : Process

3. Single mask process

- We invented new single mask process which is more simple and don't use Ni-plating.

■ Single mask process without Ni plating

(1) Laminate the photoresist film on CCL

(2) Form Honeycomb structure circuit on the thick copper side

Single mask process without Ni-plating : Results

3. Single mask process

Type3

■ Results

Item	Gating foil
Hole size	304μm
Hole pitch	335μm
Rim width : F-side	27μm
Rim width : B-side	31um
Insulator thickness	12.5μm
size	100mm x 100mm
Processing time	70min (only laser)
Optical aperture ratio	82.3%

Many problems happened...

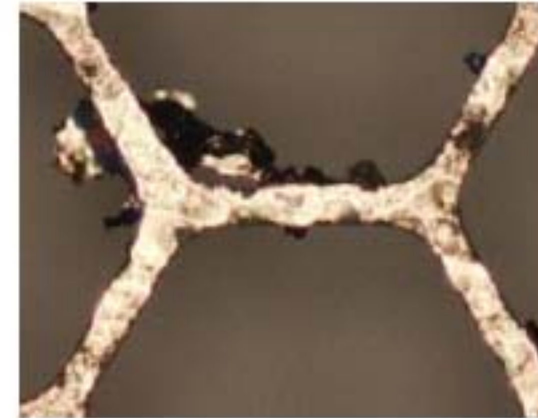


Fig13-1. Problem1
Effect of copper grain size

Fig13-2. Problem2
Effect of contact surface treatment on copper

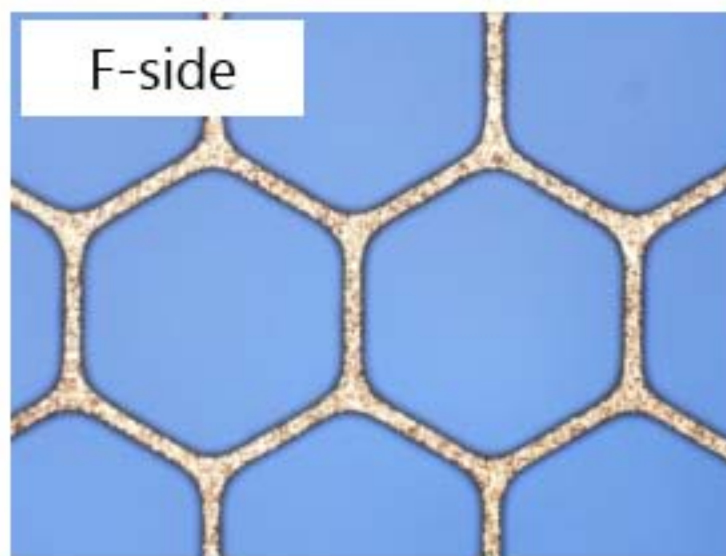


Fig13-3. Surface of F-side

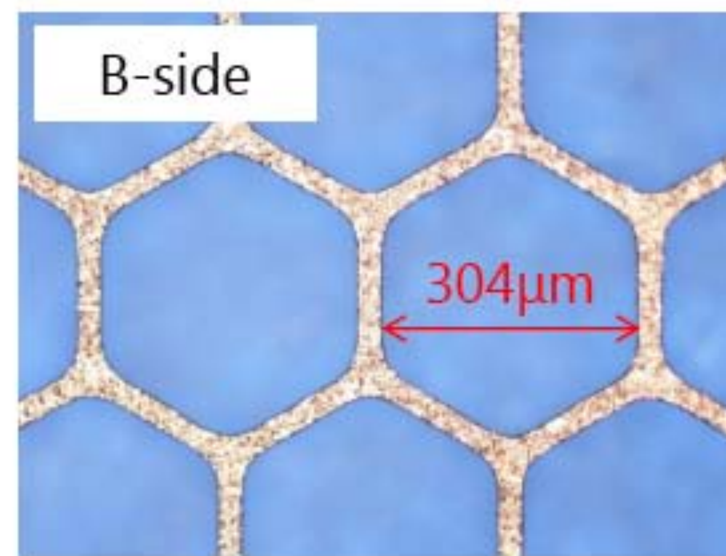


Fig13-4. Surface of F-side

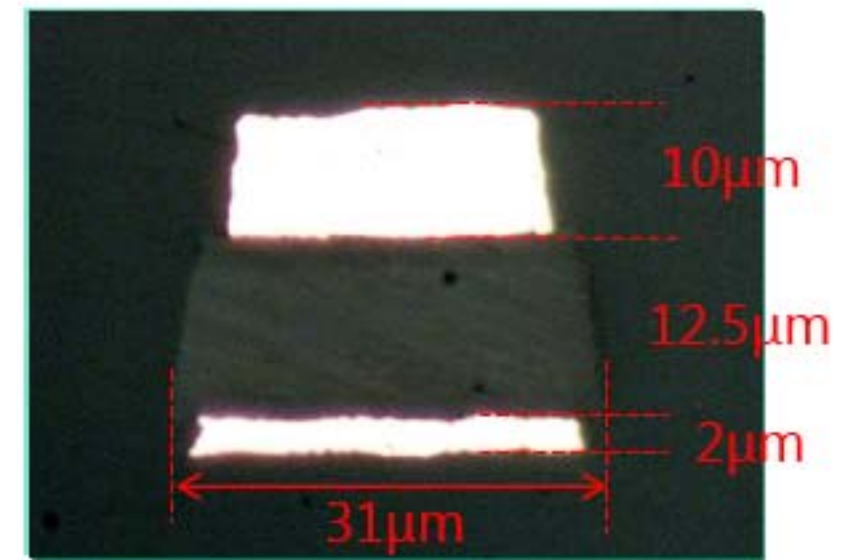


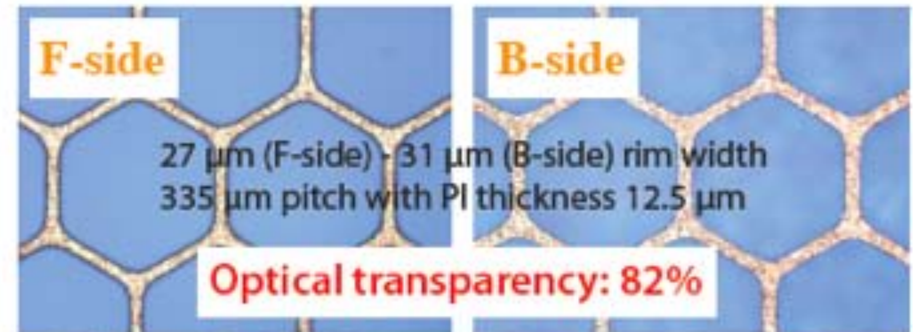
Fig13-5. Cross section of rim

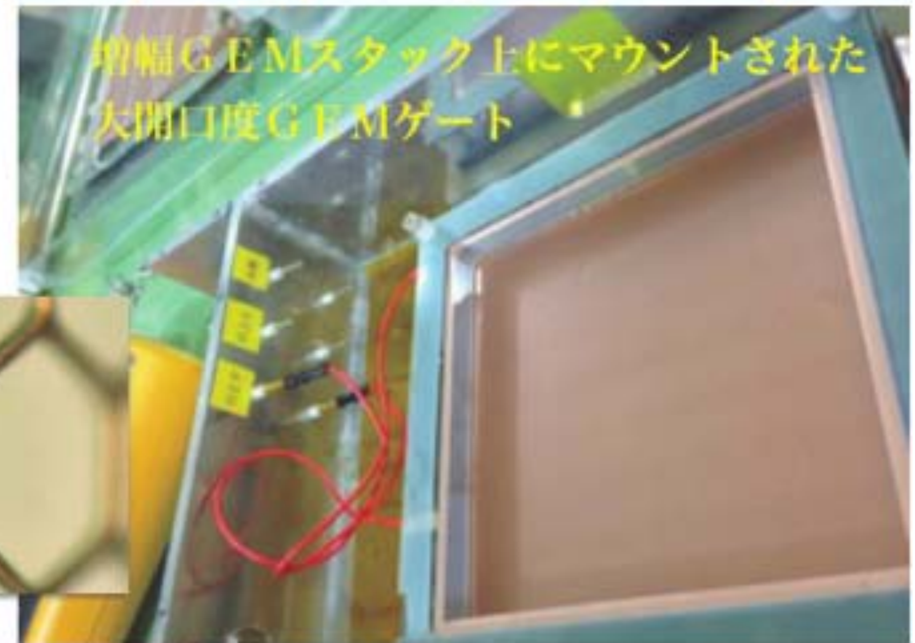
Gate performance

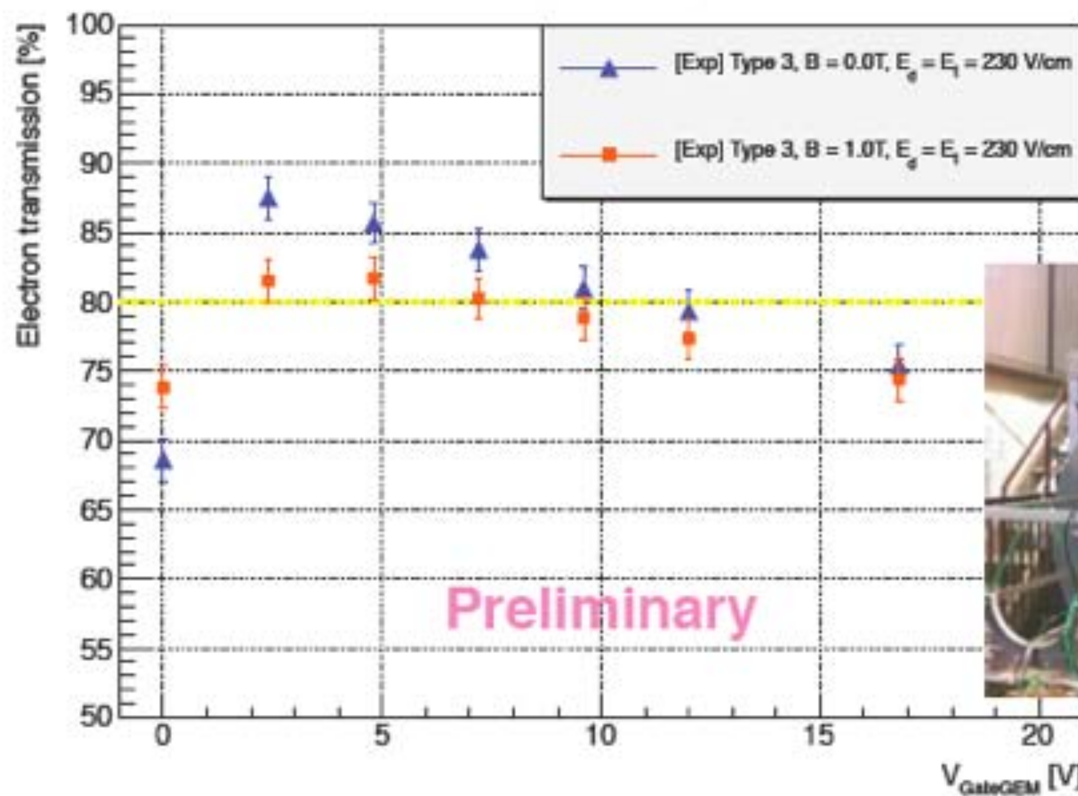
Electron transmission

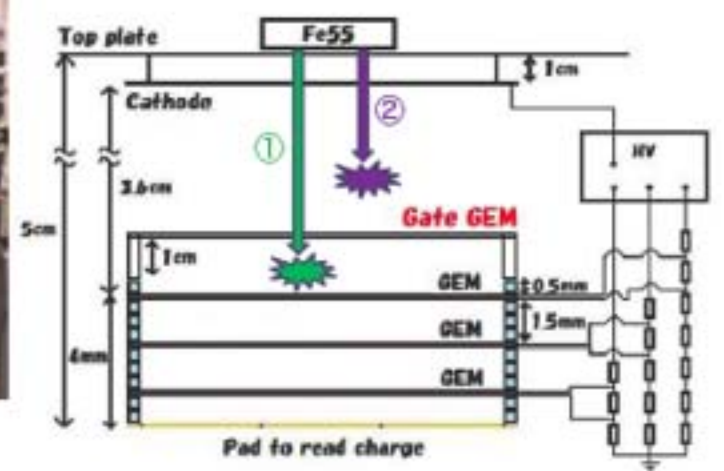
High optical transparency = Minimize rim width of GEM holes (which has hexagonal layout)

Need electron transmission measurements under high magnetic field !
By comparing signal charge passing through the Gate-GEM to signal without Gate-GEM using a small test chamber irradiated with an ^{55}Fe source, which is installed in a 1 T MRI type super-conducting solenoid at KEK cryo center





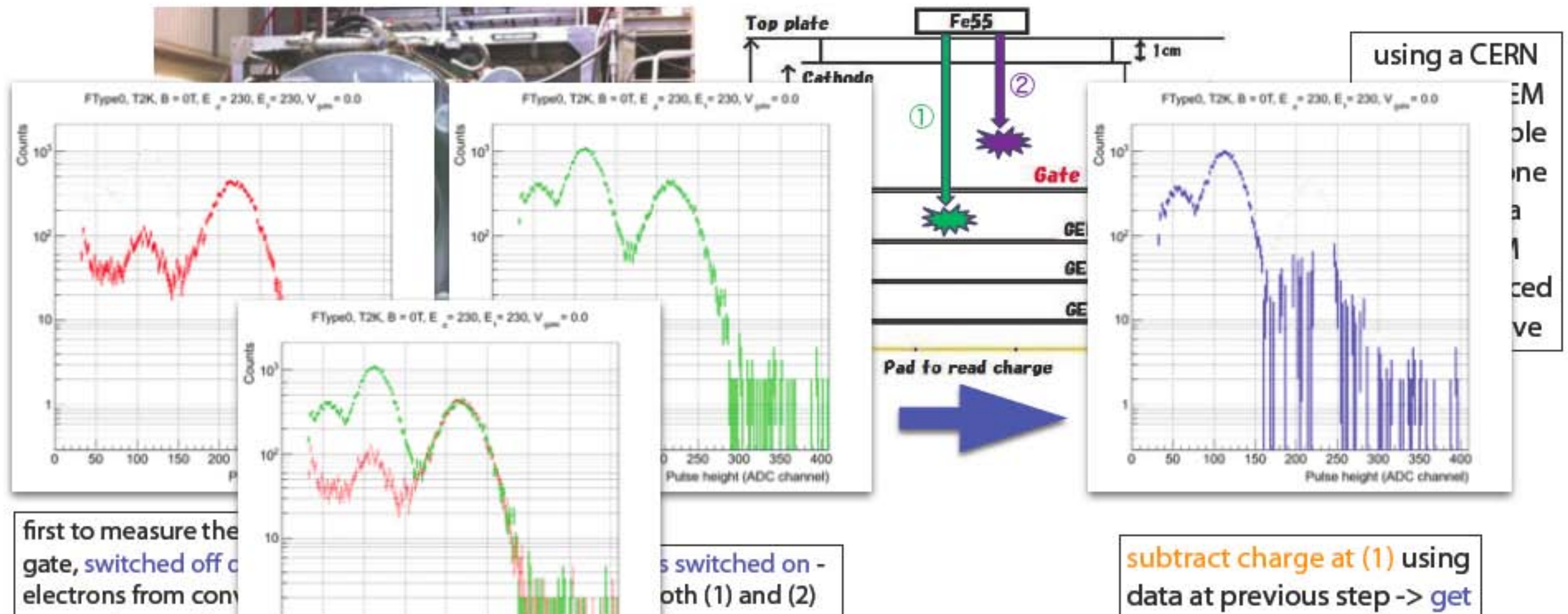




Electron transmission measurement

Motion of electrons is strongly restricted to the direction of the magnetic field => need measurements under high magnetic field!

- **Measurement method**
  - by comparing **signal charge passing through the Gate-GEM** to **signal without Gate-GEM** using a small test chamber irradiated with an ^{55}Fe source, which is installed in a 1 T MRI type super-conducting solenoid at KEK cryo center



Method:

As transmission become good, main peak of drift and trans. region overlap each other. ->
We need to measure 0 drift data(main peak@ trans. only)
but gain stability is no so well

Combined fit w/ physically reasonable constraint
event ratio of main/escape peak : 85~87%
peak position ratio of main/escape peak : ~0.5
width ratio of main/escape :

event rate of drift/trans. region : dip. on geometry
Transmission

We expect more stable result and easier for error estimation

Fitting function

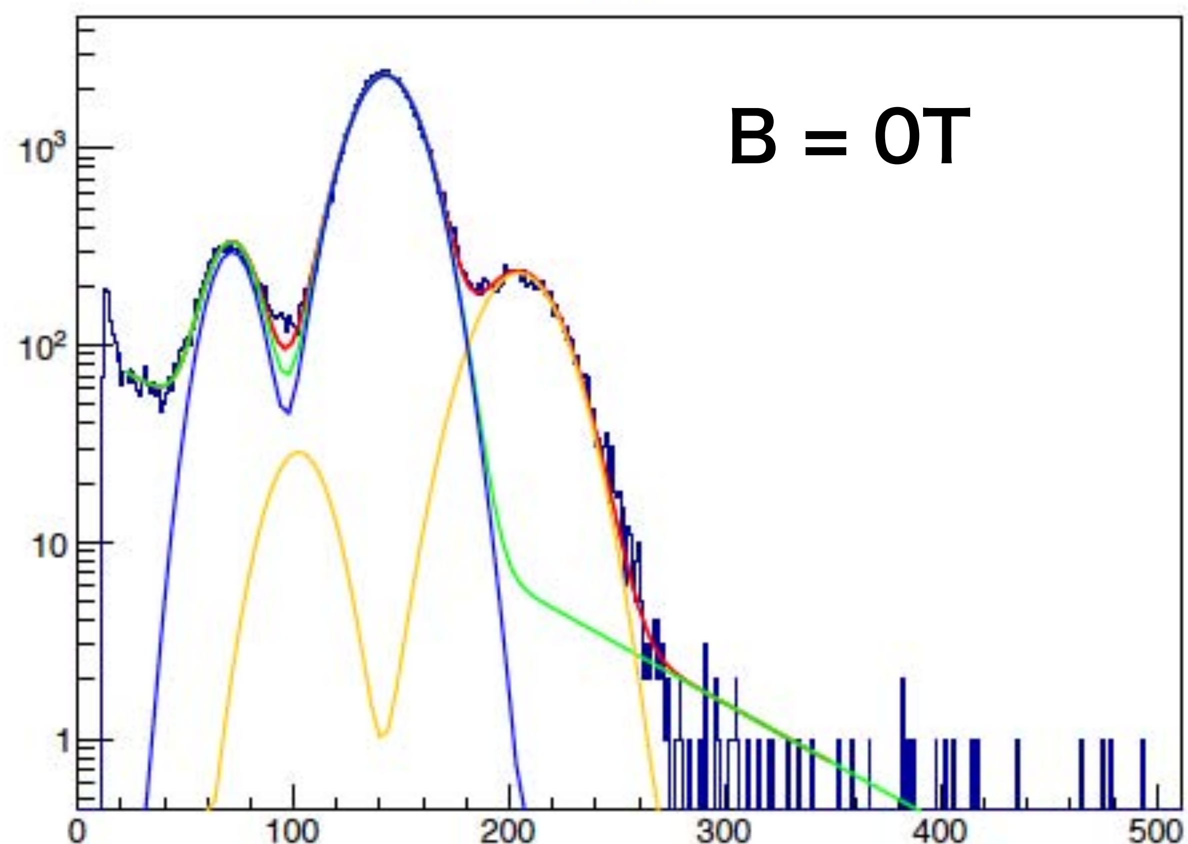
$$p_0 e^{-\frac{(x-p_1)^2}{2p_2^2}} + \frac{p_4 p_0}{p_3} e^{-\frac{(x-p_5 p_1)^2}{2(p_3 p_2)^2}}$$

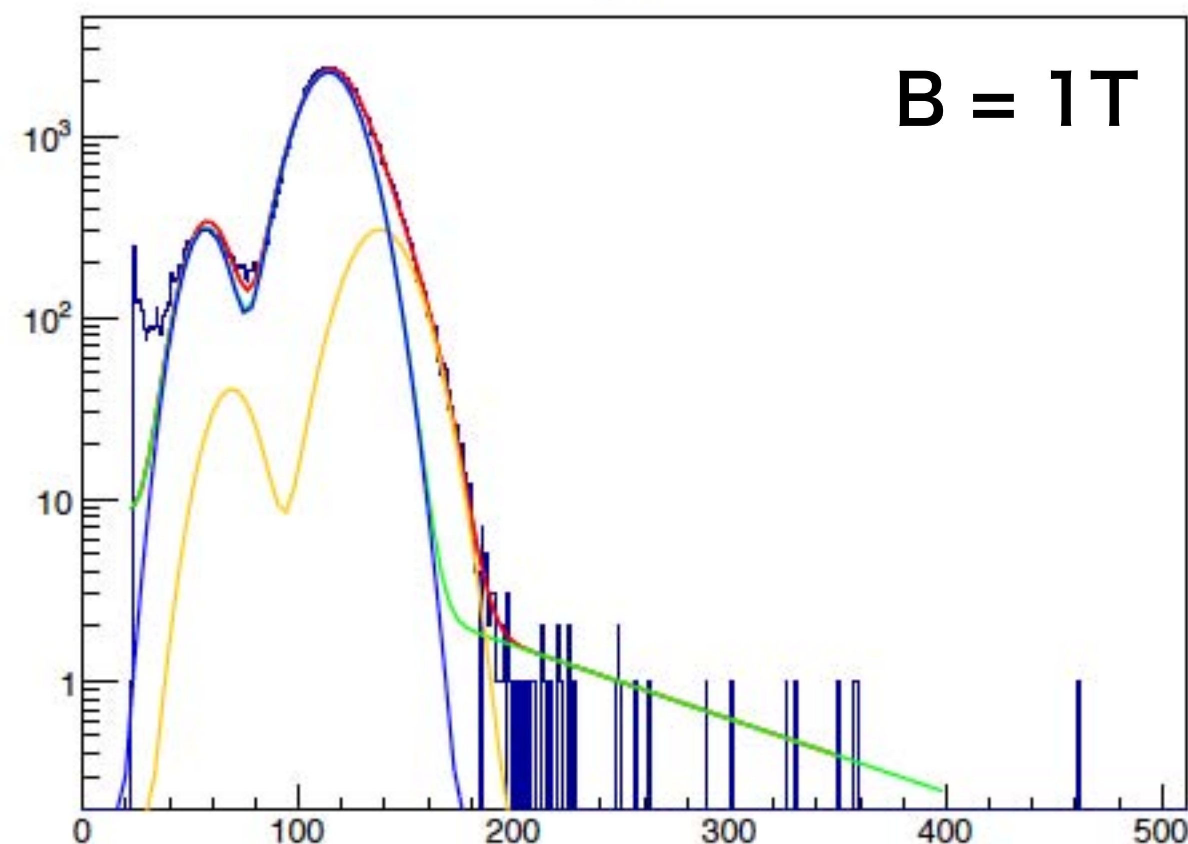
$$+p_6 e^{-\frac{(x-p_7 p_1)^2}{2(\sqrt{p_7} p_2)^2}} + \frac{p_4 p_6}{p_8} e^{-\frac{(x-p_5 p_7 p_1)^2}{2(\sqrt{p_7} p_2 p_8)^2}}$$

$$+p_9 e^{-p_{10} x} + p_{11} e^{-p_{12} x}$$

some param.
can be fixed

Transmission is p7





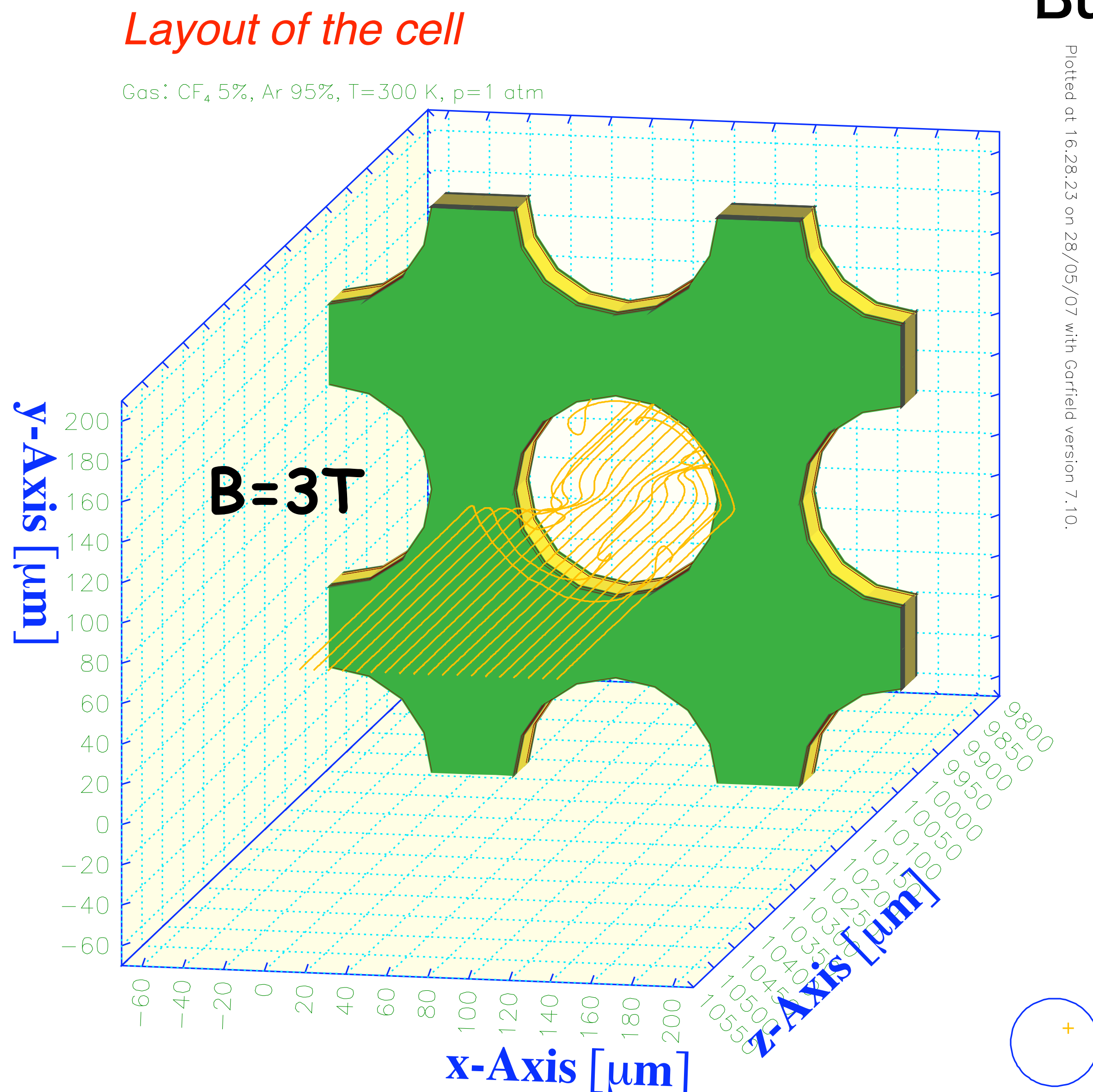
Other transmission measurement

Paul will measure Raytech Gate (10cm x10cm)
(design is same as Fujikura)
using micromegas
schedule in Autumn 2016

Time pix must be a Ideal equipment to measure transmission
just counting # of electrons
no plan ?

Effect to position information

When electron goes into hole, electron rotate around hole
due to Lorentz force.
But electron rotate back at exit.
So displacement of electron may cancel out if geom./E field is ideal and symmetric.



But actual gate hole is not straight shape

no symmetry at entry/exit

Simulation study is on-going

modeling of ANSYS
implement realistic geom.
garfield

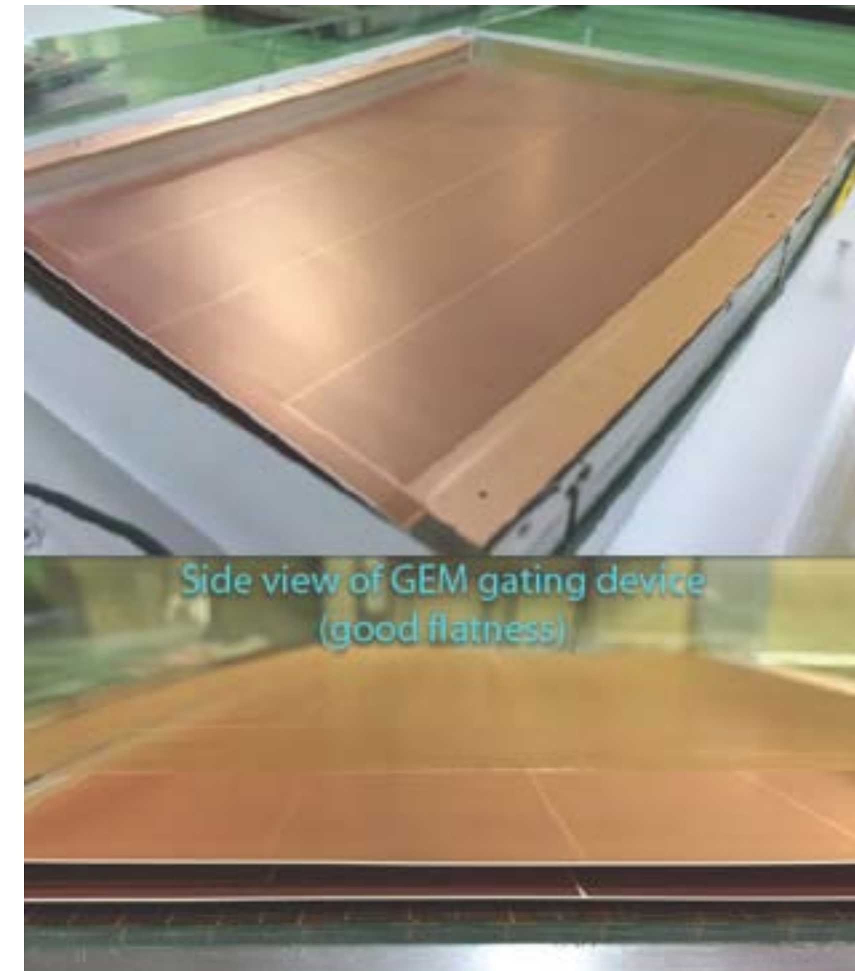
Performance check at Beamtest

Position Resolution is expected to be worth
due to Electron loss at Gate
is there any extra degradation ?

test @ 1T is enough ?
can we extrapolate to 3.5T ?
we may need another test at high B field

Asian module beamtest is scheduled at Nov.2016@DESY
We will ask DESY/LUND to help our study and
French group will also join

Gate on Asian module

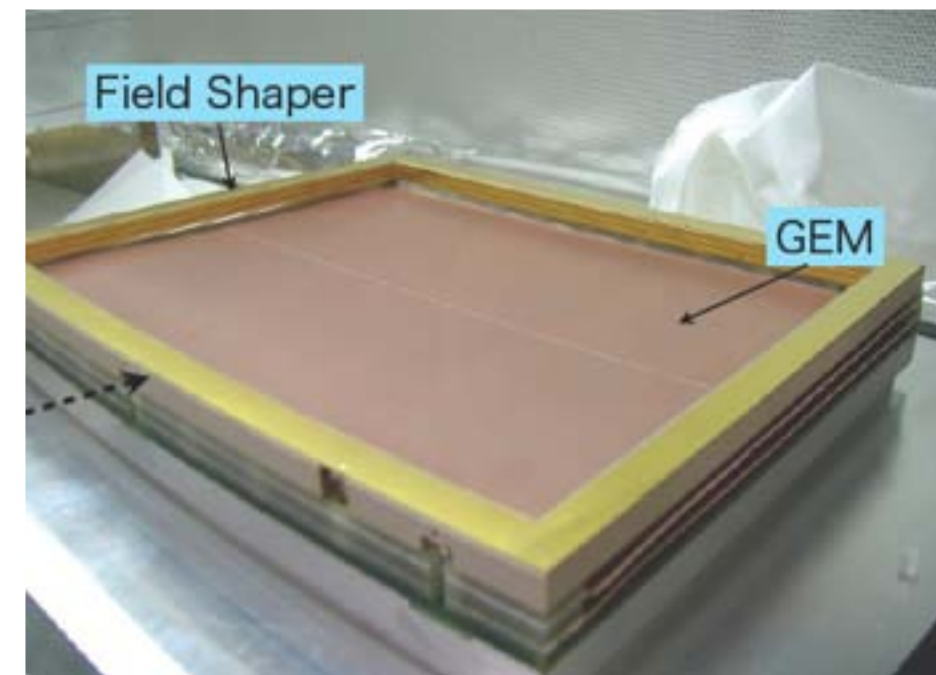


We are planning to bring two type of Gate

1. original structure - side frame less
   stretched by post
   size is also original (very aggressive)
   500um higher than Dummy endplate

2. Gate on field shaper (though FS doesn't work as it is)
   size is compromised 1mm smaller in width/height

   stretch on rigid frame : new trial
   Gate production will start soon



Each module may demonstrate with Gate ?

How to mount Gate on your module
- for micromegas module
- for DESY module

Gate for Asian module is usable ?
or make new one?

how to route HV through your module
module redesign ?

minimize duplicate study and cooperate productively

Do not forget to change backframe to the proper one.

Micromegas module:

consider possibility to use existing Fujikura Gate for the test
either old style or FS type

if it is impossible, they may make new one

mounting structure is not known yet

DESY module:

mounting method is just extension of GEM mount

New Gate design & redesign of module is necessary

TimePix module :

Probably there must be enough space for Gate on the module

Ion feedback

- Ion blocking power must be verified experimentally
  - precision must be 10^-4

- Someone should try someday

Summary

Module sized Gate will be tested on the module this Nov.
Study of detail behavior is going.

Gate for other module

IFB measurement   who will initiate?

test@high B field ?

Wire gate : exist but do we need test ?