ROPPERI

Readout Of a Pad Plane with ElectRonics designed for pIxels

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A common project of DESY and Uni Bonn (Jochen Kaminski)
LCWS Santander
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Idea

- For a GEM-based TPC readout: Match readout pitch with dimension of primary ionisation clusters
- Allow for:
  - Improved particle identification by dE/dx
  - Improved double hit/track resolution
- Implementation:
  - Use separate pad plane for high flexibility and large area coverage
  - Use pixel chip for high integration → Timepix

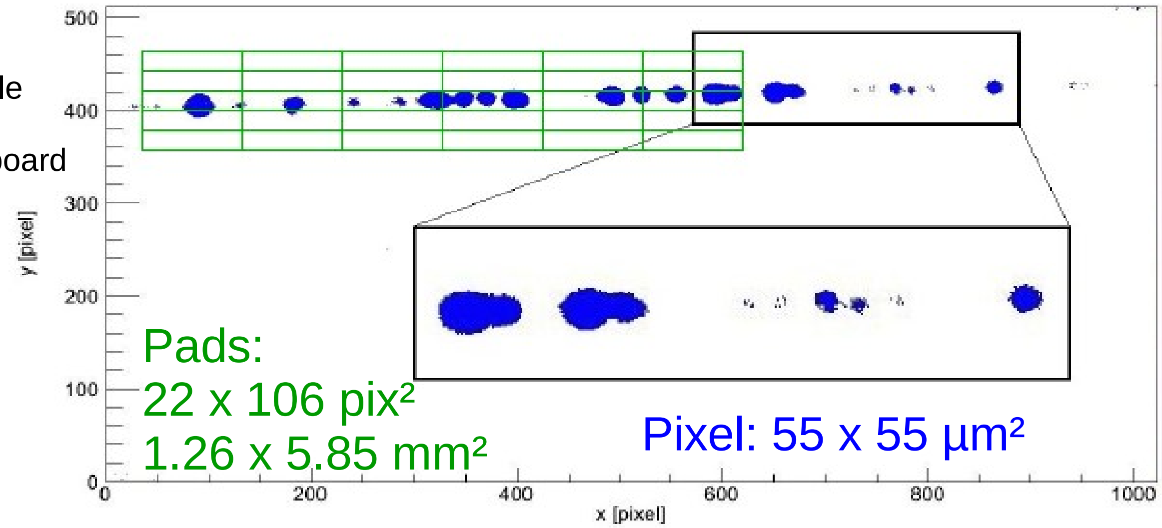
Content

- Idea
  - Cluster counting / particle identification
  - Integration of electronics / Timepix
- Current status
- Challenges, plans

Idea: intermediate solution between pads and pixels

M. Lupberger: The Pixel-TPC:
first results from an 8-InGrid module

Here: GEMs + bare Timepix-Octoboard



- Clusters contain the primary information of the ionisation
- For a GEM-based system: Can we find a solution to resolve clusters?
- What is the optimal pad size to
  - improve double hit and double track resolution,
  - does cluster counting for improved dE/dx?

  → O(200µm)

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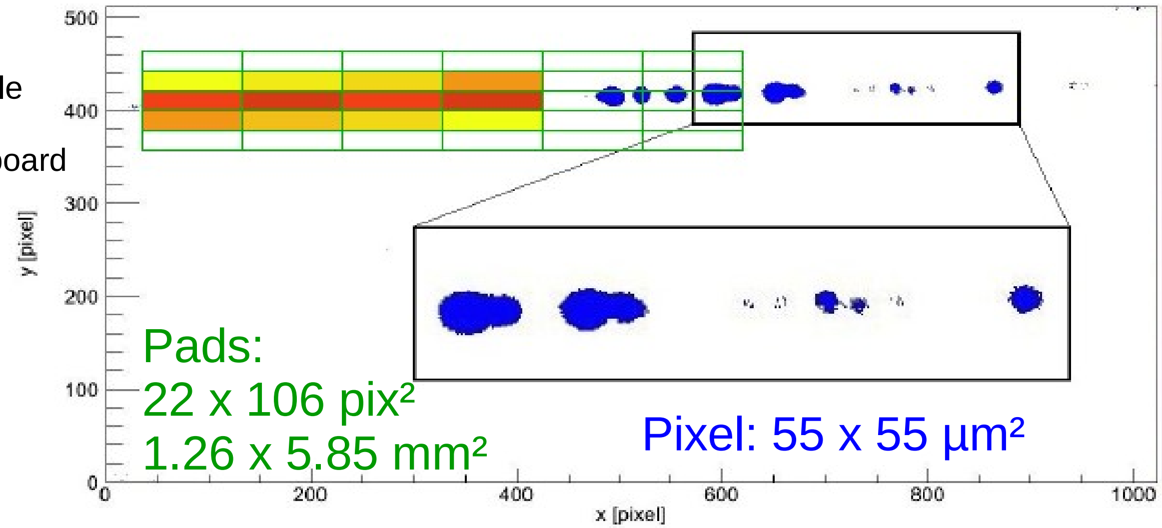

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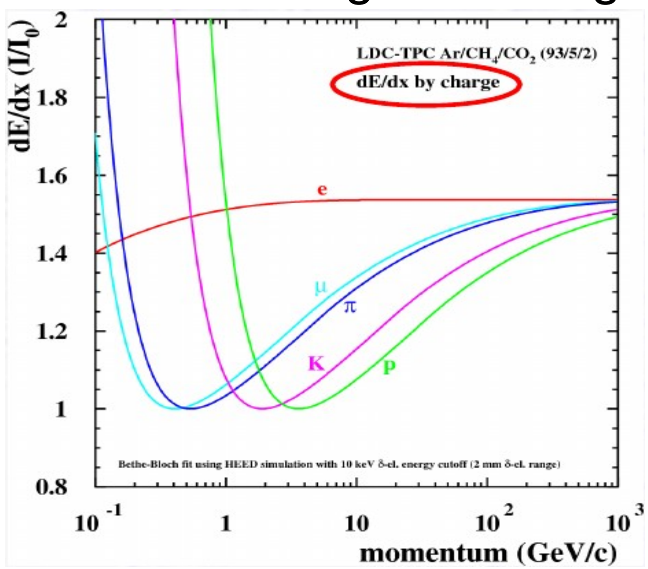
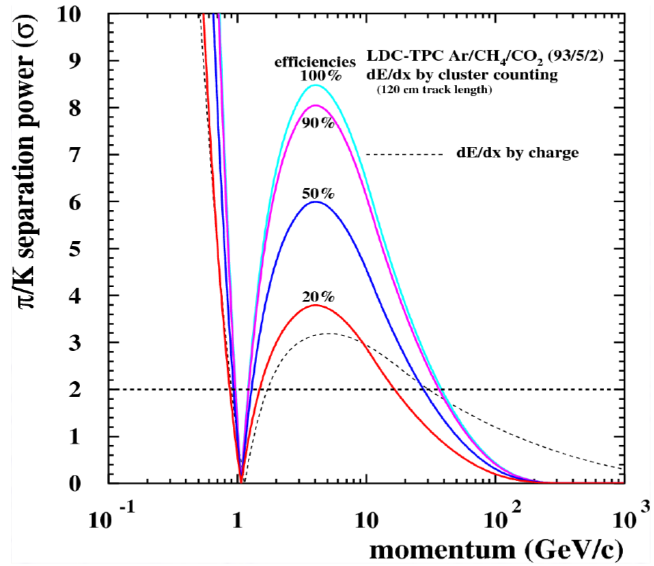
Cluster counting

- Primary ionization leads to Gaussian shaped clusters / distance distribution depending on dE/dx
- Due to large fluctuations like δ-electrons the charge / distance distribution is Landau shaped → larger RMS → worse correlation with energy loss
- Counting clusters allows for improved particle separation compared to conventional charge counting





M. Hauschild: dE/dx and Particle ID Performance with Cluster Counting; at ILC Ws. Valencia 2006

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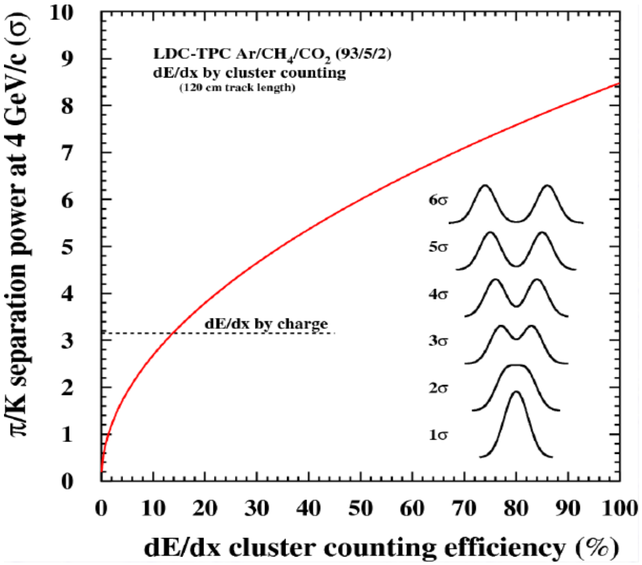

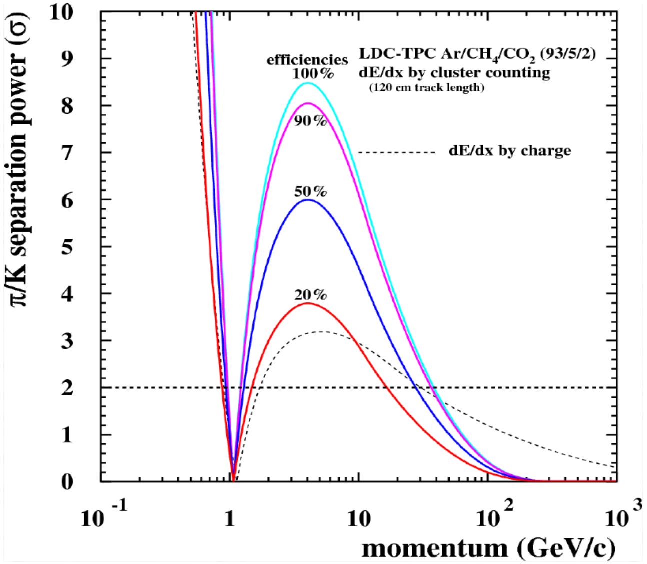

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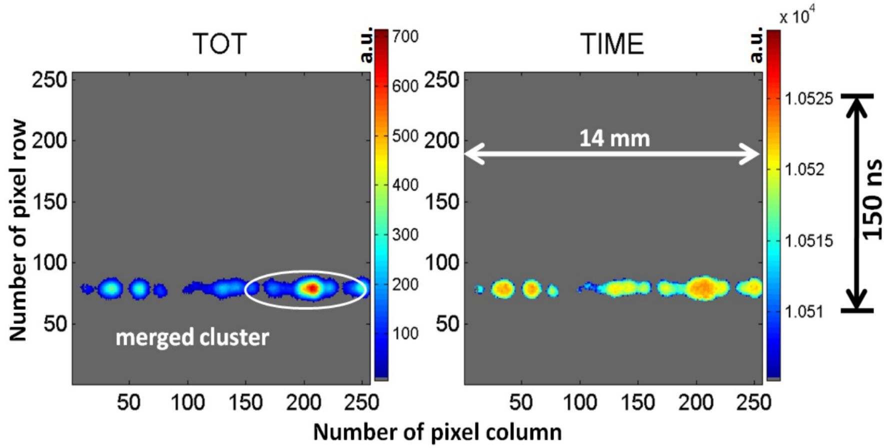
Cluster counting efficiency: ~25-30%



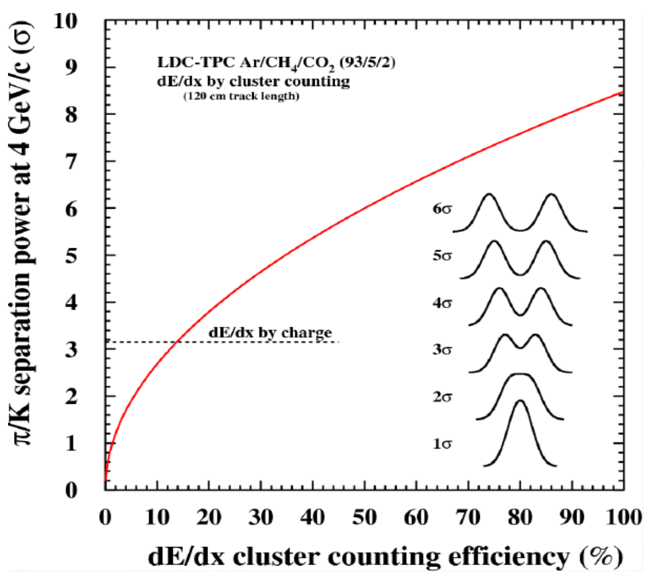
U. Renz: A TPC with Triple-GEM Gas Amplification and TimePix Readout

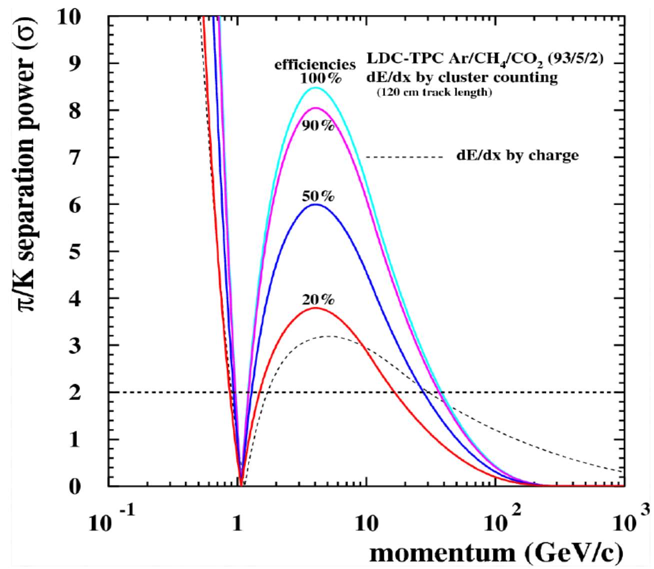
Example: Ar:CO_2 70:30

11 clusters /cm observed

40 clusters /cm expected

Efficiency may be increased with improved clustering algorithms





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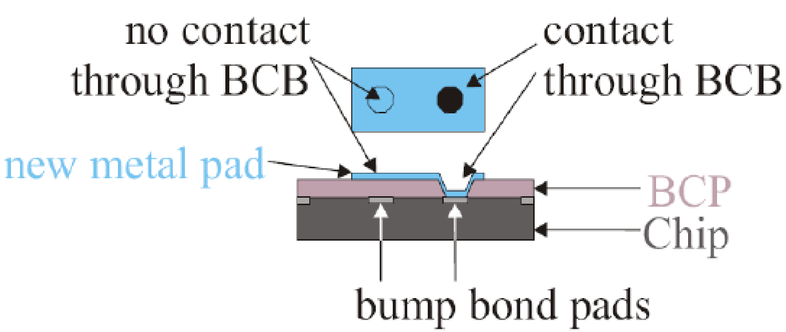
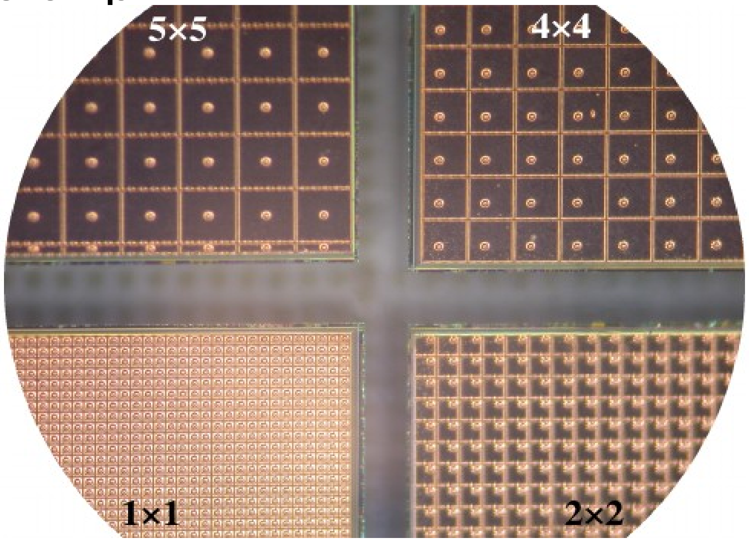
Former Tests with GEMs + pixels

- GEMs + Timepix, by Uni Bonn and Uni Freiburg
  - Charge depositions spread continuously over O(100) pixels (compared to Micromegas)
  - High gains (60k to 100k) necessary for signal/noise
- Large pixels by adding metal pads to chip

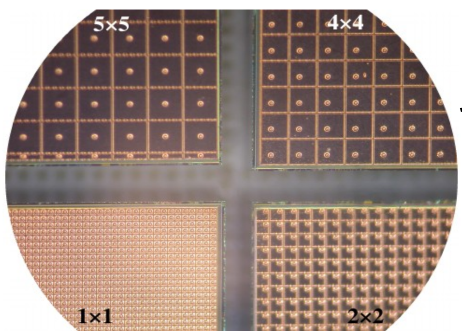


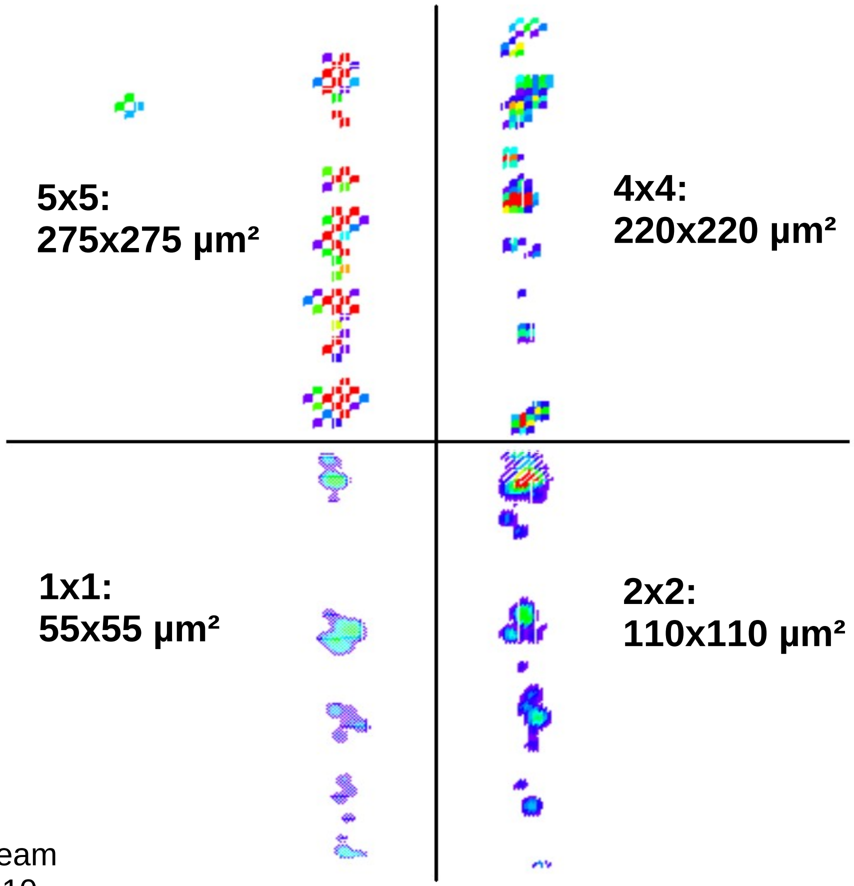


J. Kaminski: Measurements during the October test beam with the GEM-TPC and Timepix; at RD-51 meeting 2010

Former Tests with GEMs + pixels

- Clusters visible with large pixels → How large can one go?
- Similar to our approach
- But: still need up to 120+ chips per module
- Utilize full chip!
- Utilize full anode area!





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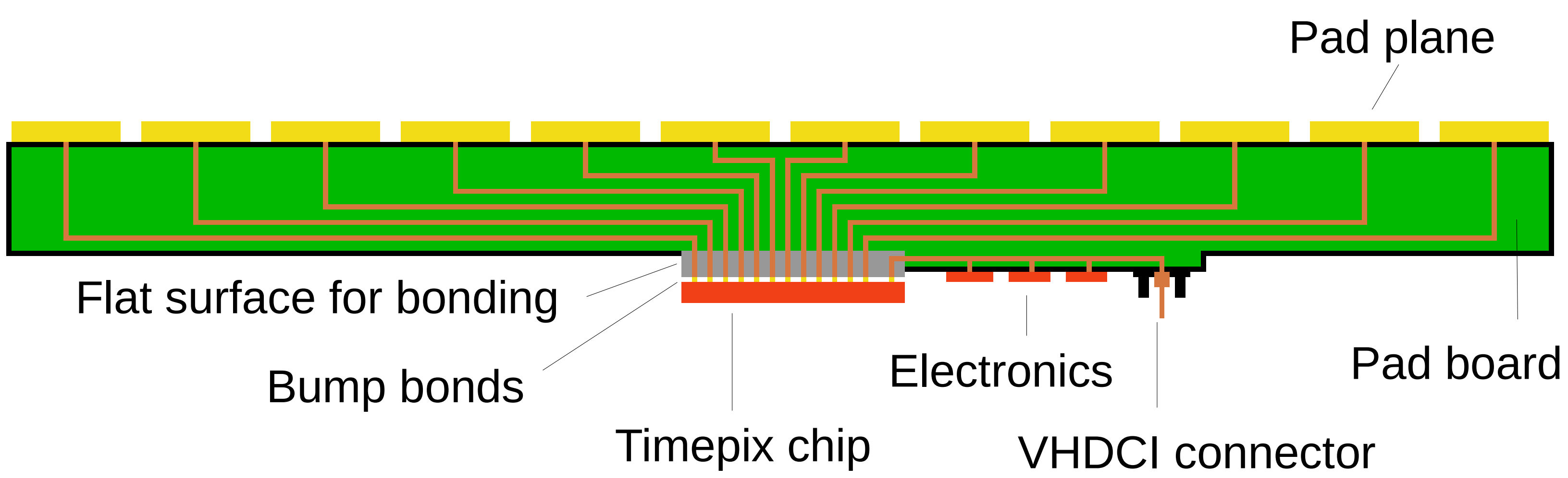
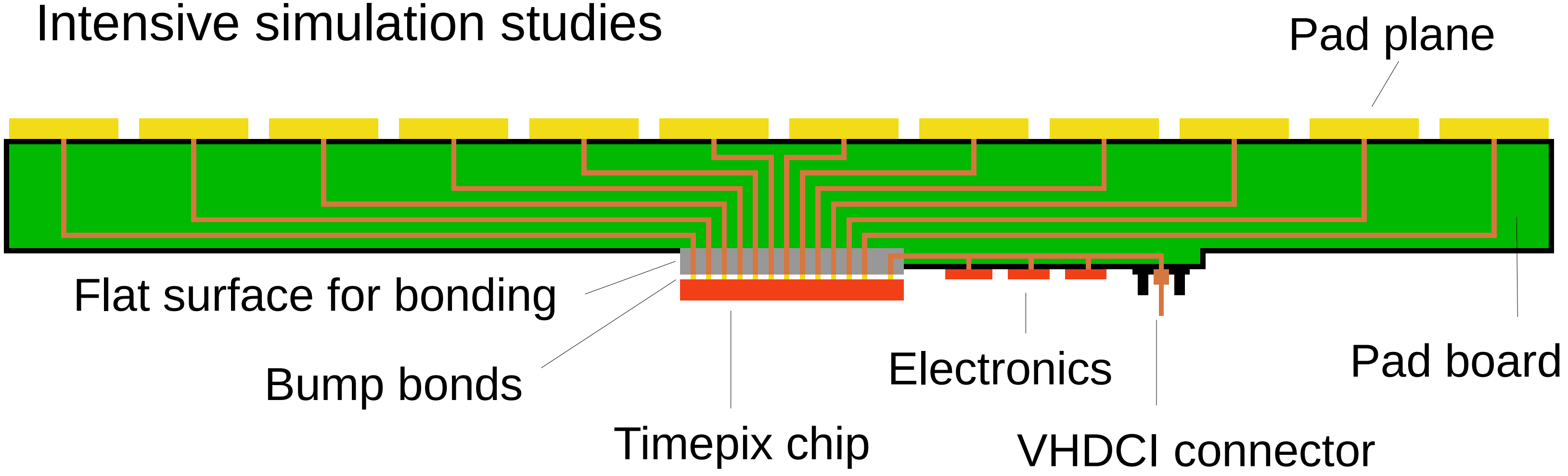
Ansatz

- GEMs, small pads, Timepix chip as readout electronics
- Connections from pads to chip are routed through the board, then bump bonded to the chip
- High level of integration
- Allow for “arbitrary” pad sizes → high flexibility



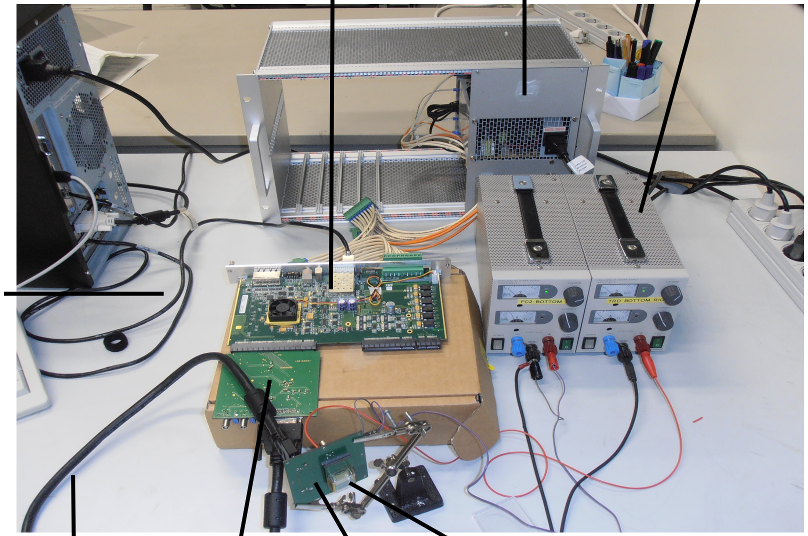
Tasks & Challenges

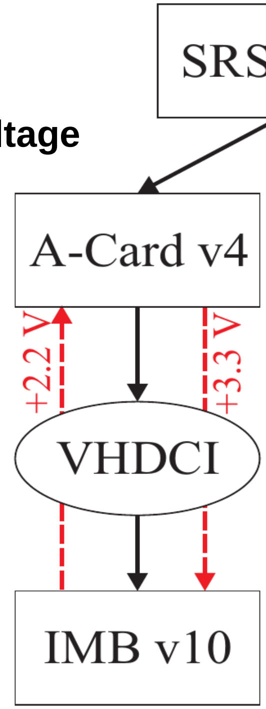
- Setting up and testing the readout chain
- Design and production of the board → routing from pads to bump bonds is complex already for 1000 channels
- Bump bonds from PCB to chip → pitch of 55µm
- Overall input capacitance should stay small
- Intensive simulation studies

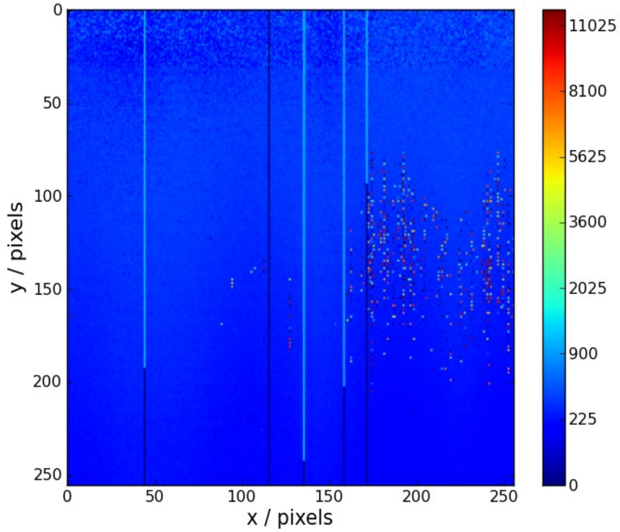


Status: Hardware

- Timepix chip + readout chain acquired from Uni Bonn and set up
- Based on the Scalable Readout System (SRS) from CERN







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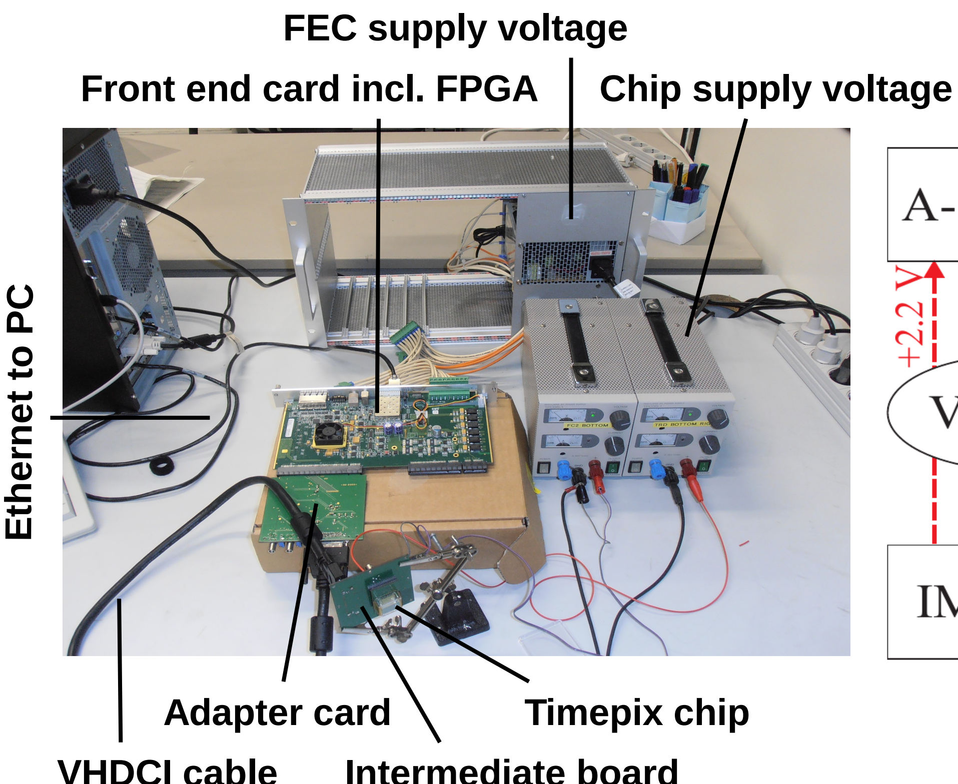
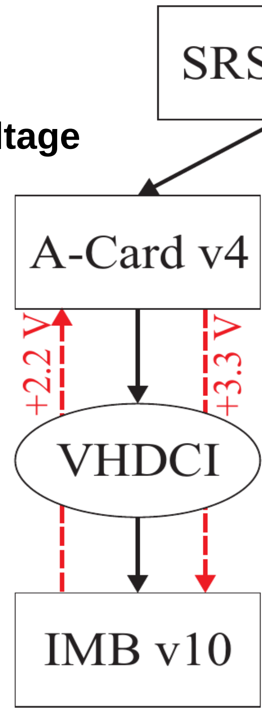
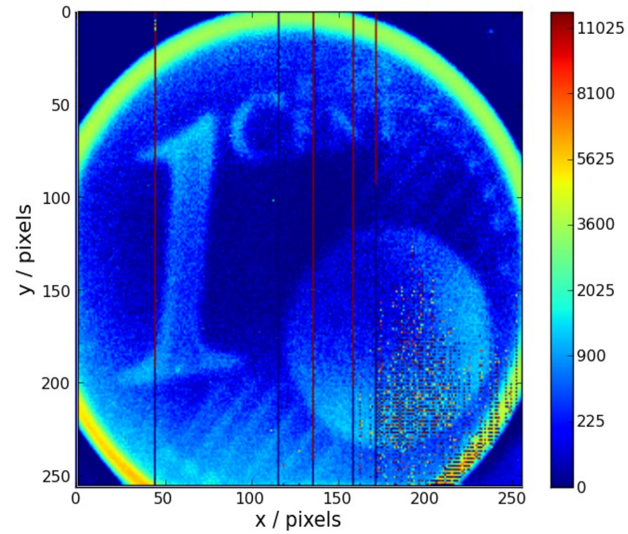


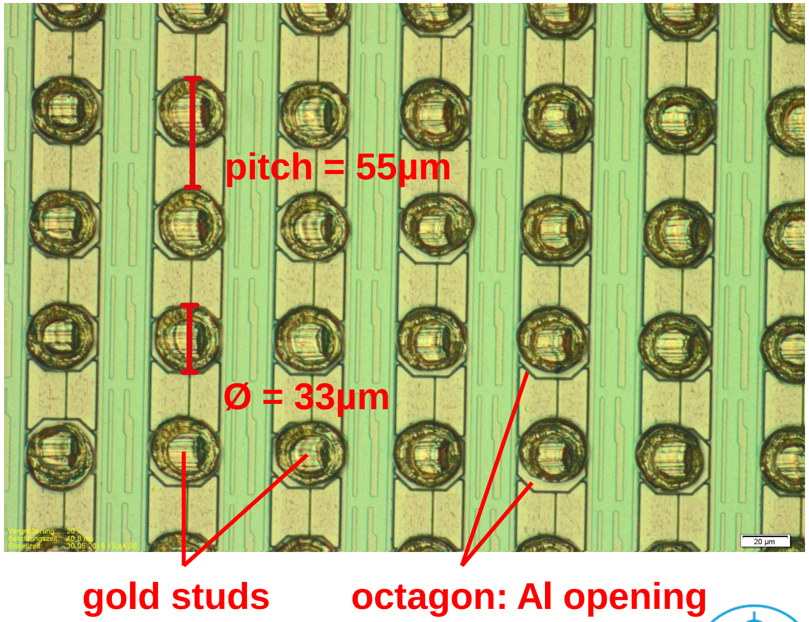




Board design and production

- Design by Jochen Kaminski (experienced from GridPix and GridGEM)
- Production and equipping by DESY
- Boundary conditions set, design will soon begin

- Bonding is done at the KIT bonding lab via gold stud bonding
- 8 chips have been sent to test the bonding technique
- Capillary and gold wire were exchanged from 20µm to 15µm
- First chip successfully bonded:

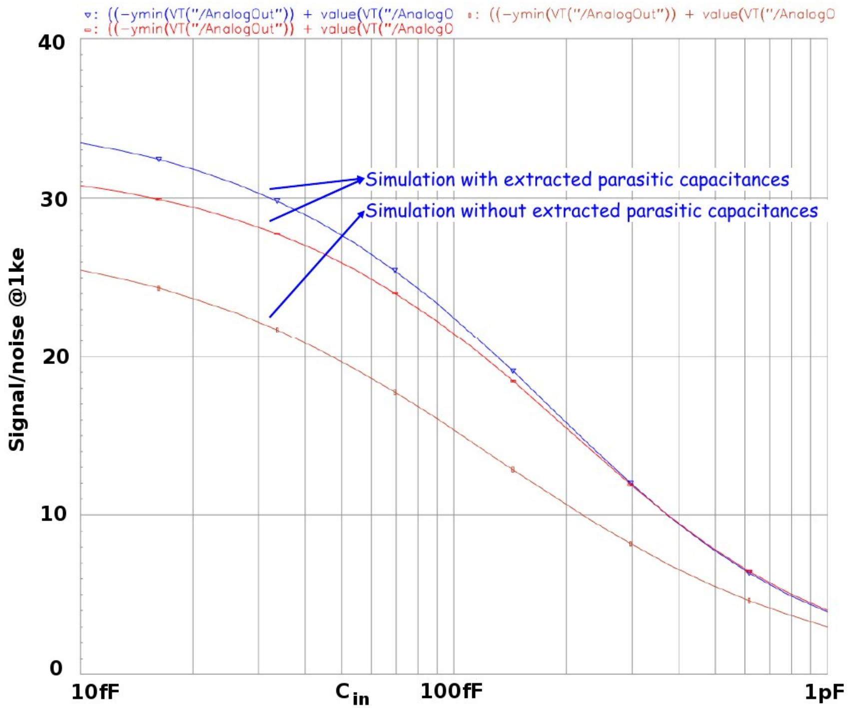


Routing

- FR-4-PCB are only usable for a 2D-pitch > 300µm
- The first test board will utilize every 8th pixel in x and y
→ 440µm pitch, 1024 channels
- Still a complicated routing
- Ceramic boards allow for smaller lines O(10µm) and vias O(100µm), but are more expensive and still not small enough
- An intermediate layer or an interposer might help
→ Silicon wafer → Different chip with larger pitch?
- Line lengths increase the capacitance and the noise

Capacitance

- With growing input capacitance the signal to noise ratio goes down
- Timepix was developed
  C < O(100fF)
- Capacitances:
  Pads: O(0.1pF)
  Lines: O(1pF/2.5cm)
  BGA connections: O(0.1pF)
- Gain for triple GEM stack: 2k-5k, potential for significant increase

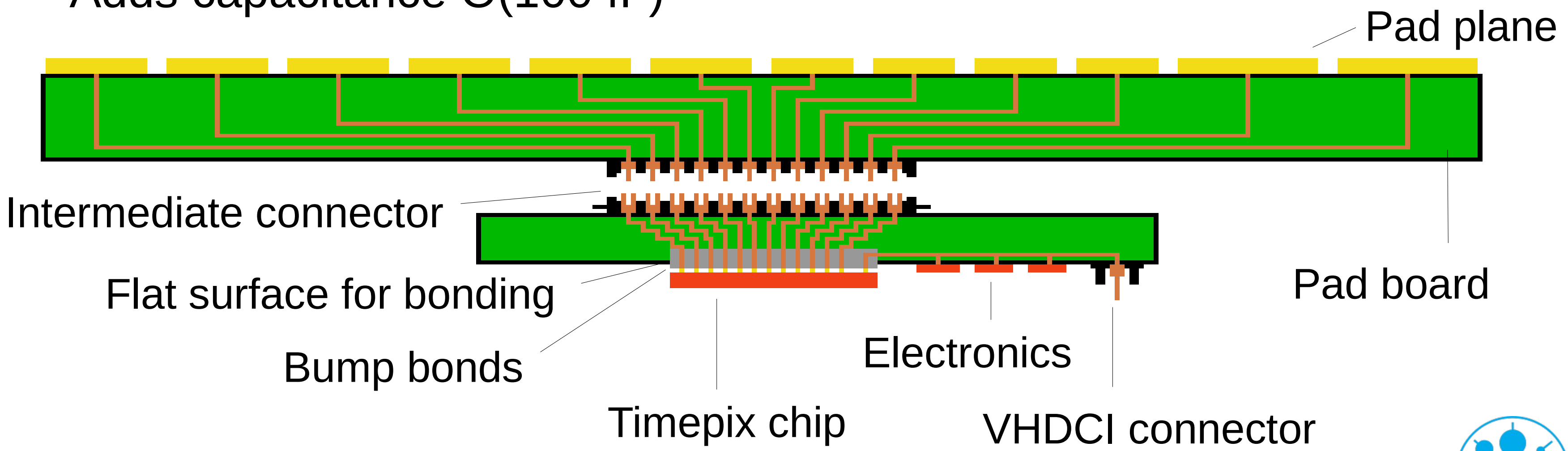


X. Llopart: Timepix Manual v1.0

- Looks feasible, more information required, will be investigated with test board

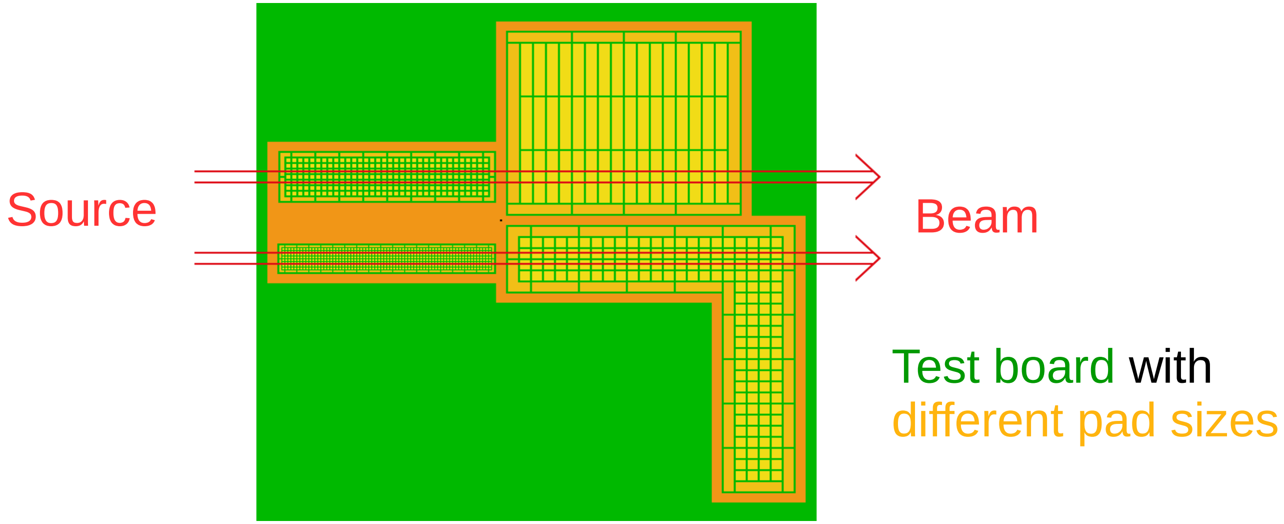
Intermediate layer: connector board

- Separate pad plane and Timepix by adding an intermediate connector from the pad board to a connector board
- Simpler exchange of pad layout or faulty chip
- Plug connector needs too large force to connect and disconnect
  → might damage bump bonds
- Zero force insertion, e.g. CPU socket, currently under investigation
- Adds capacitance O(100 fF)



Plan

- First board for proof-of-principle of bonding and capacitance
- Second board for proof-of-principle of cluster identification
  - Different pad layouts on one board
  - 10x10 cm², small TPC, radioactive source, maybe test beam



Timepix3

- Simultaneous modes “time of arrival” and “time over threshold”
- To be used after proof-of-principle
- Exchange of information and experience with photon science groups at DESY (member of Timepix3 collaboration)

Summary

- The proposal for a GEM-based high granularity TPC readout was presented
- Significant improvement of integration together with possible enhancement of performance
- Challenges are bump bonding, routing and capacitance
- Design will soon begin, simulations are ongoing
- A less granular chip might be considered, e.g. the KPiX chip
- Long-term goal: LP module