External tracking device for the DESY EUDET test facility.

Dimitra Tsionou
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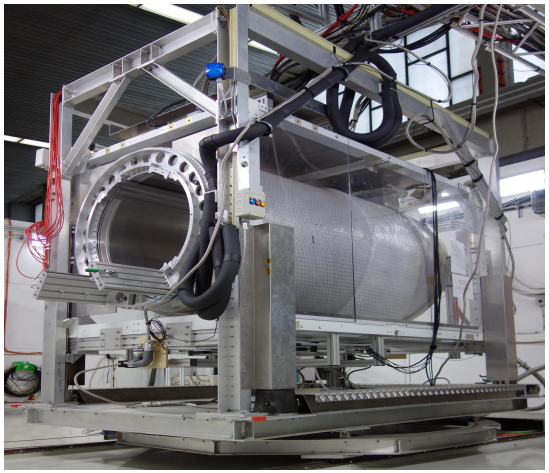
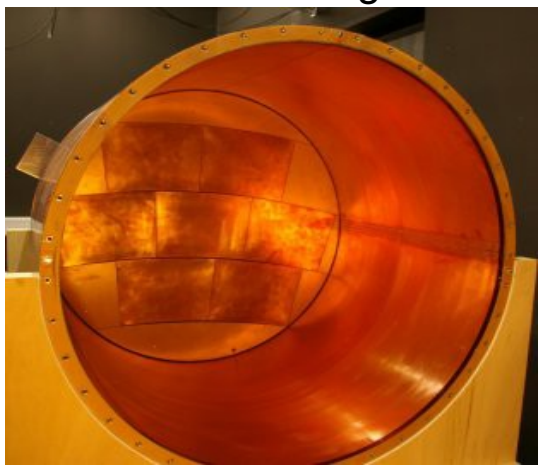
DESY

Large Prototype TPC and Current Infrastructure

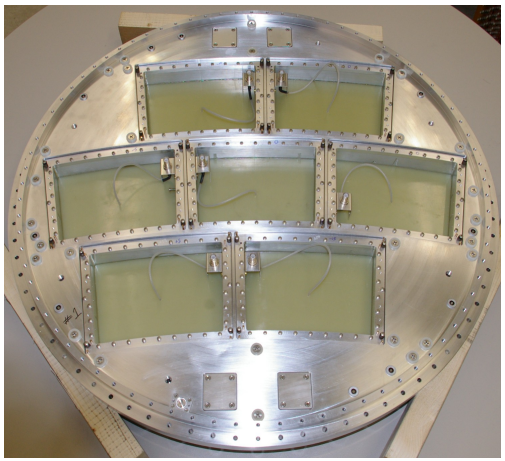
- Test beam area T24/1 at DESY (1-6 GeV e^- beams)
- Large Prototype TPC built and installed
- Infrastructure includes a large bore 1T magnet
  - 20% X_0 material budget



- LP field cage parameters:
  - Length: 61 cm, Diameter: 72 cm
  - Up to 25 kV → E_{drift} up to 350 V/cm
  - Wall material budget: 1.3% X_0

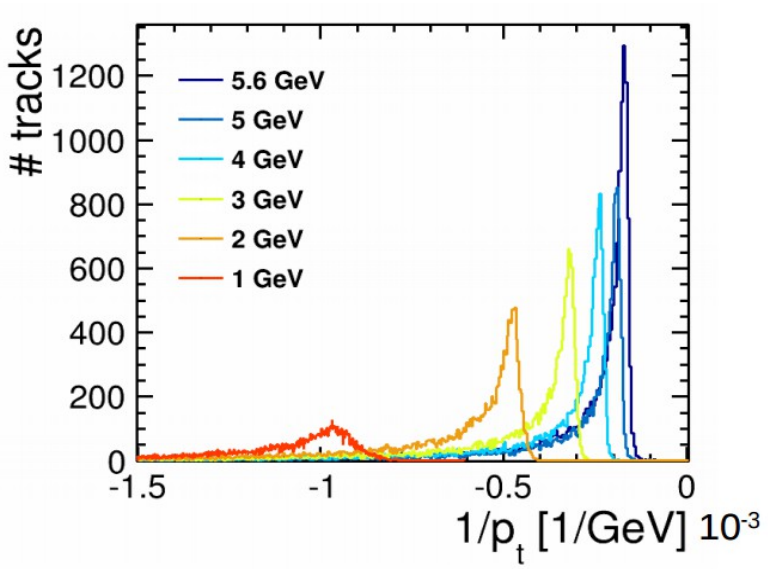


- The endplate is able to host 7 readout modules (dimensions ~22x17 cm^2)



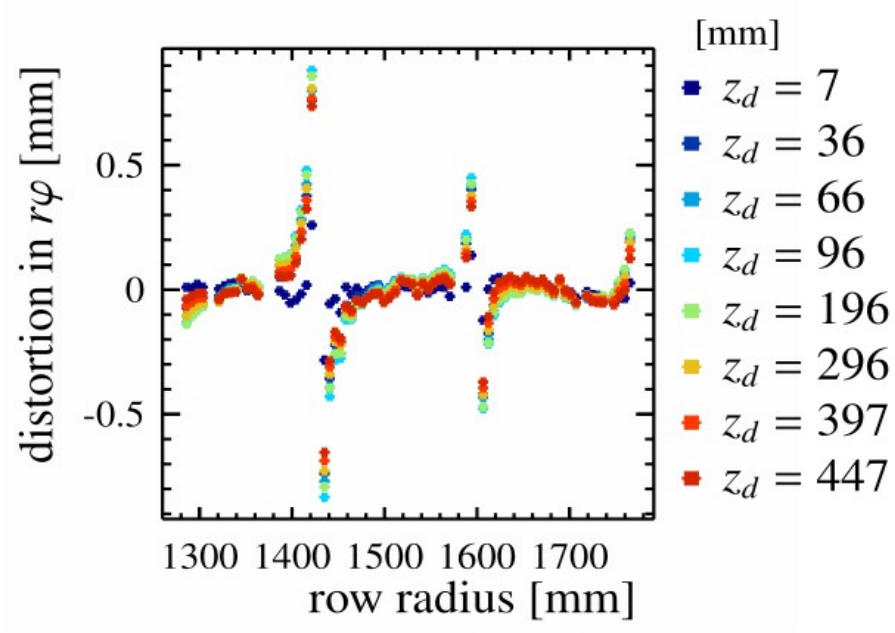
Momentum resolution measurement

- In the Large Prototype TPC case, there is a broad energy spectrum due to the energy loss in the magnet



- In addition, field inhomogenities can cause distortions

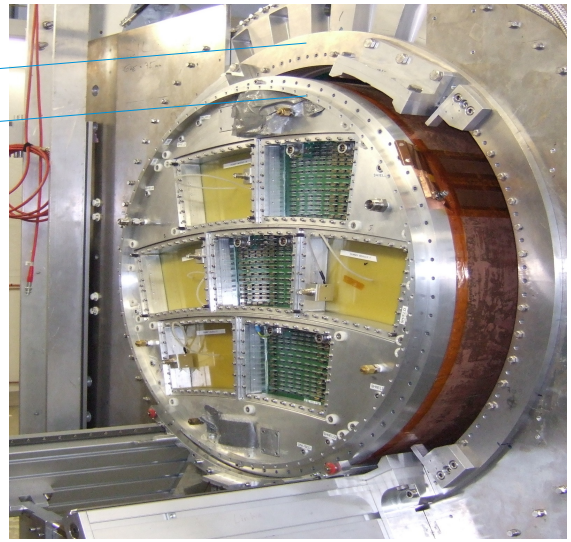
E and B (1 T) fields present



External Si tracker for Large Prototype TPC

- Solution: Build an external Si tracker (Si telescope) to provide reference tracks (entry and exit hits)

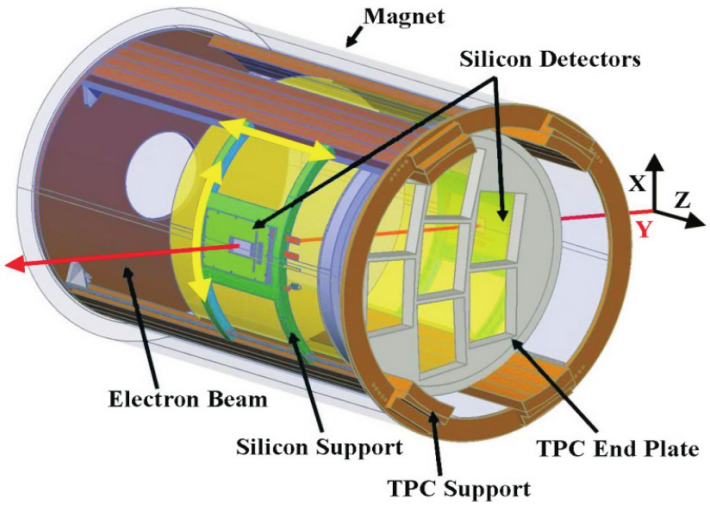
- Prototype for ILD TPC exists at DESY
- Goal: Combined test beam with LPTPC → track reference, field distortion corrections, momentum resolution measurements
- The Silicon tracker should be versatile and simple to be used as a telescope by other groups during test beams



- Challenge: The Silicon system needs to fit in the existing infrastructure (available space is ~3.5 cm)

The Silicon Tracker Project

- Simulation studies to determine the general characteristics of the system
  - Number of Silicon layers
  - Distance between the Si layers
  - Material budget
  - possible dimensions of support structure
  - optimal coverage area



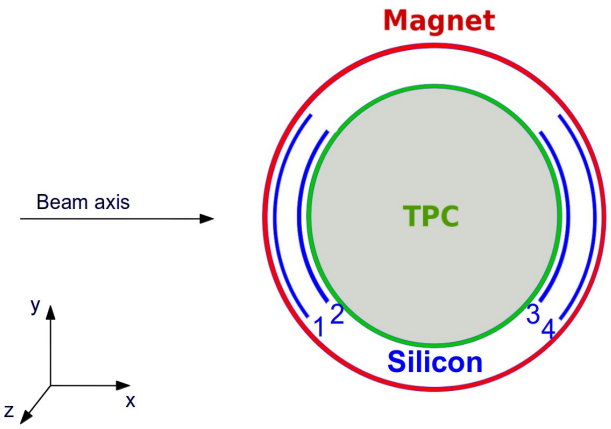
- Hardware options
  - Investigate hardware options to use in terms of sensors (pixels vs strips), chip, DAQ
  - The DAQ system will have to be combined with the current TPC one

- Design support for the Silicon tracker to fit in the current infrastructure

Simulation Studies – Description

- Simulation Studies to determine the general characteristics of the system
- Geant4 simulation to include accurate model of the current material budget of the infrastructure

- Magnet and TPC material budget and dimensions included
- Multiple scattering on
- A number of Silicon sensors placed in between
- Distance between the silicon sensors varied according to limitations (gap of 3.5 cm)



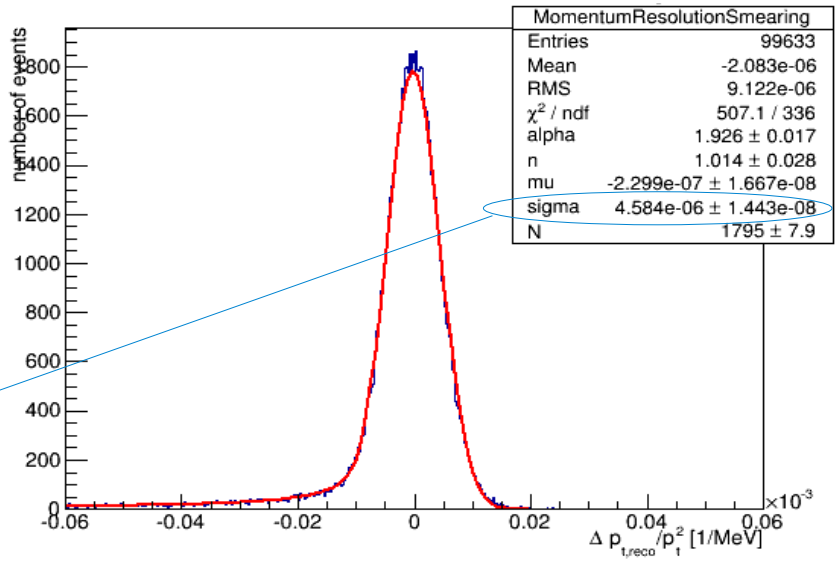
- Thickness of silicon sensors varied (also mimicking material budget of support structure)
- Space points of tracks on Silicon sensors used to fit a helix → Moving to DD4hep simulation to include ILD track finding&fitting algorithms

Simulation Studies – Requirements

- Simulation Studies to determine the general characteristics of the system

- For the Si system to be used as a reference, the Si standalone simulated momentum resolution should be better than the TPC one
  - → Criterion used to define the characteristics of the Si system

- Measuring the momentum resolution in standalone Silicon system and standalone TPC system by fitting a crystal ball function to the simulated points

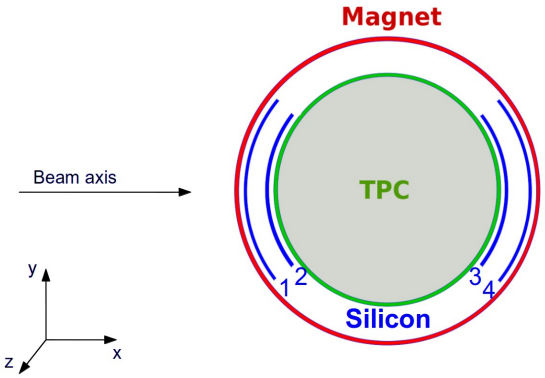


Standalone TPC simulated momentum resolution is $4.58 \cdot 10^{-6}$ MeV^{-1}

Distance between Si layers

- Dependence of sensor spatial resolution on distance between layers
  - Momentum resolution shown in units of 10^{-6} MeV^{-1}

		Distance between inner and outer Si layer			
		4 cm	3 cm	2 cm	1 cm
Sensor spatial resolution	2.5 μm	2.85	2.90	3.00	3.68
	5 μm	3.05	3.21	3.63	5.52
	7.5 μm	3.37	3.65	4.43	7.92
	10 μm	3.68	4.16	5.33	9.90
	15 μm	4.49	5.36	7.53	14.3

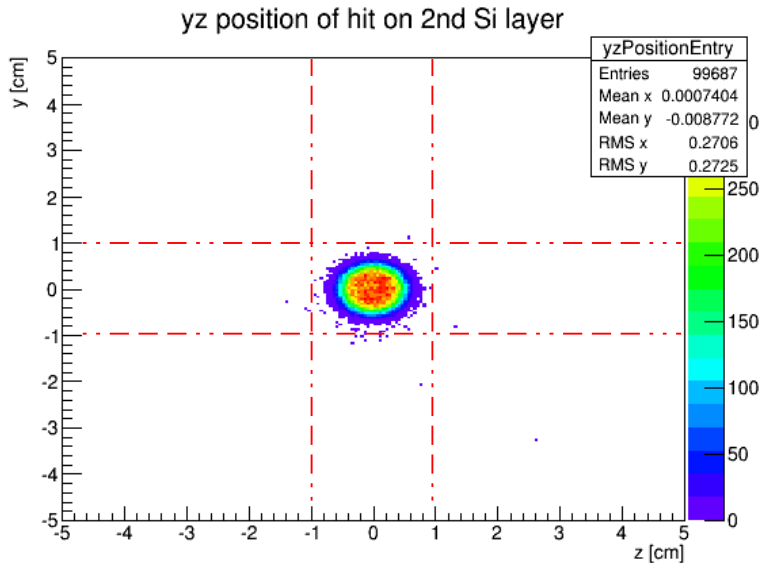


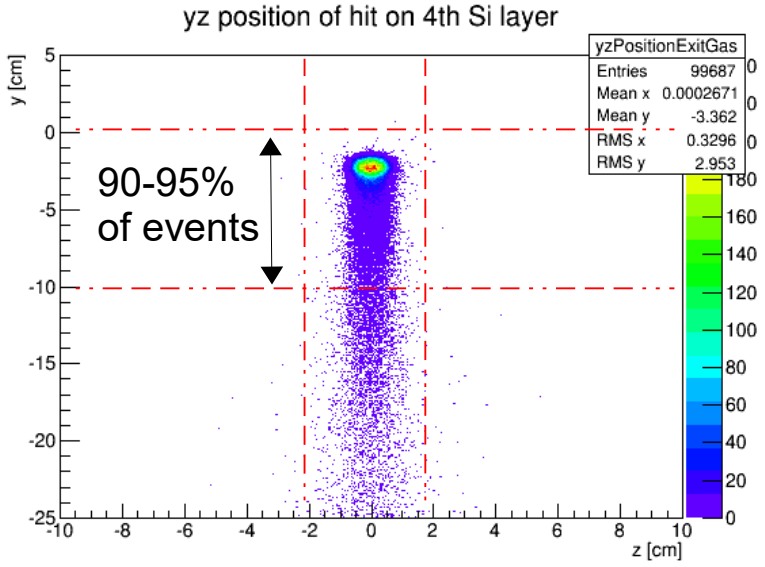
- Sensors with spatial resolution better than 10 μm are needed

ILD	ATLAS	CMS
<10 μm	12 μm (pixels)	10 μm (pixels)
	16 μm (strips)	20-30 μm (strips)

Coverage area

- Hit positions on front and back sensors for 5 GeV e^- beams

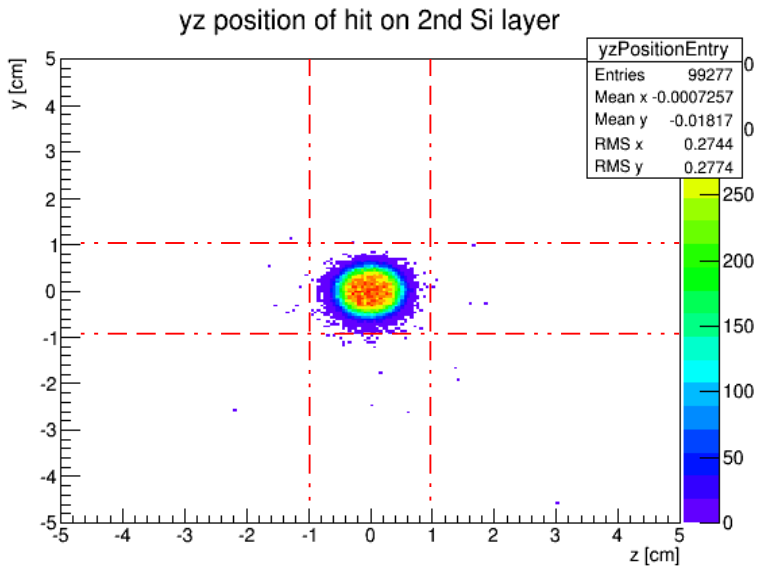


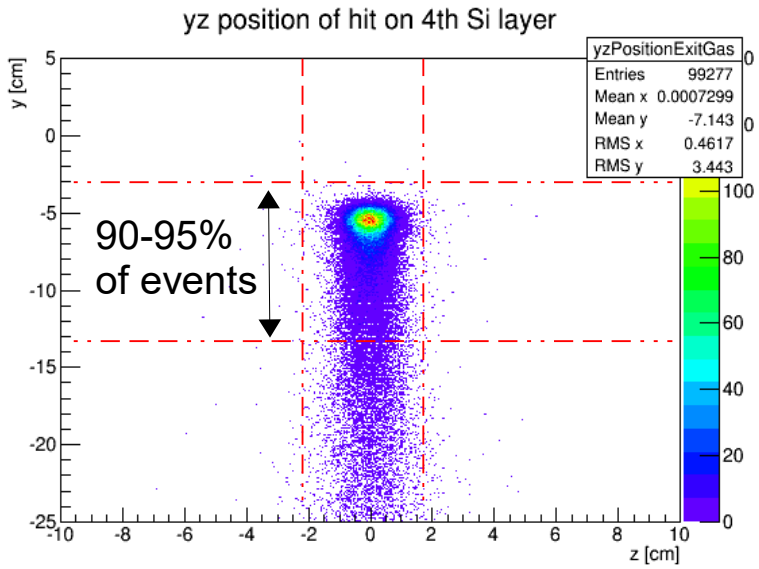


- For lower energy beams, the hit distribution on the back sensors is more spread and shifted to lower y values

Coverage area

- Hit positions on front and back sensors for 2 GeV e^- beams





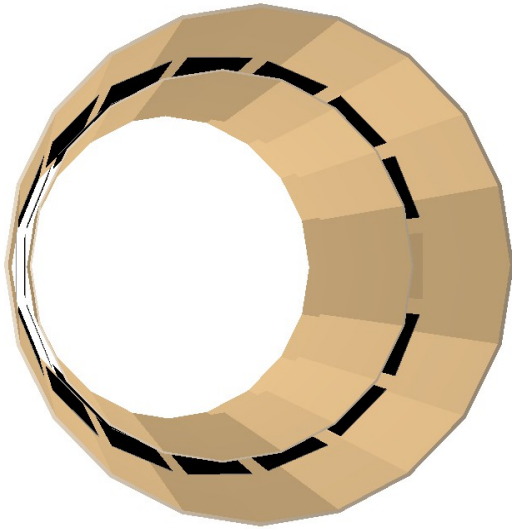
- For lower energy beams, the hit distribution on the back sensors is more spread and shifted to lower y values

- Minimum coverage area: ~2x2 cm^2 for front and 4x10cm^2 for back sensors

- Larger coverage area is beneficial (e.g. less moving and alignment of the system)

Simulation – Next steps and Challenges

- Ongoing effort on DD4hep simulation for the Silicon tracker in order to obtain more precise results in terms of track fitting



- In the future, we will need common simulation and reconstruction framework and analysis software for the Silicon tracker and the Large Prototype TPC (in DD4hep?)

Hardware Options

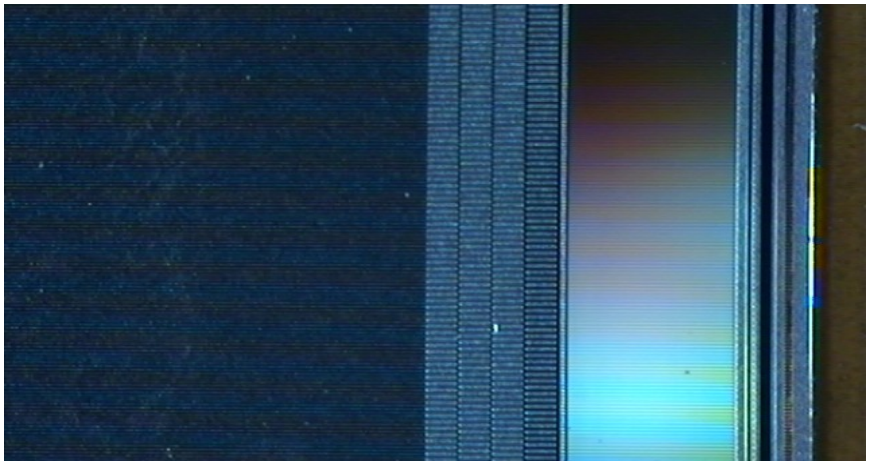
- Strip vs Pixel Silicon sensors

Strip sensors (SiD, M. Breidenbach)

- Good spatial resolution (7-8 μm)
- Large sensor surface → Able to instrument large areas (eg 10x20 cm^2)
- Medium cost

Pixel sensors (Mimosa, M. Winter)

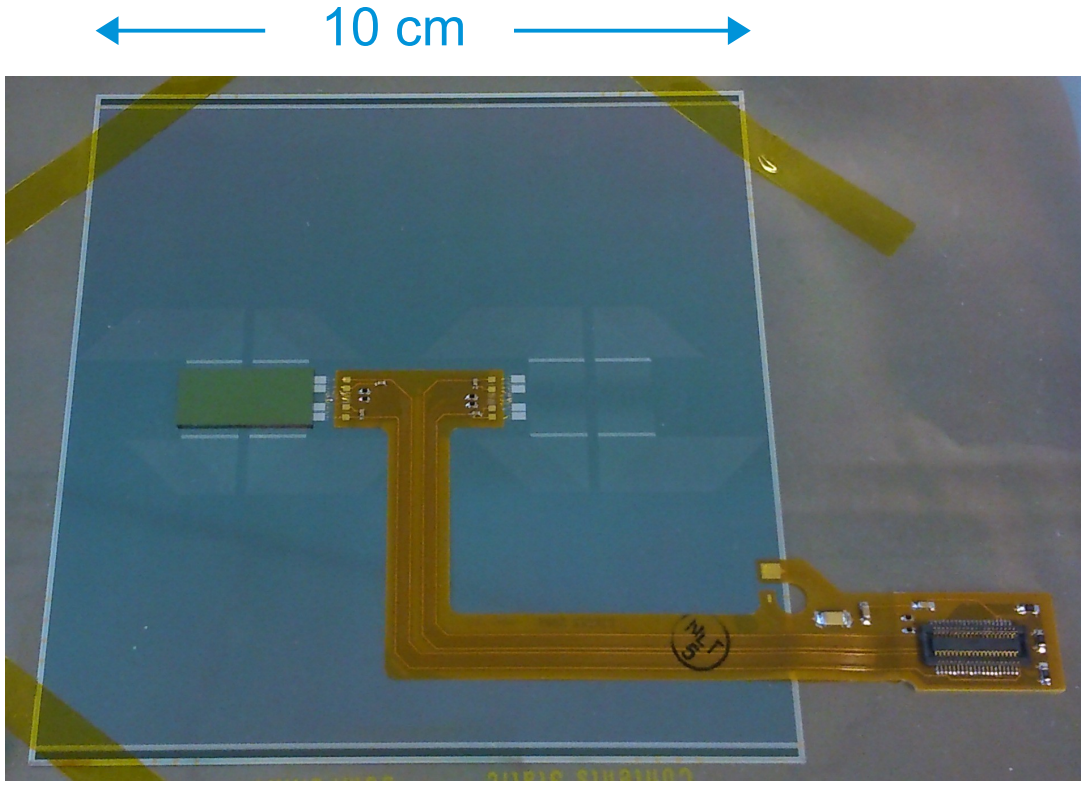
- Excellent spatial resolution (3-4 μm)
- Small sensor surface → Able to instrument minimum area only
- High cost



SiIC sensor
50 μm pitch
(Th. Bergauer)

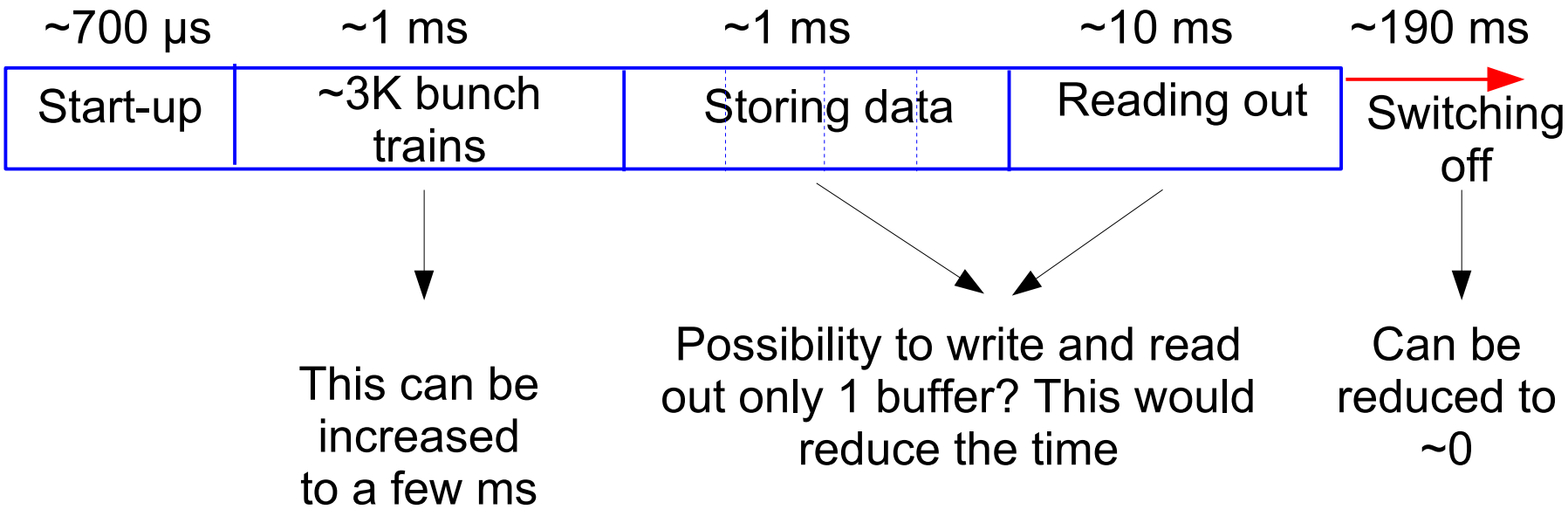
Hardware Options (2)

- Si strip sensors of 25 μm pitch (4K strips) → spatial resolution 7-8 μm
- Read out by two kpix chips bump bonded onto the sensor
- Control of sensor and kpix through wire bonding
- Kapton cable to read out the data from kpix and control the kpix and sensor



KPiX cycle

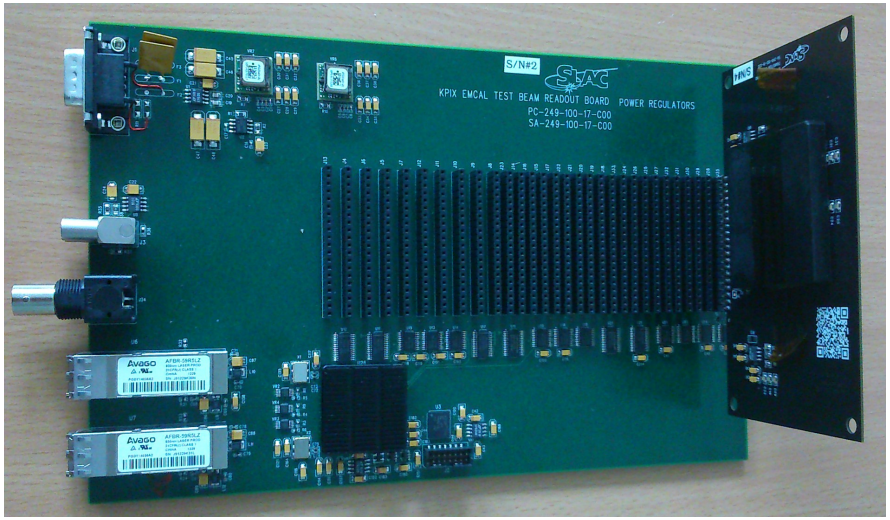
- KPiX developed for an ILC environment



- KPiX works on self-trigger or forced trigger mode
- How efficiently can we use it in the test beam (with the TPC) with such a cycle?
  - TPC receives external trigger and then goes to BUSY for data acquisition, reading, storing

Currently at DESY

- Test system to be set up that includes
  - DAQ board able to control 30 KPiX
  - KPiX



- ECal sensor bump bonded to KPiX
- Mechanical prototype of Silicon tracking sensor bump bonded to KPiX
  - For design of structure support, local tests on bump/wire bonding
- Negotiations with Hamamatsu for a production of sensors (SLAC)

Hardware and DAQ Challenges

- Acquiring sensors with spatial resolution <10 um
- Scheme for efficient use of KPiX in combination with the TPC
  - Different acquisition cycles
- Combination of the two DAQ systems (Si & TPC) in order to be able to have combined test beams in the future

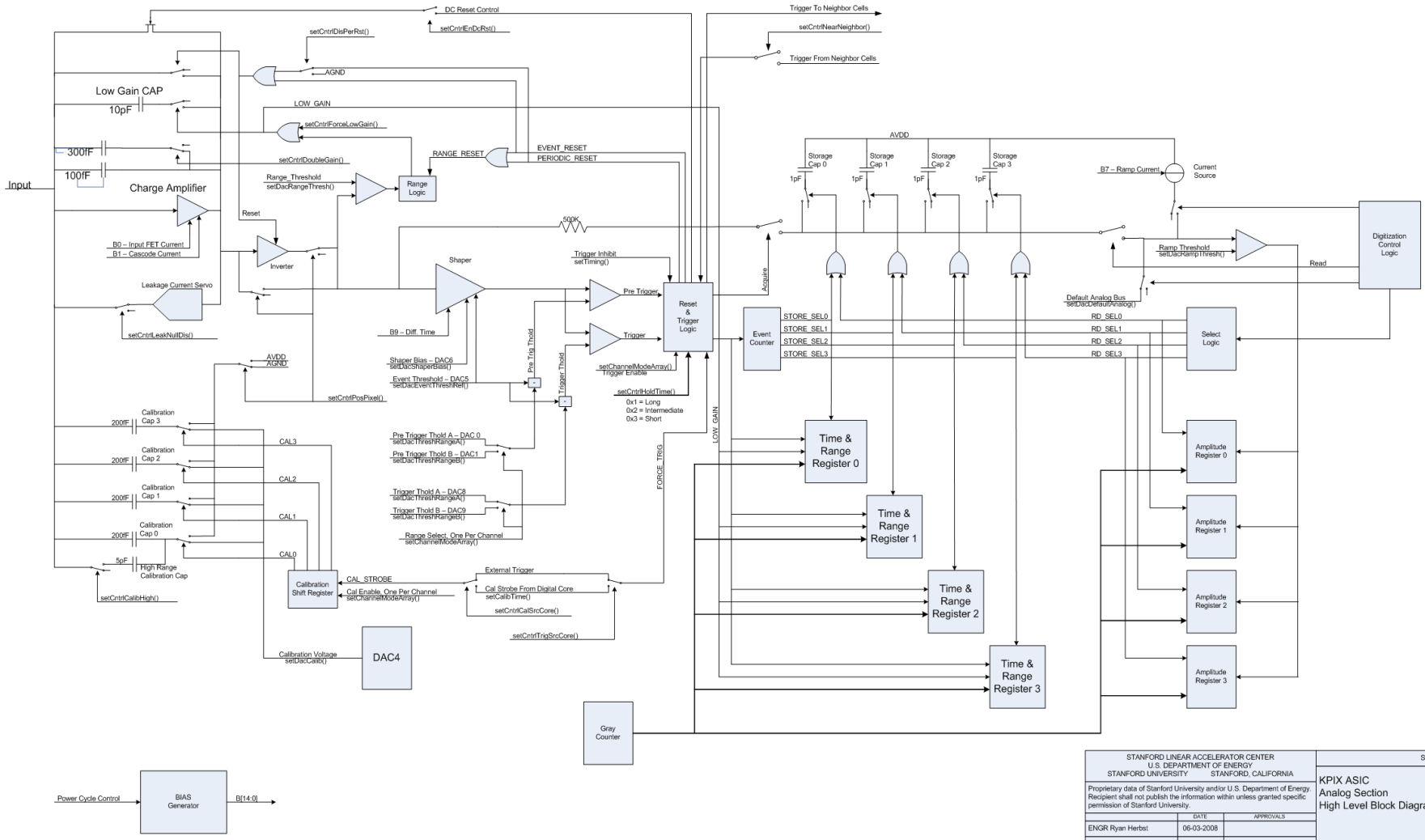
Conclusion

- Silicon tracker to accompany the Large Prototype TPC needed
- Simulation studies in order to define the characteristics of the system
  - >4 Silicon layers
  - Sensors with 10 μm or better spatial resolution
  - Large coverage area
- Hardware
  - 25 μm pitch Silicon strip sensors (discussions with SLAC-Hamamatsu. ~few months)
  - KPiX + DAQ board at DESY (system setup starting next week)
- Ongoing effort
  - Simulation studies within DD4hep (track finding and fitting)
  - Efficient use of KPiX at DESY test beam
- Next steps
  - Use of EUDAQ for the Silicon tracker (first steps in the upcoming weeks)
  - Design of mechanical support for the telescope (waiting for Hamamatsu discussions since it also depends on sensor choice)

DESY

BackUp

KPiX – Simplified Block Diagram

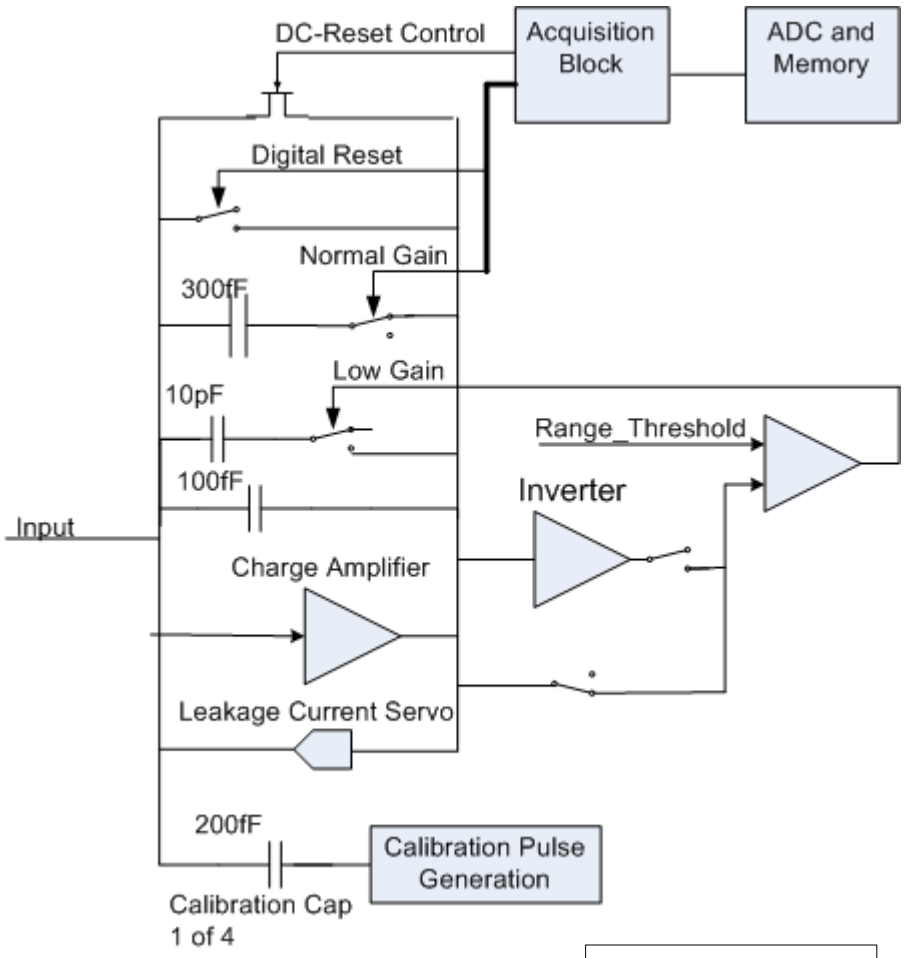


Switches are all shown in their state when control signal is de-asserted (0 Volts)

STANFORD LINEAR ACCELERATOR CENTER U.S. DEPARTMENT OF ENERGY STANFORD UNIVERSITY STANFORD, CALIFORNIA			SHEET 1 OF 1
Proprietary data of Stanford University and/or U.S. Department of Energy. Recipient shall not publish the information within unless granted specific permission of Stanford University.			KPIX ASIC Analog Section High Level Block Diagram
	DATE	APPROVALS	
ENGR Ryan Herbst	06-03-2008		
DFTR Ryan Herbst	06-03-2008		
CHKR			Rev 4.1 - 06/03/2008

KPiX – Charge Amplifier Block

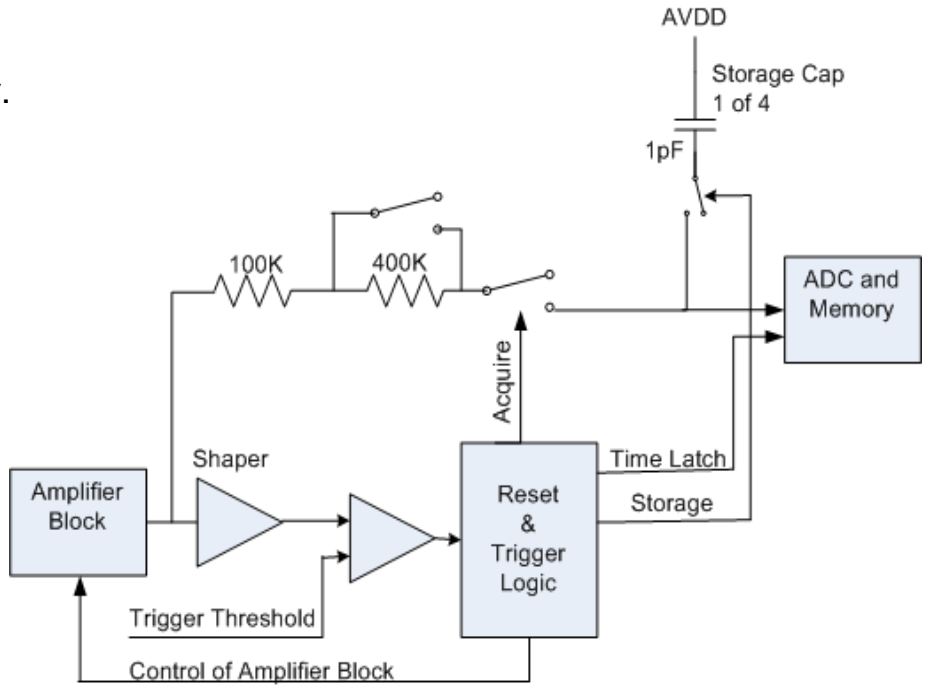
- The incoming signal is picked up by the charge amplifier and stored in the feedback capacitor (default ranges 100 fF and 400 fF).
- If the default range is exceeded, a 10 pF capacitor is automatically added to the feedback to extend the range to 10 pC.
- For negative-polarity signals, an inverter is inserted after the charge amplifier. The polarity of the calibration signal is reversed too.
- For DC-coupled signals, the leakage is compensated by a servo circuit. The amount of leakage is determined with no signal present and held during the signal period.
- A precision calibrator sends up to four signals with amplitudes and timings as defined during the set-up cycle.
- Digital reset during power-up and after each triggered event. Can be executed before each beam bunch for ILC operation.
- Option for DC reset for non-bunched signals, e.g. cosmic rays, radioactive source data.
- Periodic and digital resets are inhibited immediately after each trigger (controlled by the acquisition block)..



From D.Freytag

KPiX – Data Acquisition Logic

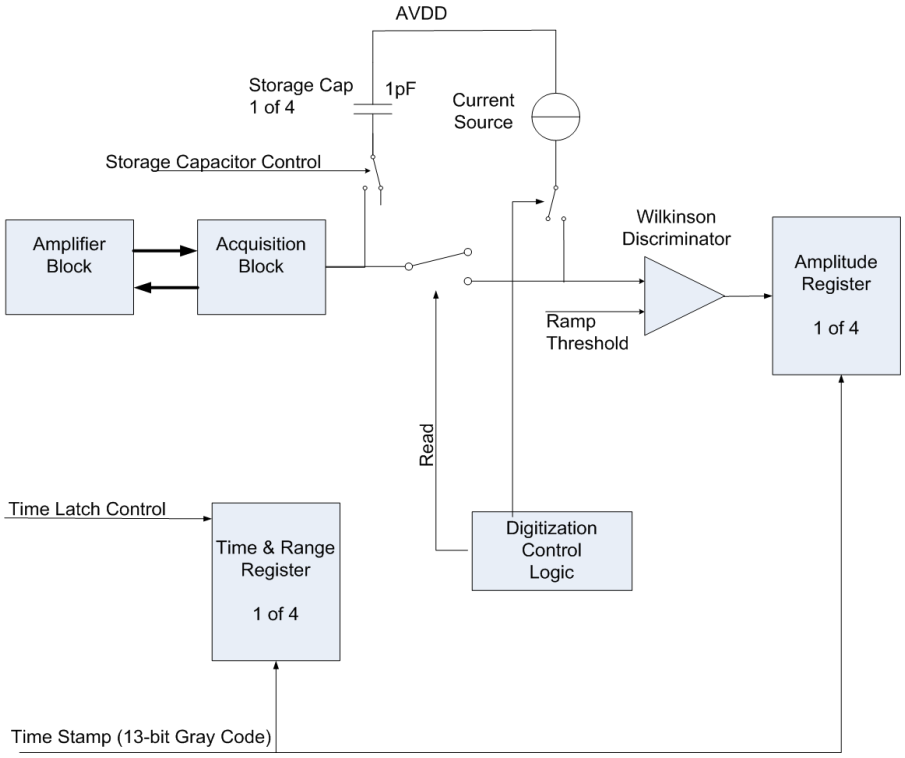
- The charge amplifier signal is amplified, shaped and sent to the trigger stage.
- For signals above trigger threshold, the digitally controlled acquisition cycle is started. After a wait period, the signal is acquired in the storage capacitor. The coupling elements form a low pass filter. Two integration constants (0.5 us and 0.2 us) can be selected.
- One of two threshold levels is selectable in each cell. High-low discrimination system to catch potential triggers early to inhibit digital and DC resets.
- For the tracker application, the trigger is carried over to the neighboring cells to catch low level spill-over signals below trigger threshold.
- After a programmable time interval, the signal amplitude is held in the capacitor and control passed to the next storage capacitor.
- The integration interval is thus precisely controlled, resulting in a stored amplitude proportional to the signal, even if the asymptotic value is not reached.
- A strobe signal is sent to the memory block to record event time.
- Amplitude and time information for up to four events can be stored for each data cycle.



From D.Freytag

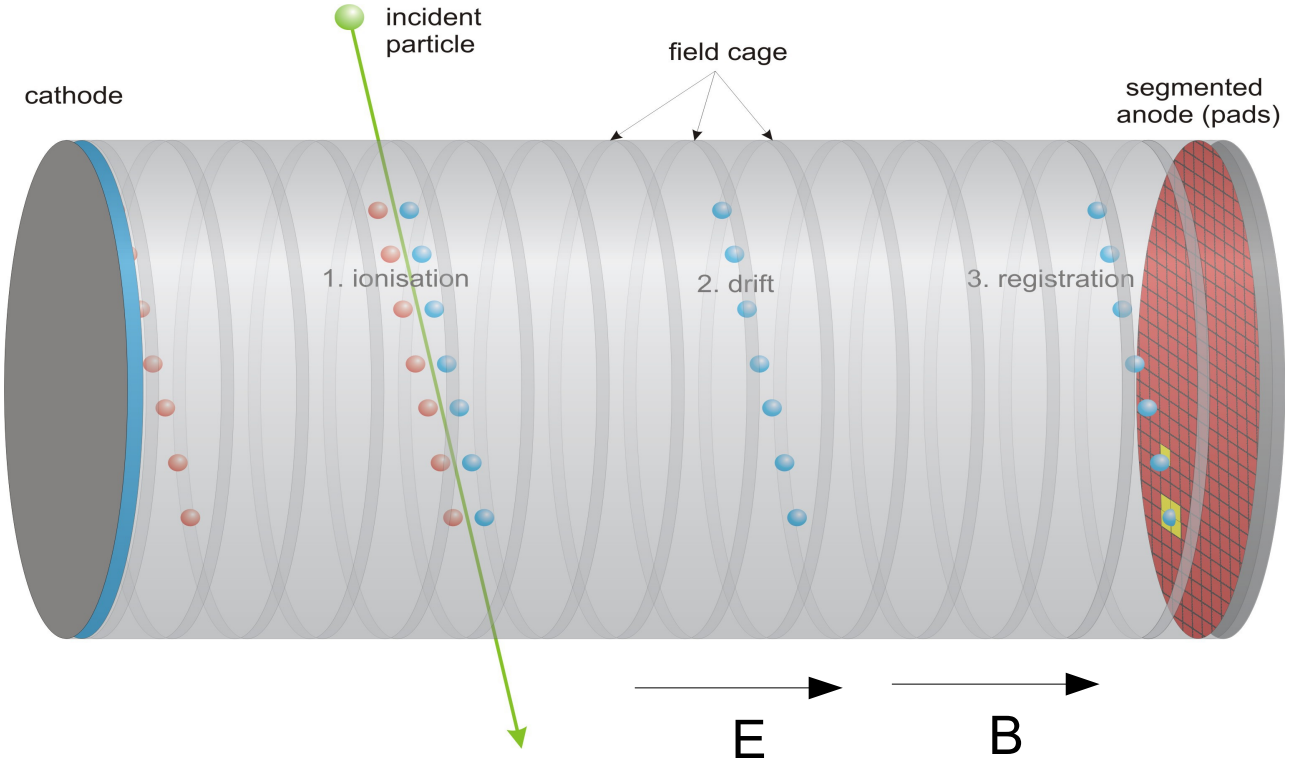
KPiX – ADC and Digital Storage

- The analog information previously stored in 4x1024 capacitors is digitized in four cycles, each for 1024 capacitors in parallel.
- The Wilkinson method is used for the conversion, with a current mirrored into each cell running down the charge in the storage capacitor. A ramp-threshold discriminator detects the transition through zero and causes the content of a common Gray counter to be stored in memory.
- The ADC has 13 bits resolution.
- This method of digitization could proceed independently in each cell, offering the possibility of continuous operation. The four buffers in each cell could be filled and read out on a rotating basis. This would require a major upgrade of the digital core.



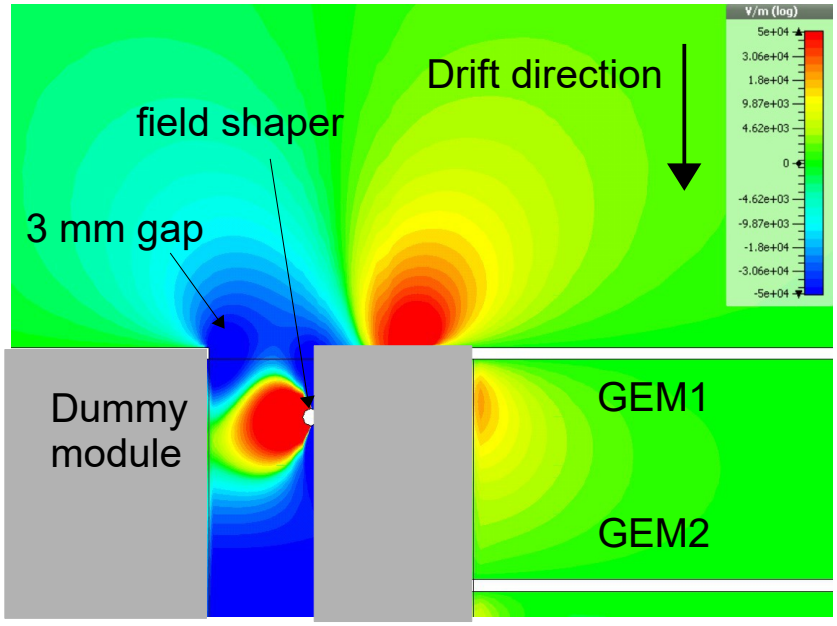
From D.Freytag

Time Projection Chamber – Working Principle



- Magnetic field parallel to the electric field
- Inhomogenities in Electric & Magnetic fields can cause distortions (ExB terms)

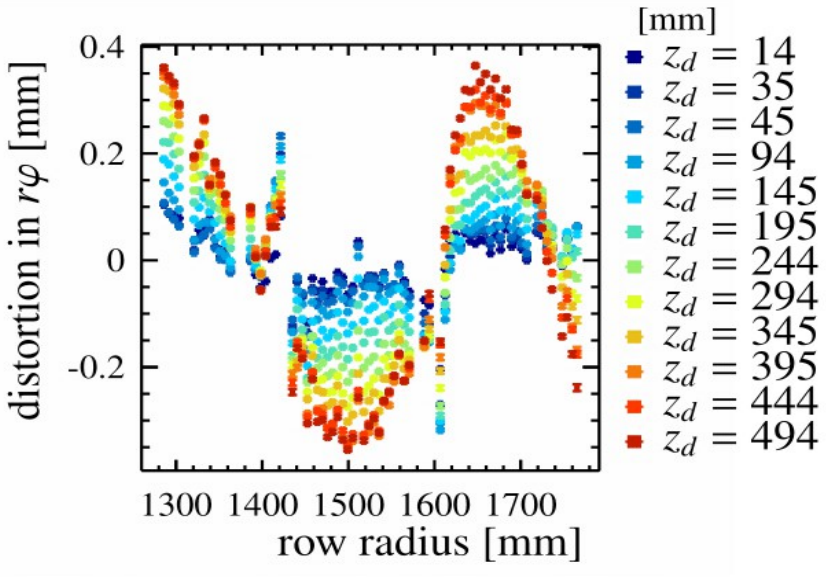
Field distortions in TPC



- Inhomogenities in Electric fields can cause distortions
- Magnetic field parallel to the electric field
  - ExB terms pronounced at module edges

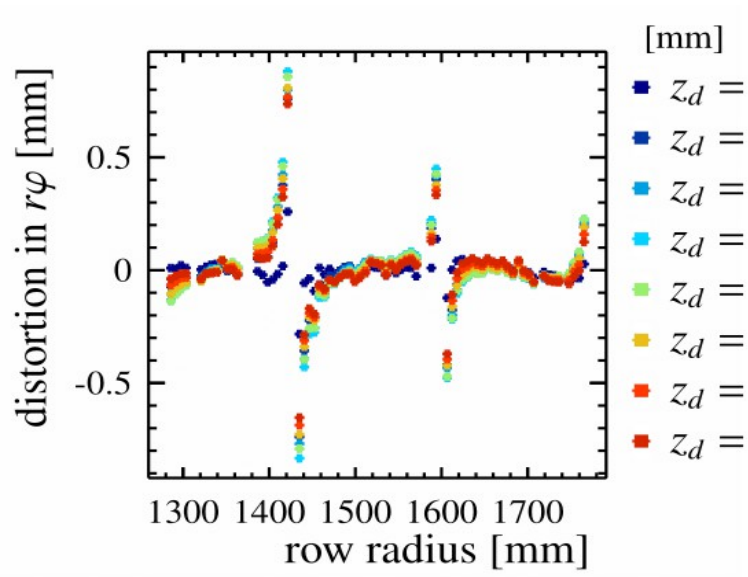
Distortions in TPC tracks

E field only



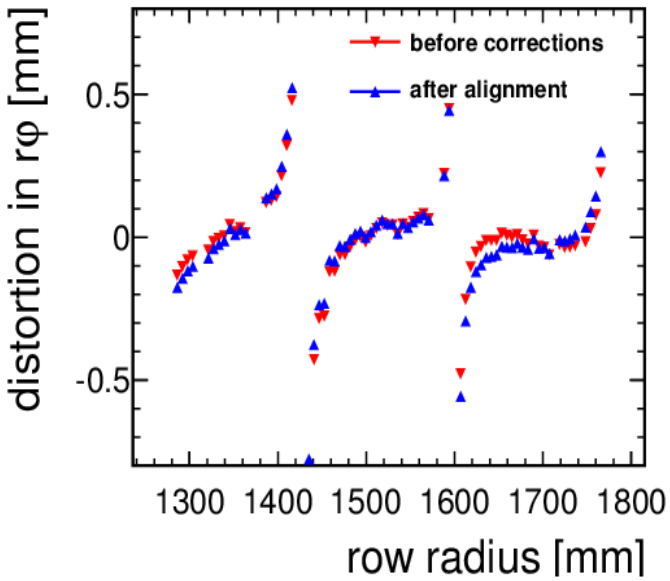
- A straight fit is used for the track → full distortions for electric field are visible

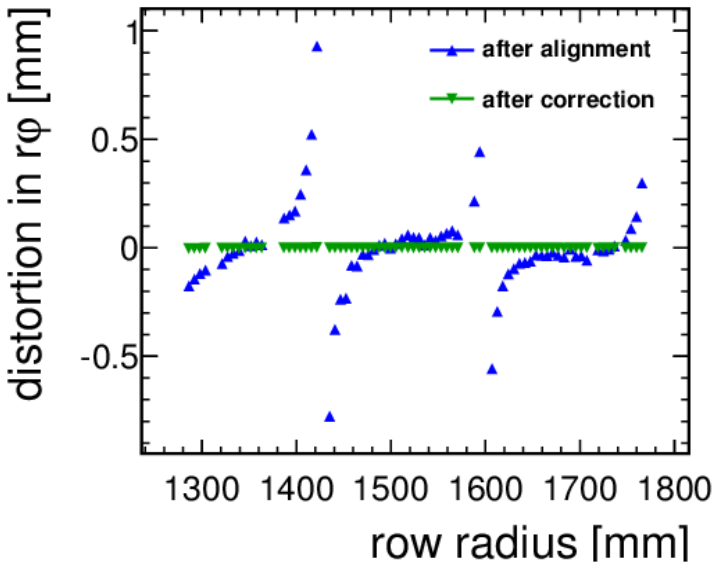
E and B (1 T) fields present



- A curved fit (helix) is used for the track → distortions can be partially absorbed in the track curvature

Alignment and Distortions





- Displacement and rotation of GEM module
- Use B=0 T data where ExB effects not present
- Corrections of 0.1 mm and a few mrad

- Distortions derived from 10% of events and applied to the rest