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EUDET Beam Telescope

Wojciech Dulinski on behalf of JRA1

Outline

- The goal: a high-precision, general purpose beam telescope
- Some limitations of solution based on existing techniques
- The beam telescope based on MAPS: novel, high precision tracking detectors
- Review of results from existing MAPS prototypes
- Telescope implementation plans and schedule
- Conclusions

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General Purpose Beam Telescope: a precision tool for testing a new generation of detectors being developed for International Linear Collider (ILC)

Technical specs:

- Compact: to be mounted inside existing magnets, transportable
- User friendly, easy to run AND to interface with various users
- Sensitive area: few sq. cm, (at least 2 cm in one direction)
- High precision tracking: down to 2 µm (or better) in the center

The goal is to have such a device in 2008!

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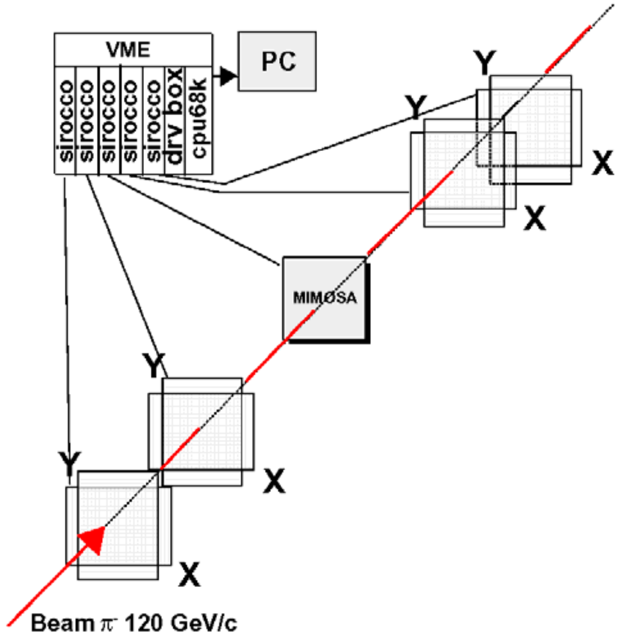
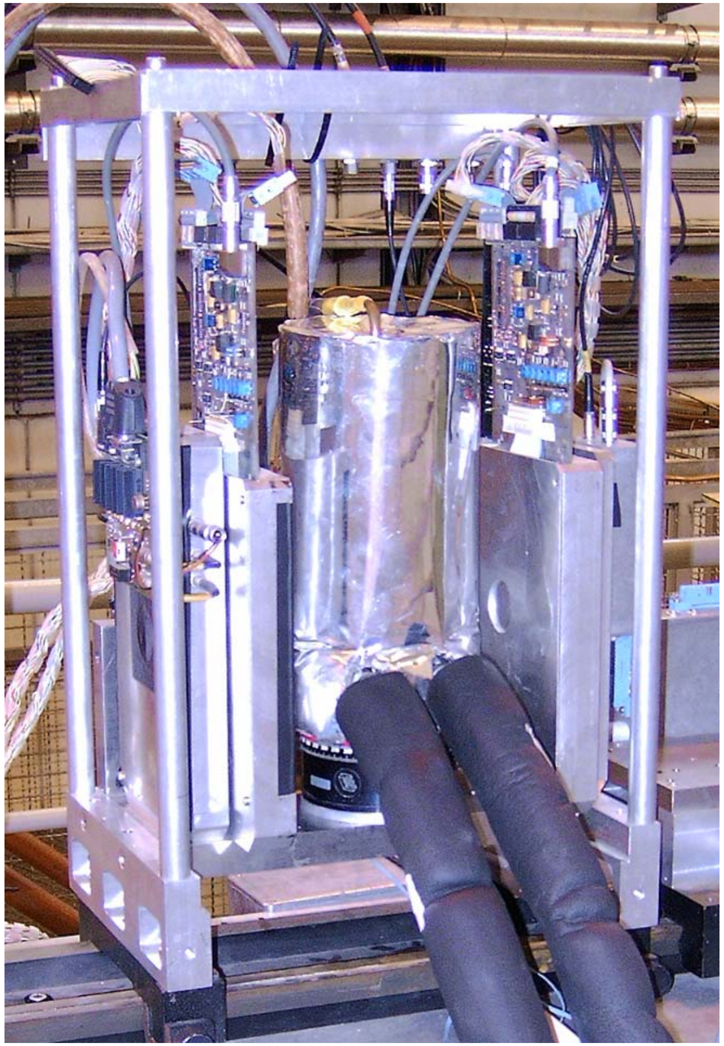
Existing solution: Strasbourg silicon-based beam telescope





The beam telescope, based on high precision silicon strip detectors. The track position in the middle of the telescope is predicted with the precision of ~1 µm

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One specific problem of proposed beam lines for ILC instrumentation testing: relatively low energy (few GeV) electrons (like at DESY)

- Performance of standard (silicon strip based) beam telescope highly degraded (down to ~10µm in the center), because of multiple Coulomb scattering

- Our solution to overcome above problem: a use of a novel, high-precision, thin and pixellized tracking sensors, required by ILC and developed since several years in some laboratories

Today, CMOS Monolithic Active Sensors (MAPS) are mature and well adapted for this task!

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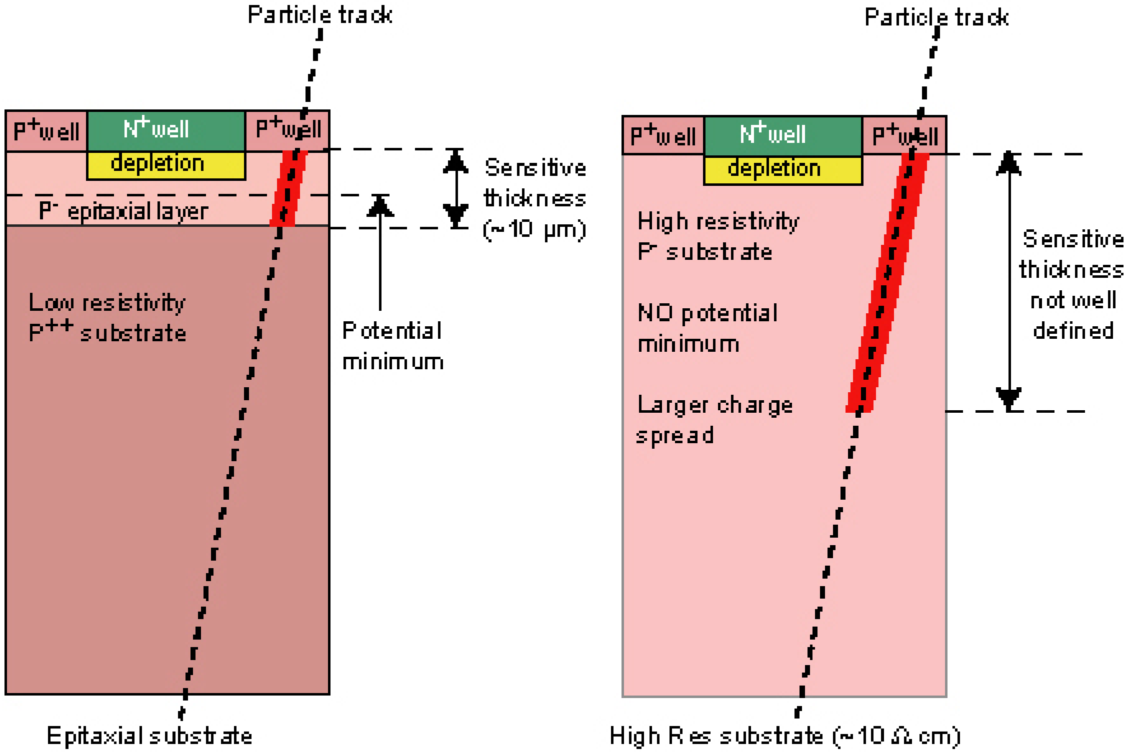
CMOS Monolithic Active Pixel Sensors (MAPS): radiation sensor and its readout electronics integrated on the same silicon wafer



- The active volume (epi-layer, ~10 μm thick) is underneath the readout electronics, providing 100% fill factor
- The charge generated by ionization is collected by the n-well/p-epi diode
- Charge collection is achieved through the thermal diffusion

The device can be fabricated using standard, cost effective and easily available twin-tub CMOS process on epi substrate. No post-processing (e.g. bump-bonding) is needed! However, it can be thinned down to less than 50 μm

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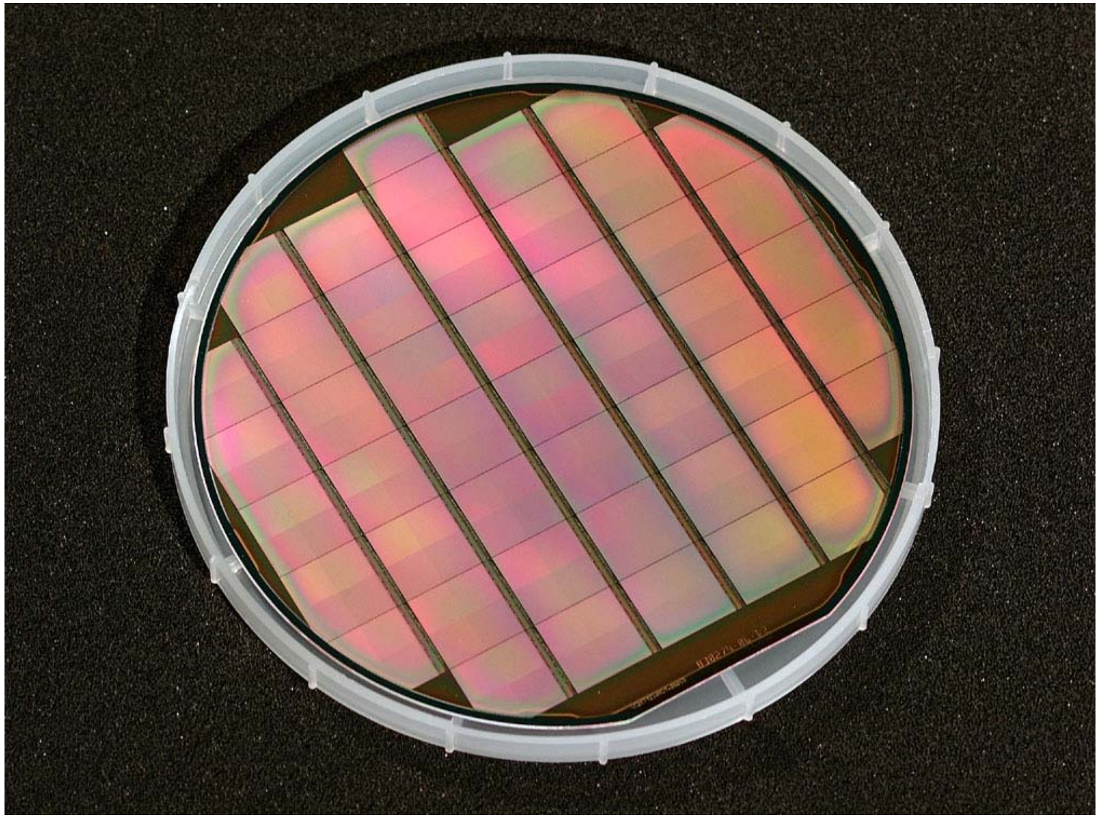
Wafer scale MAPS prototype example: Mimosa5 (10^6 pixels) in AMS-0.6 µm CMOS process



Six inch wafer hosts 33 sensors, 1.7×1.9 cm^2 each

Maximum allowed size of a circuit in a standard CMOS process: ~20x20 mm^2 (reticle)

Reticle stitching is needed, in order to get a larger device (a ladder, ~10x2 cm^2)

MIMOSA5

Each reticle is an independent circuit. Periphery logic and bonding pads layout along one side. Simplified stitching of up to 7 reticles in one direction. Still some problems with a yield (~30-40%) but it can be solved (according to some digital imager suppliers).

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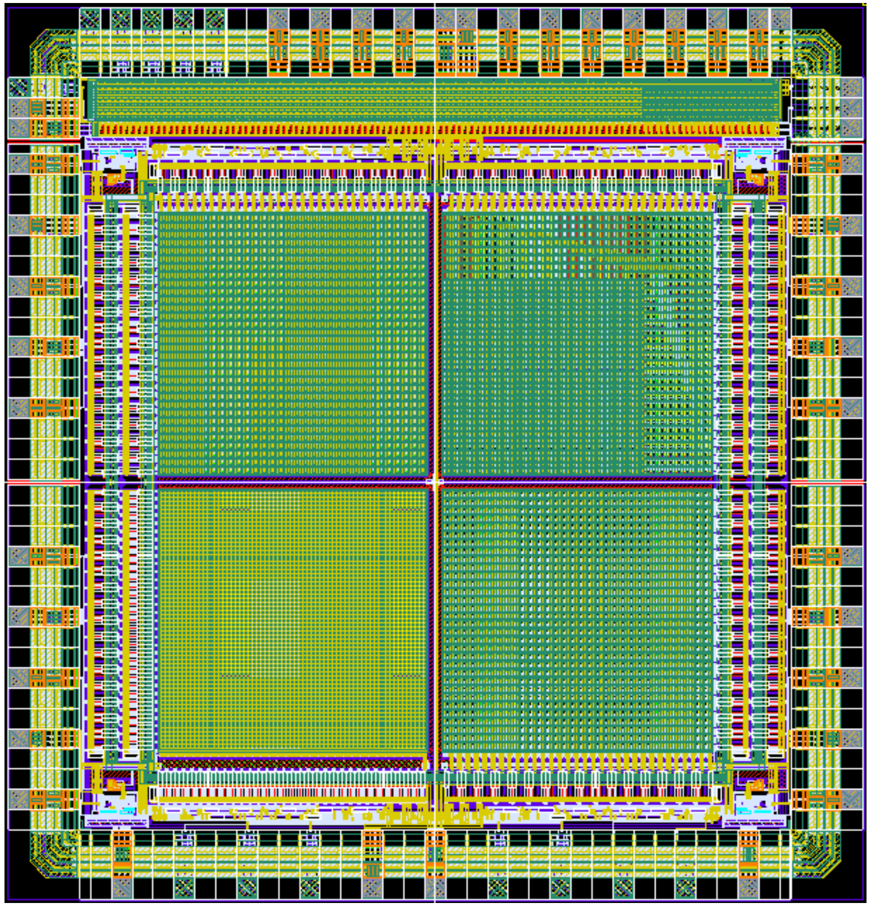
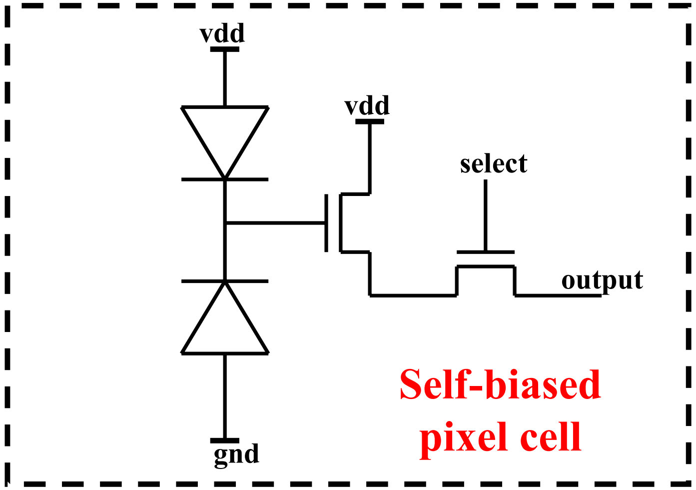
Small scale prototype MIMOSA9: "self-bias" arrays with various pitch for tracking study



Dimensions: 4.1x4.3 mm²

AMS 0.35 µm CMOS OPTO process

- Advanced mixed-signal polycide gate CMOS: 4 metal, 2 poly, high-res poly, 3.3V and 5V gates
- Optimized N-well diode leakage current
- 14 µm epi substrate (20 µm possible?)
- Availability through multi-project submissions, with a reasonable pricing



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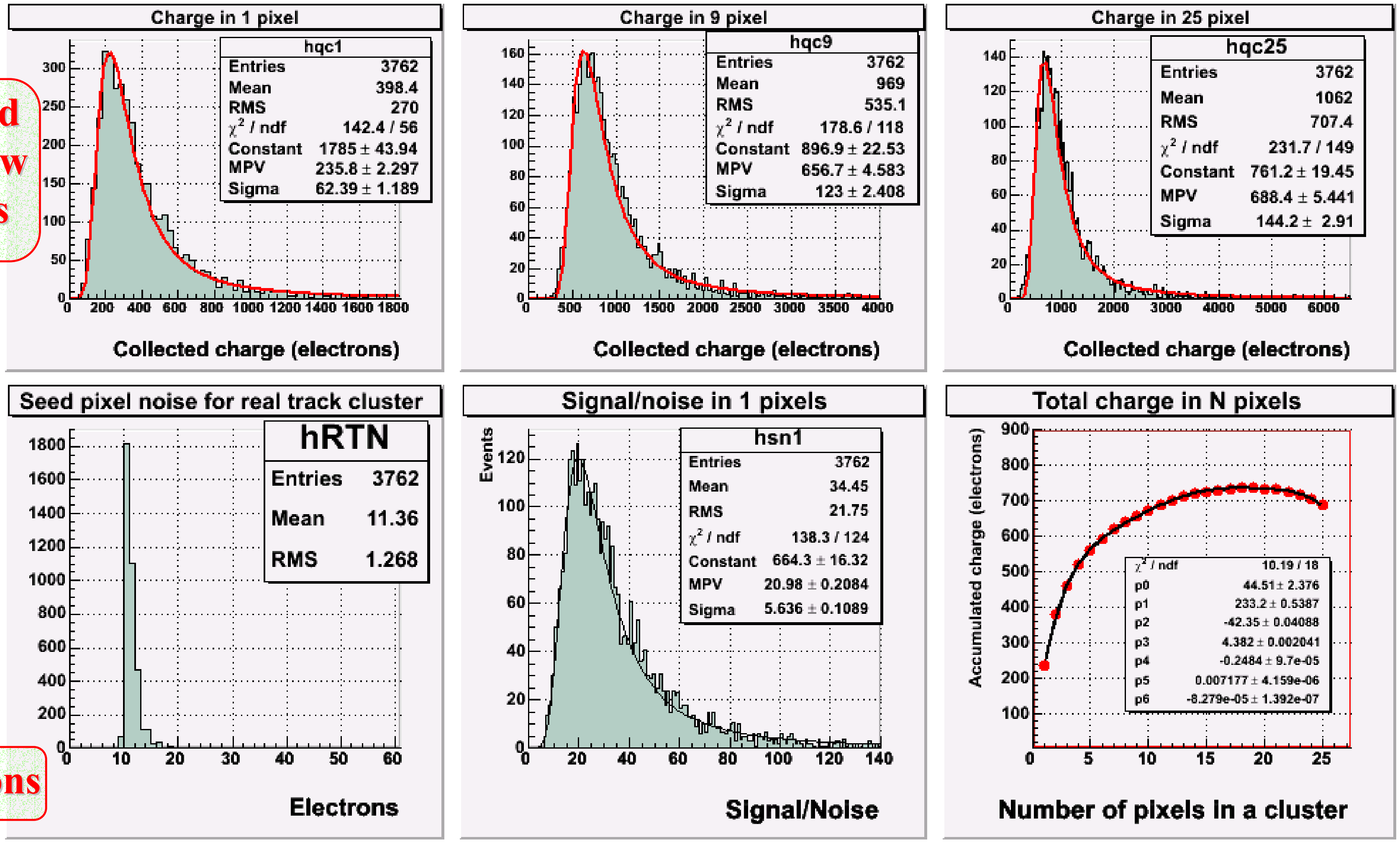
A "typical" example from the beam tests: 30µm pitch array, 20°C

M9 ; run 9534; Pl 10, dist 90; Gain 7.200; eff 99.810 +- 0.070; Seed 6.0; Neigh 4.0

Signal in the seed pixel: down to few tens of electrons



ENC: ~10 electrons

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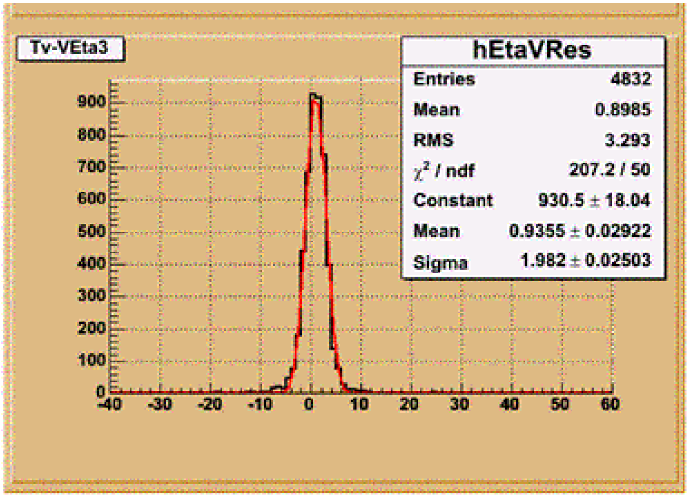
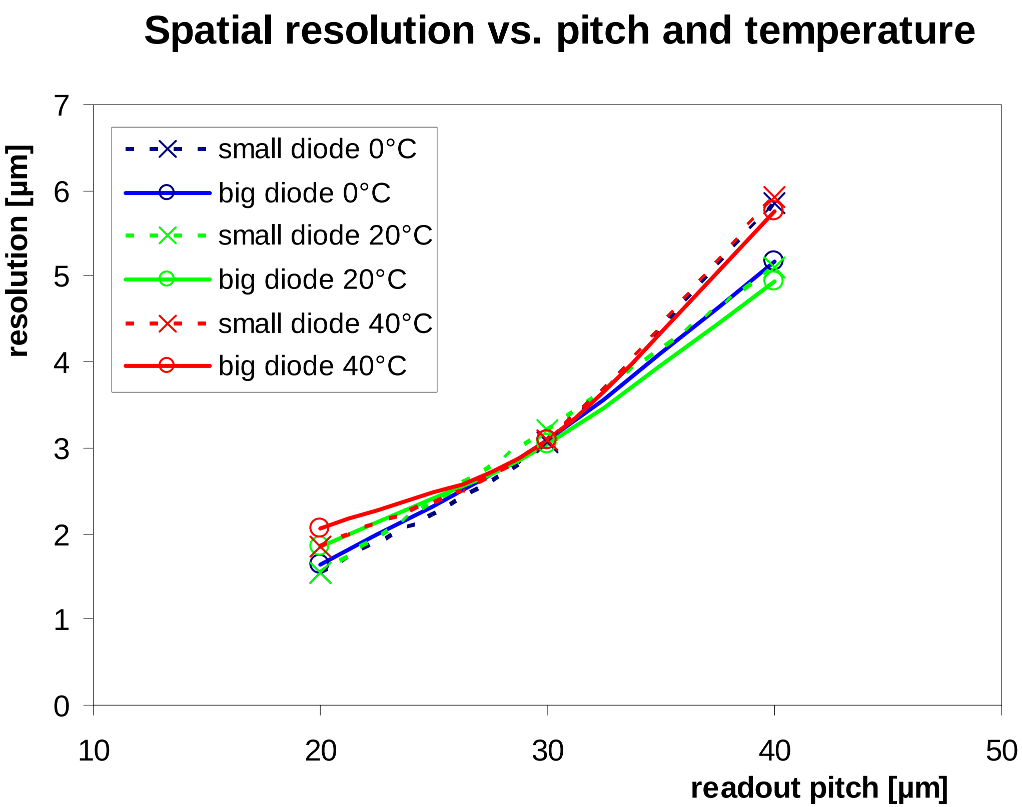
Mimosa9 beam tests: spatial resolution



Residual distributions
for 20 µm readout pitch at 20°C



Spatial resolution: down to 1.5 µm

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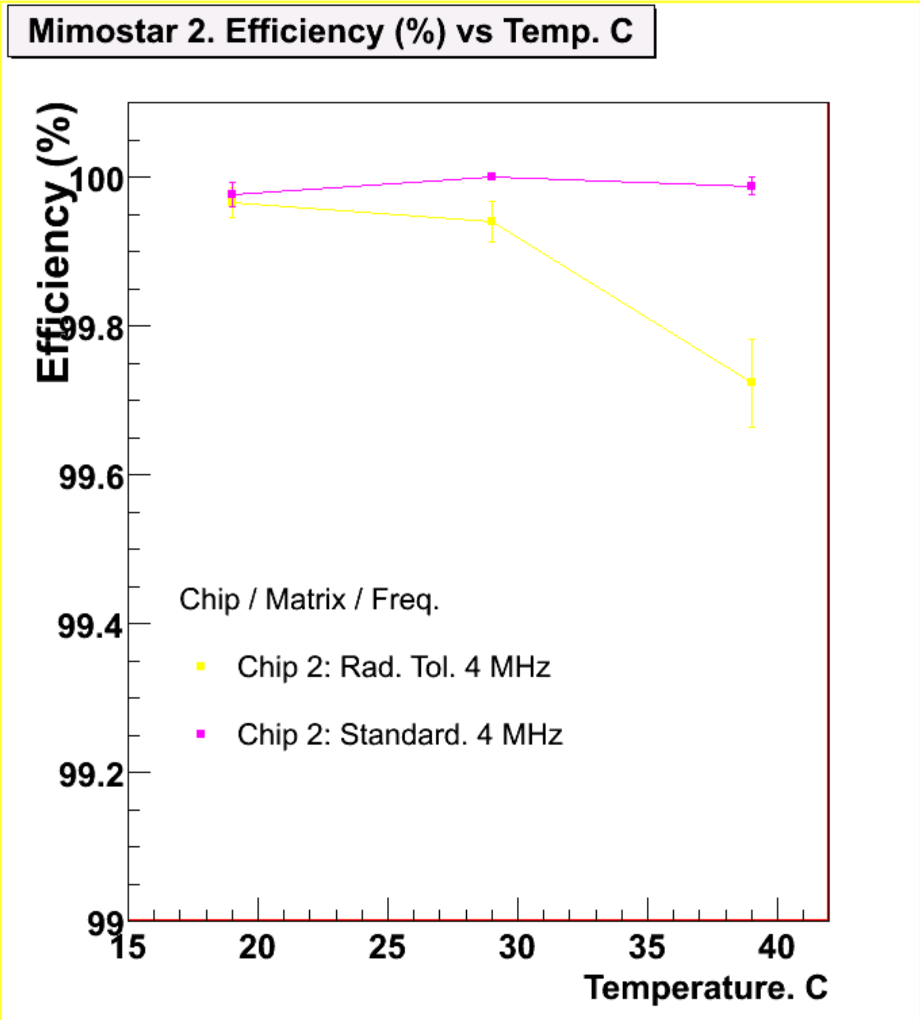
Mimo*2: the demonstrator for STAR experiment microvertex upgrade. Based on radiation tolerant N-well collecting diodes.



Efficiency >99.9 % at room temperature AND long (4ms) integration time, for the seed S/N cuts of 5 (fake hits rate <10^{-5})

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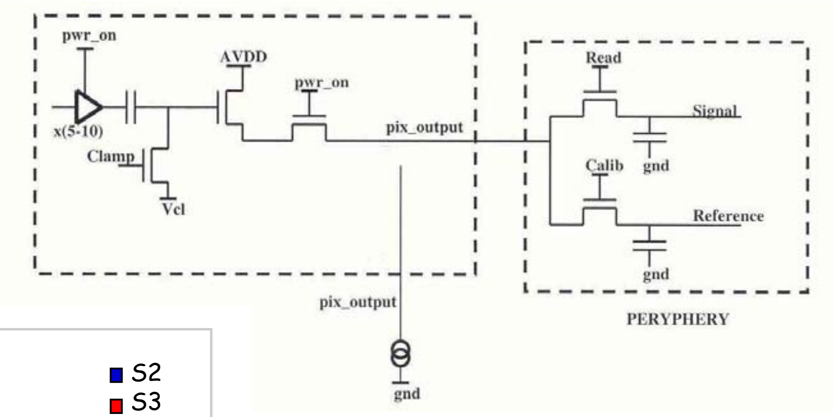
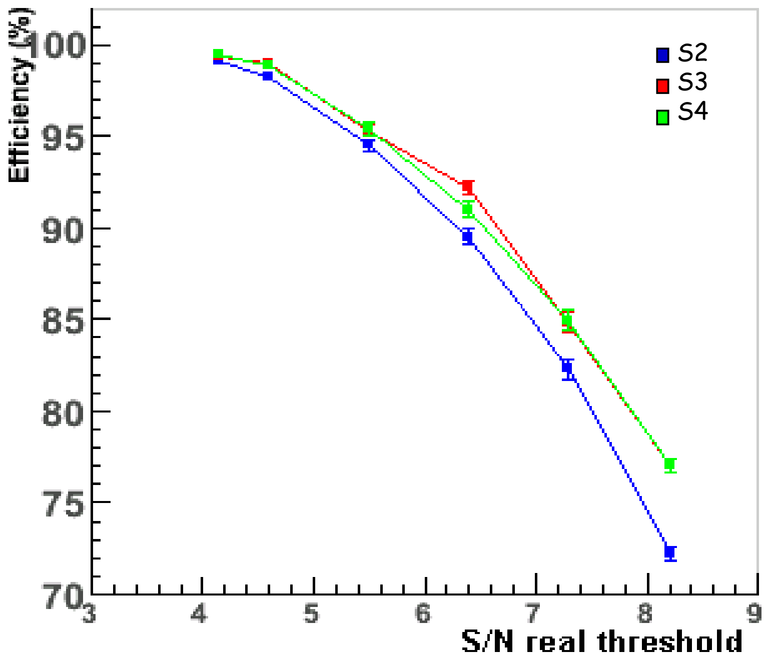
Mimosa8 (TSMC-0.25µ, 8 µm epi) – a binary readout demonstrator

Prototype in collaboration with Dapnia/Saclay

- Pixel pitch 25 x 25 µm^2
- Clamping based CDS in pixel
- On-chip FPN suppression
- On-chip discrimination (a comparator at the end of each column)





- First demonstration of feasibility of FPN correction using on-chip real time circuitry
- The design goal confirmed by the beam tests results: efficiency > 98 %

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EUDET telescope implementation plans: phase 1 ("the demonstrator")

- Use of medium-size prototypes developed for STAR microvertex upgrade (existing Mimosa5 as a back-up)
- 256x256 (640x320) device, 30 µm readout pitch, 7.5x7.5 (19.2x9.6) mm^2 sensitive area, four (two) parallel outputs, the frame readout time (equal to the integration time) < 1 ms (<2 ms), room temperature operation, internal bias setting programmable by JTAG
- Sensors available in autumn 2006, the demonstrator beam telescope ready for mid-2007
- Specific DAQ, providing real time data AND an easy interface to various users developed in parallel

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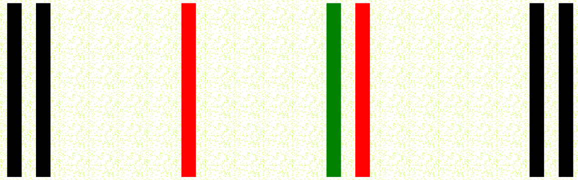
Optional high-precision modules for some specific use

- 512x512 pixels device, 10 µm readout pitch, 5x5 mm^2 sensitive area, four parallel outputs, <3ms frame readout
- Expected resolution per plane: <1µm
- Possibility of high precision tracking, even at medium energy beam conditions (DESY, SLAC, KEK)



High-precision configuration layout: the distance DUT-reference plane ~ 1 mm

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Implementation plans: phase 2 ("the ultimate device")

- Specific development for EUDET telescope application: digitally readout sensors
- 800x400 (800x800) pixels device, 25 μm readout pitch, 20x10 (20x20) mm^2 sensitive area, low resolution ADC per column(4-5 bit) for parallel processing, frame readout time (equal to the integration time) << 1 ms
- Prototype sensors (in target AMS-035 OPTO process) available in 2007, the final size devices early 2008
- The ultimate beam telescope ready for the end of 2008!

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Conclusions

Clear and well defined plans, the technology under control, a lot of basic (novel) components firmly tested.

Ready to start, confident about the result!

Major responsibility within JRA1:

Sensors: IReS-IPHC (Strasbourg), DAPNIA (Saclay) plus LPSC (Grenoble) and LPC (Clermont-Ferrand)
DAQ (very important!): Geneva University, INFN (Milano, Ferrara, Como), Bristol University
Integration aspects: DESY, Bonn, Mannheim