Calorimeter data acquisition R&D

C. Barham, B. Fromant, M. Goodrick, R. Shaw, D. Ward
Cambridge University

P.D. Dauncey, A.-M. Magnan, D.R. Price, O. Zorba
Imperial College London

D. Bailey, R. Barlow, R. Hughes-Jones, M. Kelly, S. Kolya
University of Manchester

G. Boorman, B.J. Green, M.G. Green
Royal Holloway, University of London

M. Lancaster, N. Pezzi, M. Postranecky, C. Targett-Adams, M. Warren, M. Wing
University College London

Talk outline

- **Administrative and general introduction**
- **General principle of DAQ research in UK**
- **Details of five areas of DAQ research**
- **What we want to achieve**
- **Issues for R&D on DAQ for prototype design and EUDET project**
- **Plans**

Administrative introduction

CALICE-UK is a group of seven institutes: those mentioned plus Birmingham and Rutherford.

Applied together for funding from PPARC: have a 3.5 year programme started on 1 October 2005.

Performing R&D in a number of areas:

- CALICE test-beam programme
- Data acquisition
- Use of monolithic active pixel sensors
- Thermal and mechanical issues
- Simulation and physics

Also part of EUDET specifically for DAQ work - provide DAQ system for future prototypes.

DAQ system - general R&D work

Have come up with a conceptual design of a DAQ system for the ECAL:

- **Make assumptions as to what can be done in the chip on detector and electronics at the edge of the detector. May be different options, cannot predict what will happen. So need to be flexible. Assume reading out higher volume and can definitely do anything lower.**
- **Using commercial, off-the-shelf products, so should be cheap, scalable and maintainable. Idea of "backplane-less" system.**
- **Identify bottlenecks in this concept, effects on the Calorimeter system $\rightarrow$ R&D.**
- **Should be applicable to HCAL - other non-calorimeter components?**
- **Test-bench work and demonstration of workability of concept.**
- **Then write chapter in Technical Design Report.**
- **Also practically: should be able to provide DAQ for prototype calorimeters being developed.**

DAQ system - assumptions

The ECAL consists of 6000 slabs containing 4000 silicon diode pads of 1 $\times$ 1 cm^2, giving a total of 24 million pads.

The TESLA design for 800 GeV: bunch crossing every 176 ns, with 4886 crossings in a bunch train. The bunch train length is 860 μs and the period is 250 ms, giving a duty factor of 0.35%.

Assuming 100 particles/mm^2, have 10 000 mip in a 1 $\times$ 1 cm^2 pad, so ADC dynamic range is 14 bits.

With 2 bytes per pad per sample, raw data per bunch train is 24 $\cdot$ 10^6 $\times$ 4886 $\times$ 2 = 250 GBytes, which is 0.3 – 2.5 MBytes/ASIC (assuming each ASIC processes 32 – 256 channels).

Within a bunch train, potential data rate is 0.4 – 3 GBytes/s.

Threshold suppression and/or buffering could reduce this rate. Calibration data will increase the rate.

DAQ system - areas of R&D

Connection from the VFE to FE

- **Readout of prototype VFE ASICs**
- **Study of data paths on 1.5 m PCB**

Connection from on- to off-detector

- **Connection from on-detector to off-detector receiver**
- **Transport of configuration, clock and control data**

Off-detector receiver

- **Prototype off-detector receiver**

Last three bullets part of EUDET work. Technical design can be independent of other CALICE developments, but links needed for prototype DAQ. Specific details of its design affects our DAQ system.

Readout of prototype VFE ASICs

Collaboration between IC, providing DAQ, and French groups, building ASICs.

Reading out development ASICs may be possible with current DAQ board and system - no significant hardware development needed for DAQ.

But significant firmware changes needed to current board.

Future ASIC designs - DAQ hardware development necessary.

Also help in understanding DAQ needed for prototype.

Study of data paths on 1.5 m PCB

Design issues for a full PCB:

- **Can a 1.5 m PCB be built - ask manufacturers.**
- **Is this more reliable, price competitive with stitching boards together.**
- **Use of copper or optical data paths:**
  - **Optical: faster, chip-to-chip becoming industry standard, connector sizes, light transmission and its power.**
  - **Copper: simpler, noise interference.**
- **Build a mock slab for tests of effects - provide input to final design.**
- **Bandwidth and cross-talk simulated using CAD tools and compared with measurements.**
- **One transmission line per chip or multi-drop.**

DAQ system - connection on- to off-detector

Assume off-detector receiver is (some largish number of) PCI cards in PCs.

Connection off detector and receiver itself are commercial components.

Two scenarios:

- **Threshold suppression done in FE (data rate $\sim$ 5 MBytes/s/slab) data transported via network switch.**

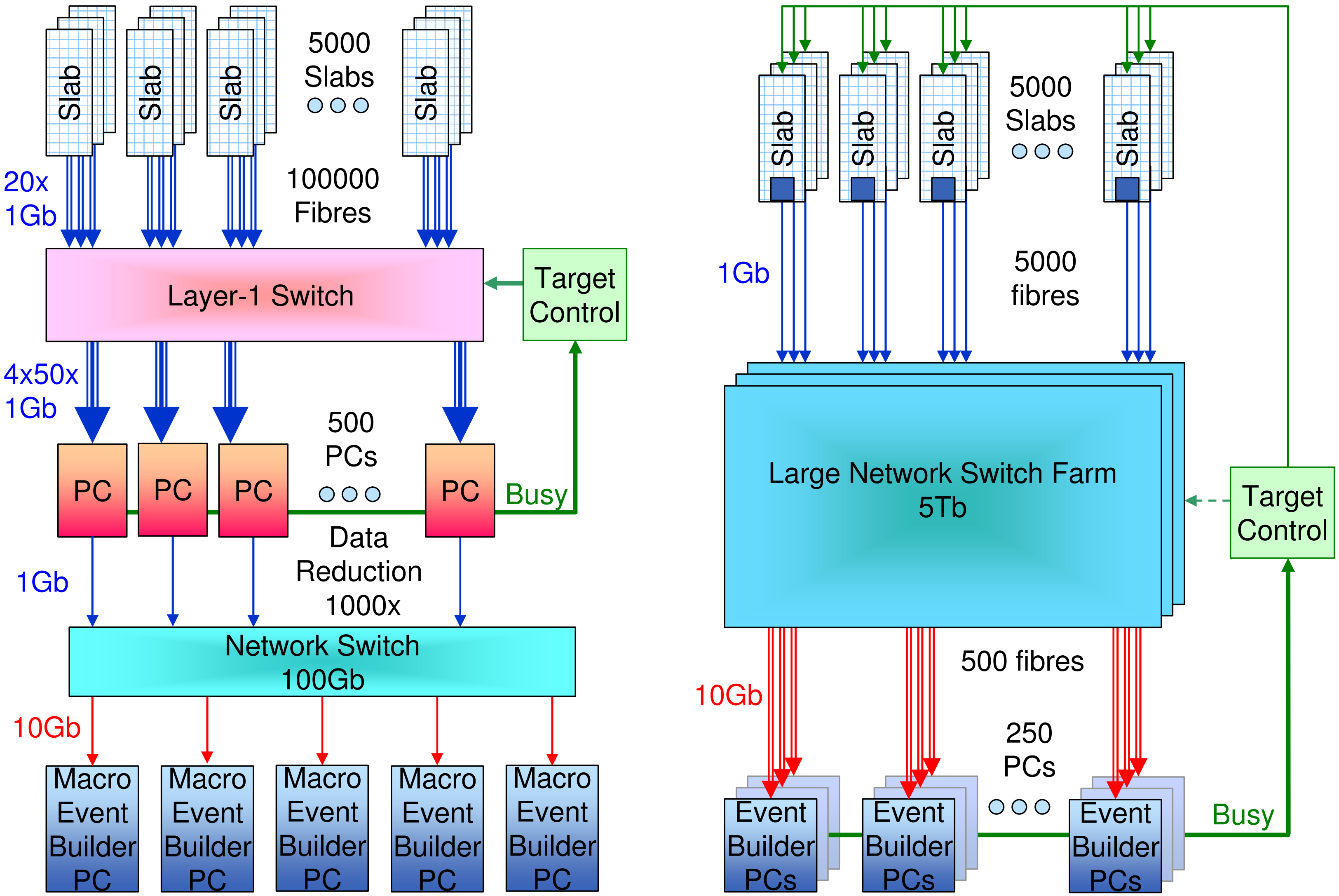
- **No FE, data directly from VFE (data rate $\sim$ 1 GBytes/s/ASIC) using optical fibre, via optical (“layer-1”) switch.**

First will work, but tests can be done. Second would need to be studied now.

FE inaccessible for long periods - need “failsafe” - able to reboot, reconfigure.

Understand clock and control and configuration of different commercial components in relation to accelerator clock.

DAQ system - connection on- to off-detector



Optical (Layer-1) Switching

Array of programmable mirrors - new technology

Programmable optical patch panel: grouping fibres from physical region

Stable and efficient router

- Change data destination per bunch-train
- Regulate load by sending data to free resources
- As PCs become busy or fail, data is directed to alternative (back-up)

Could be a solution even if data size and speed is drastically smaller than we cater for. Applicability elsewhere?

Size of arrays, switching speed, reliability, cost, manufacturers (e.g. Glimmerglass)

Off- to on-detector communication

All separate detector parts need synchronising and configuration signals

- **bunch-train start**
- **counter resets**
- **setup mode, thresholds, etc.**

DAQ system - Off-detector receiver

Receiver is system of PCI cards housed in PCs. Local clustering performed on PCI cards. (However, companies producing crates which are physically simpler to deal with.)

PCs can be unreliable, one may be busy - how good is switching between PCs?

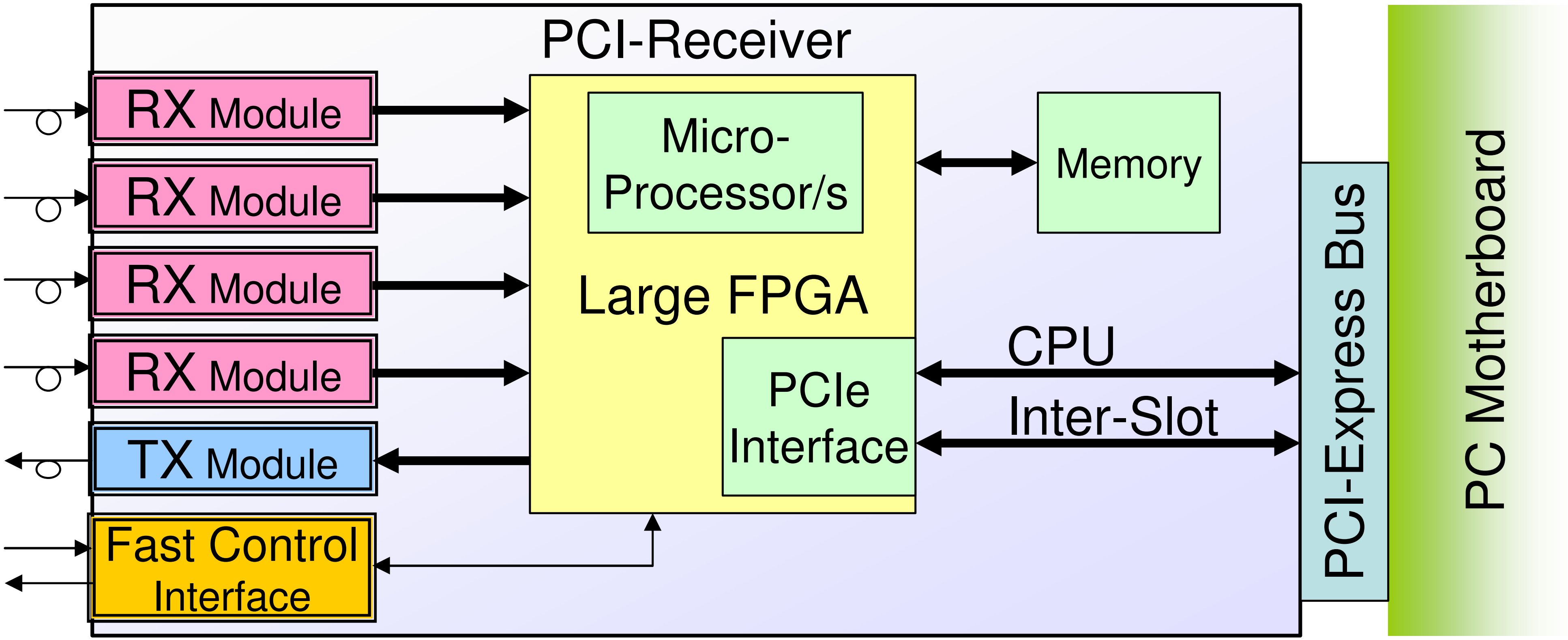
How much data (i.e. how much of calorimeter) can be sent to one PC?

How much data needs to be sent to PC for local clustering to be effective?

Design our own card for maximum flexibility

Use e.g. PCI express bus

DAQ system - Off-detector receiver



DAQ system - Off-detector receiver

Custom PCI-Express card designed to test:

- **data transfer standards/customisations**
- **Capabilities of PCI-Express**
- **Capabilities of FPGA to do data processing**
- **Use as Clock and Control source**

Rx/Tx module plug-in to allow card to be data source (for bench-tests)

What we want to achieve

Combination of test-bench verification and use for prototypes in test-beam

Flexible DAQ card which should be able to cope with foreseen rates and volume

Network systems which are tested and efficient

Can what we design be used elsewhere - generic systems useful for:

- **other sub-detectors at the ILC?**
- **another experiment?**
- **global DAQ system for ILC?**

Provide DAQ for prototype calorimeter (or calorimeters)

Prototype and EUDET project

What do we actually need to read-out:

- **ECAL prototype dimensions: 150$\times$12cm^2$\times$1 layer & 30$\times$12cm^2$\times$15 layers**
- **Cell size: 5$\times$5mm^2 $\Rightarrow$ $\mathcal{O}$(10^4) channels**
- **Number of channels per and functionality (suppression, buffering) of ASIC**
- **Functionality of data concentrator at end of module. FPGA just collecting or some data reduction, merging of ASIC data paths.**
- **Timing structure - presumably slow in some test-beam somewhere.**
- **Clock and config. provided by DAQ to FPGA and distributed to ASICs.**
- **Frequency of calibration data and scheme. All of module at same time.**
- **Similar issues (size and rate) for HCAL.**

Plans

Gain experience of reading out development ASICs

Understand transmission and data paths along large PCBs

Build and test prototype DAQ card (iterations)

Build and test prototype DAQ system

Capabilities of our system - rate, volume, efficiency, applicability, cost

Full compatibility with prototype calorimeters