Front-End Electronics Design and Construction

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LPNHE Paris

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Beam tests session

Front-End Electronics Design

Keep intrinsic detector performance

300 mm thick Silicon strip detector

- Charge: 25000 e-/1000e- = 25
  - Position ⊥ to a few μm
- Time:
  - BC Tagging
  - Position O(1) ns (Talk by Jacques David)
    ~ 1cm resolution //

Noise and Power

Noise

Source	Value	Noise
Input stage	g_m=0.69mA/V	1065 e-
Detector leak	10 nA	588 e-
Biasing resistors	10 MΩ	423 e-
Total		1288 e-

Foreseen detector noise contributions at 30 pF detector capacitance and 3 μs shaping time in 130nm CMOS technology

Power

- **Preamp + Shaper + Sparsifier**

Preamp: 70 μW Shaper: 160 μW Sparsifier: 50 μW
Sampling: 100 - 200 μW

- **ADC**

ADC: 110 μW

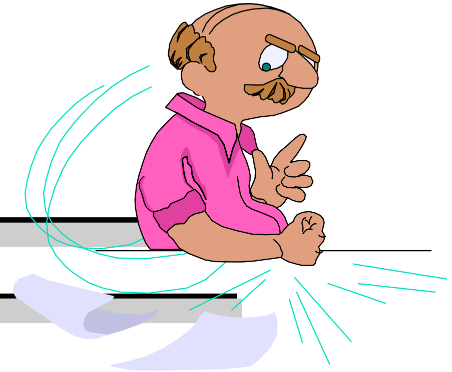
Total: 500 – 600 mW/channel Power cycling : save 99%

Front-End Electronics Design

Guidelines

As compact as possible:

- Transparency
- Less passive parasitics: better S/N
- In principle simpler...



Patrick Le Du (Saclay): Summary of current thinking

{ The ILC environment poses new challenges & opportunities which will need new technical advances in Data Collection

→ **NOT LEP/SLD, NOT LHC !**

- The FEE integrates everything
  - →From signal processing & digitizer to the RO BUFFER …
- Very large number of channels to manage (Trakers & ECal)
- Interface and feedback between detector and machine is fundamental
  - →optimize the luminosity → consequence on the DAQ architecture
- Classical boundaries are moving : Slow control, On/Off line … }

Front-End Electronics Components

Front-end Analog:

- Integrate 512-1024 channels in 130nm CMOS:

  amplifiers
  shapers — two time scales wrt strip length
  samplers — 8 samples over two peaking times
  ADC
  Power switching

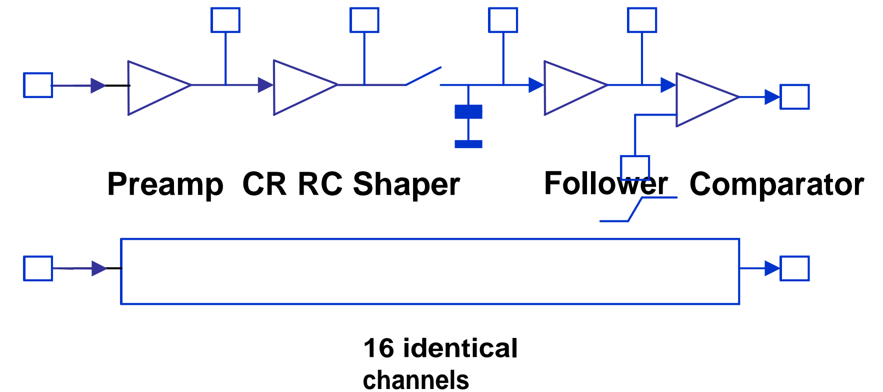
- Presently measured in 180nm CMOS

  amplifiers: 500 + 16 e-/pF
  shapers: 375 + 10.5 e-/pF

Paris Front-end 1st Prototype Chip

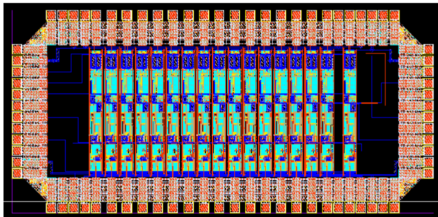
(Thanh Hung Pham's talk)

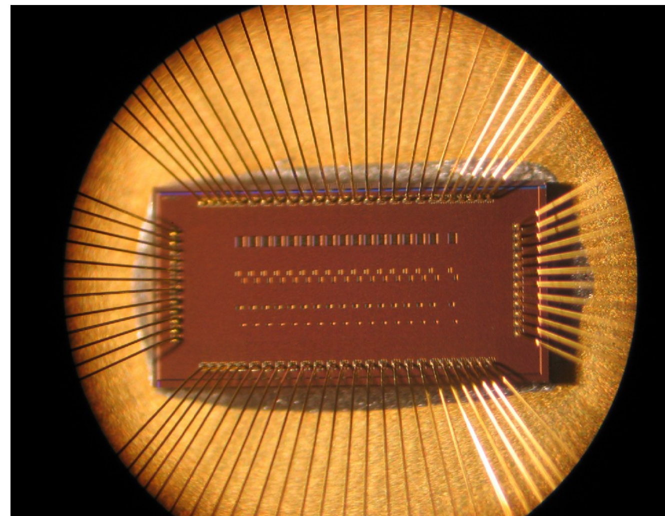
- Low noise amplification + pulse shaping
- Pulse sampling
- Threshold detection
- Power dissipation less than 500 μW/c

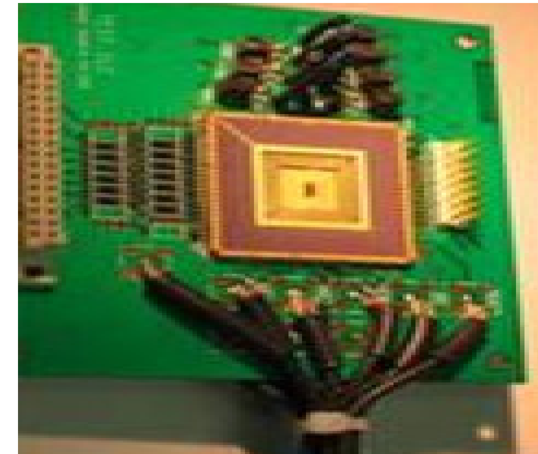


Technology: CMOS 180 nm

Successfully checked.







3mm

Next design in progress CMOS 130 nm

Front-End Electronics Components

Front-End Digital

- Buffer memory
- Processing for
  - Calibrations
  - Amplitude and time least squares estimation, centroids ?

  or/and - Raw data after zero suppression lossless compression
- Tools
  - Digital libraries in 130nm CMOS available
  - Synthesis from VHDL/ Verilog
  - SRAM memory
  - PLLs

Front-End Electronics

Passive

- Capacitors:

  Large values: Decouplings

- Cables:

  Signals: Fiber optics
  Power: Copper

Grounding & Shielding

- Signal is refered to the backplane

  AC stick preamp ground and DC supplies to this voltage
  using (large) decoupling capacitors

- Shield all detector from external interferences using a thin
  aluminum foil wrapped around the cqrbon fiber support structure

- Digital I/Os

  Use fiber optics:

  - Trains stage: 3-6 MHz BCO synchronous controls
  - Digitization stage: 100 MHz ADC clock
  - Transfer stage: >1 GHz fiber serial clock

Detector coupling

- DC coupling

  Cheaper detector process but:

  - DC current flowing through preamp may induce pedestals reduce dynamic range, saturations

  OK using synchronous reset and **sampling**

- AC coupling

  Needs an on-detector oxide layer

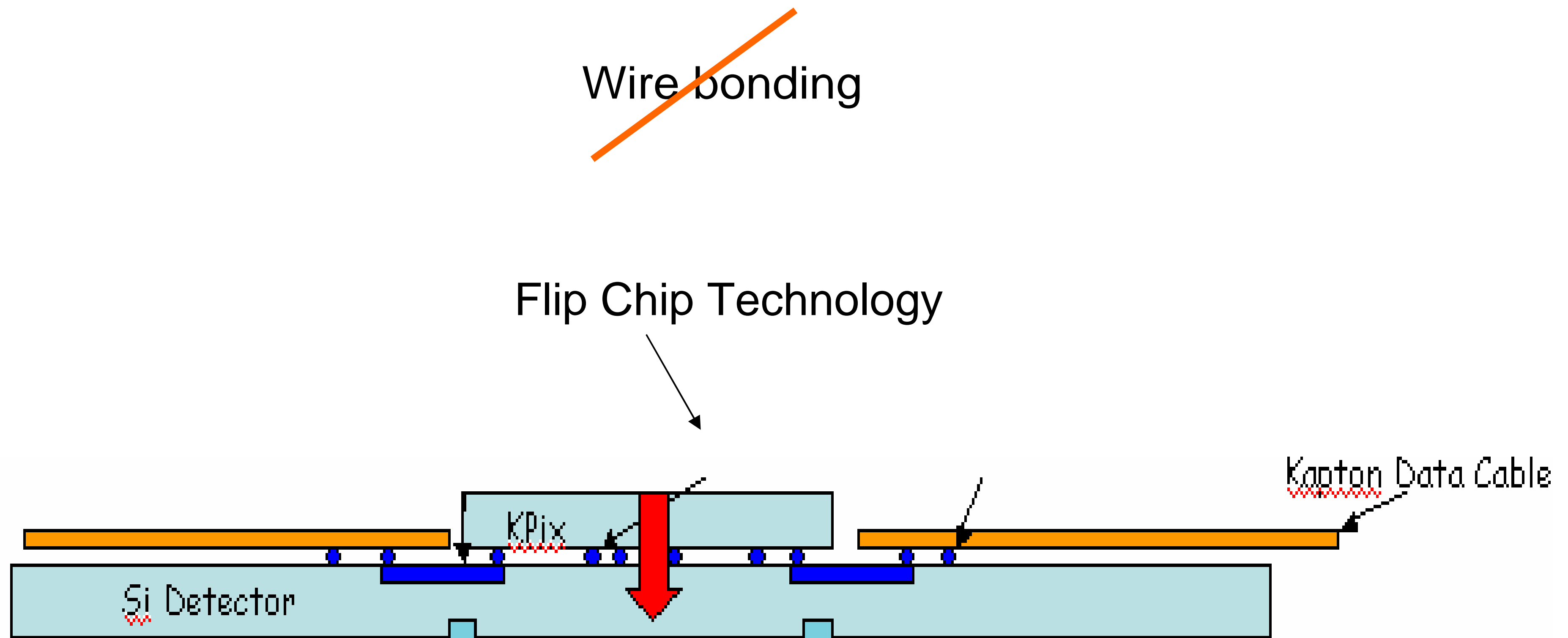
  - No preamp reset needed, but 1/f noise to be removed

  OK with **sampling**

  - Caveat: oxide pin-holes may short detector to FE chip

Conclusion: The present front-end electronics can manage both solutions, so go to the safest and cheapest !

Wiring Detector to FE Chips technology

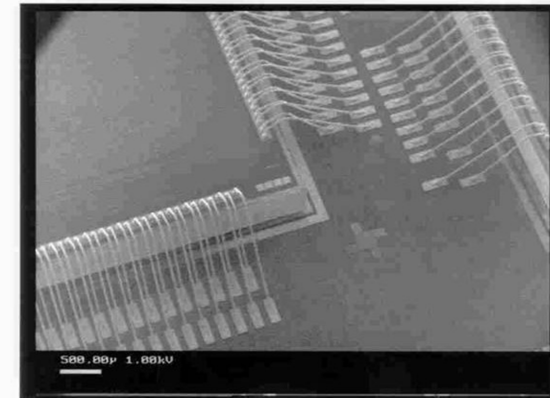


Courtesy: Marty Breidenbach (Cal SiD)

Manuel Lozano (CNM Barcelona)

Chip connection

- Wire bonding
  - Only periphery of chip available for IO connections
  - Mechanical bonding of one pin at a time (sequential)
  - Cooling from back of chip
  - High inductance (~1nH)
  - Mechanical breakage risk (i.e. CMS, CDF)
- Flip-chip
  - Whole chip area available for IO connections
  - Automatic alignment
  - One step process (parallel)
  - Cooling via balls (front) and back if required
  - Thermal matching between chip and substrate required
  - Low inductance (~0.1nH)



Manuel Lozano (CNM Barcelona)

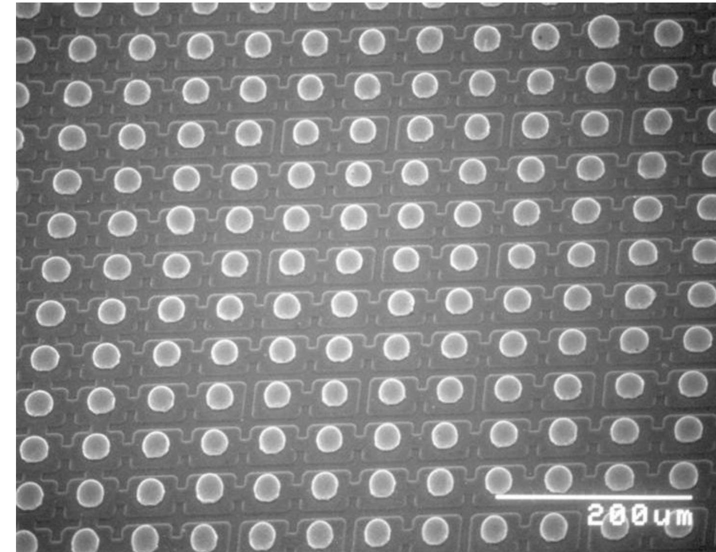
Bump bonding flip chip technology

- Electrical connection of chip to substrate or chip to chip face to face

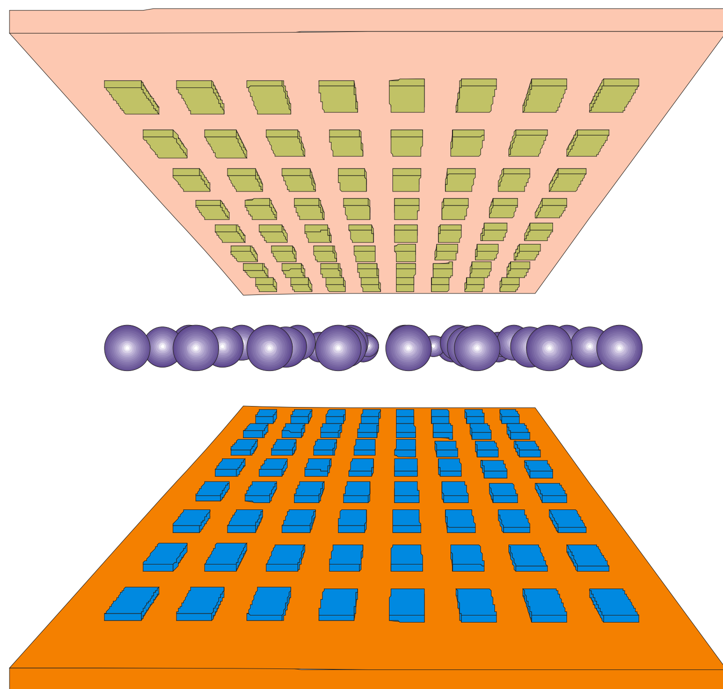
  flip chip

- Use of small metal bumps

  bump bonding



CNM



- Process steps:
  - Pad metal conditioning:
    Under Bump Metallisation (UBM)
  - Bump growing in one or two of the elements
  - Flip chip and alignment
  - Reflow
  - Optionally underfilling

Manuel Lozano (CNM Barcelona)

Bump bonding flip chip technology

- Expensive technology
  - Especially for small quantities (as in HEP)
  - Big overhead of NRE costs
- Minimal pitch reported: 18 µm but ...
- Few commercial companies for fine pitch applications (< 75 µm)

- Bumping technologies
  - Evaporation through metallic mask
  - Evaporation with thick photoresist
  - Screen printing
  - Stud bumping (SBB)
  - Electroplating
  - Electroless plating
  - Conductive Polymer Bumps
  - Indium evaporation

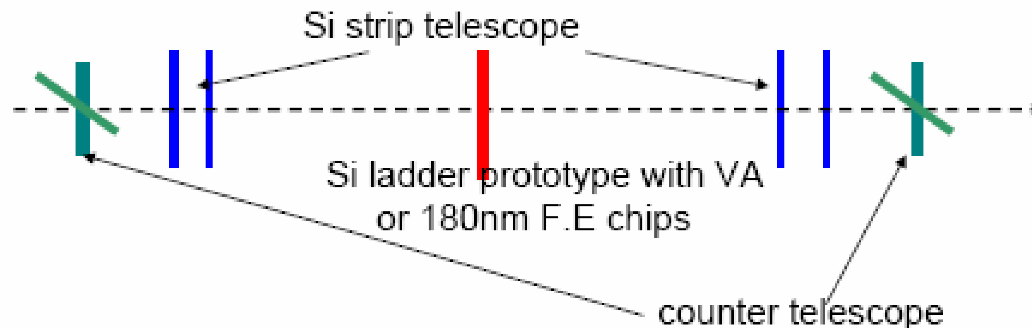
Beam-tests

At 5 Gev e- beam in DESY, no B

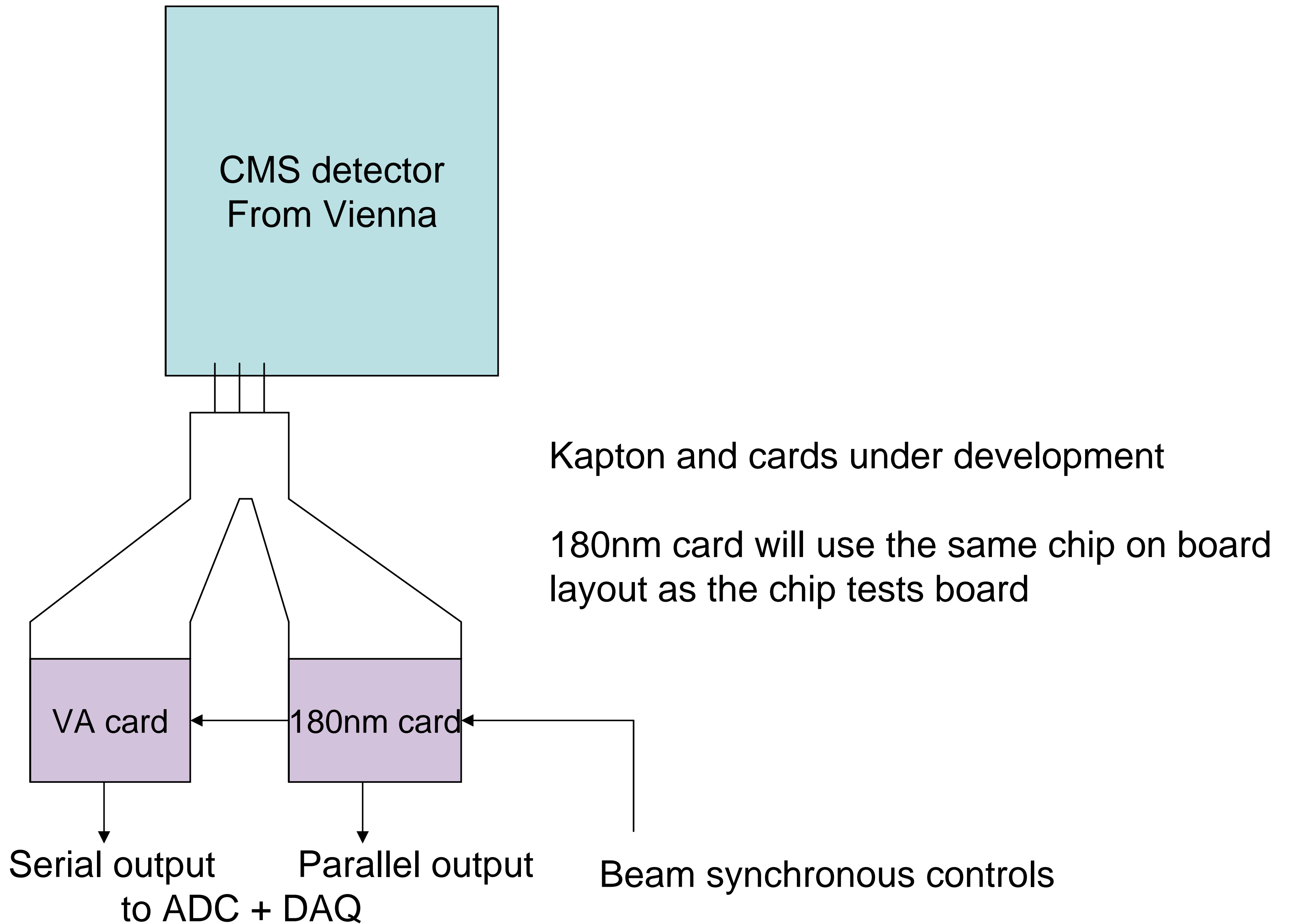
Very simple telescope set-up in Silicon strips (2 ladders of CMS strips, one read out with VA1 FE and the other one with a few channels read out with present version of new FE chip), together with a reference telescope;

Purposes:

- To check S/N for the long strip first proto measured at Lab test bench
- To characterize performances of the new FE chip in realistic conditions after doing it at Lab test bench and comparing with ref FE electronics (VA1)



Tests Hardware



Kapton and cards under development

180nm card will use the same chip on board layout as the chip tests board

Tests Software

Standard VME ?

PC + USB ?

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