SiW Ecal in AIDA2020 and HIGHTEC

Roman Pöschl

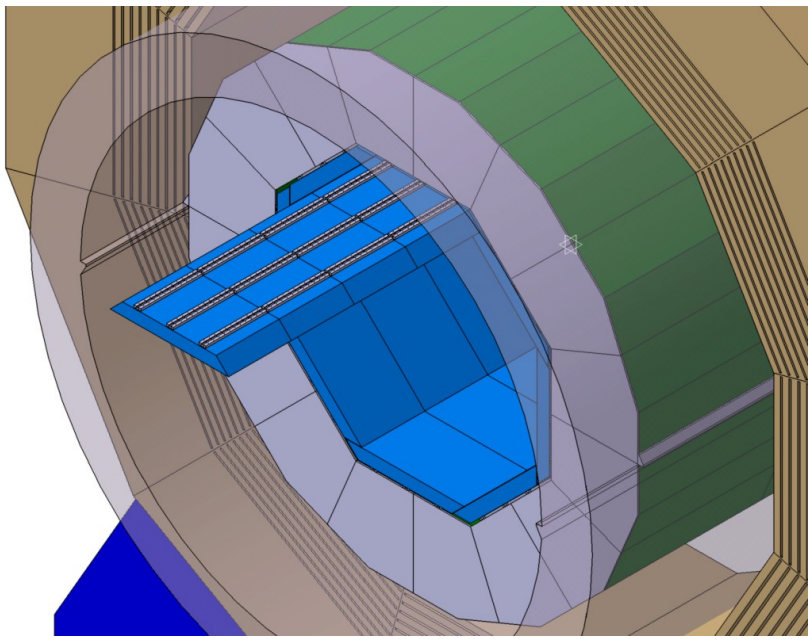
CALICE Collaboration Meeting Arlington/TX – March 2016

SiW ECAL for a future LC

- SiW ECAL is baseline for future LC detectors

  ➡ Optimized for Particle Flow Algorithm:

Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

Basic Requirements:

- Extreme high granularity
- Compact and hermetic (inside magnetic coil)

Basic Choices:

- Tungsten as absorber material

  X_0=3.5mm, R_M=9mm, Θ_T=96mm

  Narrow showers

  Assures compact design

- Silicon as active material

  Support compact design

  Allows for pixelisation

  Robust technology

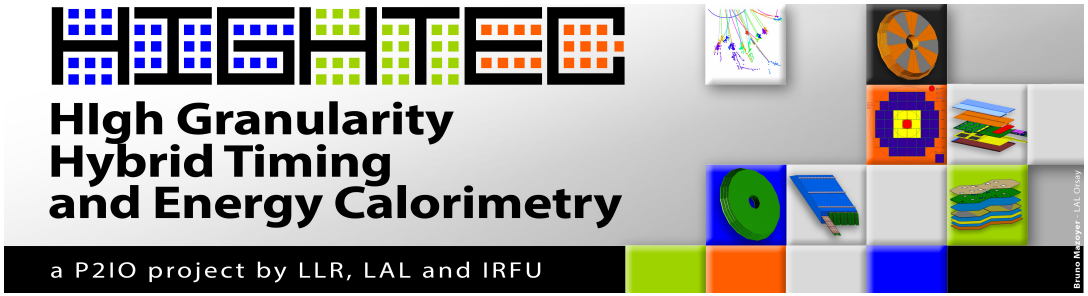
  Excellent signal/noise ratio: ~10

Introduction

- Until ~2020 SiWEcal (in France) will benefit from two approved projects

AIDA 2020

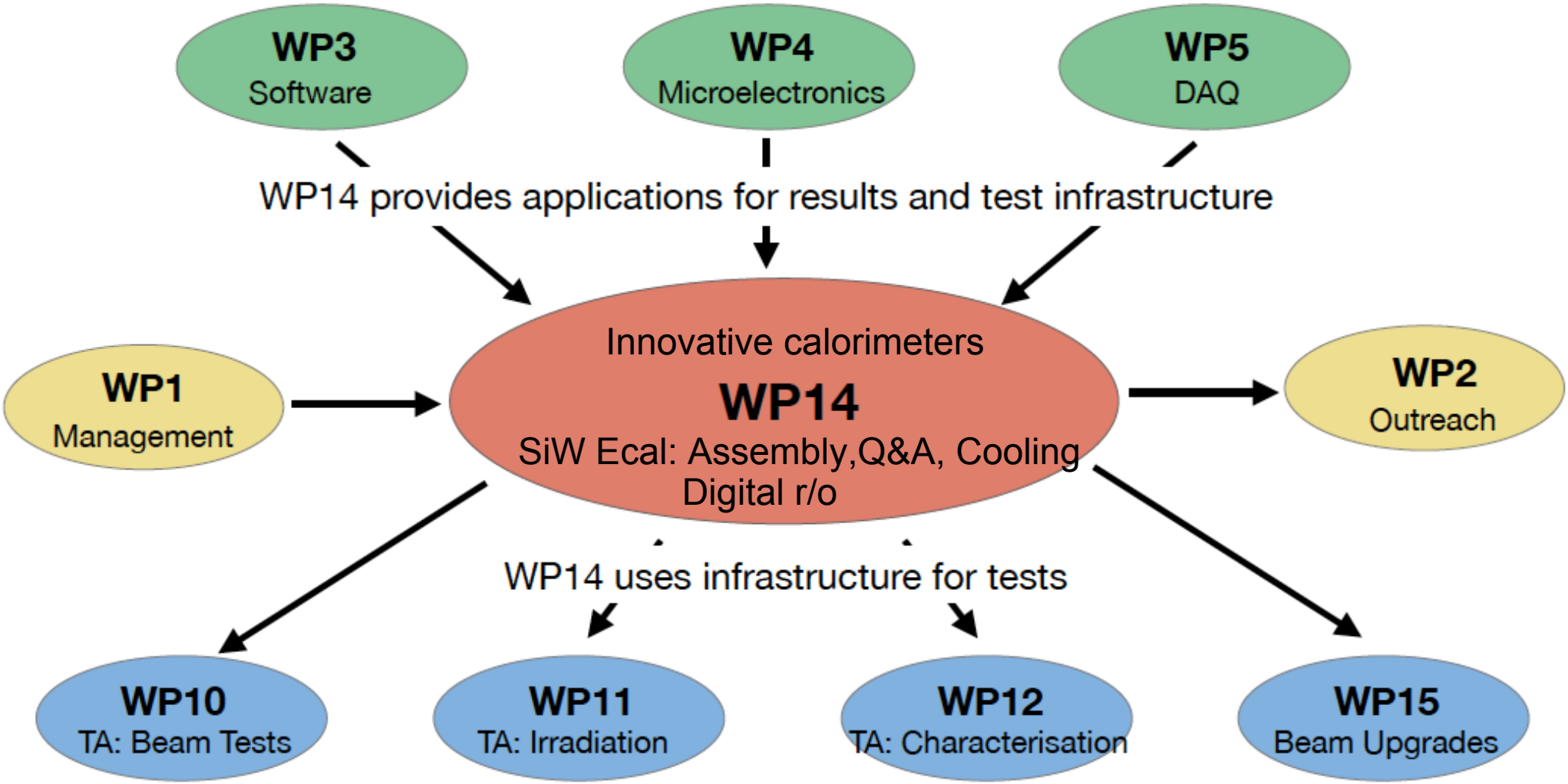
Horizon2020 European Research Infrastructure
SiW Ecal Beneficiaries: LAL, LLR, LPNHE, LPSC, OMEGA
Materiel, HR, Travel



Ile de France South Excellence
Cluster P2IO
SiW Ecal Beneficiaries:
LAL, LLR
Material, HR, Travel

Support from overarching bodies like IN2P3 and Ecole Polytechnique is herewith explicitly acknowledged as well

AIDA2020 Workpackages



First (SiW Ecal) Milestone

AIDA-2020-MS14

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

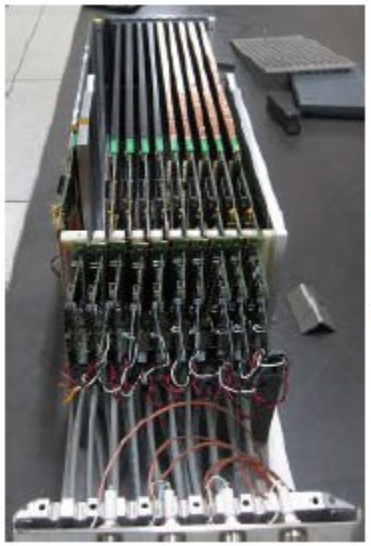
Milestone Report

Assembly and QA chain demonstration for highly granular silicon calorimeters

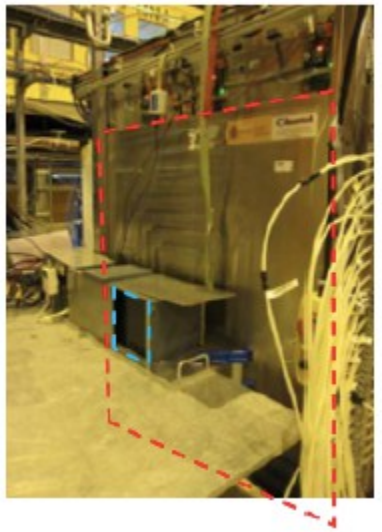
Boudry, V. (CNRS) *et al*

23 June 2016

The AIDA-2020 Advanced European Infrastructures for Detectors at Accelerators project has received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.



R. Cornat



Important validation of procedures

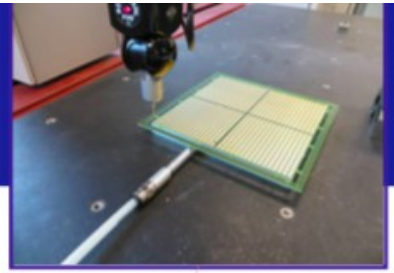
(Combined) beam test in june 2016

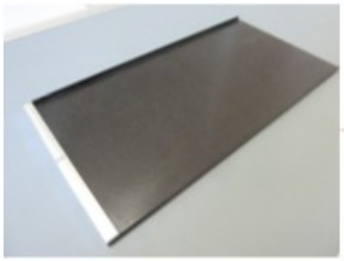
... to be continued in 2017

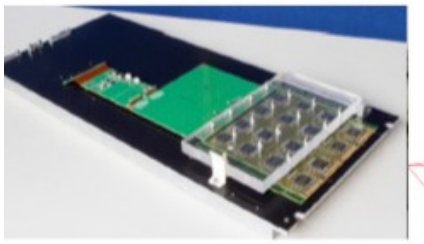
Assembly chain - Overview

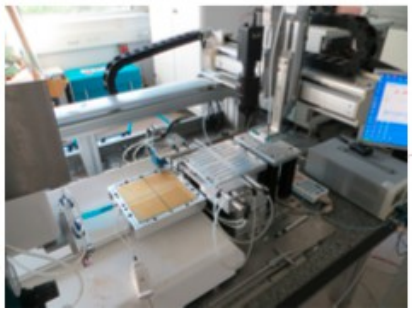
Full assembly chain

resp: R. Cornat

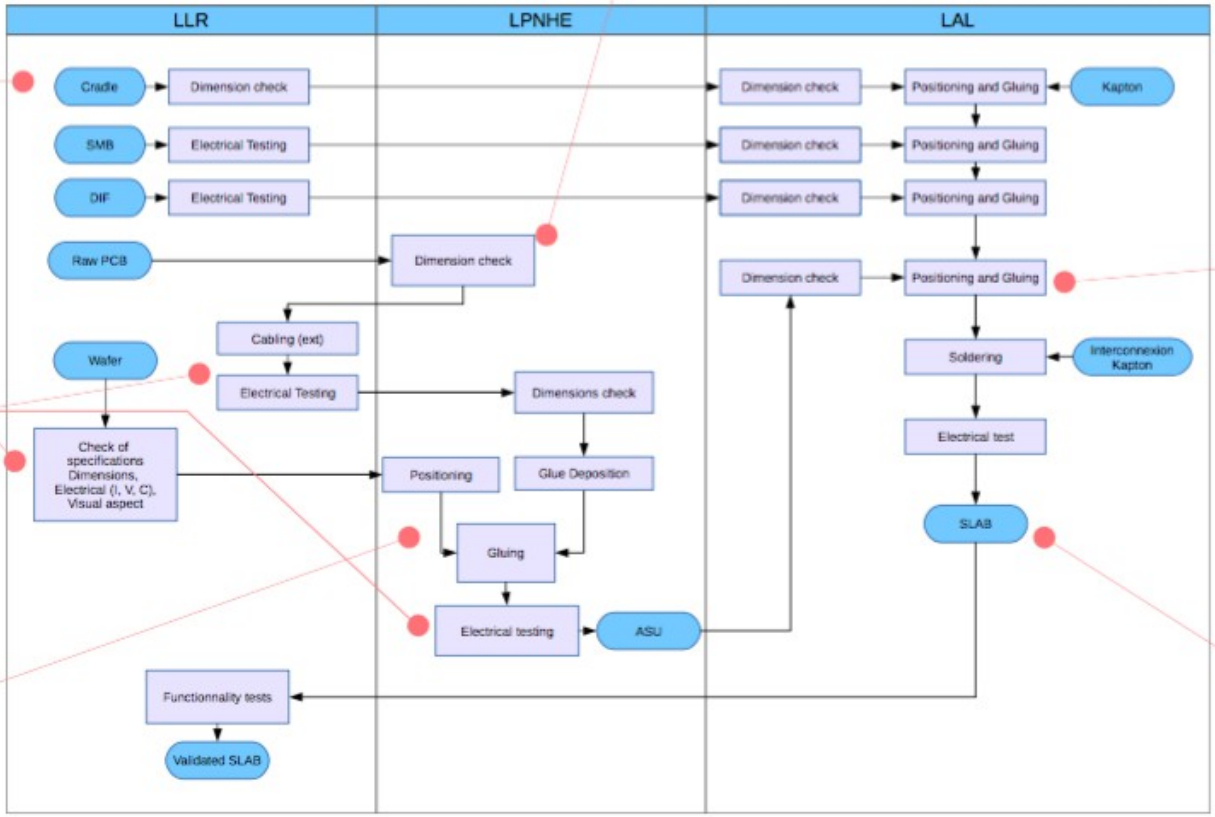


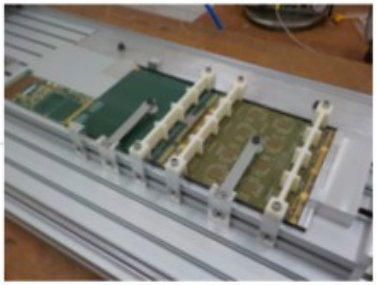


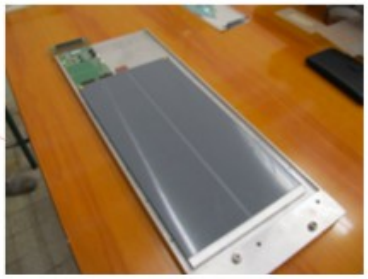




'Simplified view'







V. Boudry, ECFA Workshop 2016

Next Milestone relevant for SiW Ecal

Grant Agreement No: 654168

AIDA-2020

Advanced European Infrastructures for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDA-2020

MILESTONE REPORT

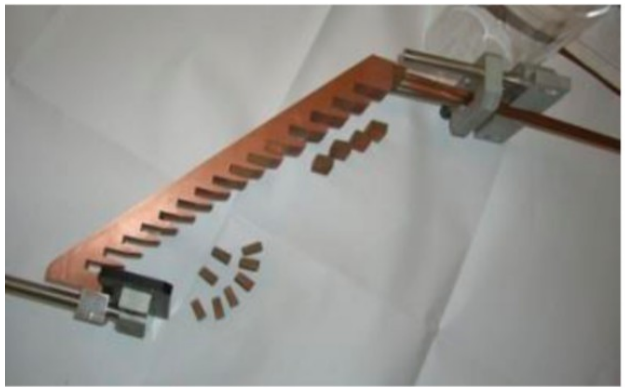
DESIGN OF COOLING SYSTEMS FOR TUNGSTEN / CARBON FIBRE AND FOR HADRON CALORIMETER STRUCTURES

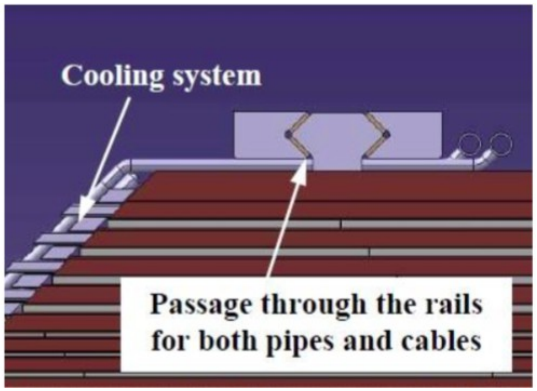
MILESTONE: MS31

Document identifier:	AIDA2020-MS31
Due date of deliverable:	End of Month 18 (October 2016)
Report release date:	Dd/09/2016
Work package:	WP14: Infrastructure for advanced calorimeters
Lead beneficiary:	DESY
Document status:	Draft

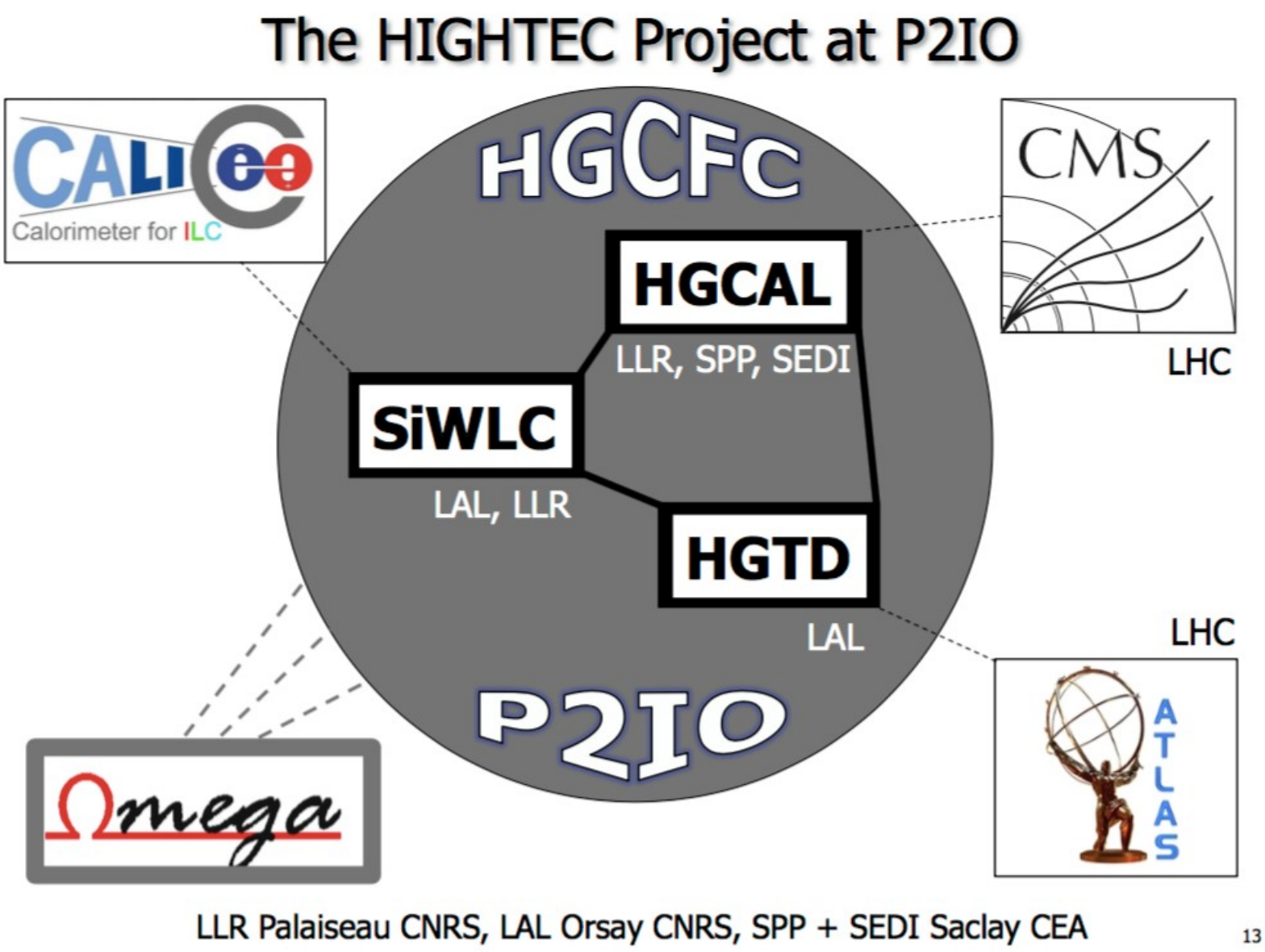
Abstract:

The front-end electronics for both highly granular silicon-based electromagnetic and hadronic calorimeters requires a highly integrated and efficient cooling. Thermal properties of tungsten and carbon fibre based absorber elements drive the cooling concepts of electromagnetic calorimeters; it is the same with the properties of steel absorber stack for hadronic calorimeters. The feasibility and the development of a large leak less water cooling system has been successfully demonstrated for low power calorimeter readout electronics. Thermal modelling and measurements performed on demonstrators constructed within the EUDET project and distributed between two participating labs, fulfil the thermal requirements.





See talk by Denis Grondin


The HIGHTEC Project at P2IO
CALICE
Calorimeter for ILC
HGCFC
HGCAL
LLR, SPP, SEDI
SiWLC
LAL, LLR
HGTD
LAL
P2IO
CMS
LHC
LHC
ATLAS
Omega
LLR Palaiseau CNRS, LAL Orsay CNRS, SPP + SEDI Saclay CEA
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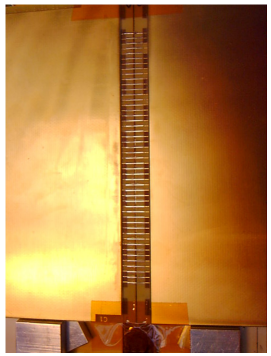
SiW ECAL – Long layer

A layer is composed of several short ASUs:

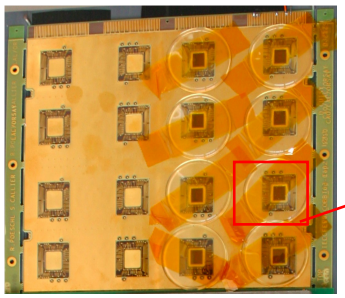
- A.S.U. : Active Sensors Units
- Similar layout for HGTD Task (> later)

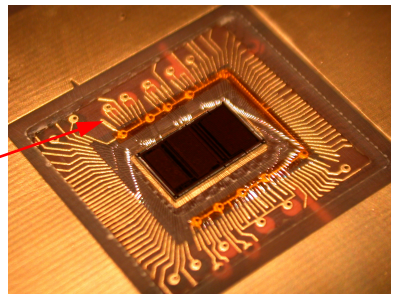


Interconnection with Flat flexible cable

ASIC+PCB+SiWafer =ASU

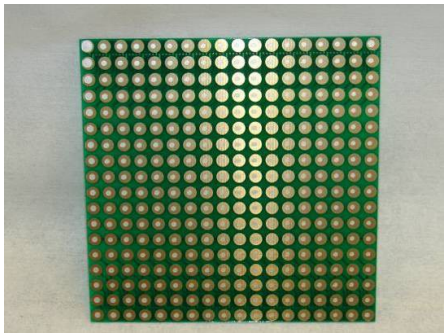
Wire Bonding or BGA





PCB is glued onto SiWafers

using a gluing robot



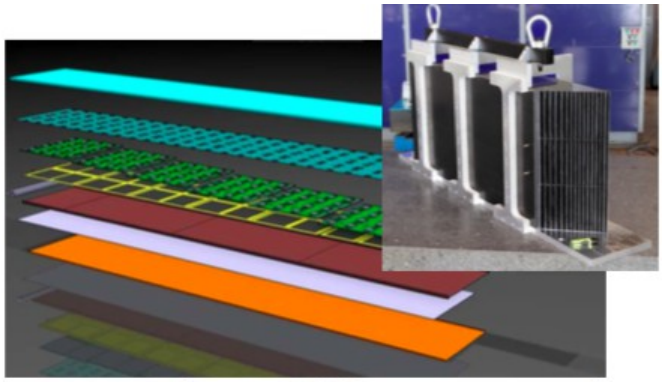
Some key numbers:
~10000 readout pads
~10000 interconnections
Current peaks >10 A for 2ms
Reliable signal propagation to be assured
Further details in backup

Successful realisation of a long layer is maybe one of the most challenging R&D projects in worldwide detector R&D

Long slab – More technical details

In principle, front-end boards will be chained forming up to 2m long detector SLAB, most of signals in bus

Issue 1 : clock distribution (5 & 50 MHz)
Interconnects are not impedance controlled (FFC)
One clock line may be loaded by 40 to 80 ASICS



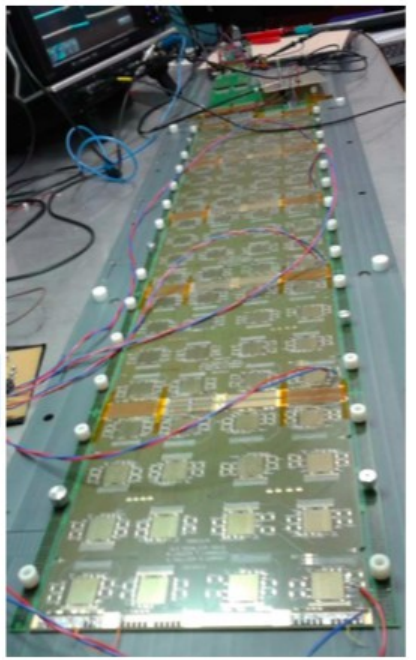
large C-W structure exists

⇨ Use of MLVDS adapted with 100 Ω on both sides, 100 mVpp remaining signal at the end
(6 Ohms loss/board, 20-40 pF/board, up to 10 boards)
⇨ Next version ASIC will have a PLL generating the highest frequency

Issue 2 : Power distribution (12 A pulses) & blocking capacitors (tested with FET switches as loads)

⇨ Current taken from a 800mF super cap (16mΩ ESR) + 2mF/board

Along 6 boards, static loss is 250 mV due to connectors (w/o chips).
May foresee to distribute power in a star topology.
4 boards SLAB being assembled at LAL



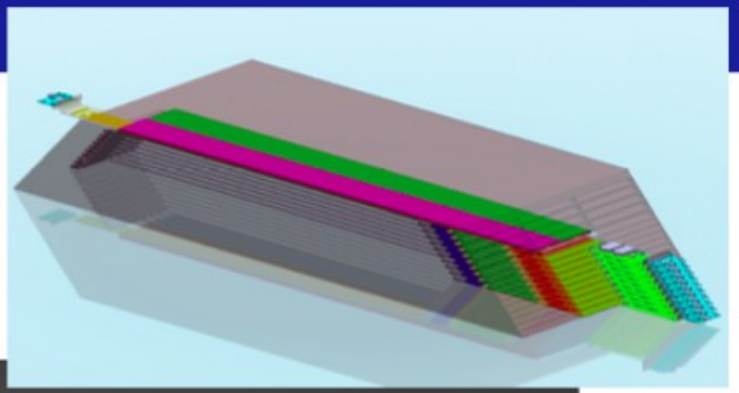
R. Cornat LLR

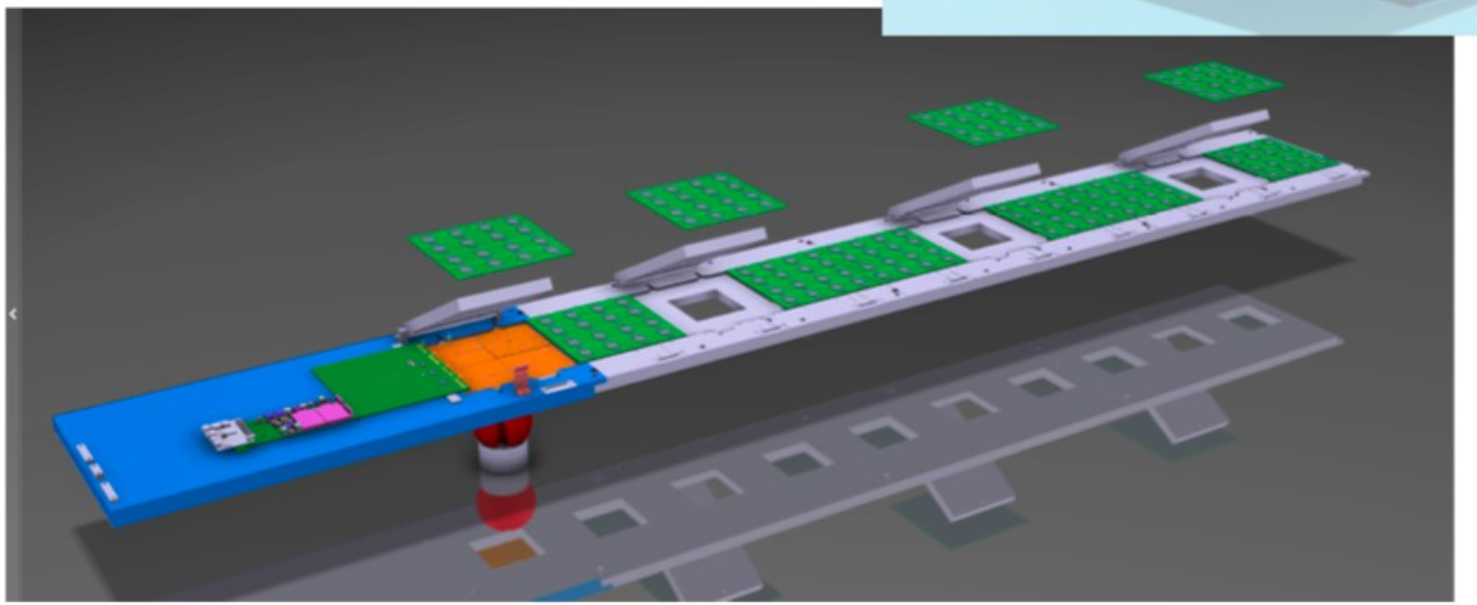
Long slab – Test bench?

Test of HW: long slab

8–10 ASUs stitched in Power-Pulsing

- what can't be done with a small RA source ?
- perf in strong B field, with PP.



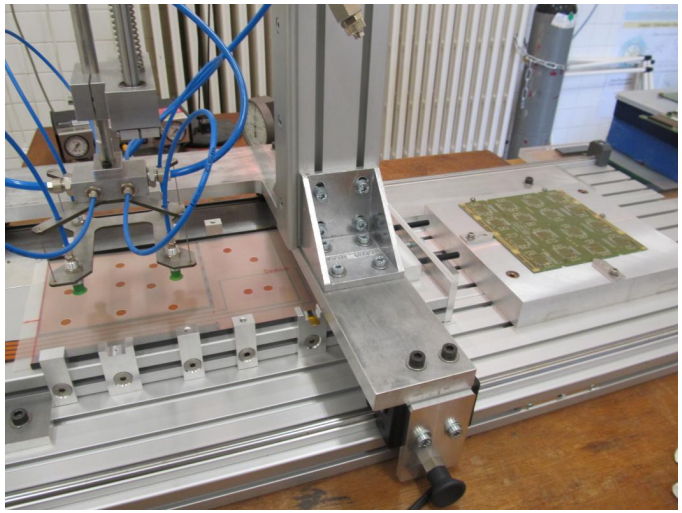


V. Boudry, ECFA Workshop 2016

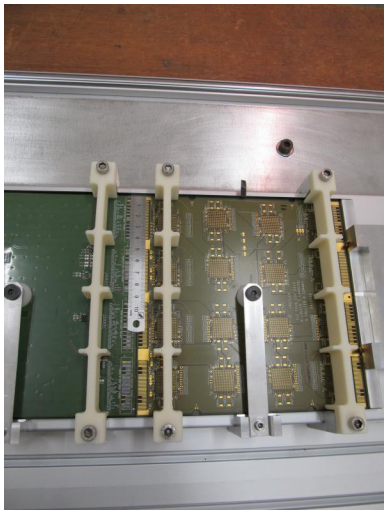
Assembly of SiW Ecal layers

SiW ECAL Assembly

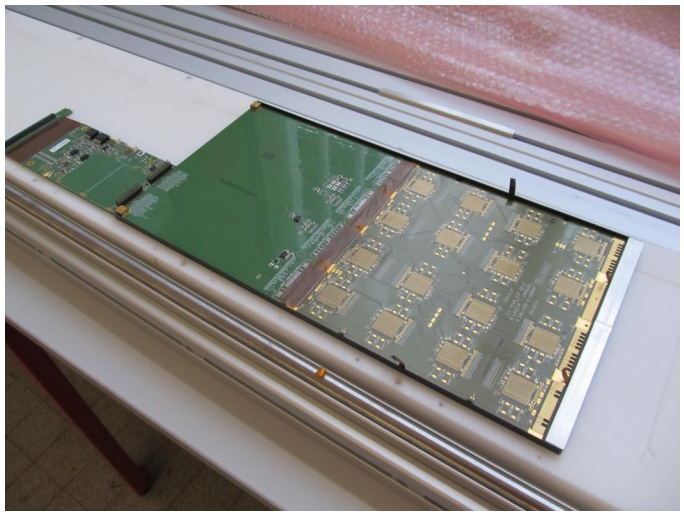
Pick and place



Precise alignment



Ready for test



- Assembly steps are validated with short layers

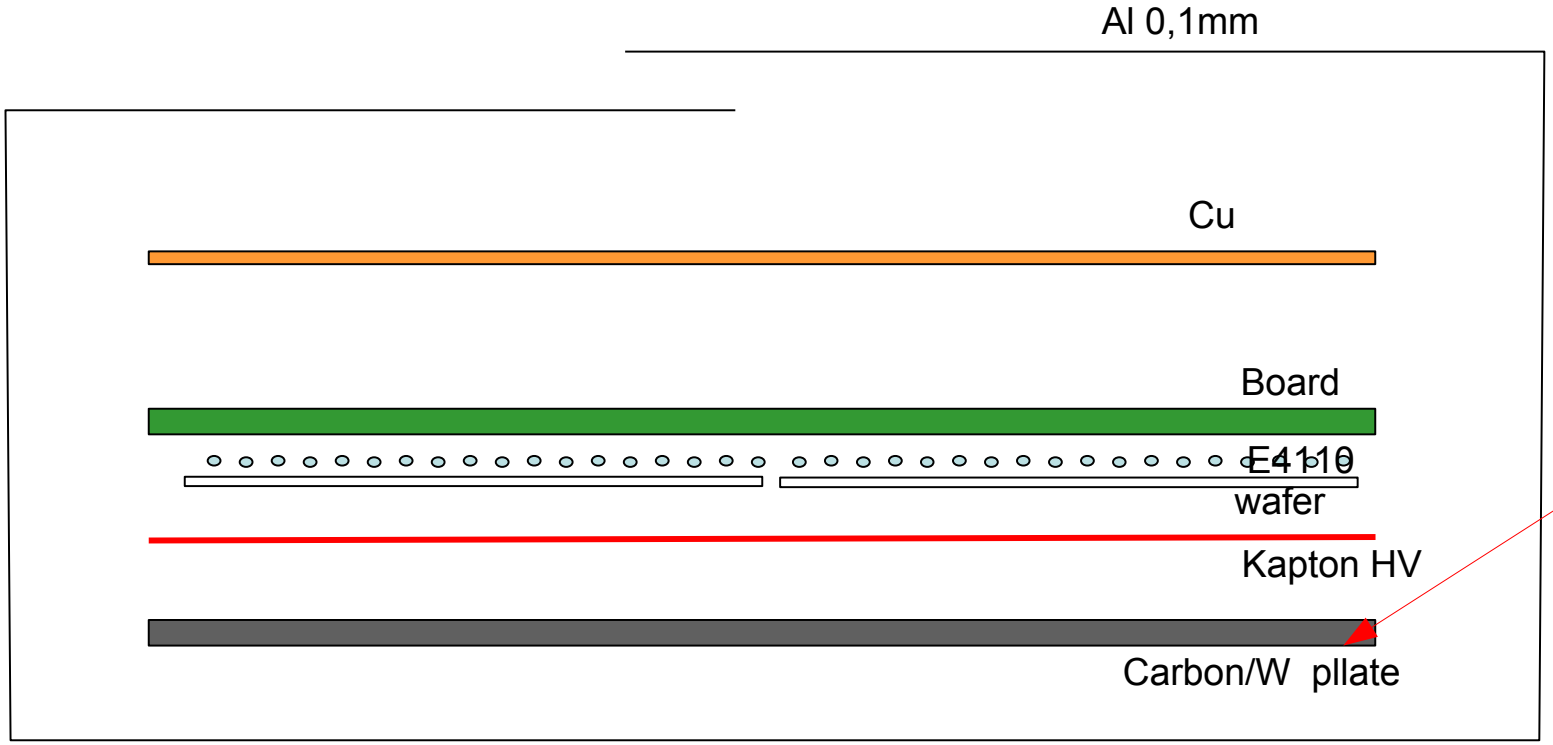
- Need big step towards long layer to assure high quality product
  - Automated pick-and-place and alignment
  - Interplay of many different working steps
    a) Assembly proper
    b) Continuous control of up to 8 ASUs during assembly

- Successful product requires a lot of testing and exercising of well trained technical staff!!!

- Strong synergy with HGTD Task and CMS Task (?)

SiW ECAL Assembly – Preliminary considerations

Guiding lines :
Ease of assembly
Easetofabricate the elements
Robustness
Compactness



J. Bonis/A. Thiebault

PCB R&D

Two major options:

BGA packaged chips

BGA version is considered as save incremental step:

test of chips before soldering ;

Space for external decoupling capacitors

Symmetric stacking will improve flatness,

good for wafer gluing

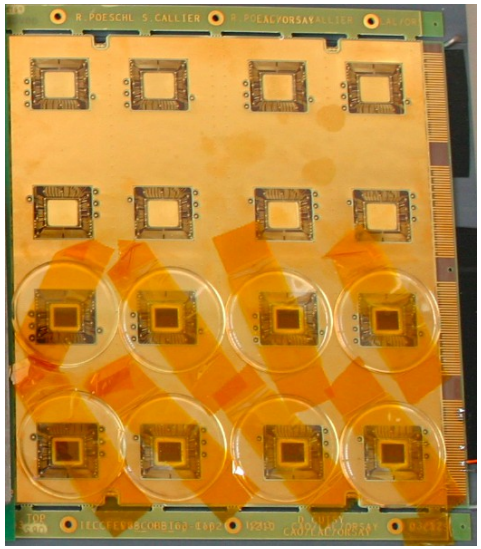
Optimal shielding of signal traces

Solution for current beam tests

May need revision to facilitate assembly process

Heat loss during interconnection

PCB with naked die

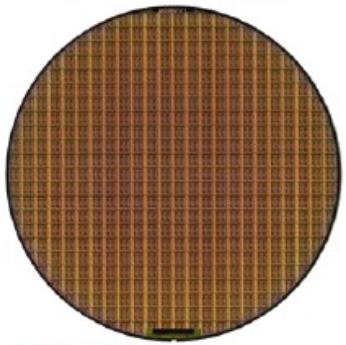


- Thin board (~1.2mm)
  => maximal channel density
- Tests since 2015
  Integration into ECAL prototype during HGCFC project
  => Intensive test programme
  e.g. Noise and cross talk

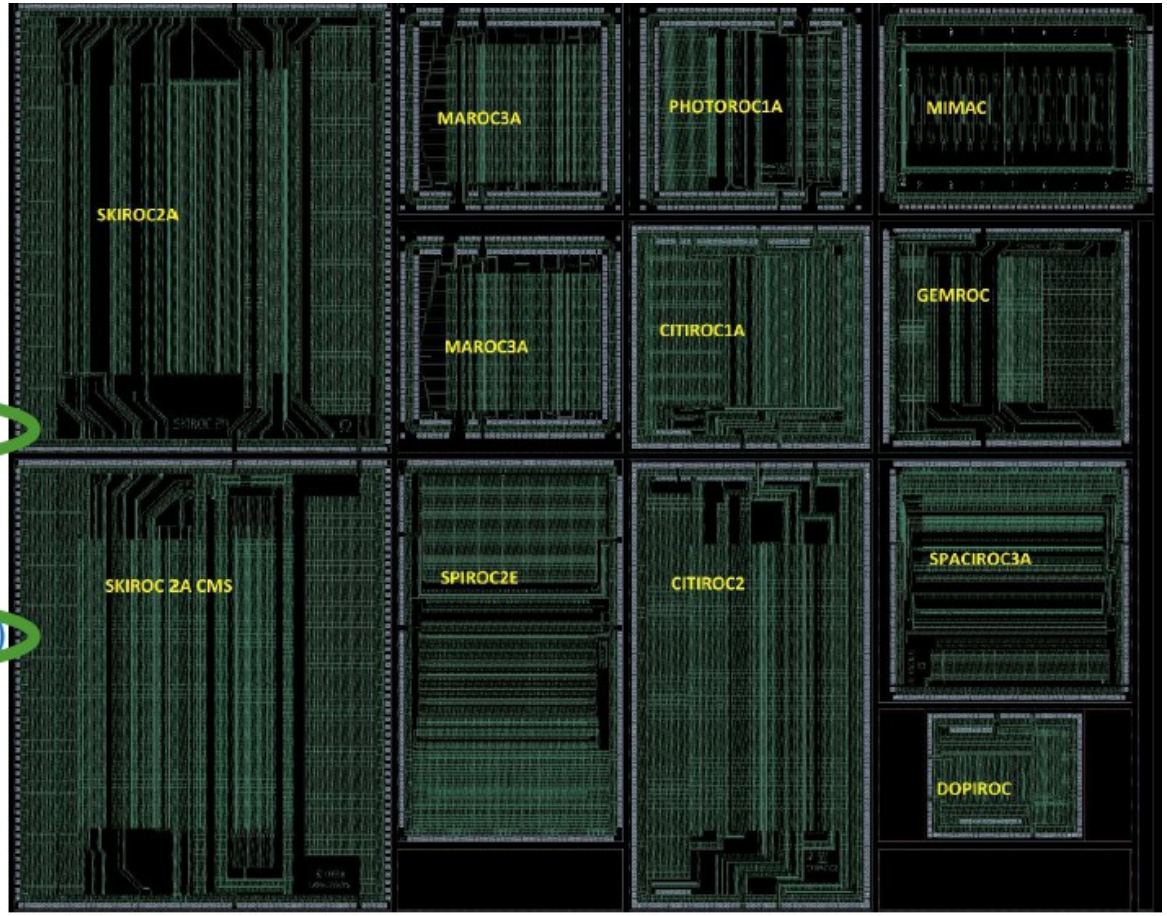
Details see previous talk

ASICS

- CITIROC1A
- CITIROC2
- DOPIROC
- GEMROC
- MAROC3A
- PHOTOROC1A
- SKIROC2A (PIN)
- SKIROC2-CMS
- SPACIROC3A
- SPIROC2E (SiPM)
- 1 other chip



http://omega.in2p3.fr



Schedule : Chips expected for middle of May 2016

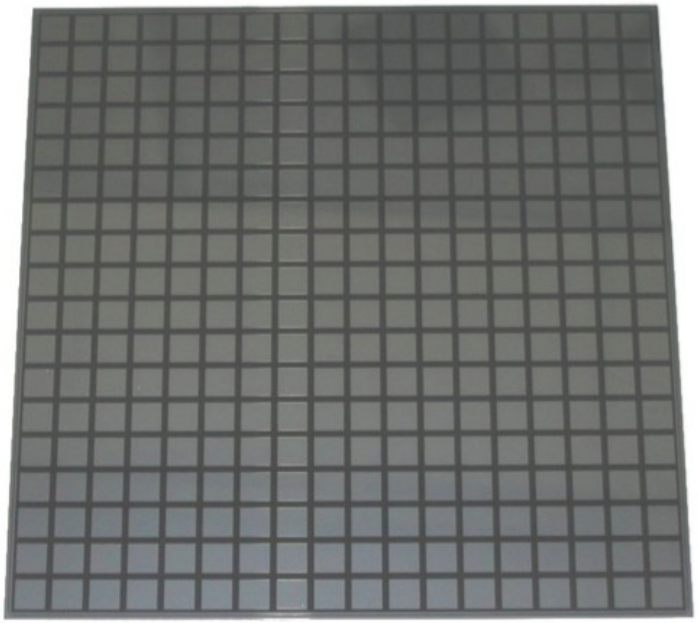
Dicing and packaging : June 2016

callier@omega.in2p3.fr

2

Details see electronics session this morning

SiW Wafer R&D



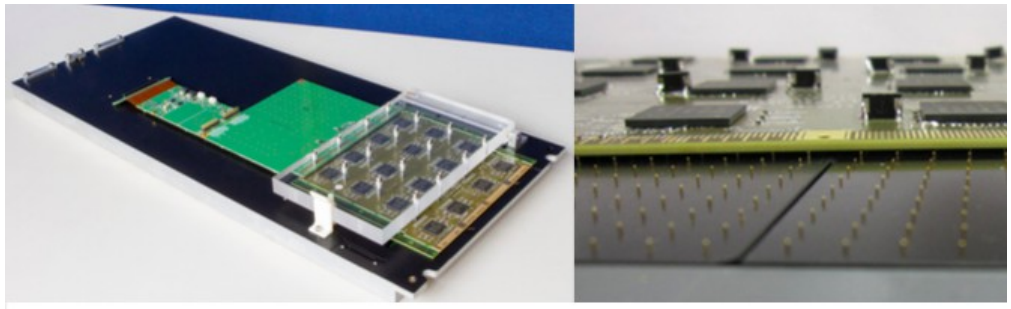
High resistive Si Wafer from Hamamatsu Photonics

- Excellent quality!!!
  e.g. leakage current O(nA/pixel)

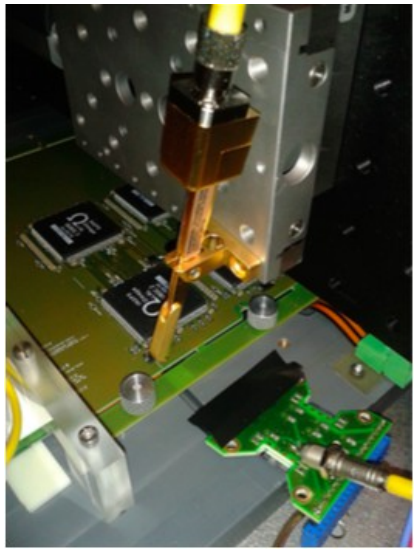
- However, expensive (2kEUR/wafer) and
  Large quantity needed requires quest for
  Further producers e.g. LFoundry

SiW Wafer tests:

Desktop setup with unglued sensors

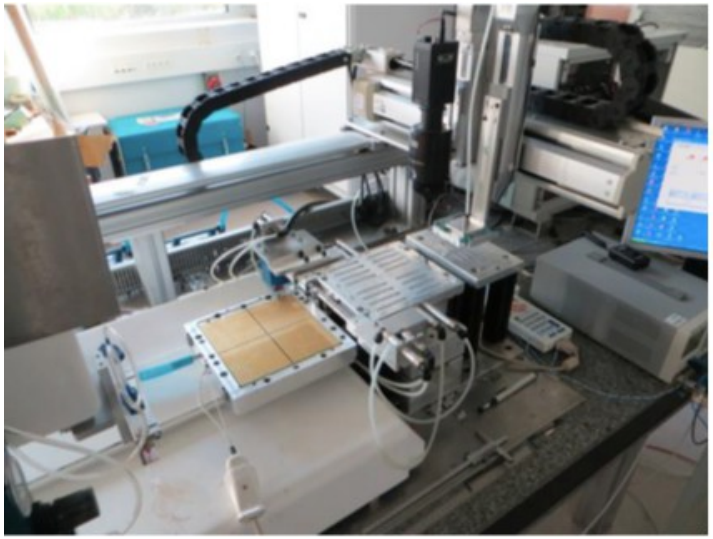


Laser station

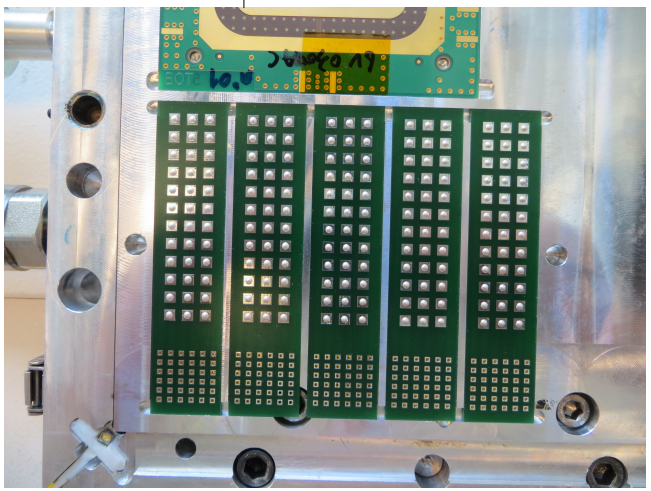


Well advanced infrastructure for full wafer characterisation
=> Wafer tests within HGCFC
Common interest of all branches of project

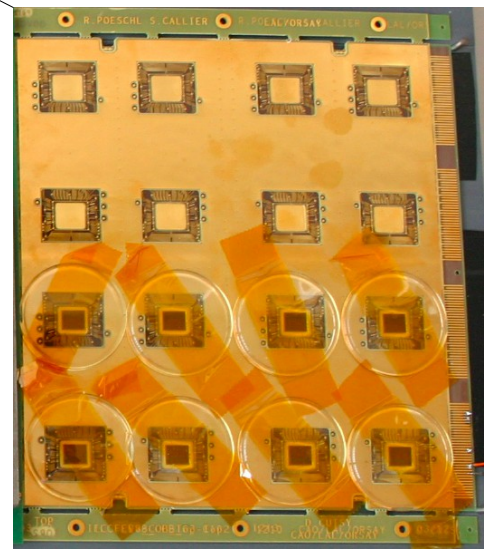
Versatile Gluing Robot



Done, FEV11_BGA



Done, HGTD-LGAD

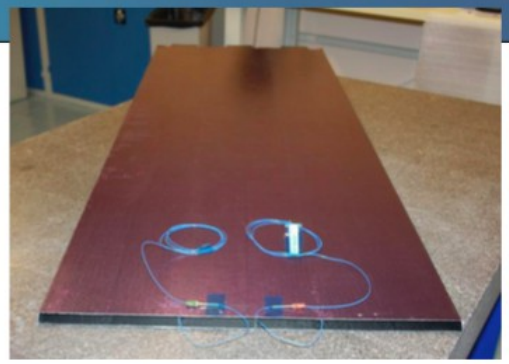


Under discussion, FEV_COB

Study of composite structures

Use of Fiber-Bragg Gating Sensors for the characterisation of deformation of composites structures

LLR demonstrator

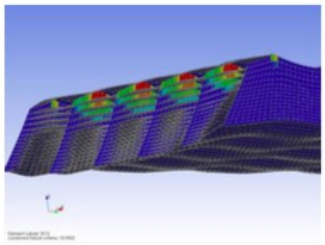


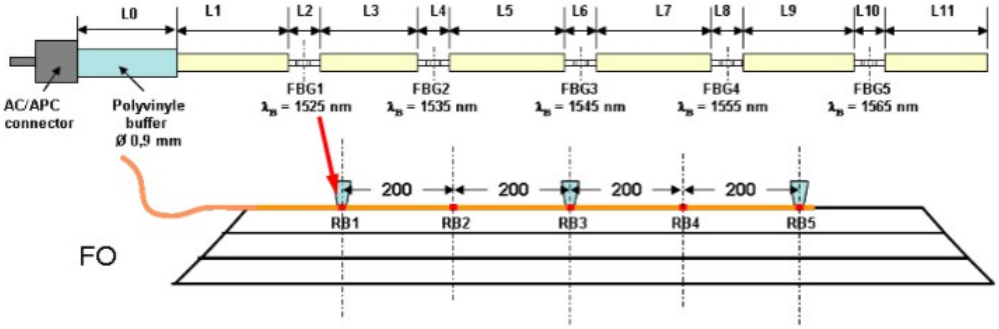
Bending tests (3 and 4) on demonstrator equipped with 5 FBGs per fiber

Choice of demonstrator:

1) A representative monolayer structure (3 cells)

2) implementation of FBG in the most stressed areas (directly under the rails: FBG1/FBG3/FBG5) + area with high elongation (FBG2/FBG4).

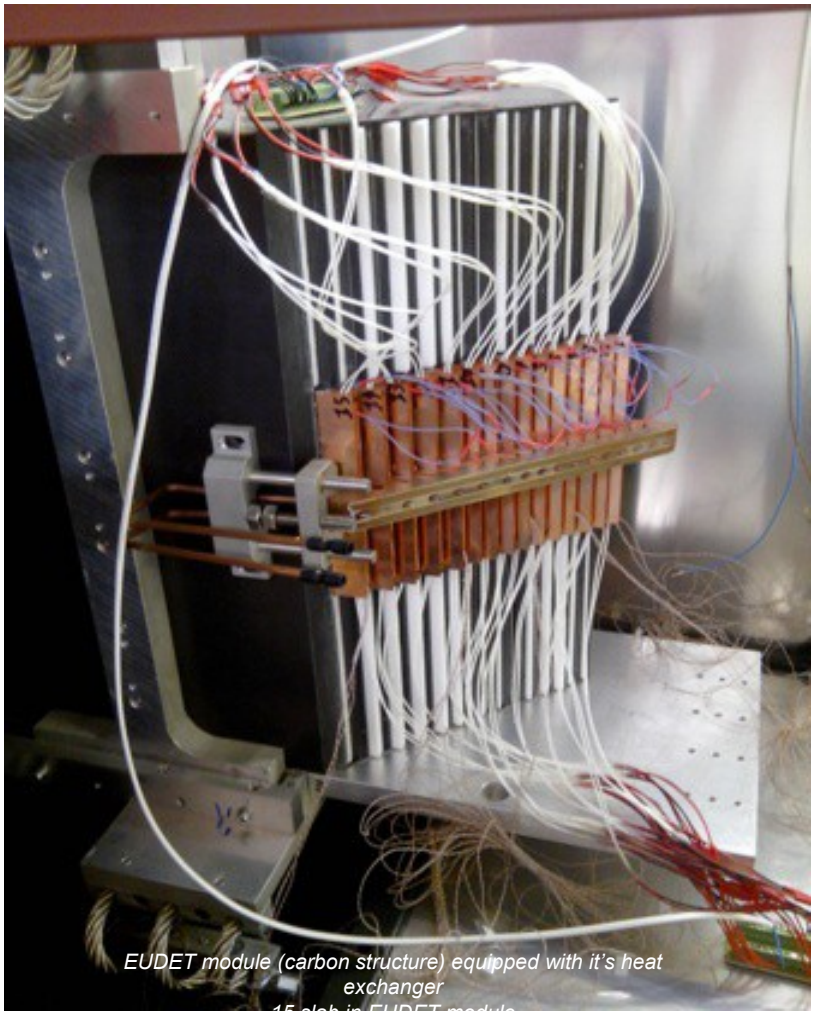




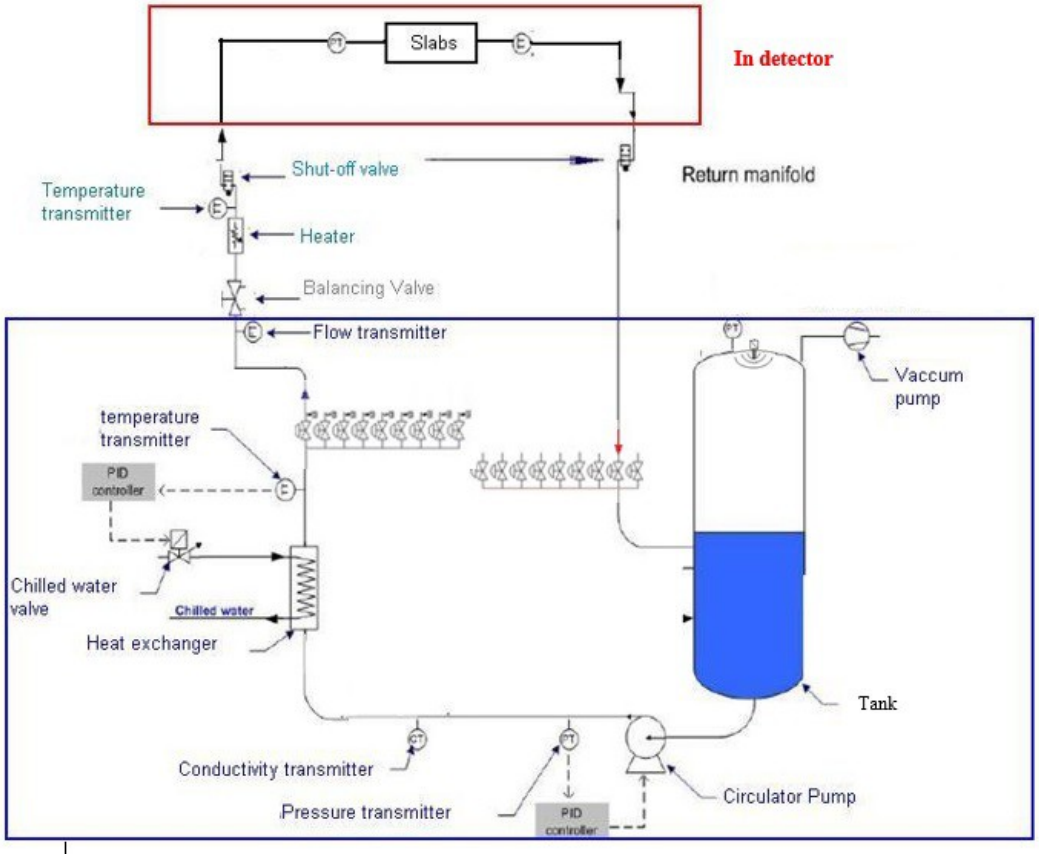
Positioning of FBGs based on simulations

3) Optical fibers directly embedded into inter-cell walls, during the manufacture of the demonstrator

Towards Full Sized Cooling system



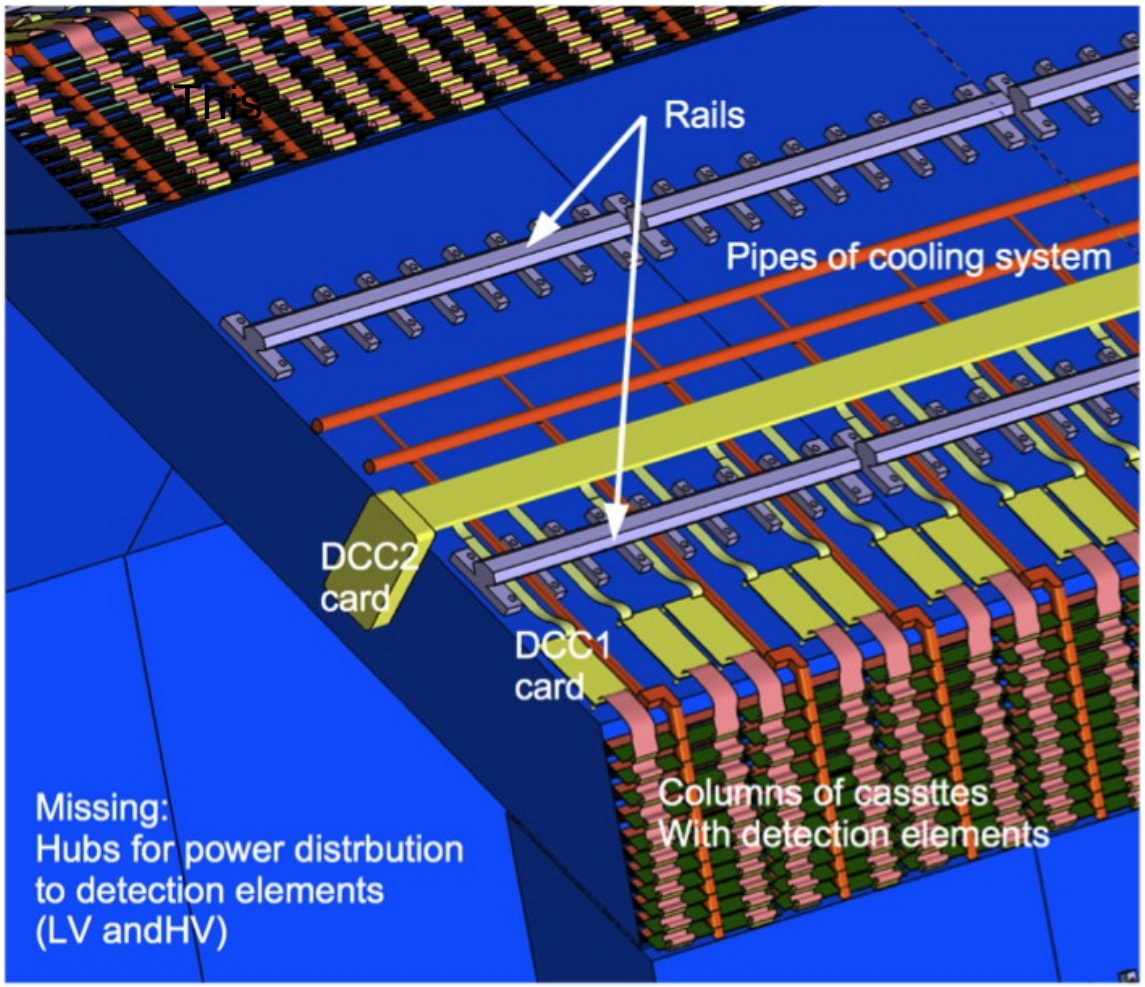
EUDET module (carbon structure) equipped with it's heat exchanger



Details in next talk

Readout, power supply and all that ...

How to fit services into ~3cm between Ecal and Hcal in ILD

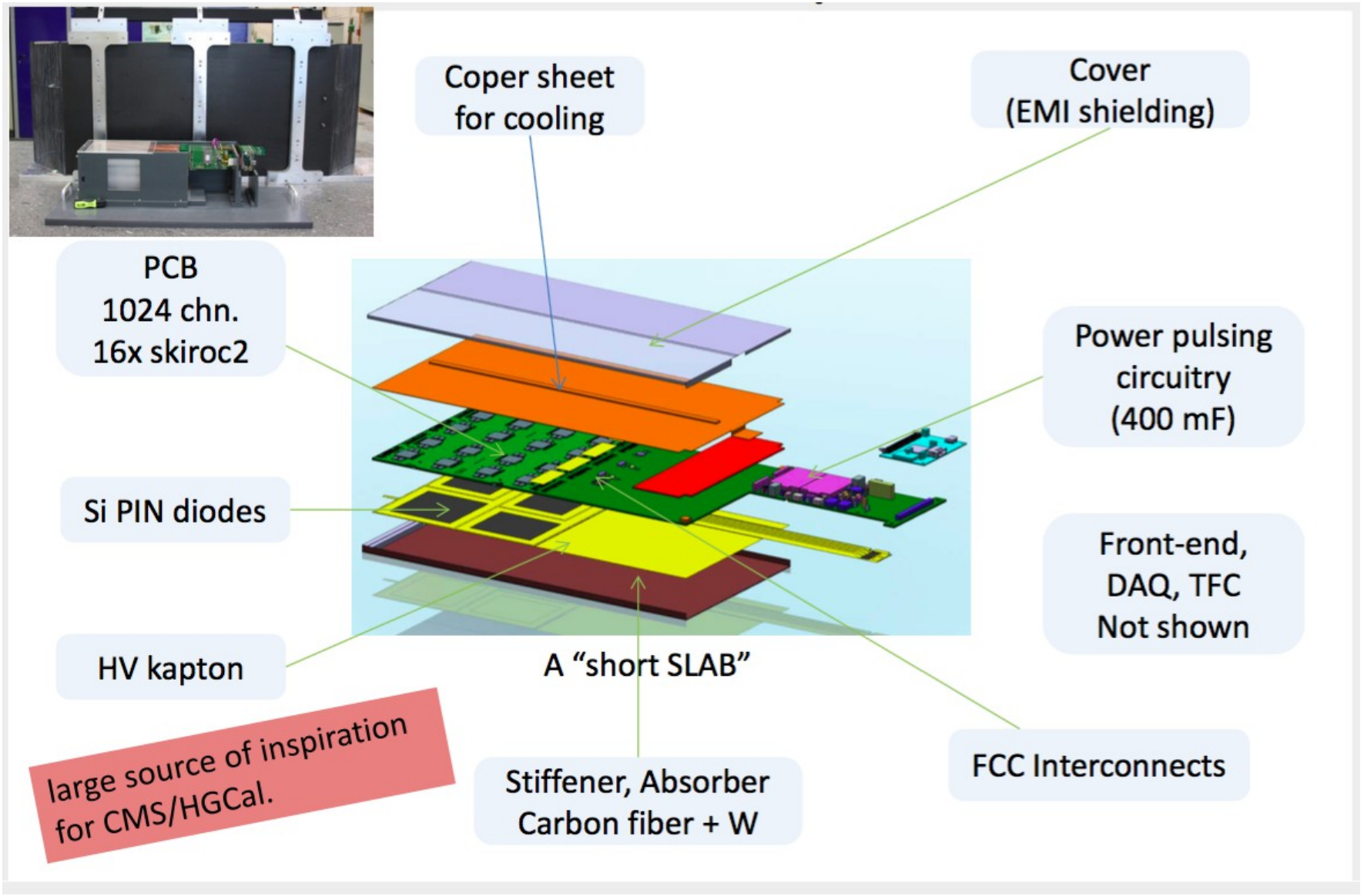


N.B. Image by M. Anduze and H. Videau
Labels by R.P., picture will vanish from uploaded slides

Conclusions

- SiW Ecal R&D is more challenging than ever
- Beam tests with short layers
- Gradual move to system aspects
  - **Long layers**
  - Full sized cooling system
  - Service integration in tight space
  - Quality and assembly chain
  - Stress tests for alveolar structure
- Important R&D on core components and techniques
  - Silicon wafers
  - ASICs
  - Thin PCBs
  - Gluing
- HIGHTEC and AIDA-2020 provide significant funding for these studies
  - Projects run until ~end of 2019
  - May match decision period on ILC or not
- Synergies with ongoing LHC detector R&D

SiW ECAL – Short layer

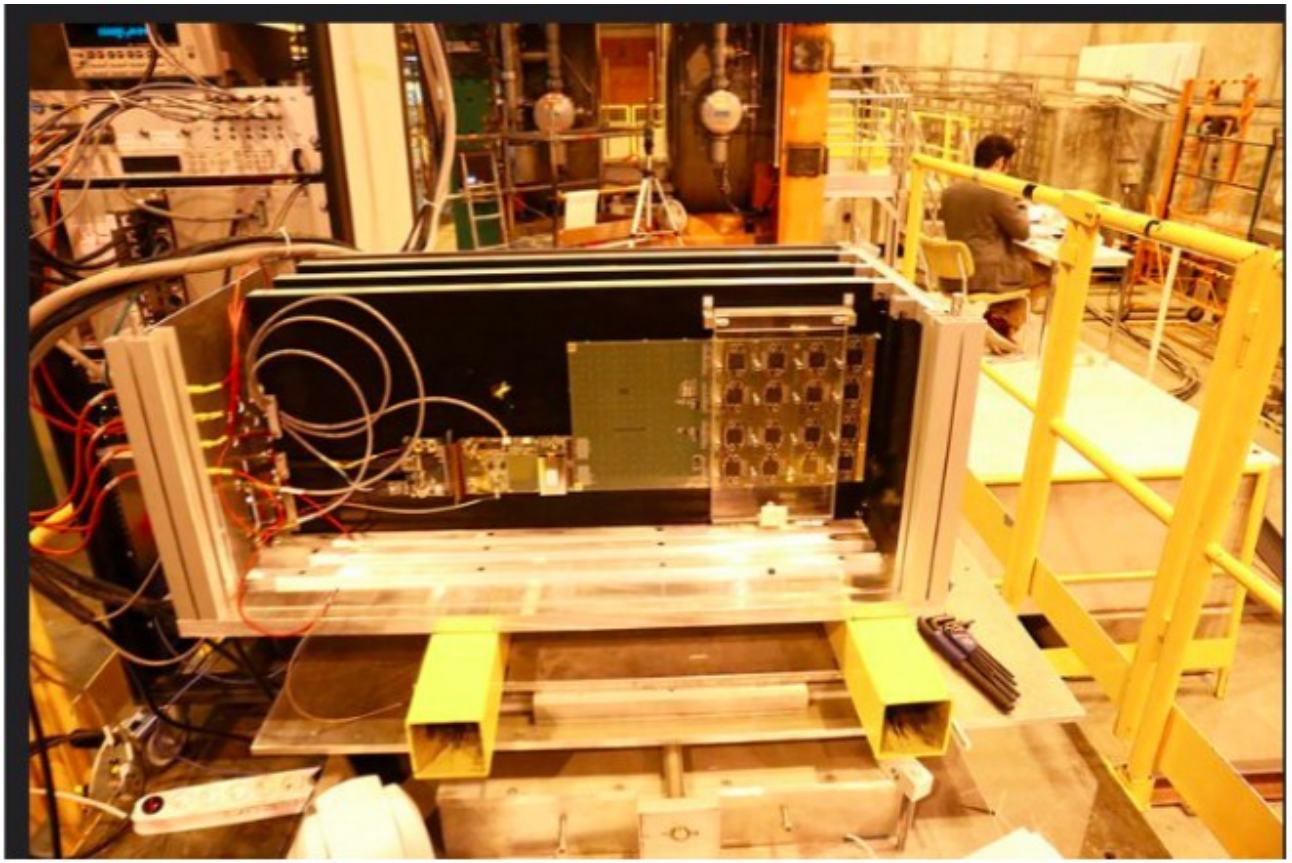


Between 12 and 15 short layers for HGCFC beam tests

R. Cornat LLR

SiW ECAL – First short layers

Test bench and beam test setup of first short layers with preliminary assembly

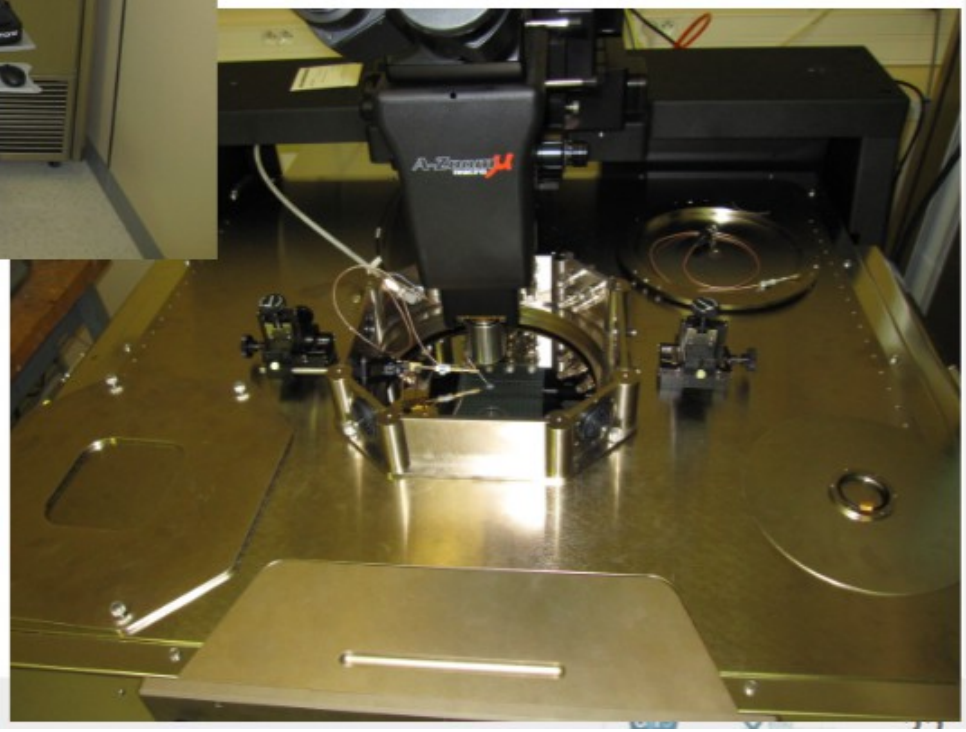


V. Boudry LLR

Backup

Platform CAPTINNOV

A semi-automated test machine



Project of platform driven by CALICE developments (+ATLAS@LAL)

Interest from STM

... has been already used for CALICE wafer cahracterisation

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