AHCAL electronics.
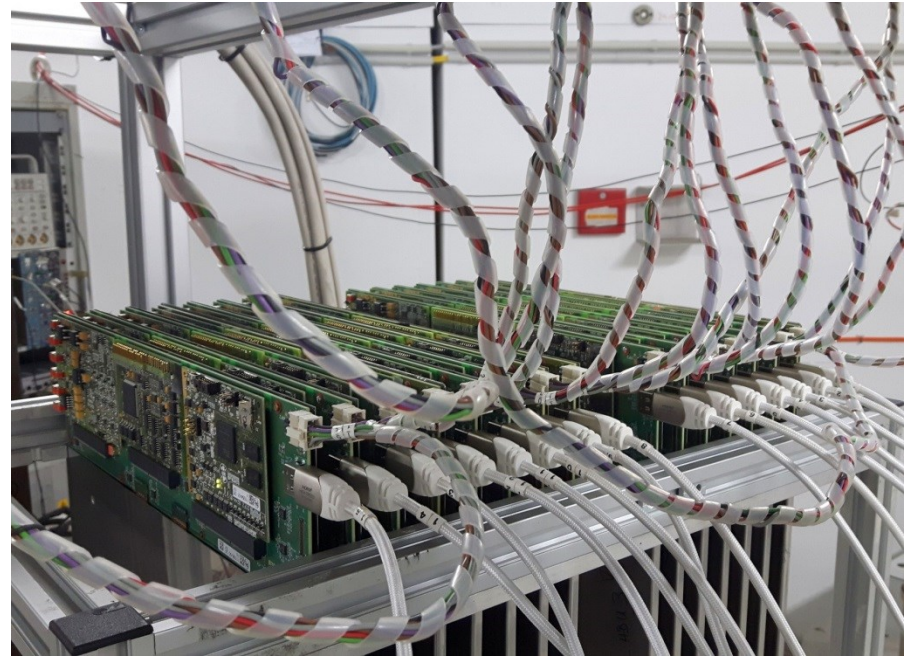
Status and Outlook

Mathias Reinecke
CALICE main meeting
Arlington, Sept. 14th, 2016
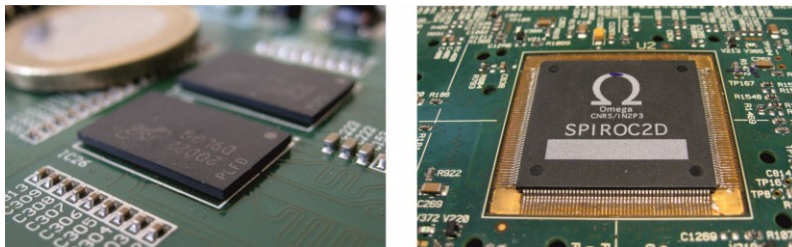
Outline

> Hardware Status

- HBU5_BGA

- SPIROC2E Testboard

- DAQ Interface Boards

> Status power pulsing

> SP2E – first results

> *The new MPPCs*

15 detector layers in DESY testbeam July 2016

HBU5_BGA

> New HBU generation

- new SP2E in 1.0mm BGA package. No cavities in HBU.

- New Hamamatsu surface mount MPPCs S13360-1325PE.

> HBU thickness increased by ~100µm.

> HBU pcb cost reduced significantly.

> 2 Boards in production, expected end of September with untested SP2Es (testboard not ready). At first without MPPCs.
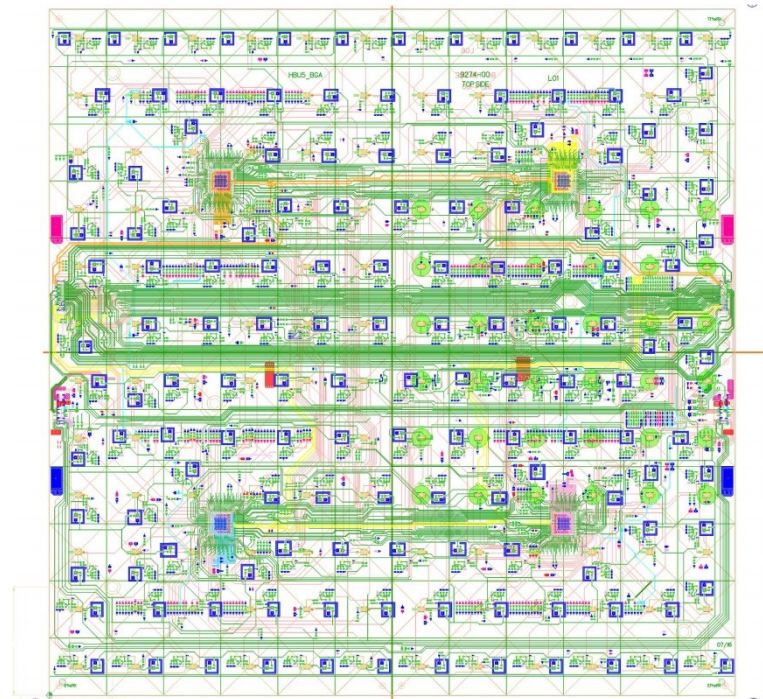
HBU5_BGA Layout

SP2E Testboard - Status

> Testboard for newest SPIROC generation: SP2E in BGA package.

> Interface to our common DAQ: Reuse all software packages for operation and data analysis.

> Close cooperation Uni Wuppertal – DESY

> 2 Boards in production, expected mid Oct. (end Oct. latest).
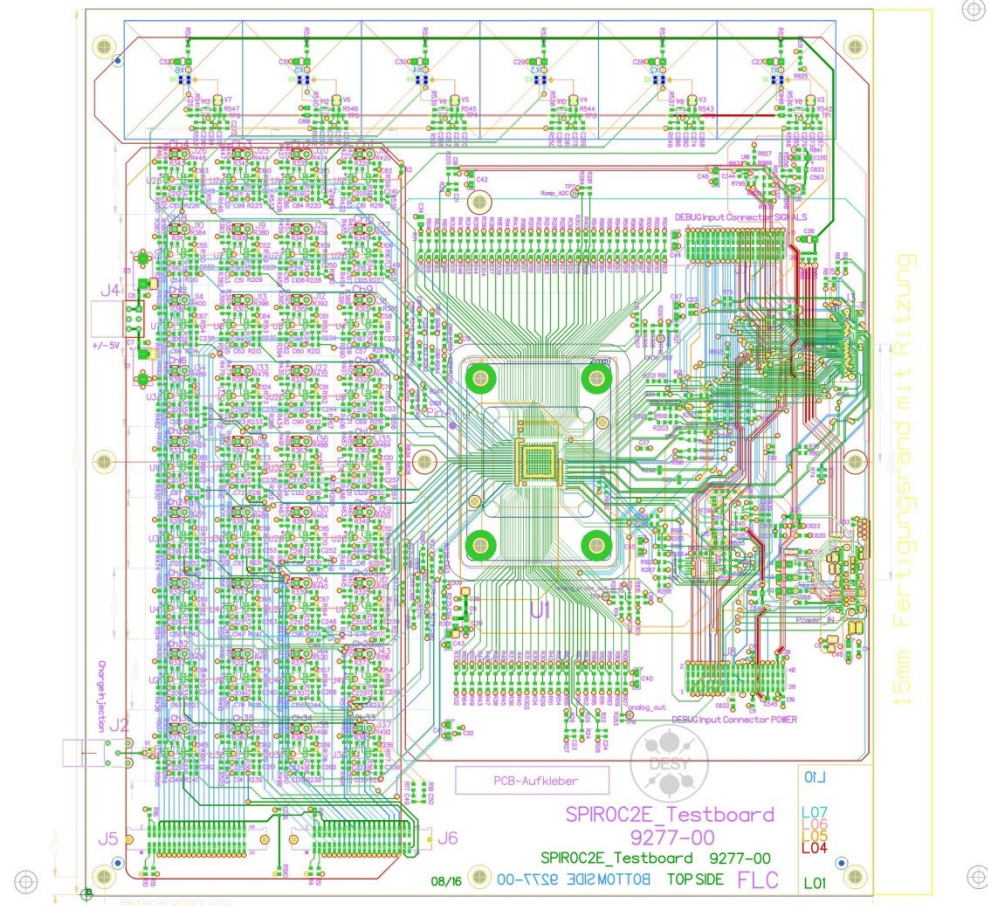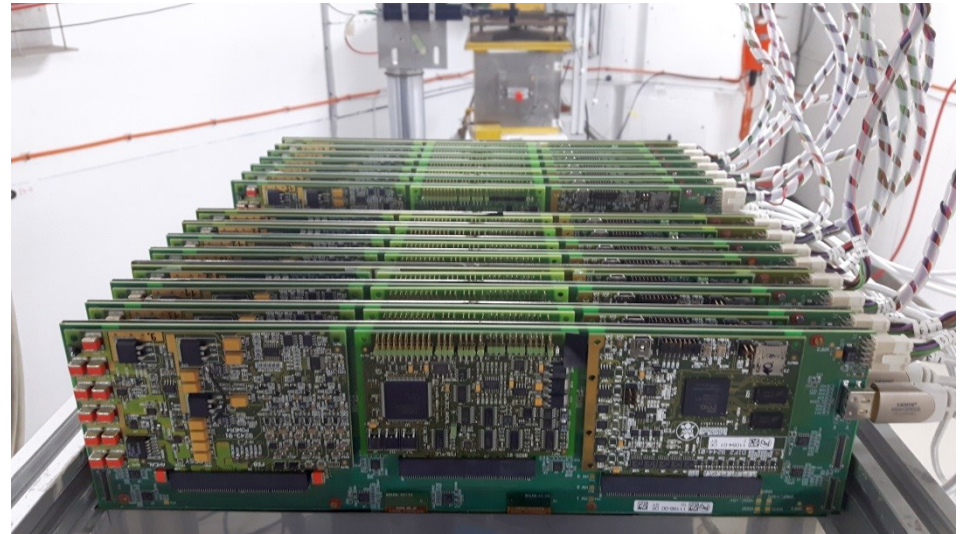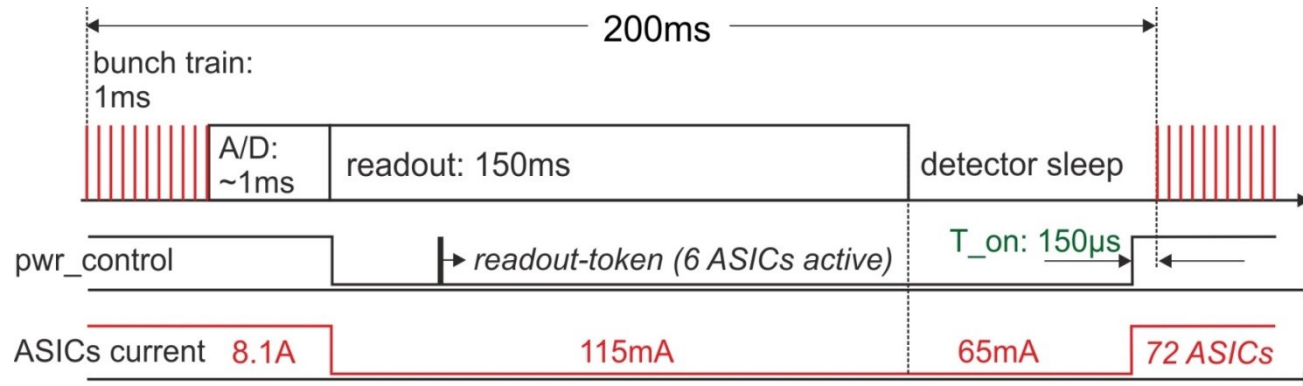

SP2E Testboard Layout

DAQ Interface Modules

> New generation of DAQ Interface Modules DIF, CALIB, POWER and CIB.

> Not interchangeable with old generation. => <u>Replace old boards</u>.

> Connects to all HBUs/EBUs.

> First 20 sets in operation.

15 detector layers in DESY testbeam July 2016

No. Channels: 72 SPIROCs x 36 = 2592

On-Time	SPIROCs empty	SPIROCs full
SP2B: 1%	185µW/ch	232µW/ch

> Power pulsing tested successfully in lab and testbeam (see Katjas's talk).

> Switch-on time for full slab 2ms (2012) => 150µs (2016)

> Aimed 20µW per channel not reached, but:

> At low duty cycles: Off-current more important. Improved in SP2E!

> See more: IEEE NSS 2016: N24-2 (M. Reinecke)

New SPIROC2E – First Results

> SP2E has been packaged in BGA housing (OMEGA).

> Received first two brand new SP2Es in CQFP from OMEGA.

> Both SP2Es assembled on SP2D-HBU2. One SP2E broken.

> Tests in close cooperation with OMEGA.

> SP2E used in next big prototype?

> Main tests: Charge injection!
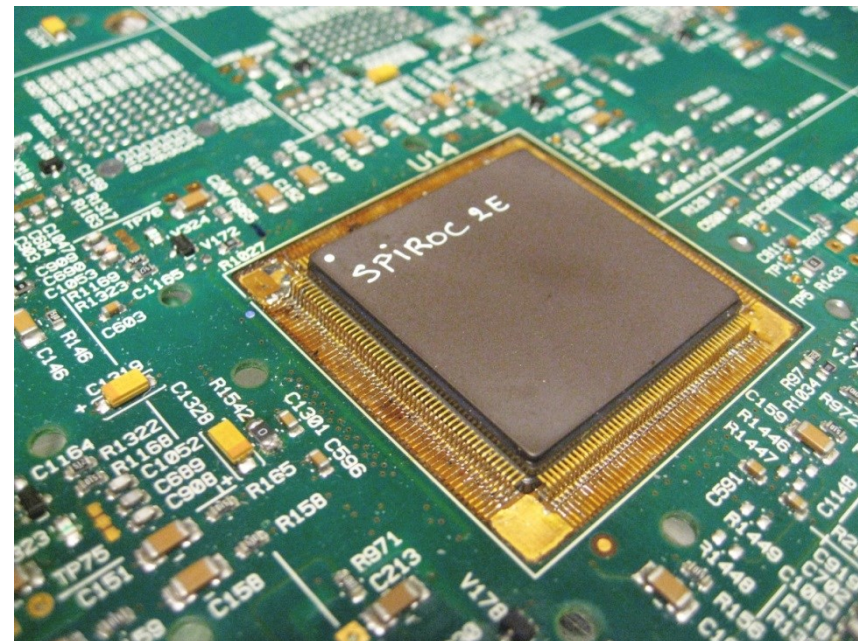
SP2E in CQFP on HBU2

Tests @ DESY:
Lourdes U. Gomez
Adrian Irles
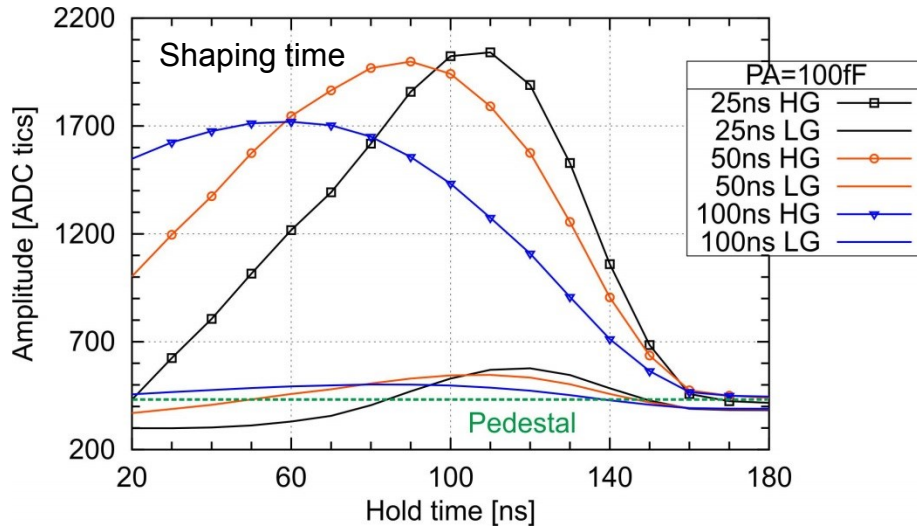*Mathias Reinecke*

SP2E – Input DACs (inDACs)
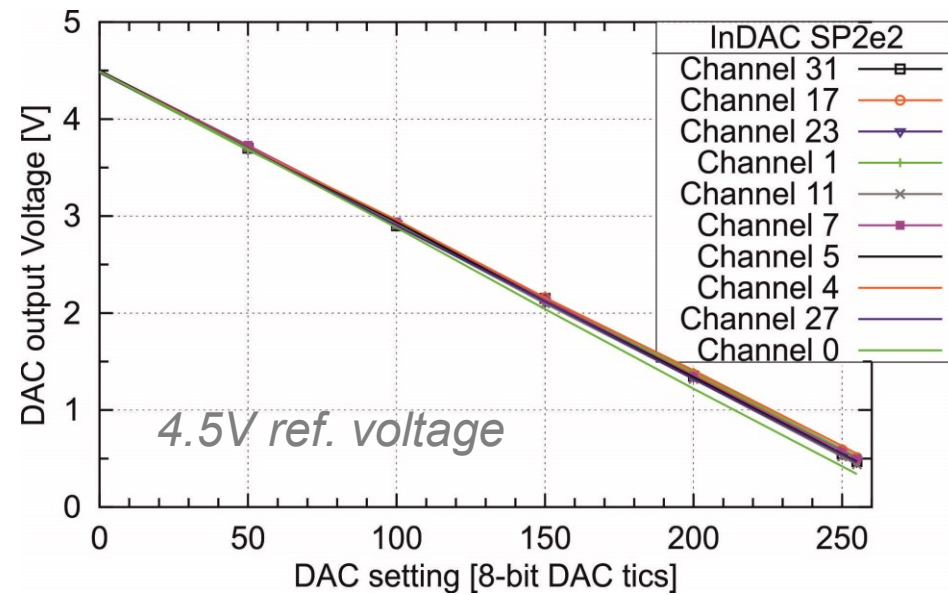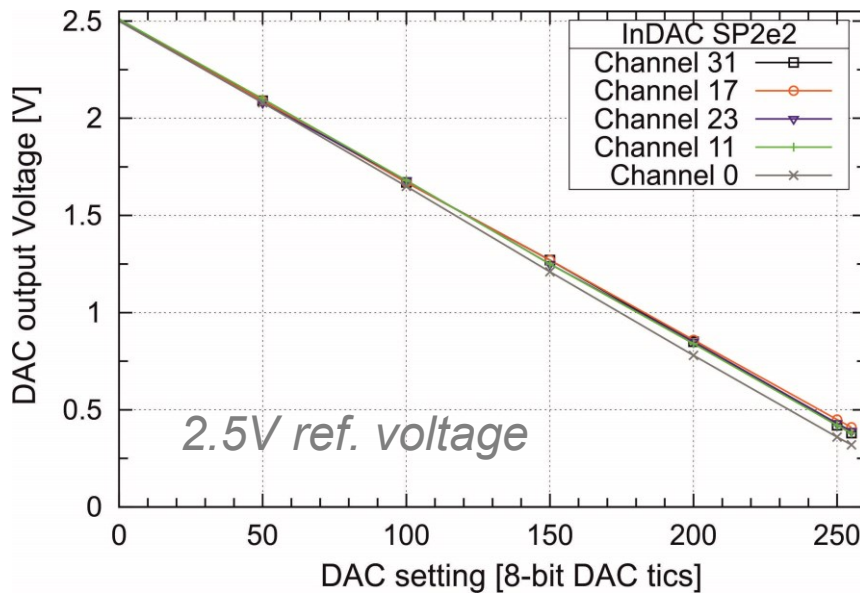
> InDACs with two output modes: 2.5V and 4.5V, choose in slow-control data.

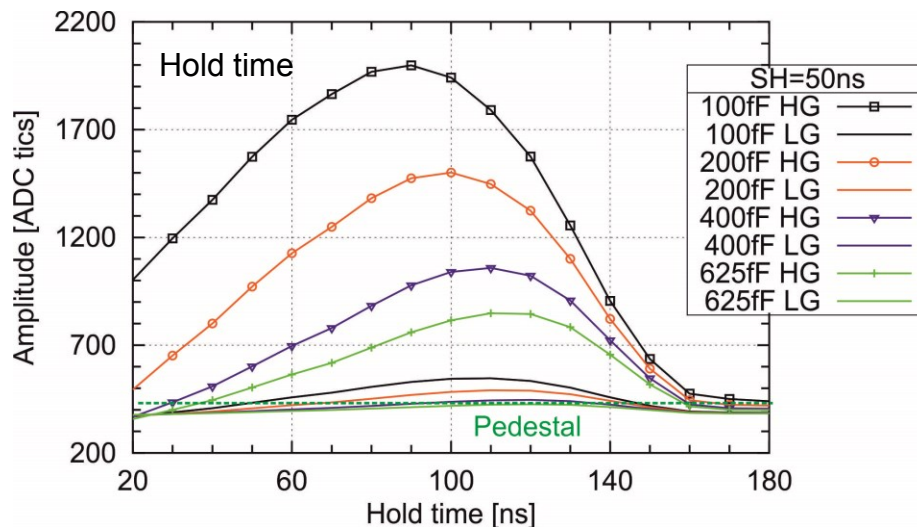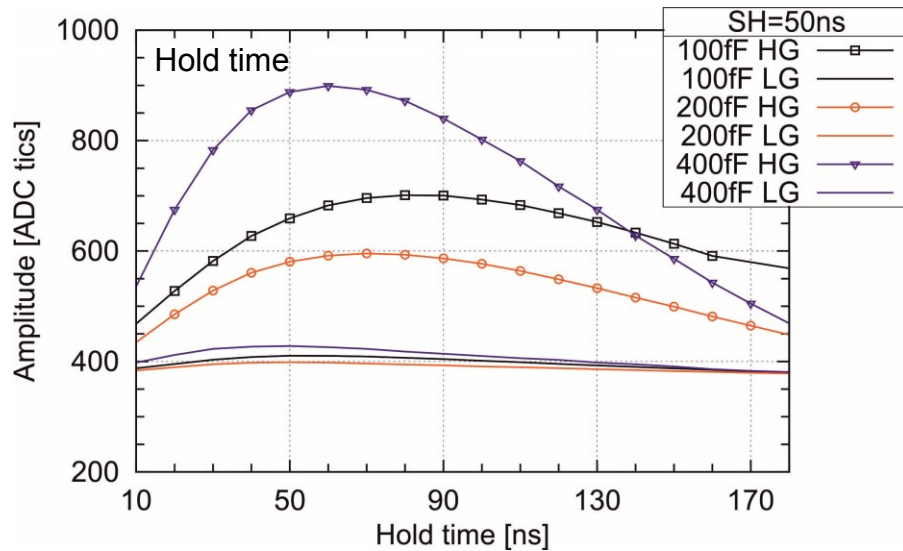> Still some spread at inDAC=255 – not to quantify with only one SP2E.

SP2E – Hold-Scan in External Trigger

> SP2E does not have delay cell for ET-Hold-time adjustment. Hold time is defined by CALIB board and main Labview.

> Time axis reversed!

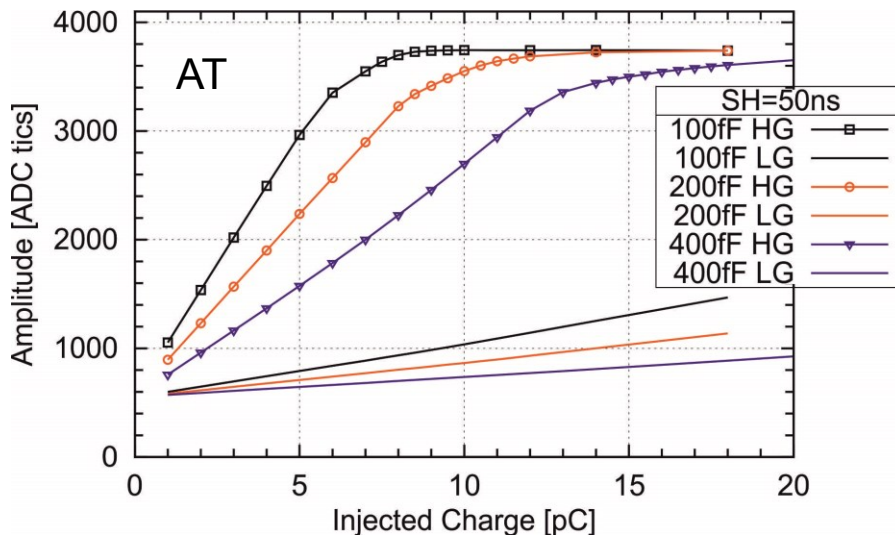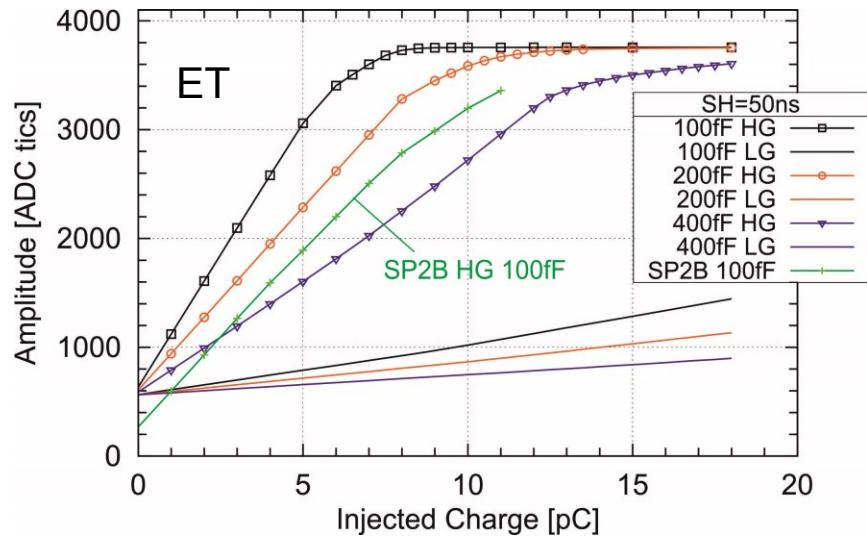> Shaping- and Hold-time behaviour comparable to SP2B.

SP2E – HOLD-Scan in Autotrigger

> Hold time in AT is defined in slow control data: <u>1ns per tic</u>!!

> Hold-time behaviour comparable to SP2B.
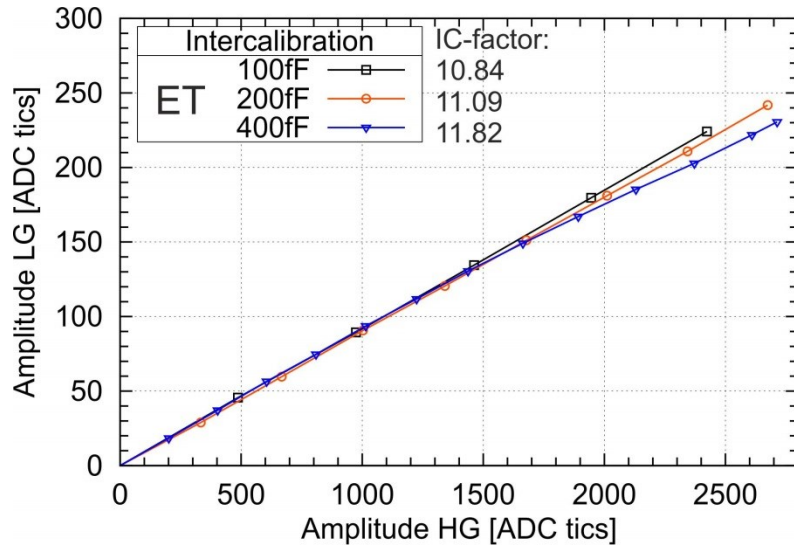
SP2E – Dynamic Range

> ADC ramp slopes needed bias adjustment.

> Rather high pedestal ~600 ADC tics.

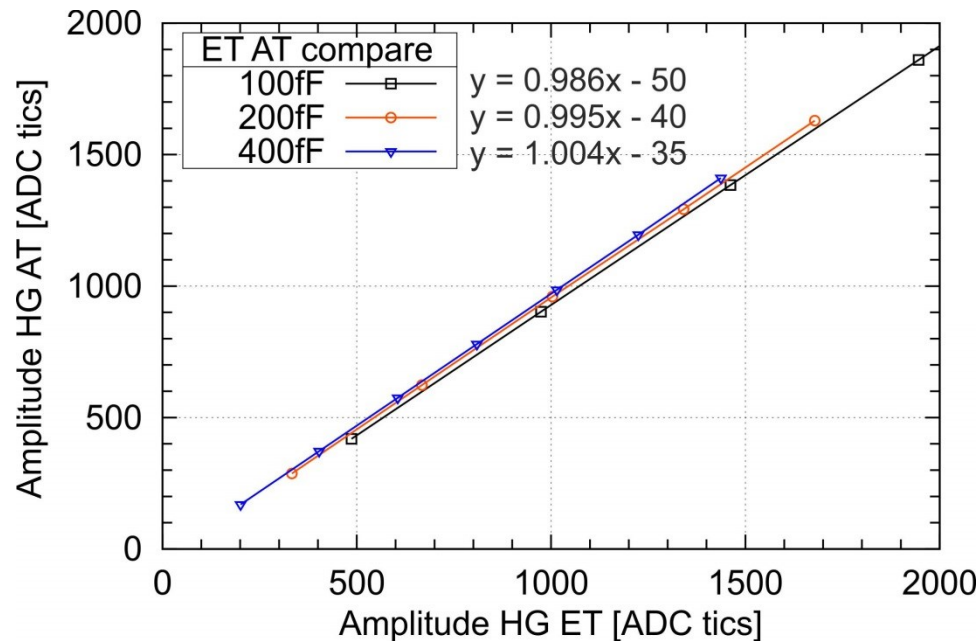> Distortions in PA=400fF curve – as in SP2D.

> Gain in SP2B lower.

SP2E – Intercalibration (IC)

> How does the input charge divide up between HG and LG: IC factor.

> IC factor slightly dependent on PA setting and ET/AT mode.

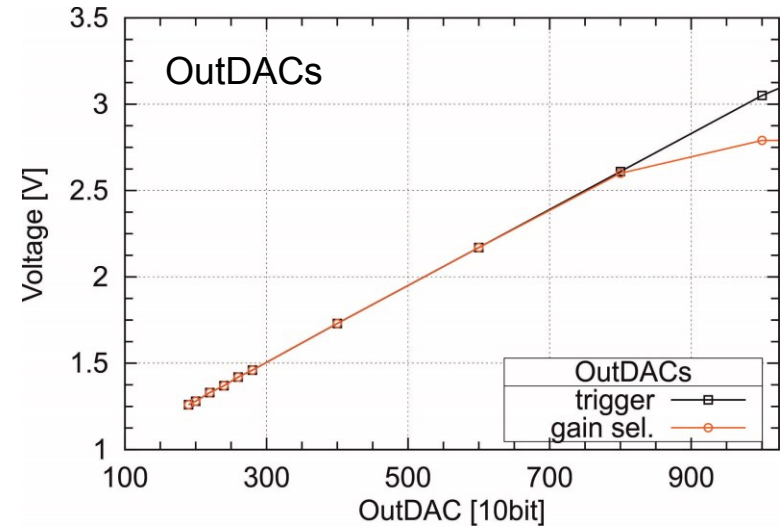> Data is pedestal subtraced. In AT, pedestal of ET is used. Optimum hold time used for each PA setting.
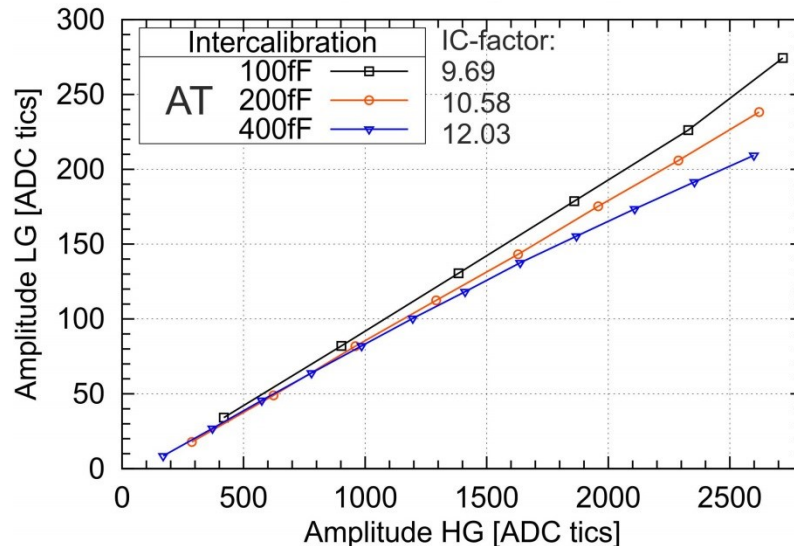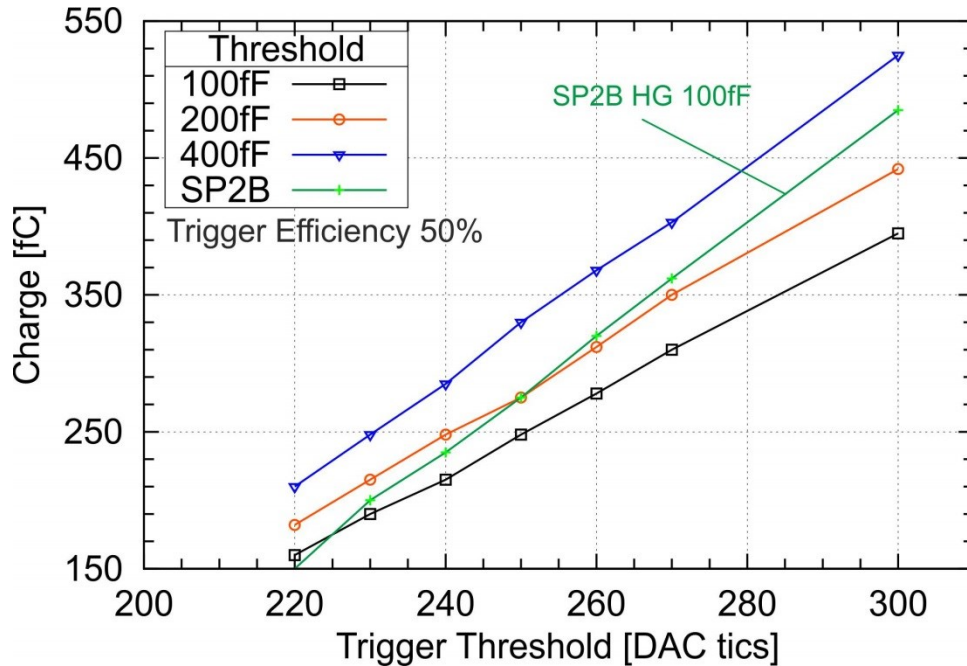
SP2E – AT/ET comparison

> Is the response to the same injected charge in ET and AT the same?

> Problem: pedestal subtraction in AT. Pedestal of ET used.
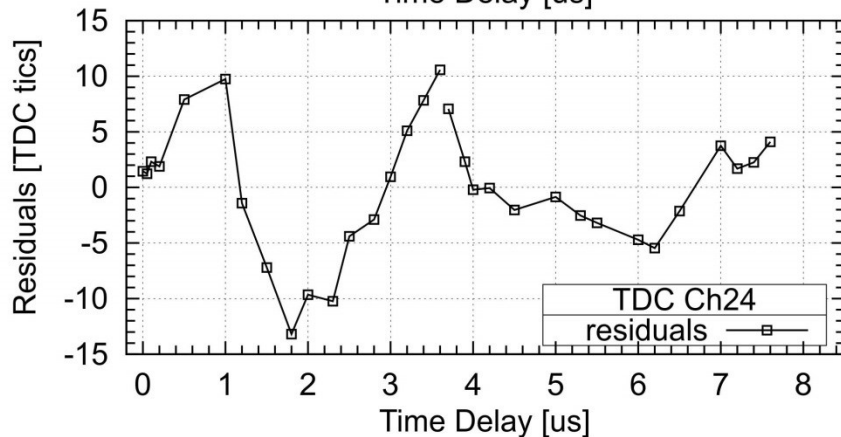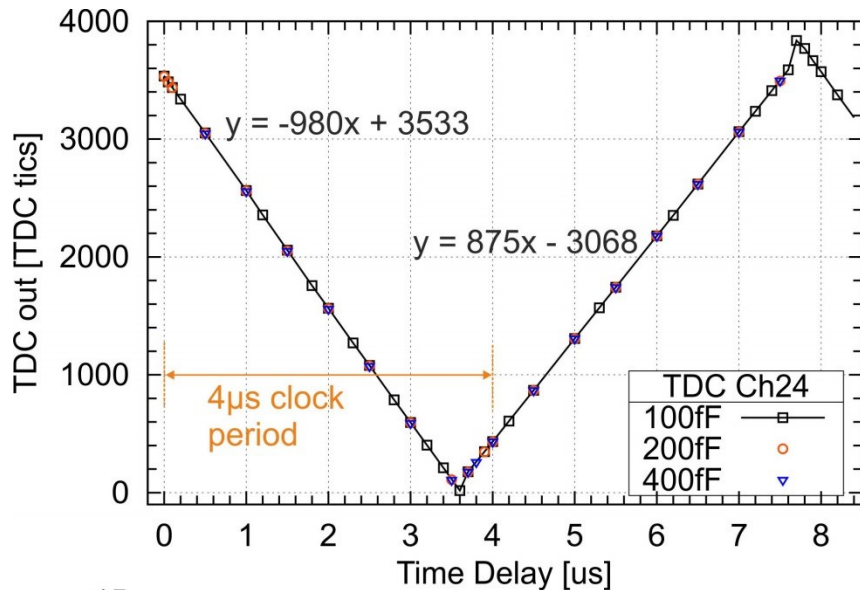
> Slight differences in response (AT/ET).

SP2E – AT Threshold Scan

> Which autotrigger threshold corresponds to which input charge?

> Slight differences to SP2B.

> DACs for trigger- and gain-thresholds (OutDACs) behave as in SP2B.

SP2E – TDC

> SP2E: One up- and one down-ramp as in SP2D.

> Bias points for ramp slope needed adjustment.

> Linearity much better than in SP2B.

> Sometimes single wrong results from TDC. To be checked.

> In testbeam mode with 250kHz clock: 1.14ns per TDC tic. ILC mode not checked so far.

SP2E – pedestal stability

> 8 channels have been equipped with tiles (12k „new" KETEK).

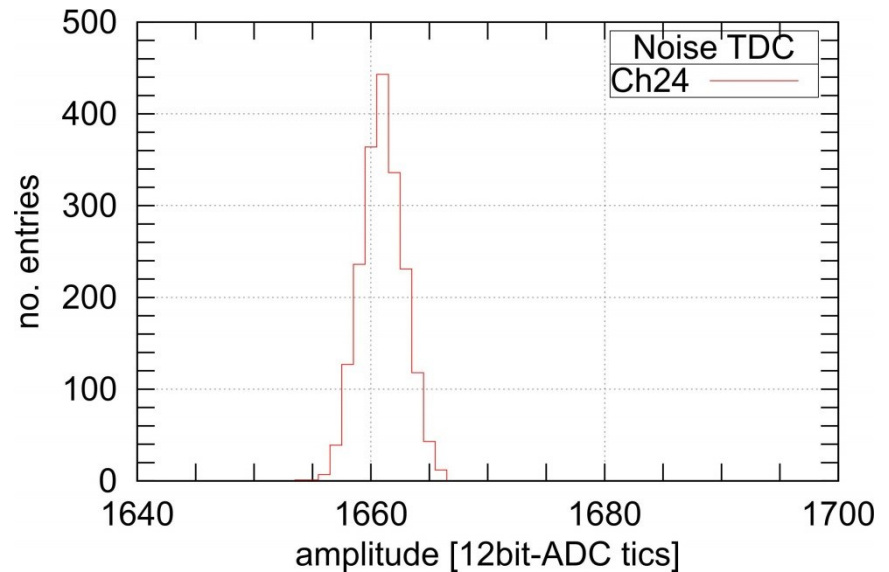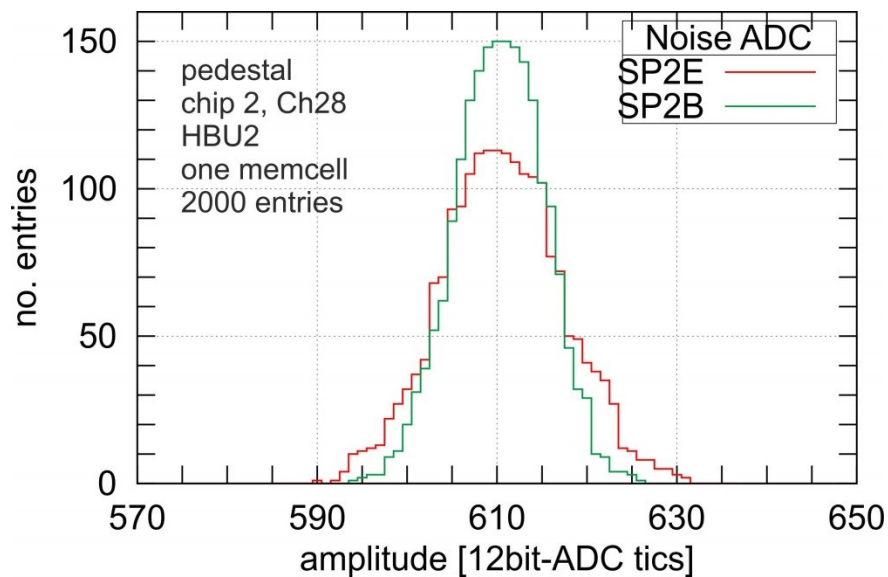> Increase signal amplitude in the 8 channels, observe pedestal of the others:
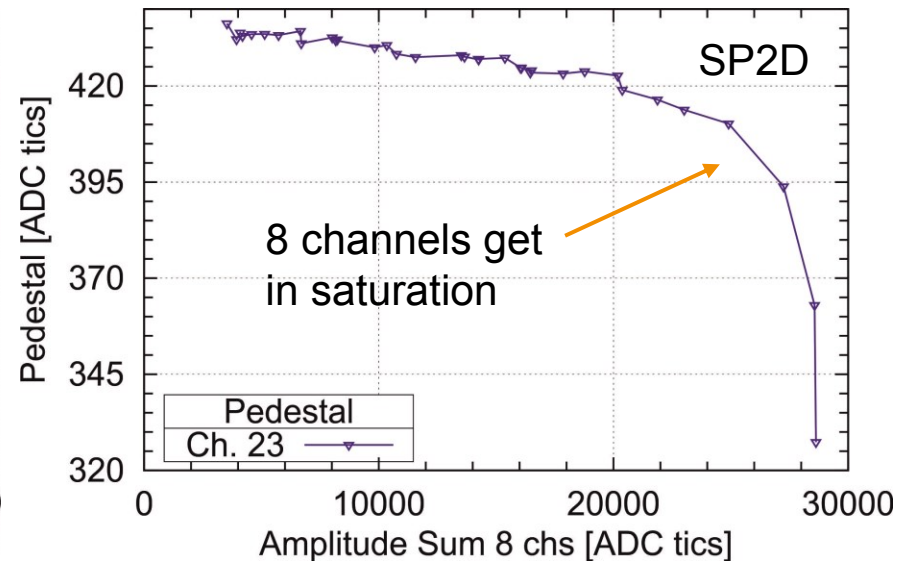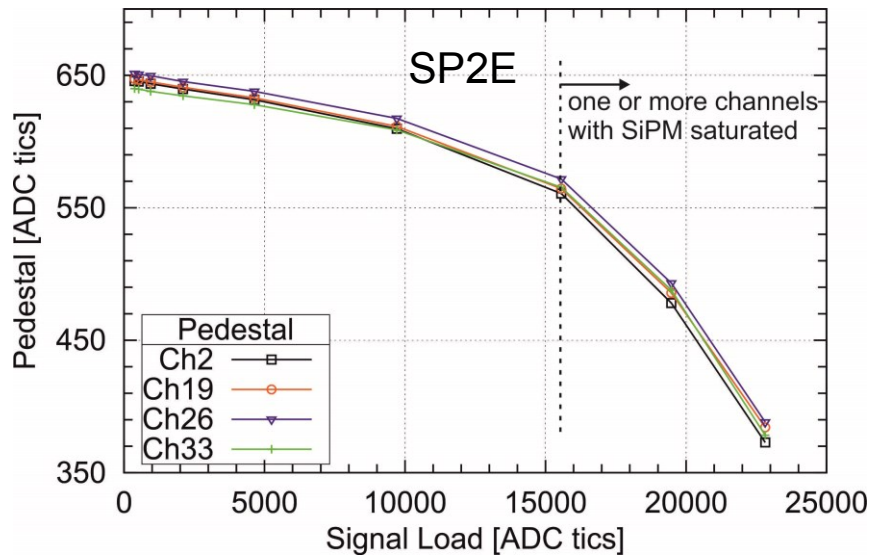
> „Pedestal-shift" seems higher than in SP2D. The CQFP package might have influence (e.g. bond wire resistance)! To be checked in BGA.
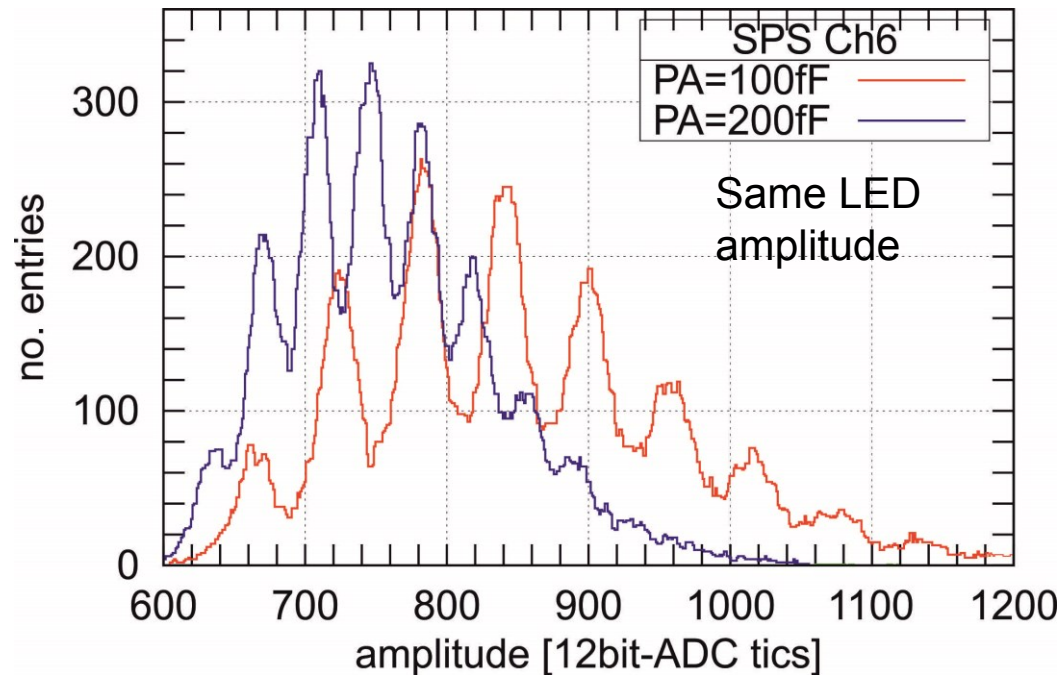
SP2E – Noise (pedestal)

> Noise in ADC increased compared to SP2B. CQFP package might be the reason. To be checked in BGA.

> Increased noise observed at OMEGA as well.

> Noise in TDC is very low (sigma << 2).

SP2E – first SPS

> SPS for 12k „new" KETEK (ITEP) with an SPS distance of 56 ADC tics.

> Good S/N at this high gain – noise needs to be checked in BGA package.

SP2E conclusion and open points

> A lot of promising results, no show-stoppers so far.

> First memory cell works for ADC, but not for TDC!

> Noise in ADC is higher than in SP2B – to be checked in BGA package.

> LED/SiPM: Saturated Channels flip from 4095 to 0 in HG ADC.

> HitBit in ET only set when signal above threshold, as requested!

> Not checked (wait for BGA):

  ▪ Event validation

  ▪ Channel-wise trigger threshold

  ▪ Testbeam (MIP response)

  ▪ Power Pulsing / Supply Current

  ▪ ILC mode (5MHz data taking)

> Last checks: Wait for SP2E on HBU5_BGA before SP2B replacement.

Last but not least – the new MPPCs
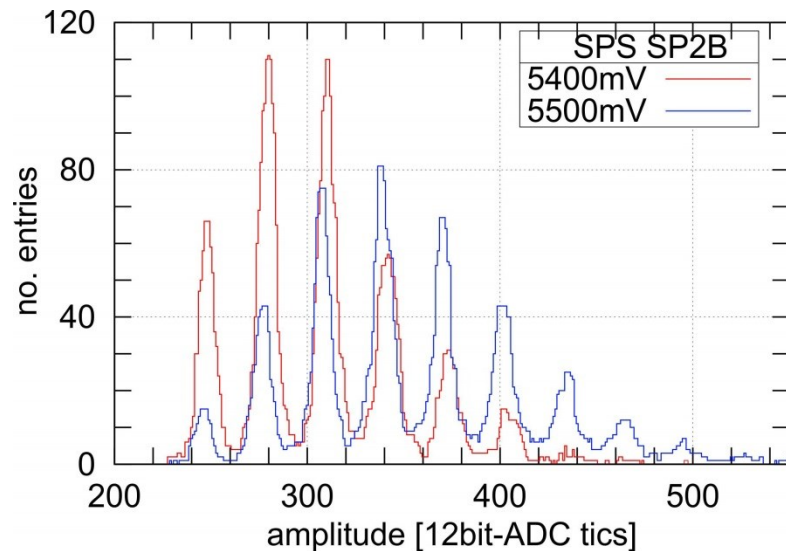
> New Hamamatsu S13360-1325PE on HBU4_SMD (SP2B).

> Good S/N=10 (pixel distance=30 ADC tics).

> Settings: ET, PA=200fF, Sh=50ns, H=001110, one memcell, ILC-mode (CLK 5MHz), nominal bias voltage, SPS plot:binning=2.
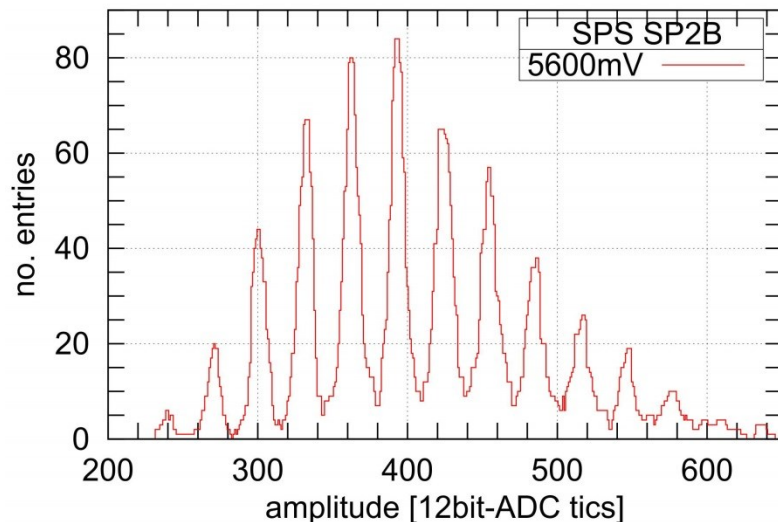
New MPPCs – Characterization

> New HBU4_SMD with Hamamatsu S13360-1325PE in climate chamber, measure gain g=f(temperature,bias-voltage).

> For detector operation: Measure T – adjust global V (with new POWER4).

MPPC studies:
Yuji Sudo

dg/dT = 1.1%/K

dg/dV = 1.6%/100mV