News on the KLauS ASIC

- New KLauS prototype
  - The ASIC
  - Power consumption
  - Digital part & IO
- Test board

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New multi-channel prototype

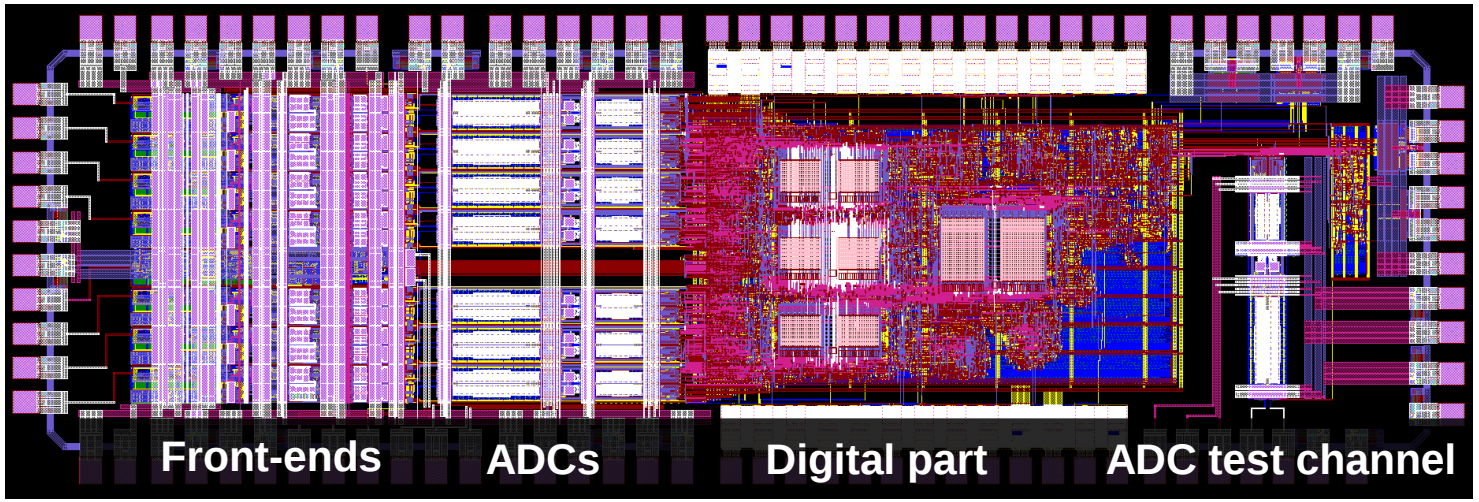
Taped out first multi-channel prototype in May 2016
Expected back in next weeks
1.5 x 4.5 mm² miniASIC (Final 36 channel chip size 5x5mm²)
Initially planned 10 channels, limited space did not allow this, so:

7 Front-End + ADC + digital channel control modules
1 TDC-only channel (external time reference)

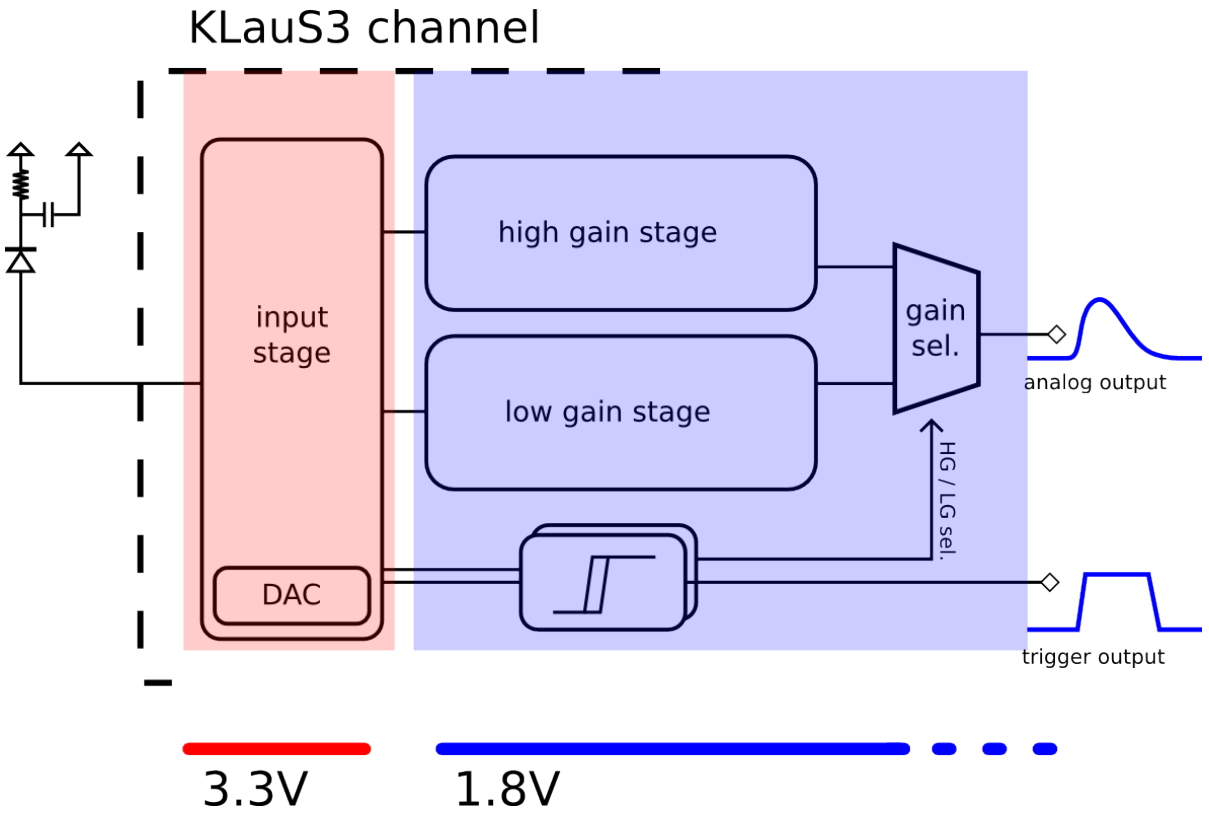
1 ADC test channel (separate)

Digital part

Structured as future 36 channel version
Different readout options: Fast LVDS (160Mbit/s), slow I²C link



Front-end: Blocks



Input stage:

Distribute current signal to 4 processing branches:

Analog processing

"High gain" - *SiPM gain calibration:*

Small range, low noise (ENC)

Expected noise ~3fC

"Low gain" :

Full SiPM dynamic range

Expected range ~160pC

Comparator branches

Event trigger

initiate ADC conv., time stamp

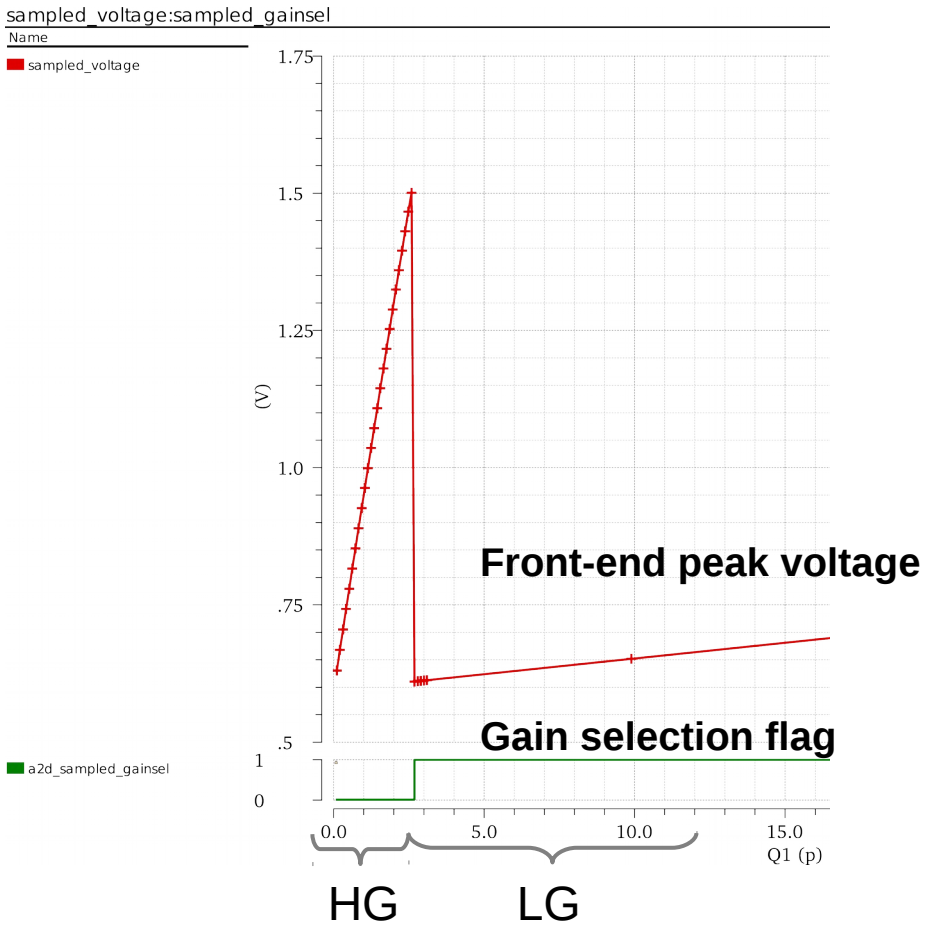
Lowest threshold

~1-2p.e. for 10um MPPC (20fC)

HG/LG selection

→ **1 to 1 coupled to ADC**

Front-end connection to ADC & Digital part



Front-end outputs in automatic HG/LG selection mode

One ADC reading / event
- No analog memory
- Direct conversion to digital

ADC input Selection:
- Force HG readout
- Force LG readout
- Automatic HG/LG
- External source (ADC calib)

2 ADC modes
- 10bit for MIP quantization
- 12bit for single photon spectra

Time stamping
- 12Bit coarse counter (25ns bins)
- TDC with fine bins in future versions

Power consumption & gated operation

DC power consumptions (when switched on)

Channel	≈ 2.9 mW
Shared bias block	≈ 2.4 mW

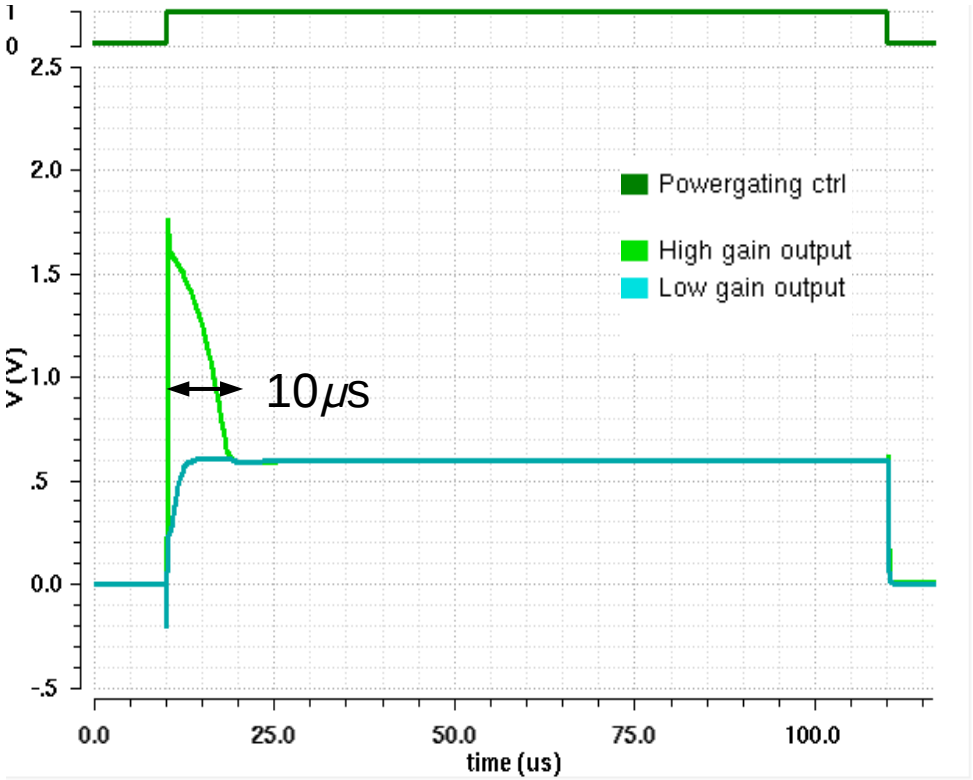
Power pulsing control

Single CMOS control pin

Internal power-up delays tunable using the slow control interface

Pedestals stable after ~10-15µs

Duty cycle can be reduced towards 0.5%



Power consumption, pulsed operation

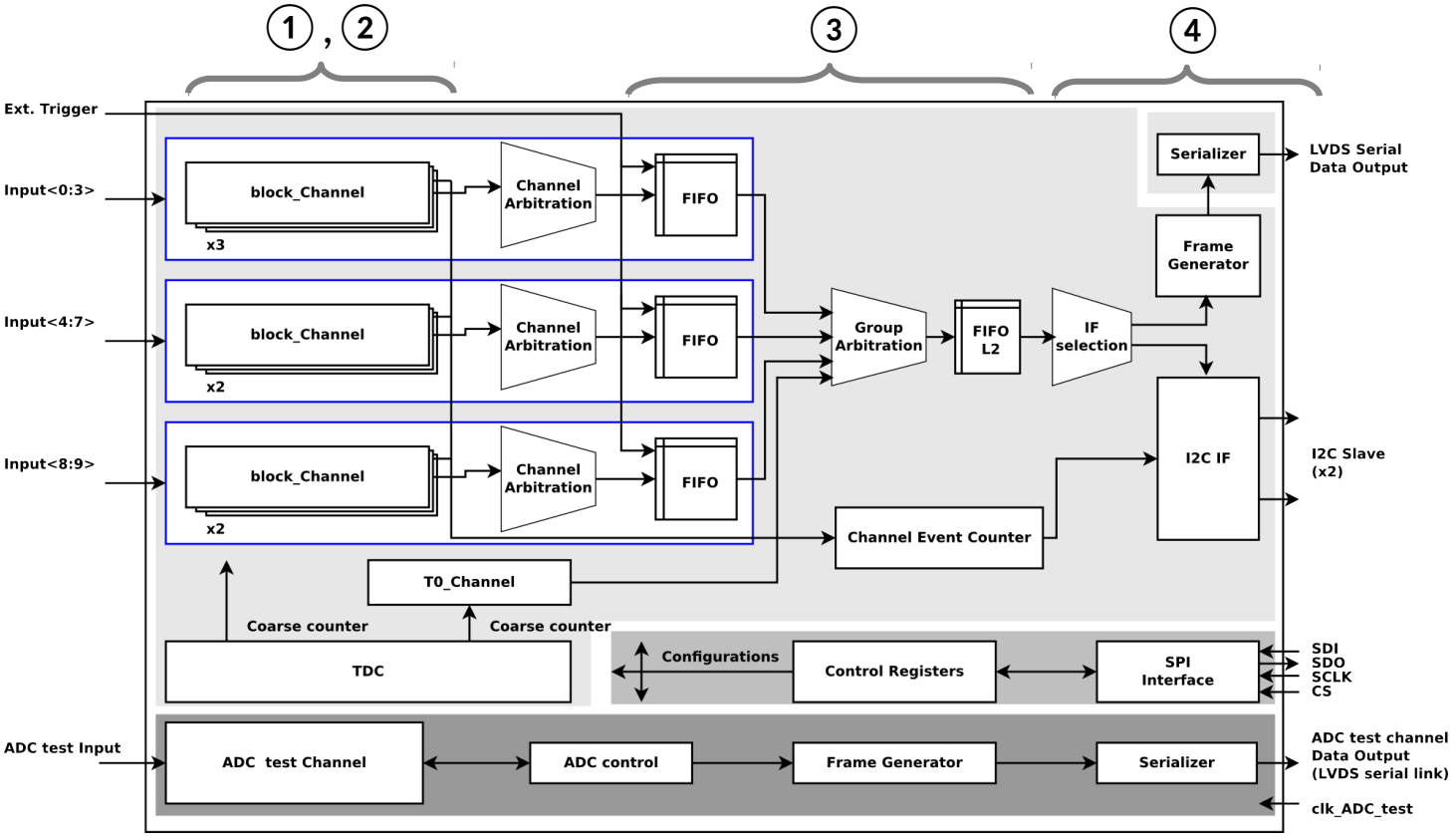
*Extrapolated to 3*6 channel chip

Front-end & ADC, Bias block ; no digital part

1% duty cycle: **37 µW/ch**

0.5% duty cycle: **22 µW/ch**

Digital part: Overview



① Hit processing in analog stage
② Channel digital part: control ADC conversion of peak voltage, storage of TDC data & flags
③ Storage in internal buffer (2 levels of FIFOs)
④ Serialization through LVDS or I^2C interfaces

Channel hit counters read out by I^2C transaction (SMBUS block read)
Slow control via SPI, will be replaced by I^2C later (SMBUS block r/w)

Digital part: Data flow

Event data only stored in buffer when hit

<u>3 Levels of data storage</u>

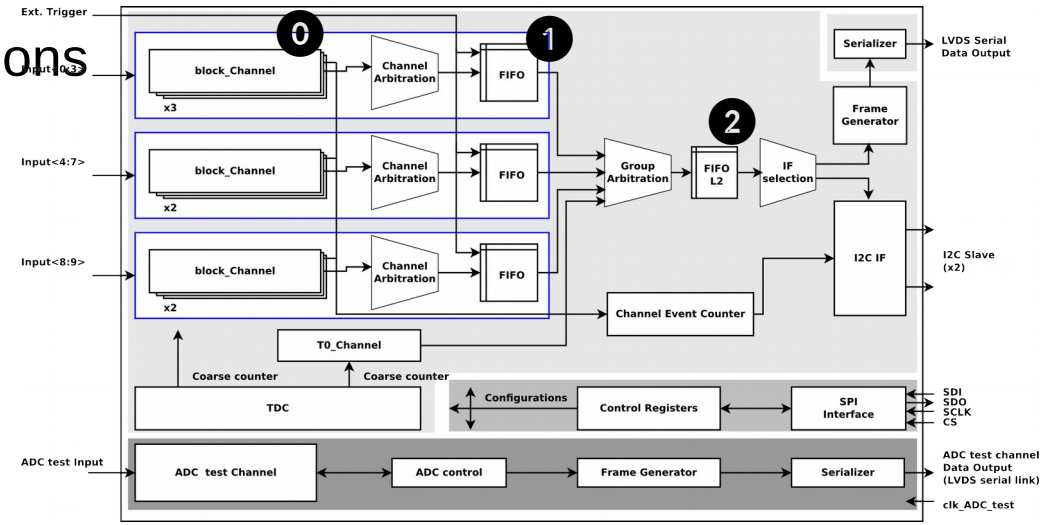
(L0) – Channel digital part:
For each channel, 2 hits depth

(L1) – First level FIFO buffer:
3 Groups of channels, 64 hits depth

(L2) – Second level FIFO buffer:
For all channel groups, 128 hits depth

→ **Total buffer size 330 hits**

Possible to adjust as needed in later versions

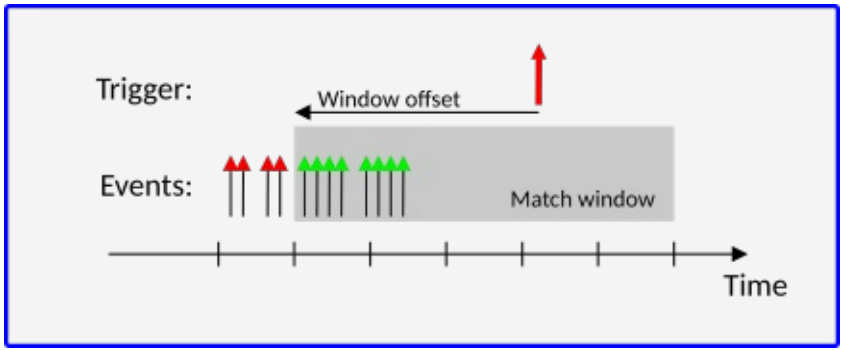


Digital part: Event validation

In first level FIFO:

- Keep events until validation decision
- Drop non validated events in window

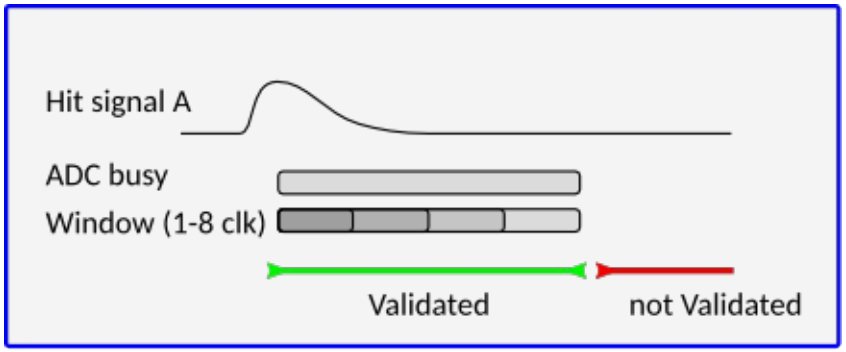
- Larger matching window
- Configurable width and offset
- External source

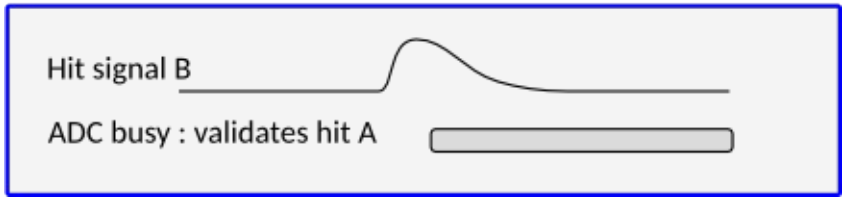


During ADC conversion:

- Cancel ADC conversion if not validated

- 25ns-200ns window
- External source, or
- Neighboring channels
  (basic coincidence building)





KLauS4 test board

New test board is being designed by the KIP electronics workshop

<u>Allows to validate chip in lab-setup</u>

- Charge injection connectors
- Single SiPMs (pin headers)
- ADC test channel connectors
- Test both read out options (I^2C, LVDS), analog monitor outputs

→ *Validate chip in lab setup*
Noise, Dynamic range, Powergating behavior ...

Test performance under realistic conditions

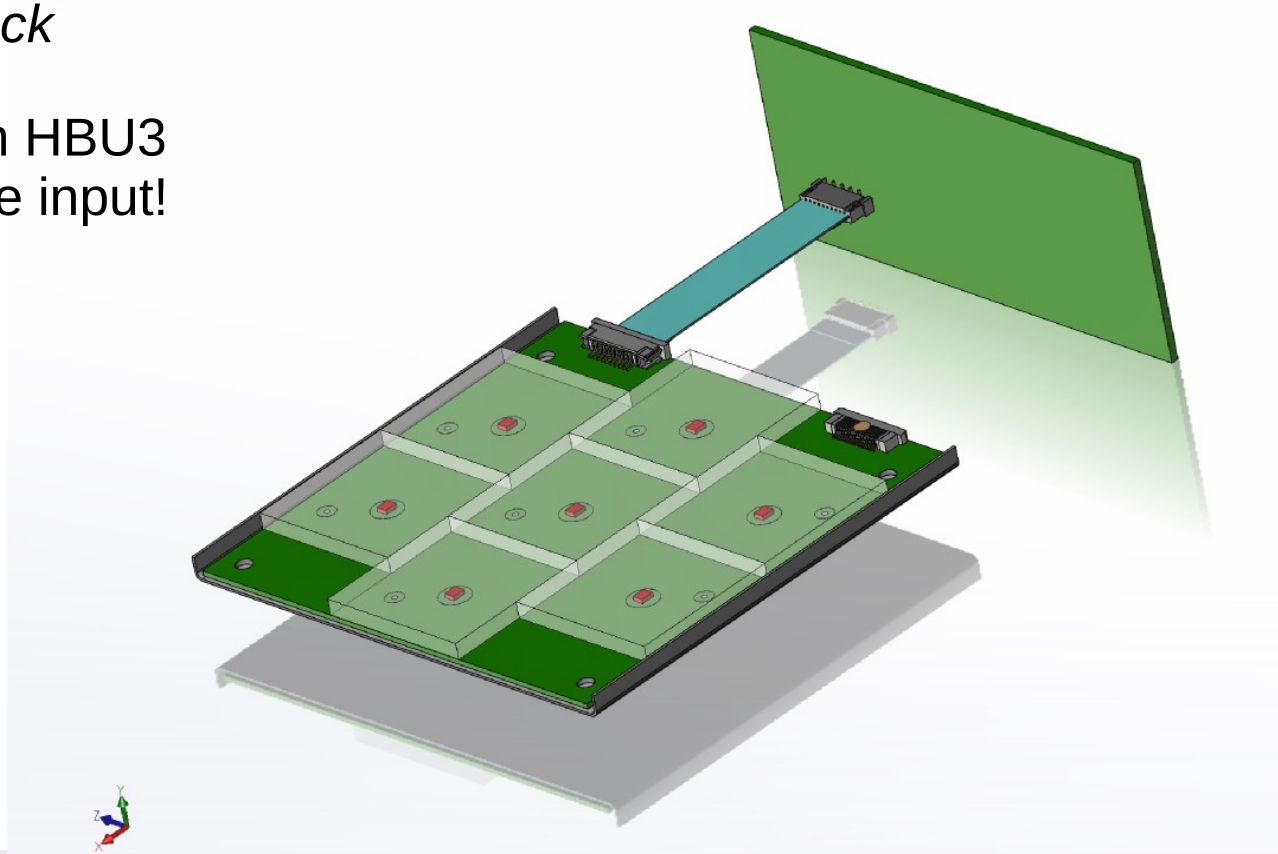
KLauS4 test board

Compatibility with CALICE HBU dimensions

- Possibility to participate in future CALICE testbeam campaigns
- SMD MPPC pads distribution similar to HBU

- Form factor & overall height *(PCB thickness, component height) allow insertion into EUDET stack*

- LED system design taken from HBU3
  Thanks Mathias & Katja for the input!



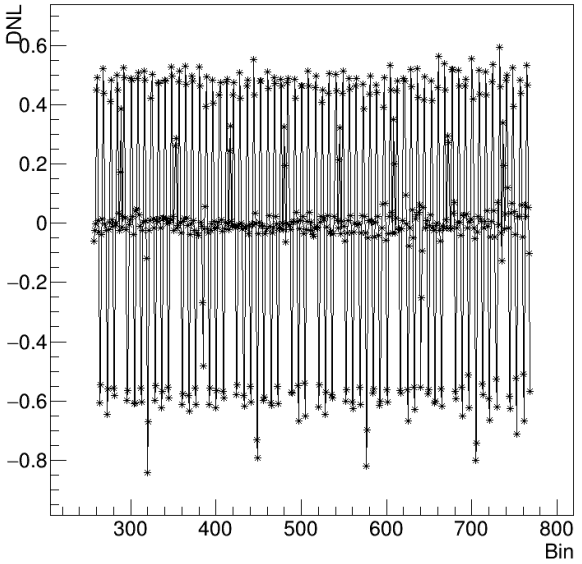
Summary & further development

- 7 channel chip will arrive this month
- Full characterization until end of Q1 2017

- Participation in following test beam campaigns planned
- 36 Channel version available until end of 2017 / beg. 2018

Backup slides

SAR ADC development for KLauS



1 ADC per front-end channel

Development of low power,
fully differential SAR-ADC

Two operation modes:

MIP quantization – **10bit resolution**

9+1(sign) bit SAR ADC

SiPM gain calibration – **12bit resolution**

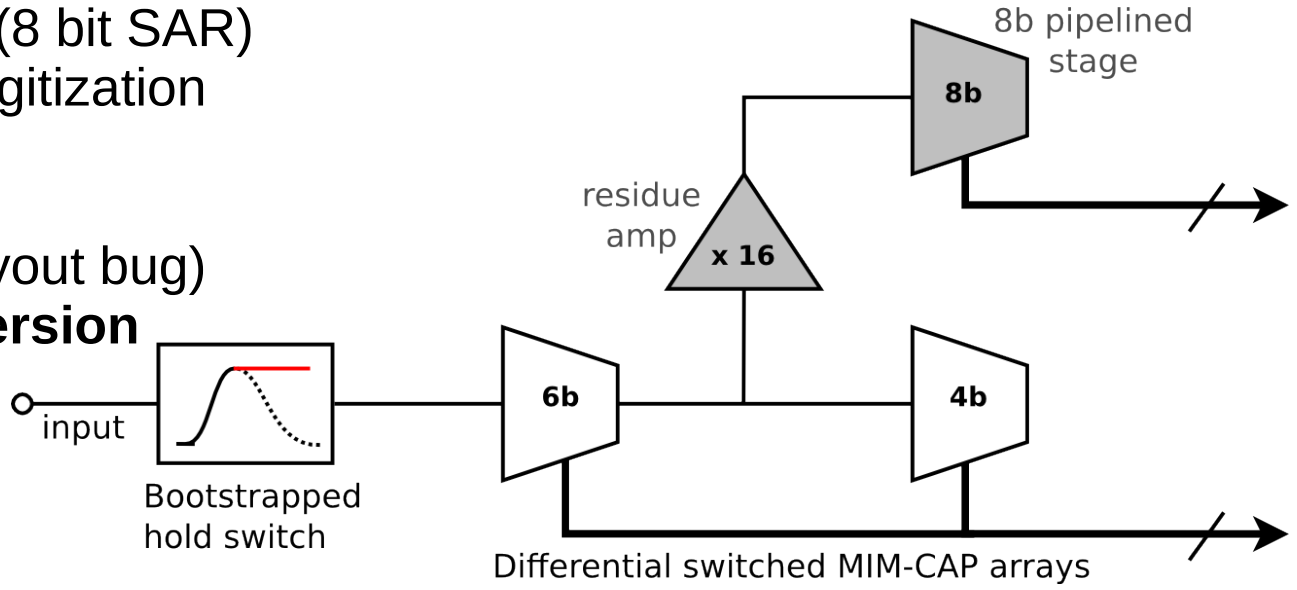
Additional pipelined stage (8 bit SAR)

Residue amplification & digitization

First prototype:

DNL larger than expected (layout bug)

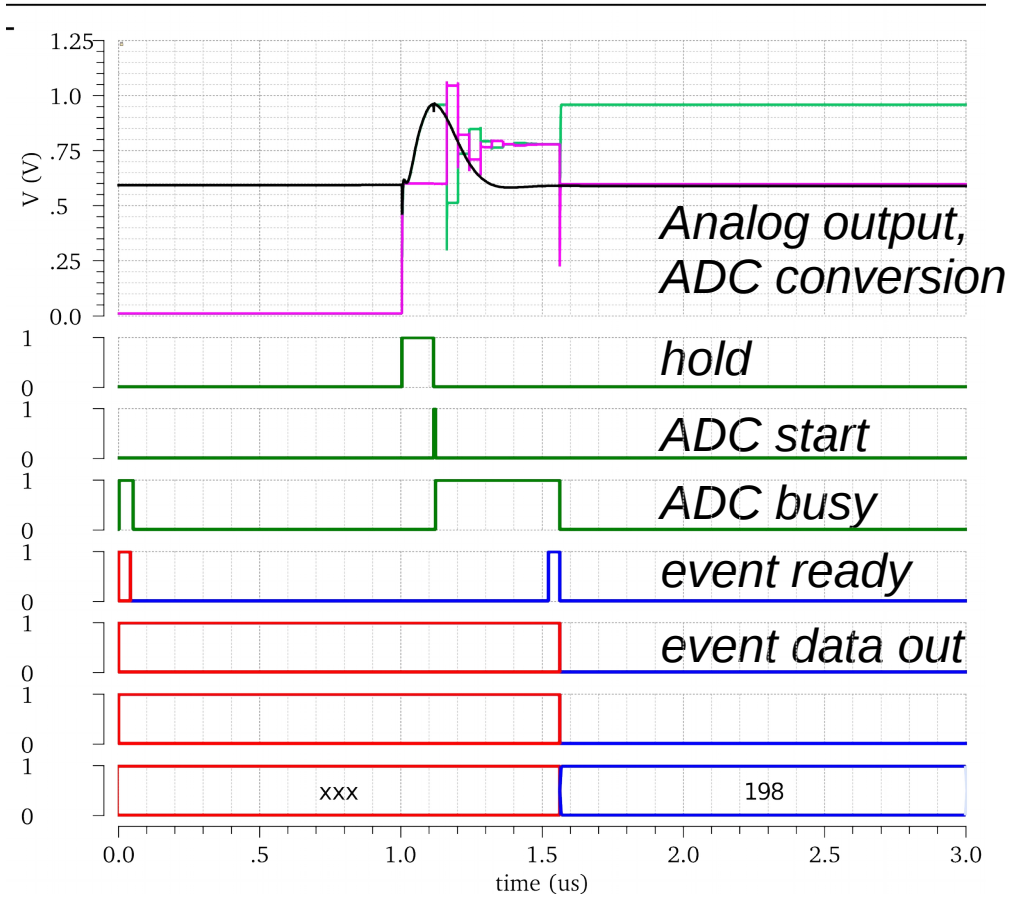
→ **Improved layout in new version**

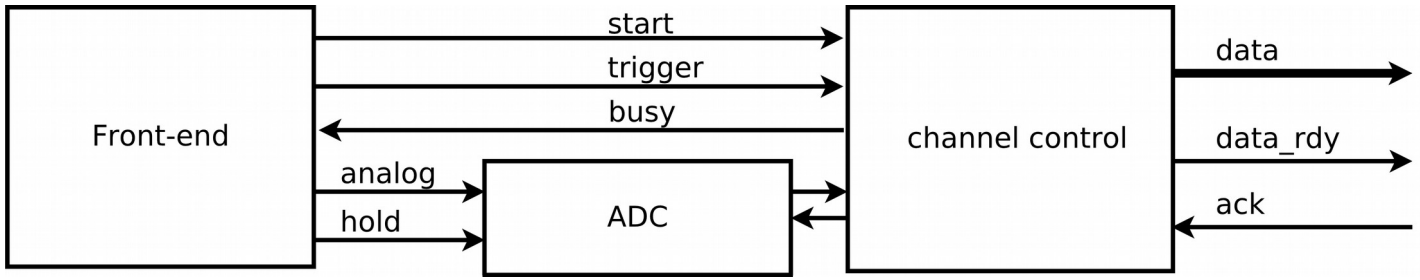


Front-End, ADC & channel digital control

Digital sources from front-end:
- External / self generated trigger
- Gain selection result
- Hold & Start signal for ADC

FE hitlogic block:
→ Initiate conversion after peak sampling
- Handshake with ADC control: start, busy
- Mask trigger pulses while ADC is busy



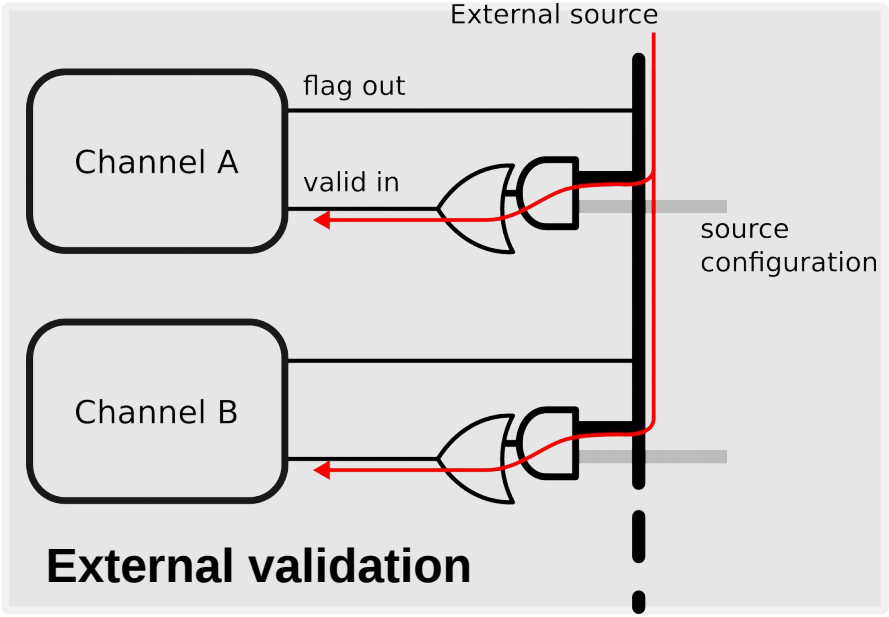


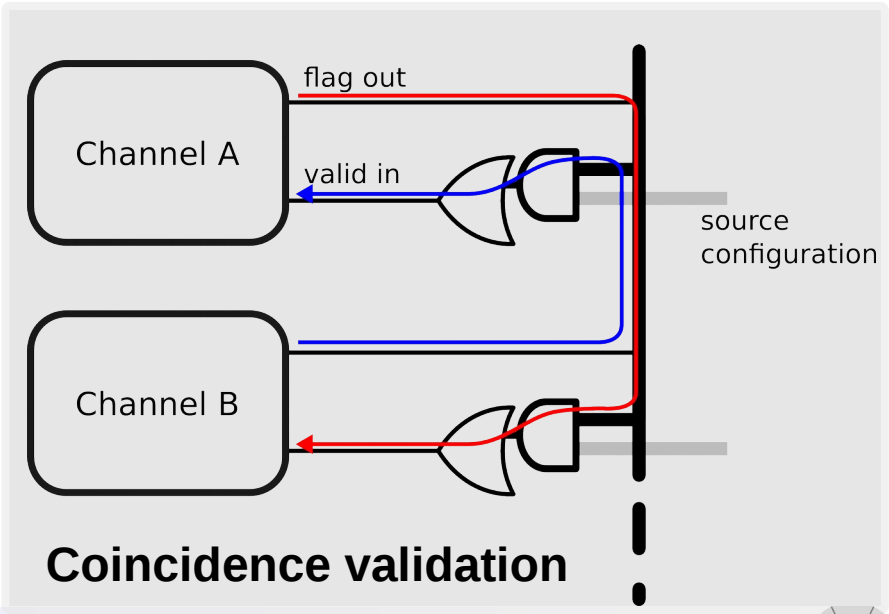
L0 & Coincidence event validation

First level event validation:
No validation flag - ADC conversion canceled
→ Also reduces dead time

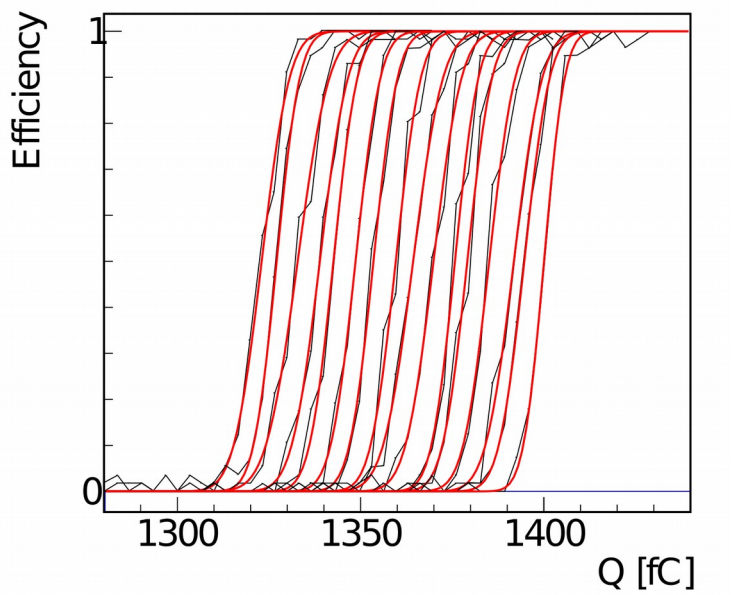
Validation signal sources:
- External source
- Internal validation:
  Coincident events between channels
  Configurable OR of group of 12

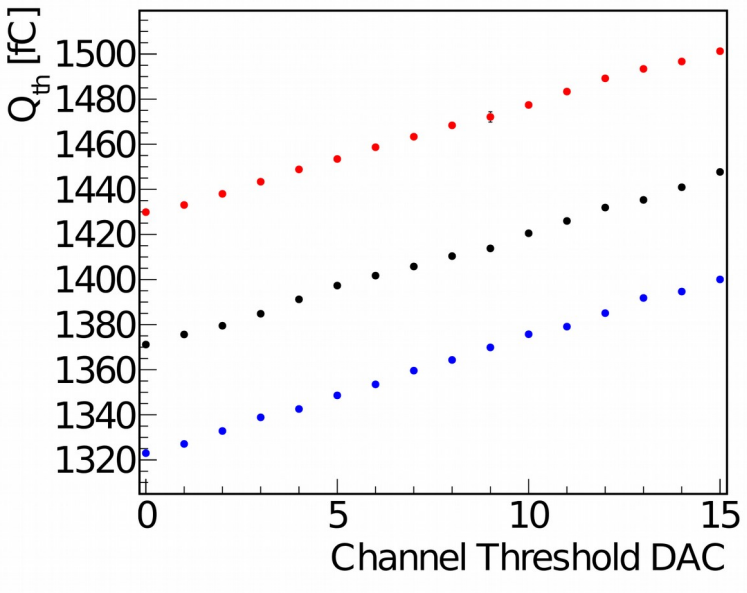
→ Validation window 1..8 Clock cycles
→ External validation:
  maximum delay: ~300-500ns





Trigger branch: Threshold setting





Two DACs to tune threshold:
- Global 6 bit DAC + scaling (for all channels)
- 4 bit DAC for fine-tuning (each channel)

→ Charge noise: 8fC typ.
→ Threshold configuration resolution (4b DAC): 5fC

Data structures

Channel hit information comprised of 38 bit

To send the data byte-wise, two bits are appended at the end → 5 byte / hit

GRP ID	CHAN_ID	Gain select	ADC busy hit	Main ADC	PIPE ADC	TDC CC
2 bit	4 bit	1 bit	1 bit	10 bit	8 bit	12 bit

LVDS interface:

- 160Mbit/s, 8b10b encoded data stream
- Frame structure consist of

  Header (clock synchronization, frame size, frame ID), event data and Trailer (CRC16)

I^2C interface:

- Raw I^2C read access from the chip,
- When buffer empty: Invalid events flagged by Channel number == 63