FPGA
STATUS WORK IN IFJ PAN

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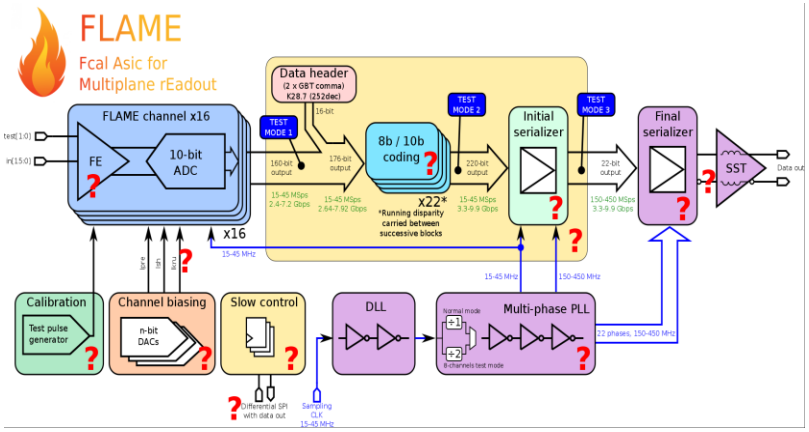
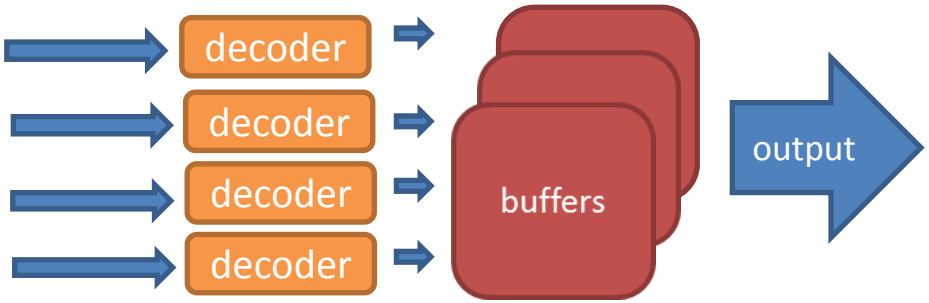
The new readout board design - elements

FLAME system (AGH UST)



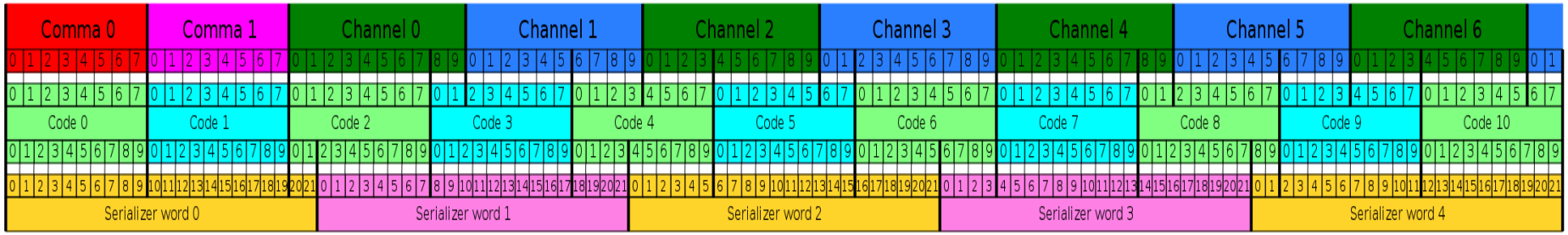
Data received from ASIC's of the FLAME readout sytem

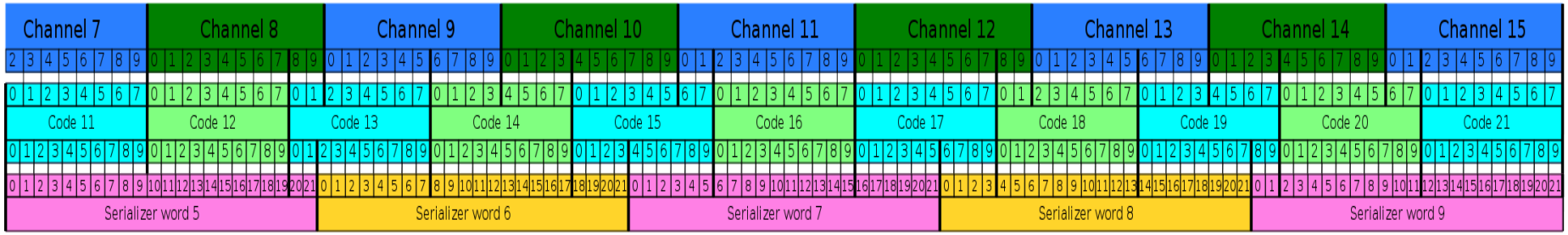
FPGA board (IFJ PAN)



Others . . .

ASIC output: 220 bits in 22 words (16 channels x 10b + 2 x 8b (commas) + coding (8b/10b)





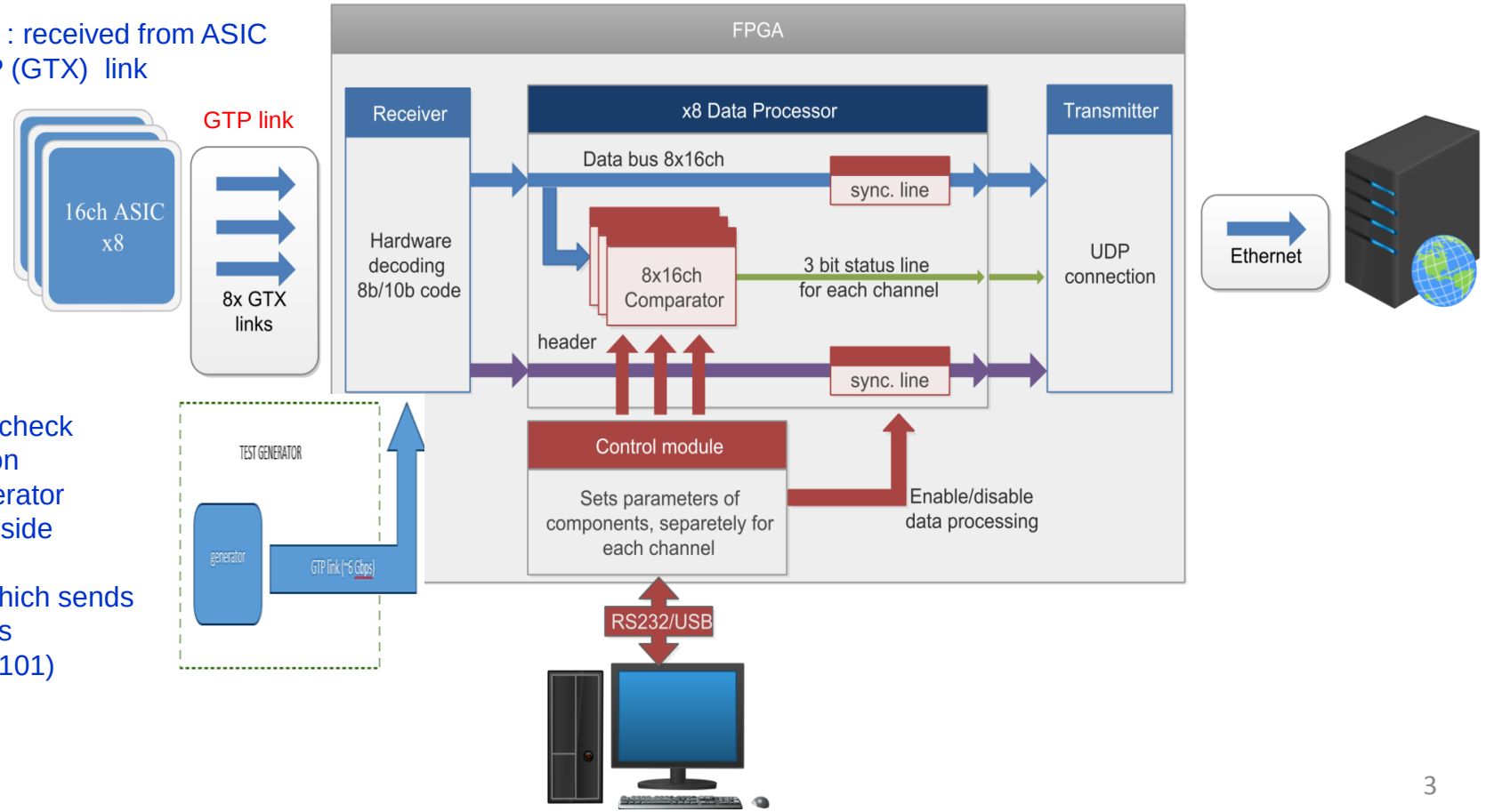
FPGA - Data flow

In working with FPGA the whole project is devided to smaler modules and XILINX provides special functions to support them.

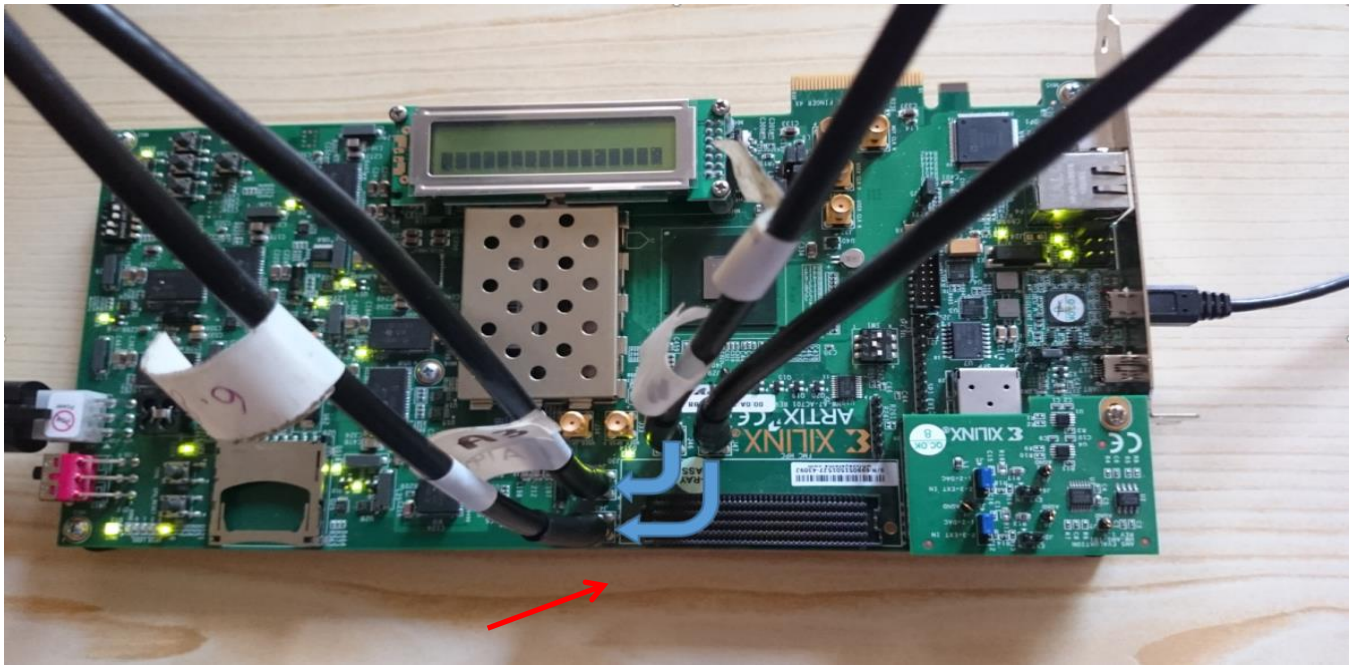
Schematic view of the data flow within the FPGA,
with some active modules between which the data flow take place

Real data : received from ASIC using GTP (GTX) link

Test data: check transmission using generator available inside the FPGA structure which sends string of bits (like 01010101)



FPGA - motherboard test of the transceiver



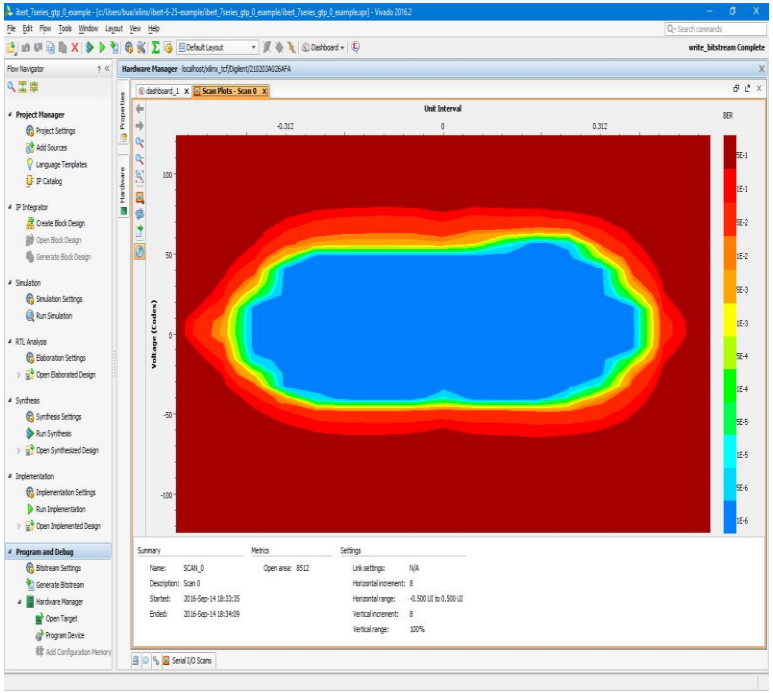
Arrows show direction of movement of the signal

- Used a transceiver on the board with the transmitter connected to the receiver
  Tests of receiver were started after the implementation the transmitter
- At this stage we have defined a sequence of bits thad are send and verify at receiver.
  Everything works also on a single cable
- Work is ongoing on the final generator target data frames with 220 bits coming from ASIC.
  It will be string of bits (with comma's inside) and receiver should recognize where is a comma what allowing for proper bits interpretation in this string until the new comma will appear

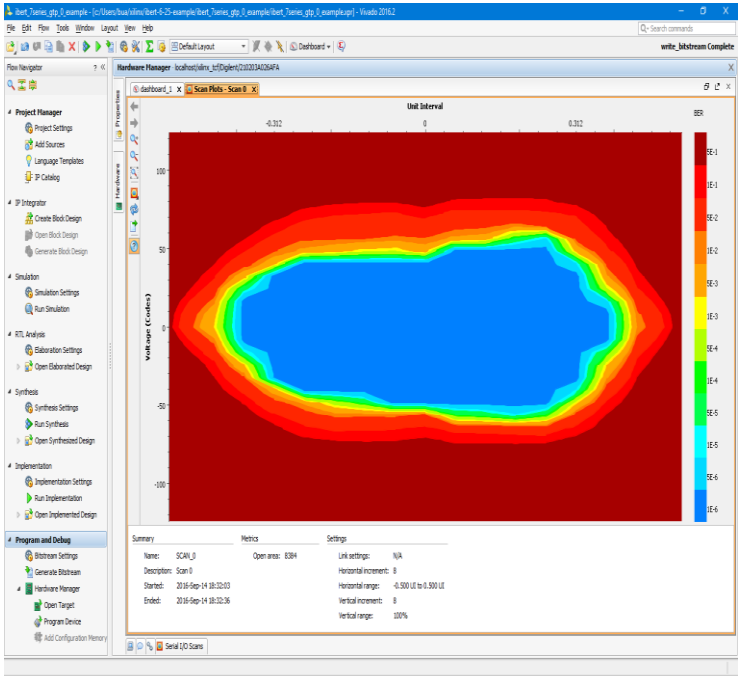
Evaluation board contains FPGA-Artix 7 XC7A200T (XILINX) with GTP transceivers with the maximum bandwidth 6.6 Gb/s.
For 1 ASIC working with 20 MHz sampling, the expected rate is 4.4 Gb/s and GTP link is enought for tests it and for SMA connectors only one transceiver can be set

Transceiver test - 3.125 Gb/s rate

The bit error ratio mesurement. A map shows the ratio of the error count to the sample count, and a color map represents log10(BER) – bit error ratio. The blue color represents area with a small number of errors and red one where attempt to read signals gives the only errors (using IBERT function)



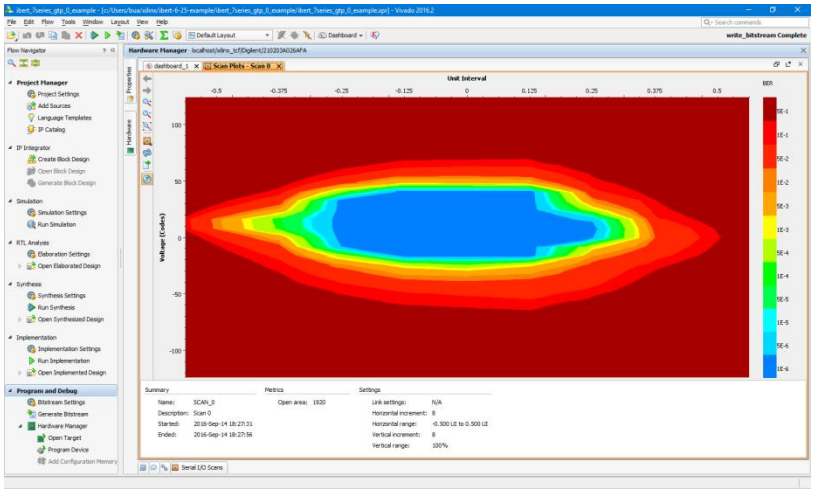
thin cable



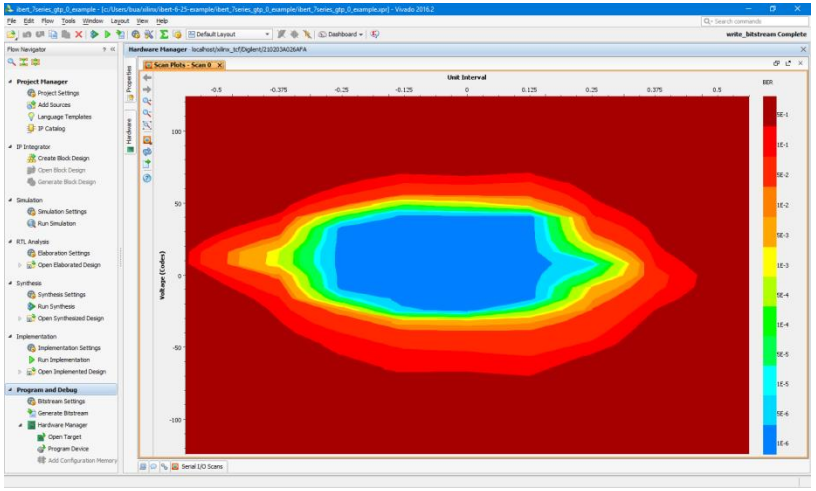
thick cable

It is not observed change in the signal
transmission quality for cables with different thickness

Transceiver test (cd) - 6.25 Gb/s rate

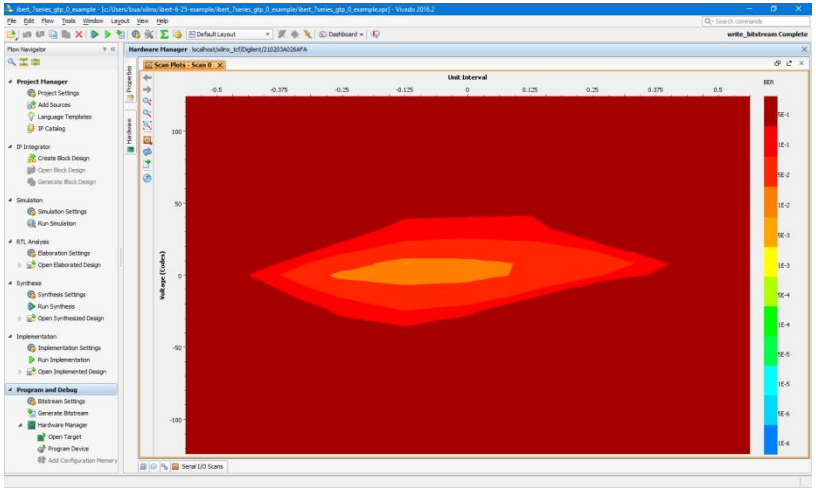


thin



thick

Cables of different thickness: the change in signal qulity for the thin cable
Large effect can be expected for the long cables

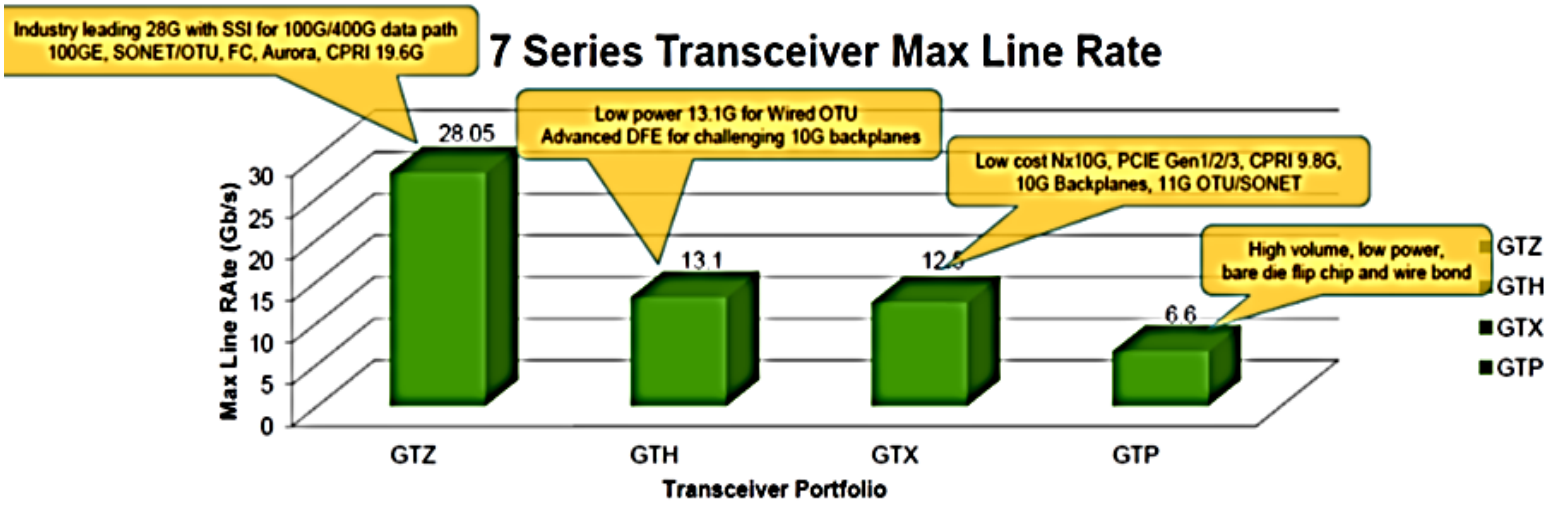


Big distortion of the signal shape
when cables had different length

Other Xilinx FPGA board

For developing the project of the new readout board another FPGA board is considered

Xilinx 7 Series Transceiver - Portfolio and Bandwidth



- 7 series offers a full transceiver portfolio for variant customer needs
  - Ultra-high performance GTZ: **28.05Gb/s X 16**
  - High-end Low-power GTH: **13.1Gb/s X 96**
  - Mid-Range GTX: **12.5Gb/s X 32**
  - High-Volume Low-Power GTP: **6.6Gb/s X 16**
- Virtex-7 HT has up to **2.802Tbps** total transceiver bandwidth
  - 16 GTZ and 72 GTH transceivers

SUMMARY

- Test of transceiver on the FPGA board was curried out for simple bits configuration using internal generator.
  No problem was found, everything works properly

- Work is ongoing on the generator which will provide the bit string structure, the same as those received from real ASIC output. This will be implementation a piece of FPGA structure