AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

Readout ASIC for LumiCal

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On behalf of FCAL Collaboration

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Agenda

- New readout for LumiCal:
  1) Motivation
  2) FLAME ASIC architecture
  3) FLAME blocks development

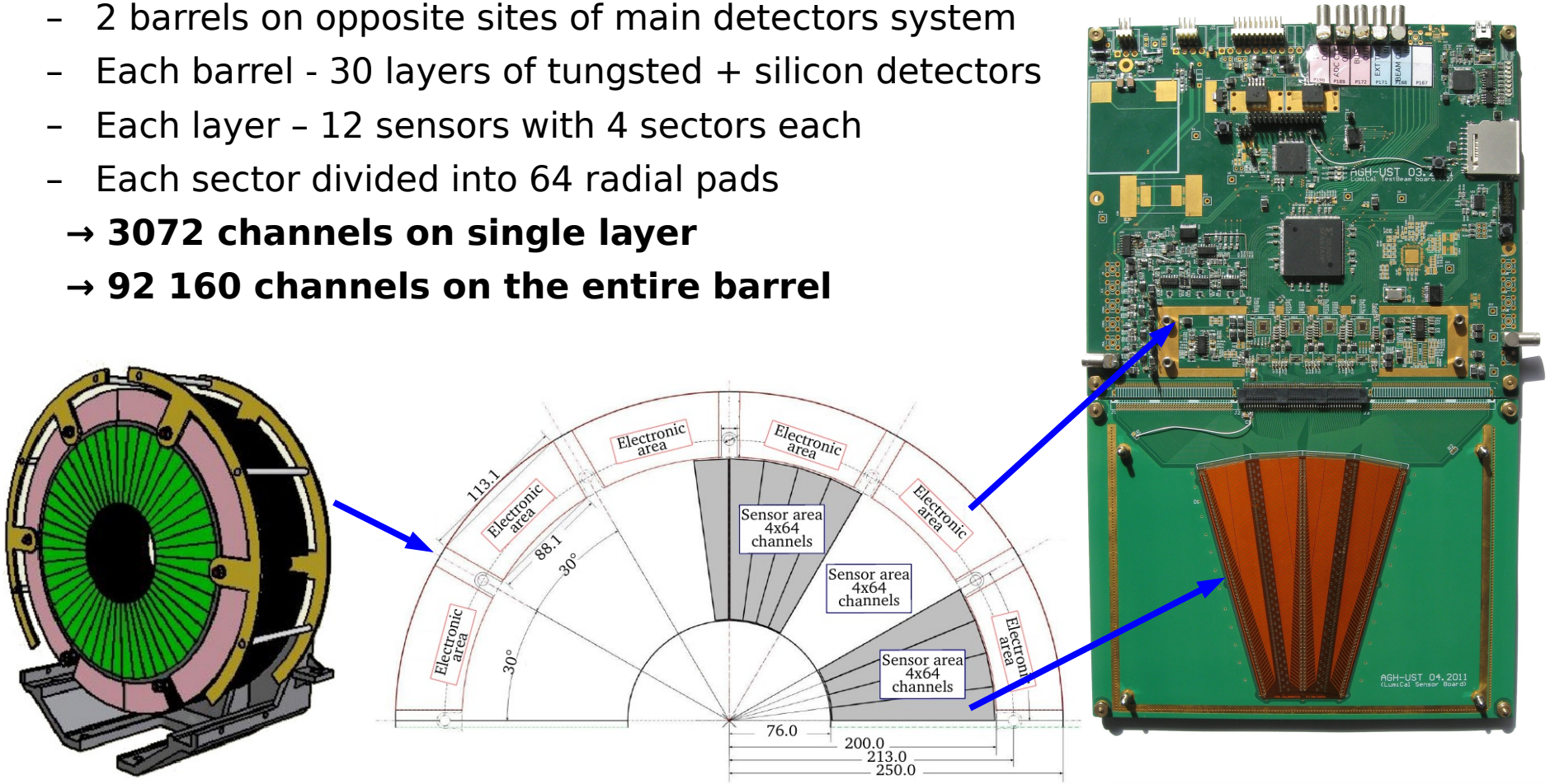
LumiCal – dedicated luminosity calorimeter

- Dedicated luminosity calorimeter **LumiCal**:
  - 2 barrels on opposite sites of main detectors system
  - Each barrel - 30 layers of tungsted + silicon detectors
  - Each layer – 12 sensors with 4 sectors each
  - Each sector divided into 64 radial pads

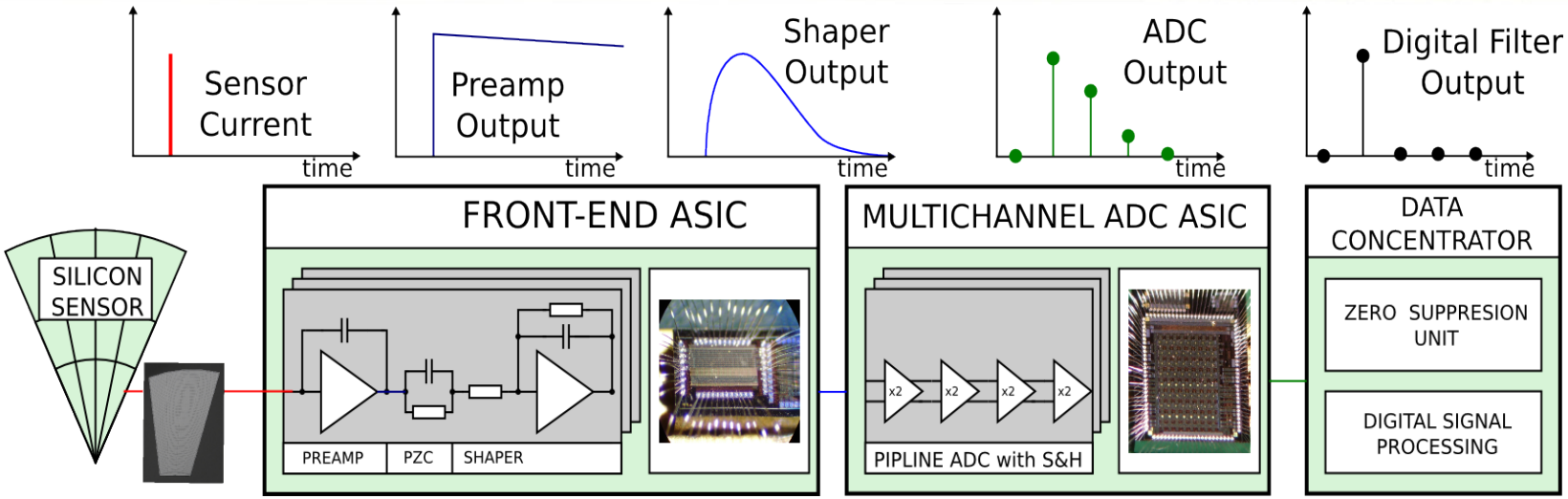
  → 3072 channels on single layer

  → 92 160 channels on the entire barrel

Old readout board –
4 x 8-channel ASICs



LumiCal readout chain



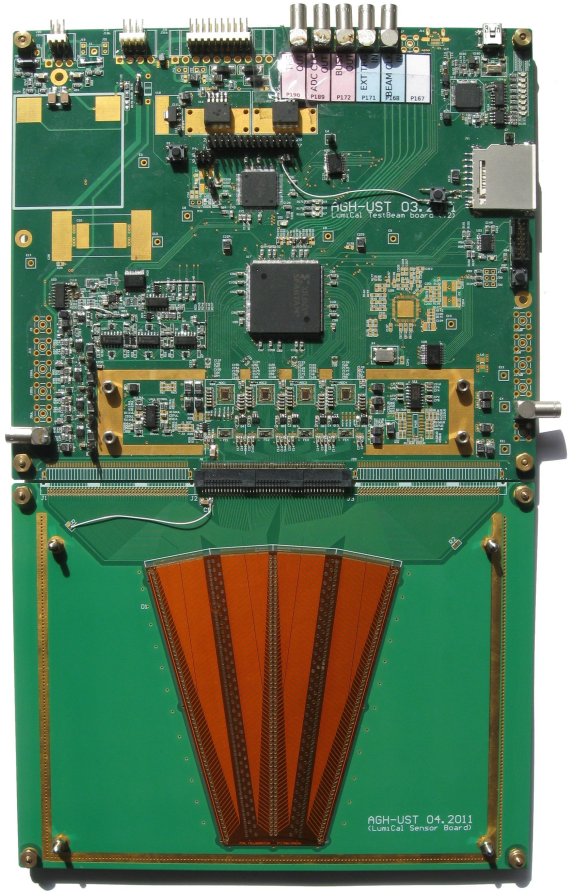
Existing (old) LumiCal detector readout comprises:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW (**AMS 0.35um**)
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz (**AMS 0.35um**)
- FPGA based data concentrator and further readout

New development for LumiCal detector readout:

- 16 channel FLAME ASIC comprising all functionalities – Front-end & ADC in each channel + fast serializer + biasing DACs + slow control, etc. (**CMOS 130nm**)
- New FPGA based DAQ

New LumiCal readout – motivation

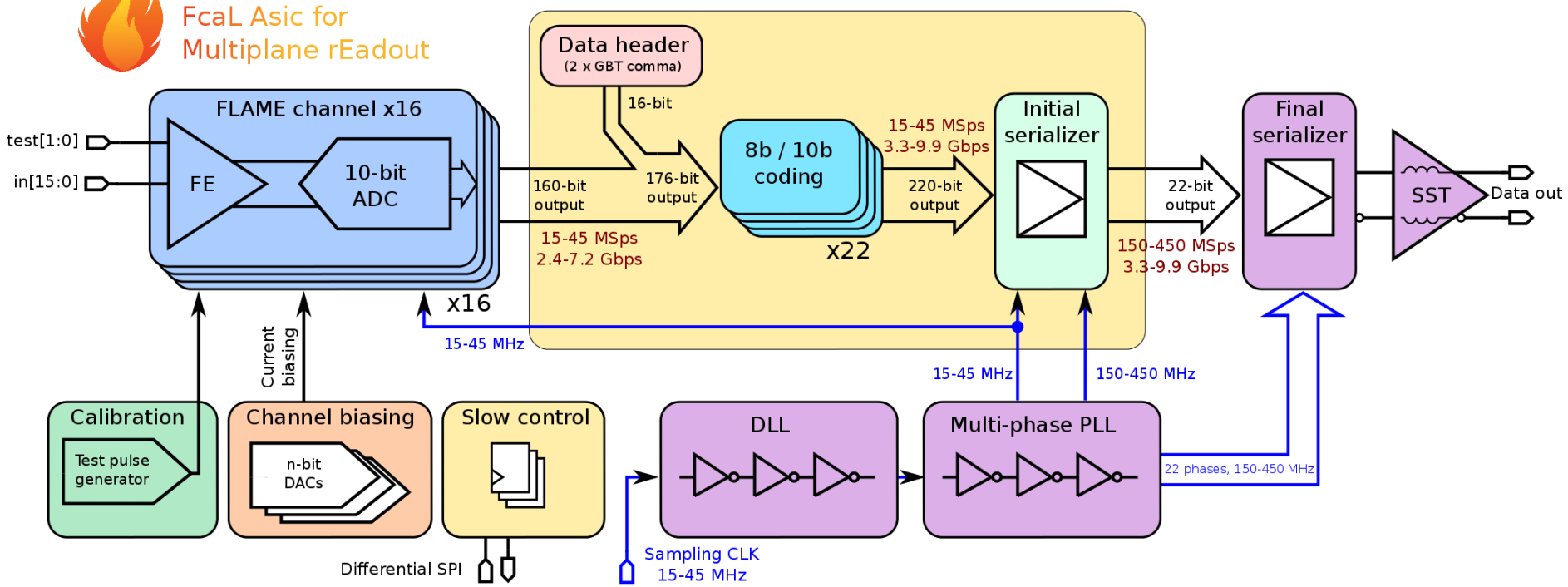


Weak points of present **LumiCal** readout system:

- Readout board too thick – 4.5 mm thickness required
- Sensor board too thick – 1 mm thickness required
- Present 8-channel FE and ADC ASICs:
  - External biasing requires high PCB complexity
  - FE ASIC has single-ended outputs – only half of ADC dynamic range used
  - ADC output data serialization – one data link per channel + clock + data start (10 links/ASIC) – too many output signals
  - Old 350 nm technology – high power consumption and lack of radiation hardness

FLAME – FcaL Asic for Multiplane rEadout ASIC architecture

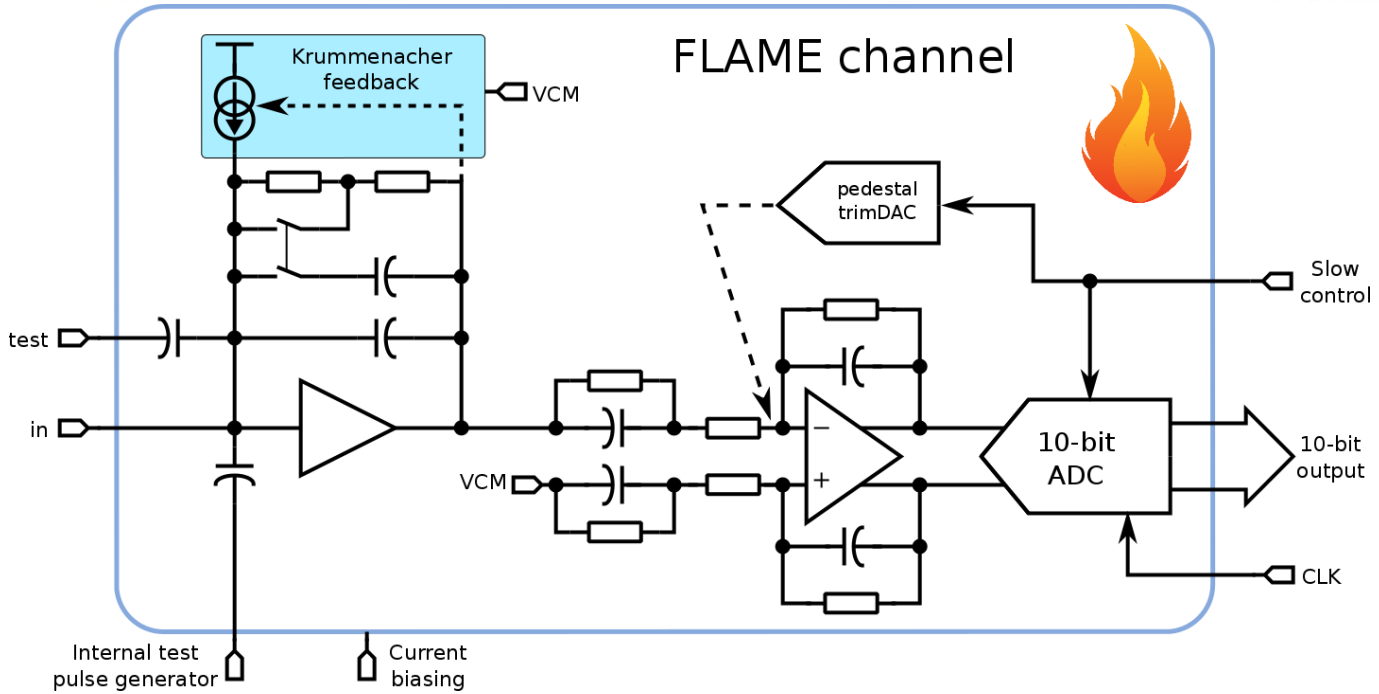
FLAME
FcaL Asic for Multiplane rEadout



- Complete readout ASIC integrating whole functionality (biasing, calibration, etc.)
- 16 mix-mode channels comprising:
  - Variable gain front-end
  - 10-bit SAR ADC

- Data encapsulation and 8b/10b coding (according to the Xilinx MGT specification)
- DLL for clock alignment (for synchronous sampling)
- Multi-phase PLL based fast serializer (up to 10 Gbps)
- Fast SST driver (up to 10 Gbps)

FLAME – FcaL Asic for Multiplane rEadout Channel architecture

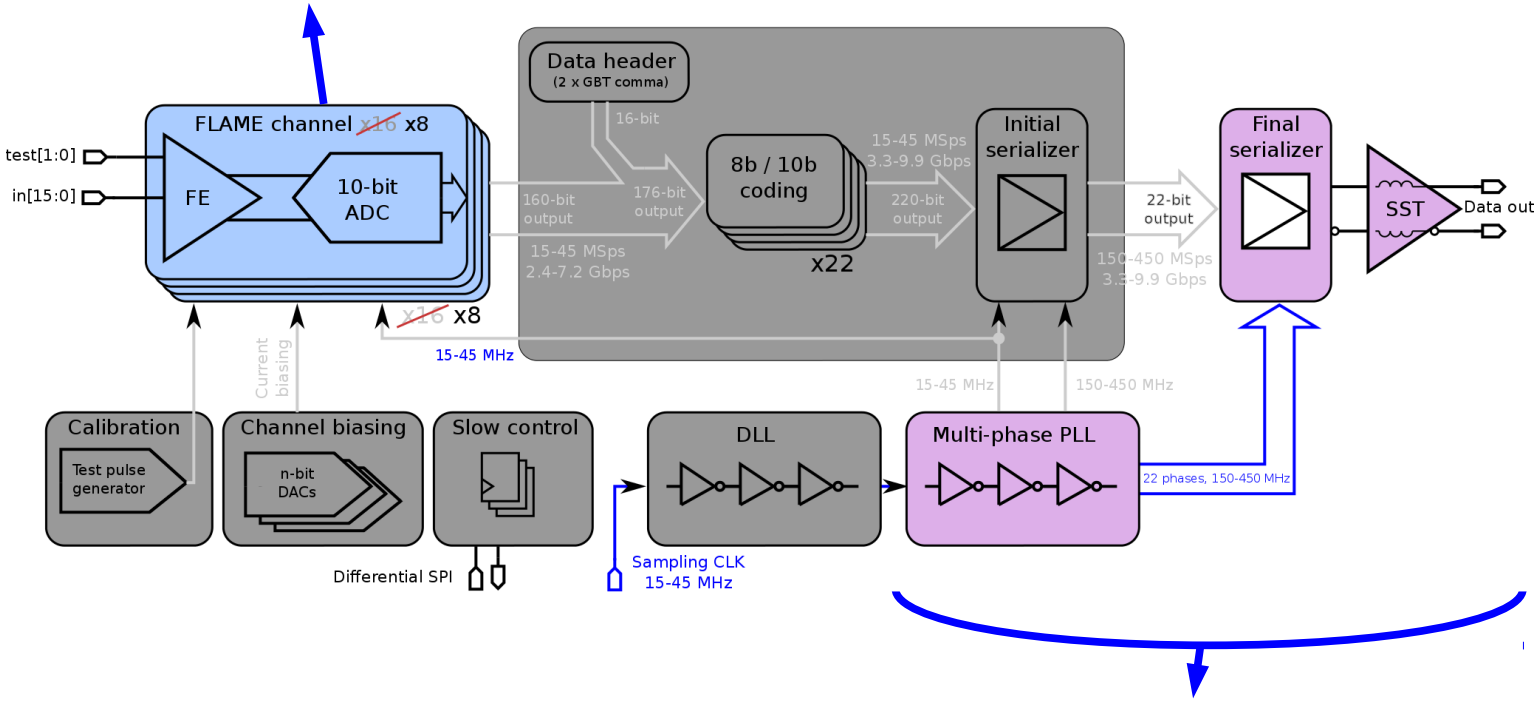


- Analogue front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – MIP sensitivity for calibration
    - Low gain – for shower development (up to 6 pC)
  - Differential CR-RC shaper with 50ns peaking time
  - Krummenacher feedback and pedestal trim DAC

- 10-bit multichannel SAR ADC
  - Sampling rate up to 40 MSps
  - DNL, INL < 0.75 LSB
  - ENOB > 9
  - Ultra low power consumption (below 1 mW per channel at 40 MSps)

Current development in CMOS 130nm 8-channel FLAME v0 and serializer ASICs

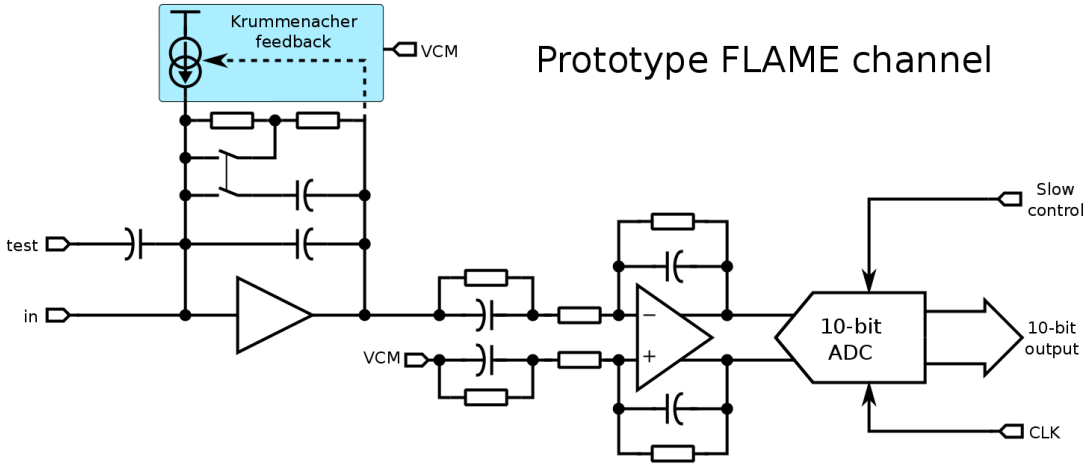
- Prototype ASIC comprising 8 almost fully functional FLAME channels:
  - Front-end with variable gain charge preamplifier and differential CR-RC shaper, Tpeak = 50ns
  - 10-bit multichannel SAR ADC
  - Test backend – same as in old readout board (one link per each channel)

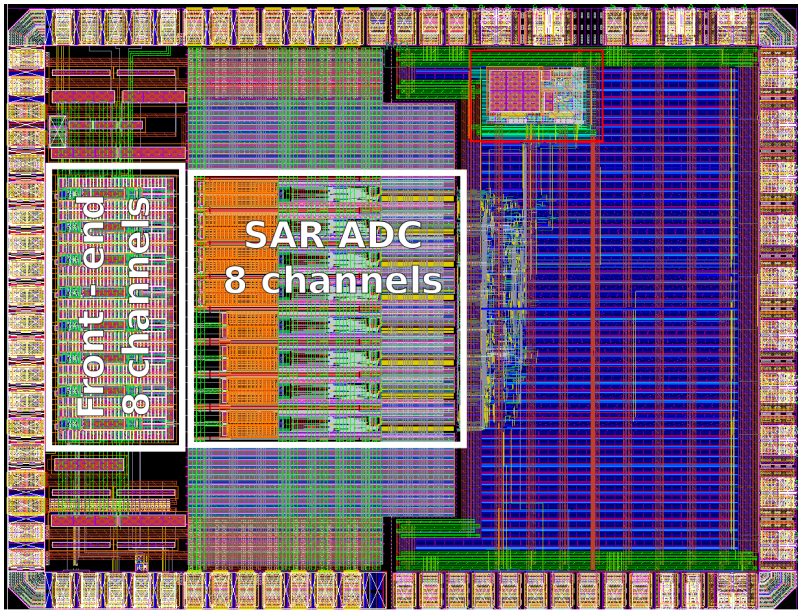


Prototypes submitted on November 2015, test board developed, tests already started...

- Prototype serializer ASIC comprising:
  - Fast, ultra low power, ultra low jitter multi-phase PLL
  - Fast serializer 22b → 1b
  - Fast SST driver

Current development in CMOS 130nm 8-channel FLAME v0





2600 µm x 2000 µm

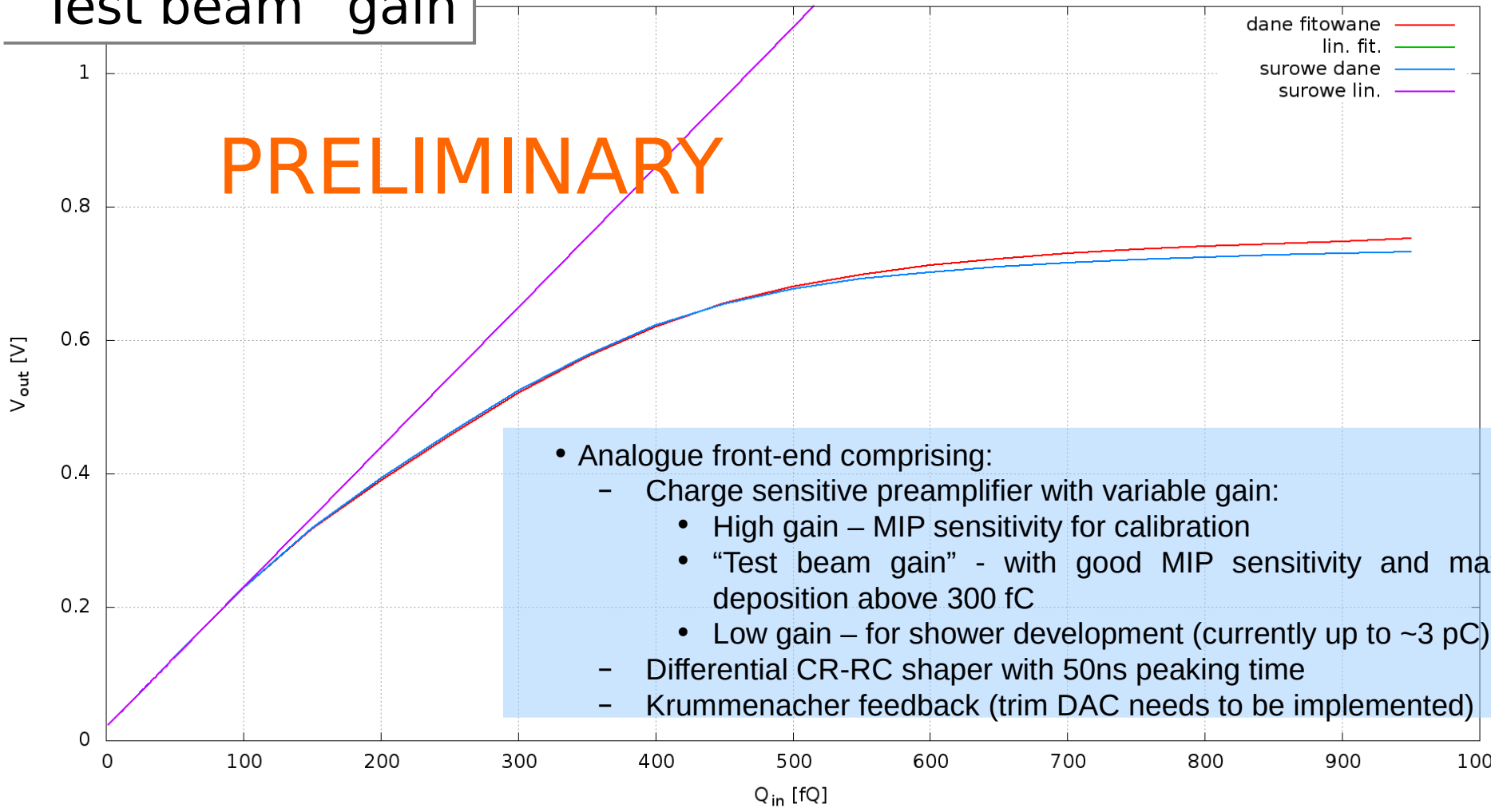
8-channel FLAME v0 prototype:

- Charge sensitive preamplifier:
  - Cdet ≈ 5 – 50 pF
  - Variable gain (calibration and physic mode)
  - ENC ≈ 950 e^- at Cdet = 20 pF in calibration mode
- Differential first order shaper (Tpeak ≈ 50 ns)
- Front-end power consumption ≈ 1.2 mW per channel
- 10-bit SAR ADC
  - INL, DNL < 0.5
  - ENOB > 9.5
  - Power consumption ≈ 660 µW at 40 MSps
- Testing backend from ADC prototype

Design submitted on November 2015, tests already started...

FLAME blocks development in CMOS 130 nm
Analogue front-end

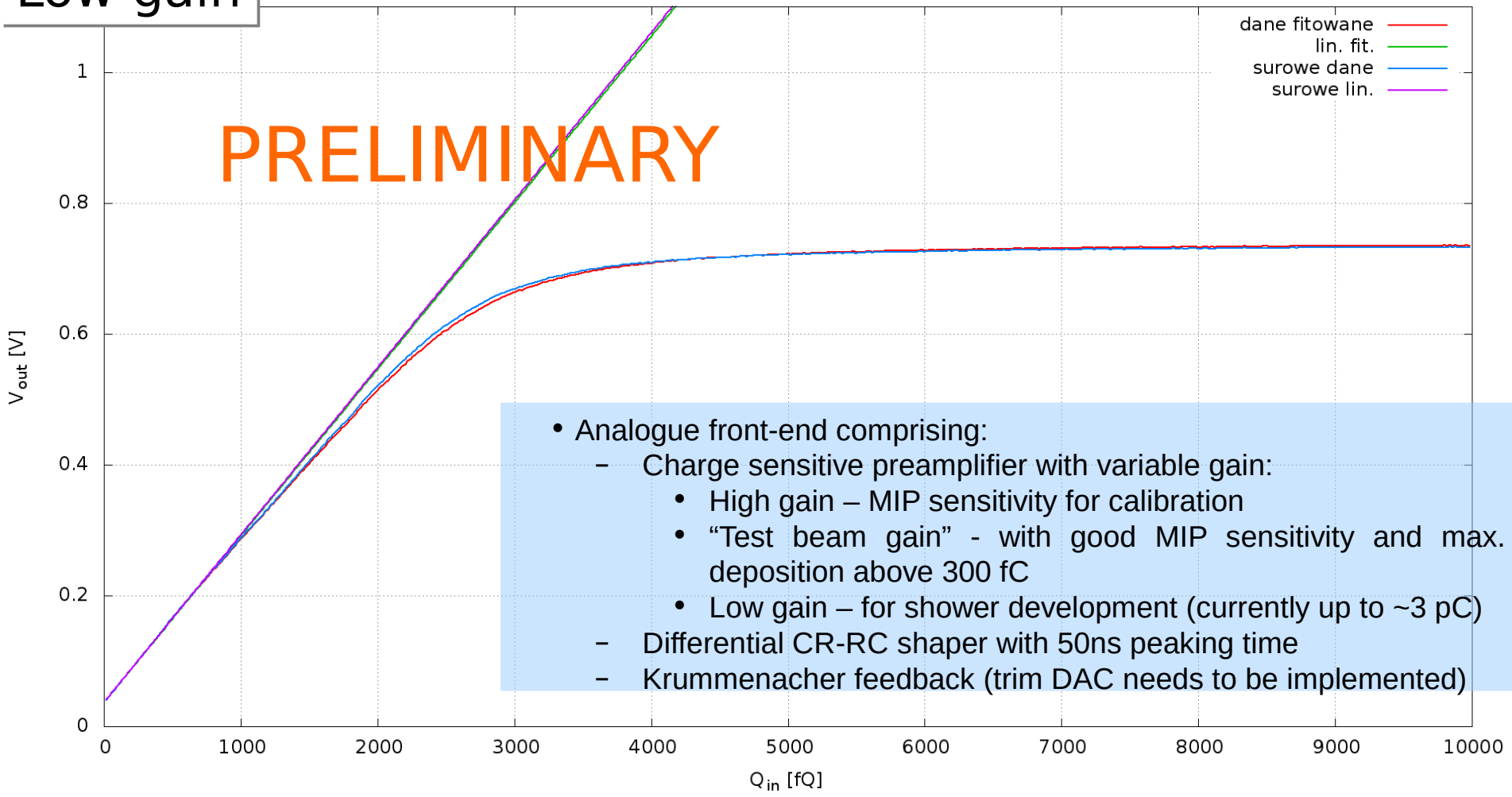
“Test beam” gain



- Analogue front-end comprising:
  - Charge sensitive preamplifier with variable gain:
    - High gain – MIP sensitivity for calibration
    - “Test beam gain” - with good MIP sensitivity and max. deposition above 300 fC
    - Low gain – for shower development (currently up to ~3 pC)
  - Differential CR-RC shaper with 50ns peaking time
  - Krummenacher feedback (trim DAC needs to be implemented)

FLAME blocks development in CMOS 130 nm
Analogue front-end

Low gain



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FLAME blocks development in CMOS 130 nm
Analogue front-end

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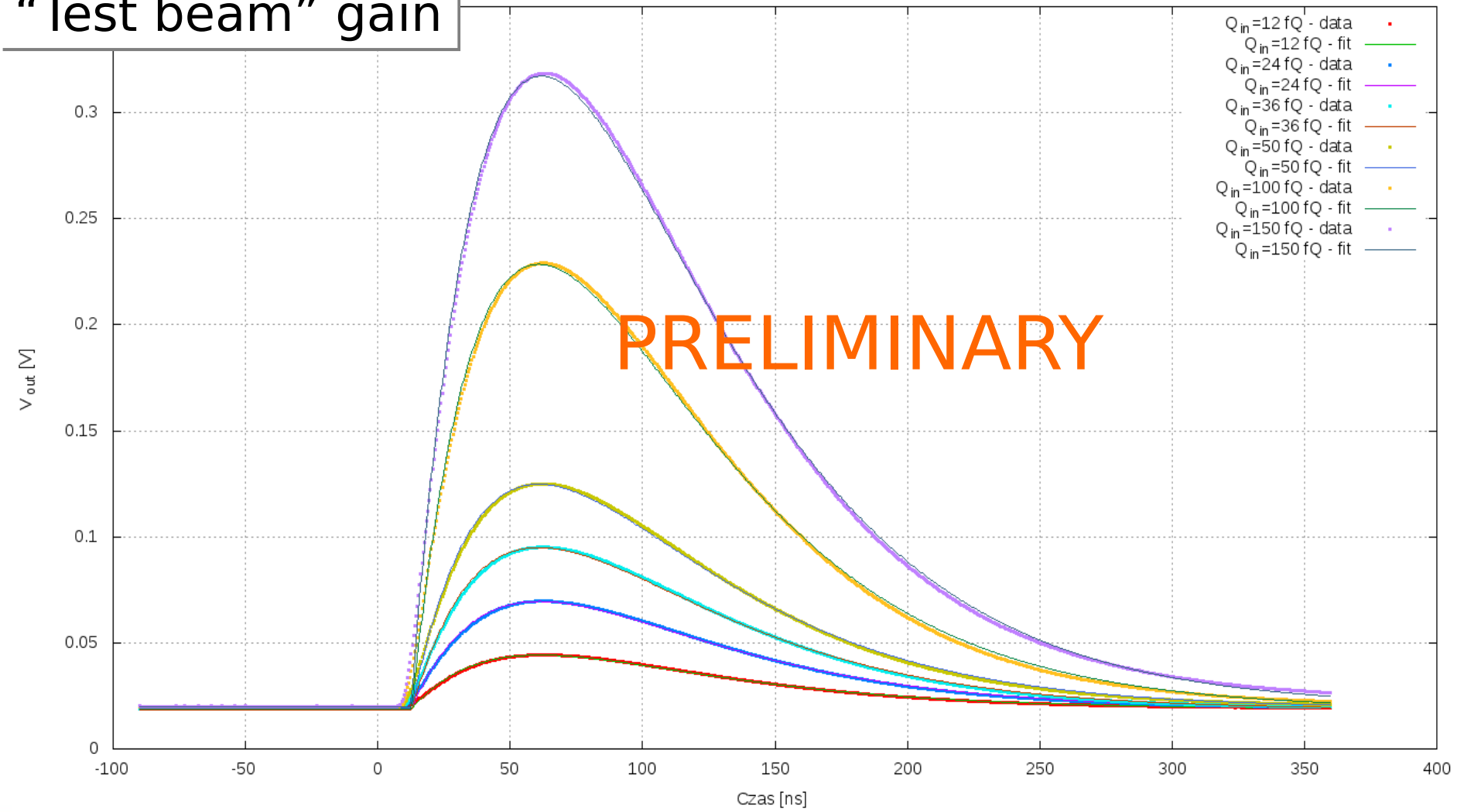
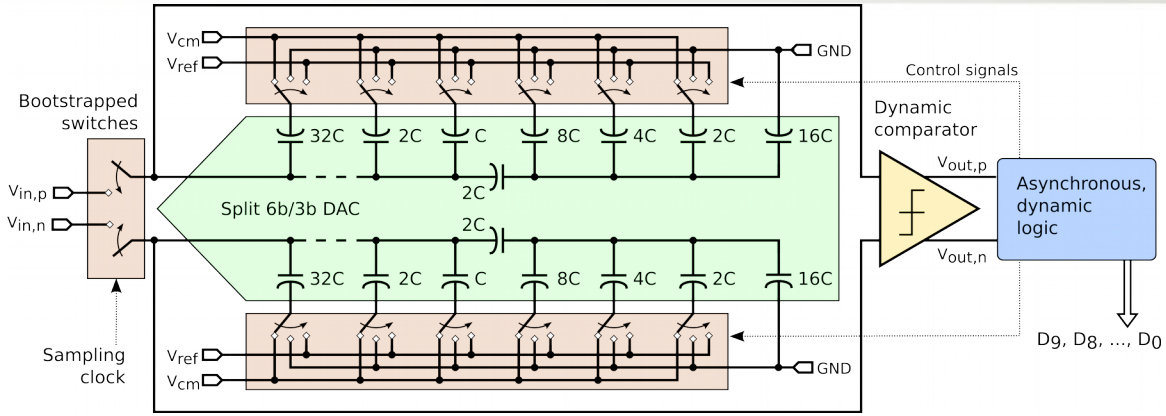


FLAME blocks development in CMOS 130 nm
Fast multichannel 10-bit SAR ADC

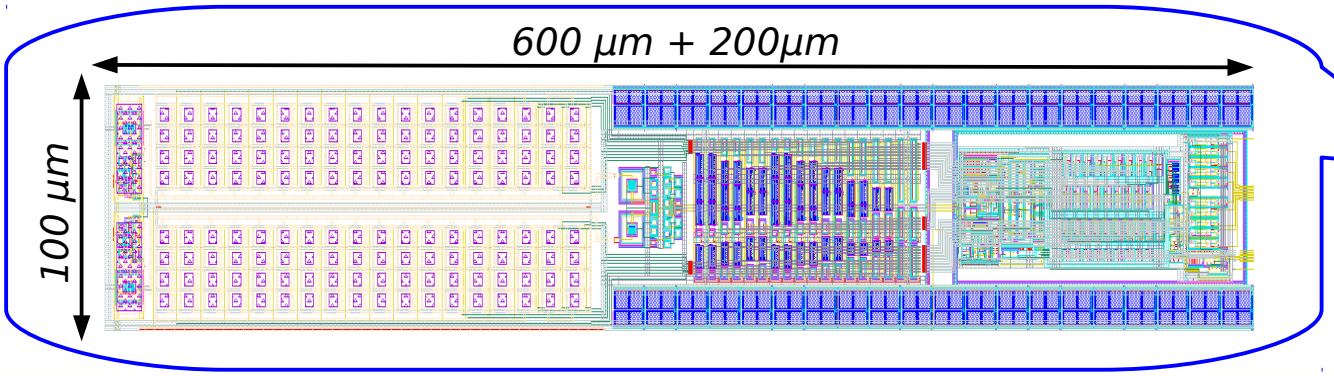


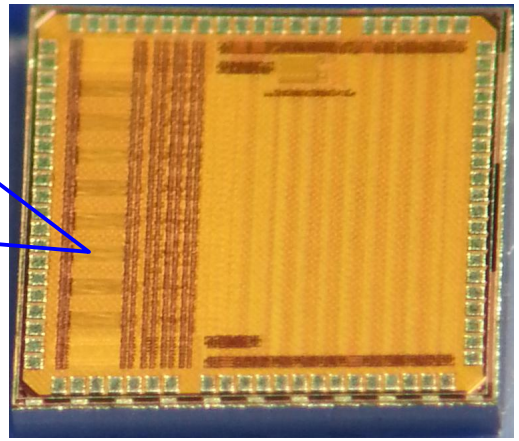
Design consideration:

- Technology CMOS 130 nm
- 8 SAR ADC channels
- Power scalable with sampling frequency (up to >40 MS/s)
- Power cons. <1mW@40MS/s
- Power pulsing (no clk=no power)

Architecture of 10-bit SAR ADC

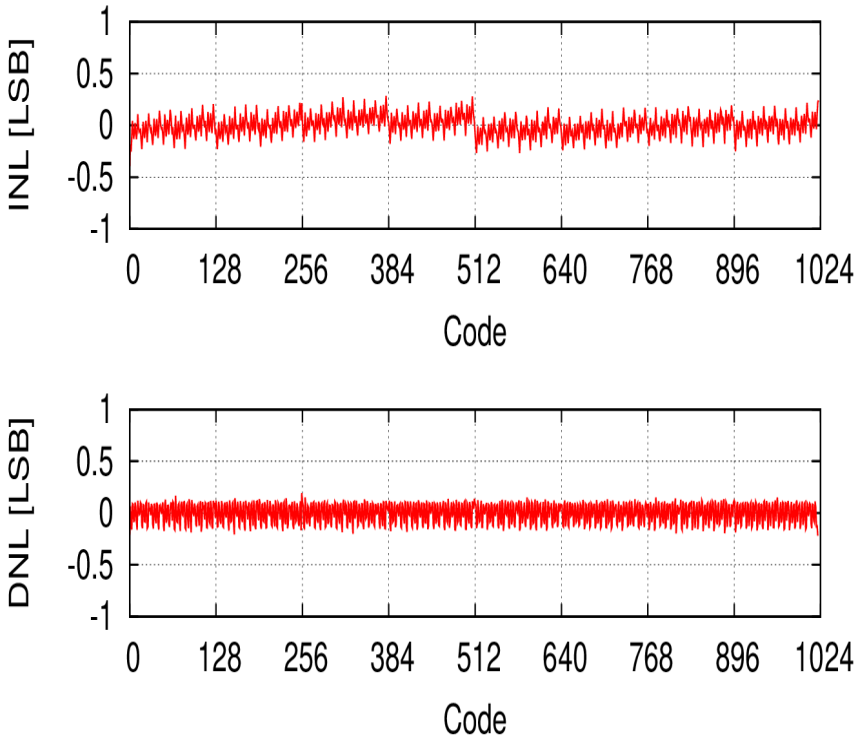
- Differential segmented/split DAC with MCS switching scheme – ***ultra low power***
- Dynamic comparator – ***no static power consumption, power pulsing (no clk=no power)***
- Asynchronous logic – ***no clock tree, power saving, fast***



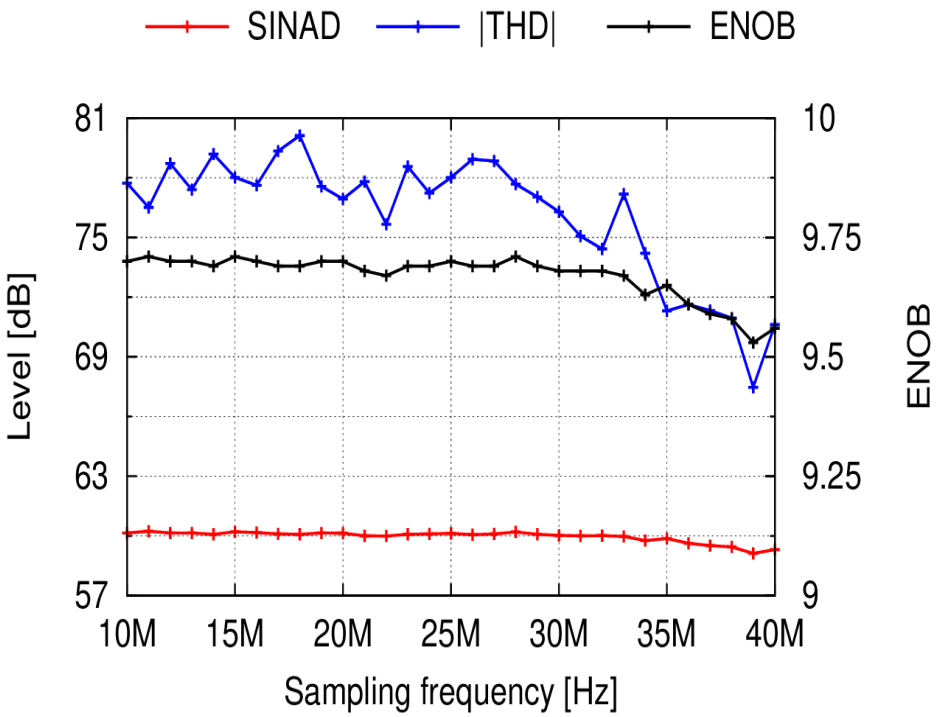


FLAME blocks development in CMOS 130 nm
Measurements of 10-bit SAR ADC

Static performance
example at 10 MS/s



Dynamic performance
scan over f_{sample} for f_{in} at 0.1 Nyquist



Excellent ADC performance: INL,DNL < 0.3 LSB and ENOB > 9.5

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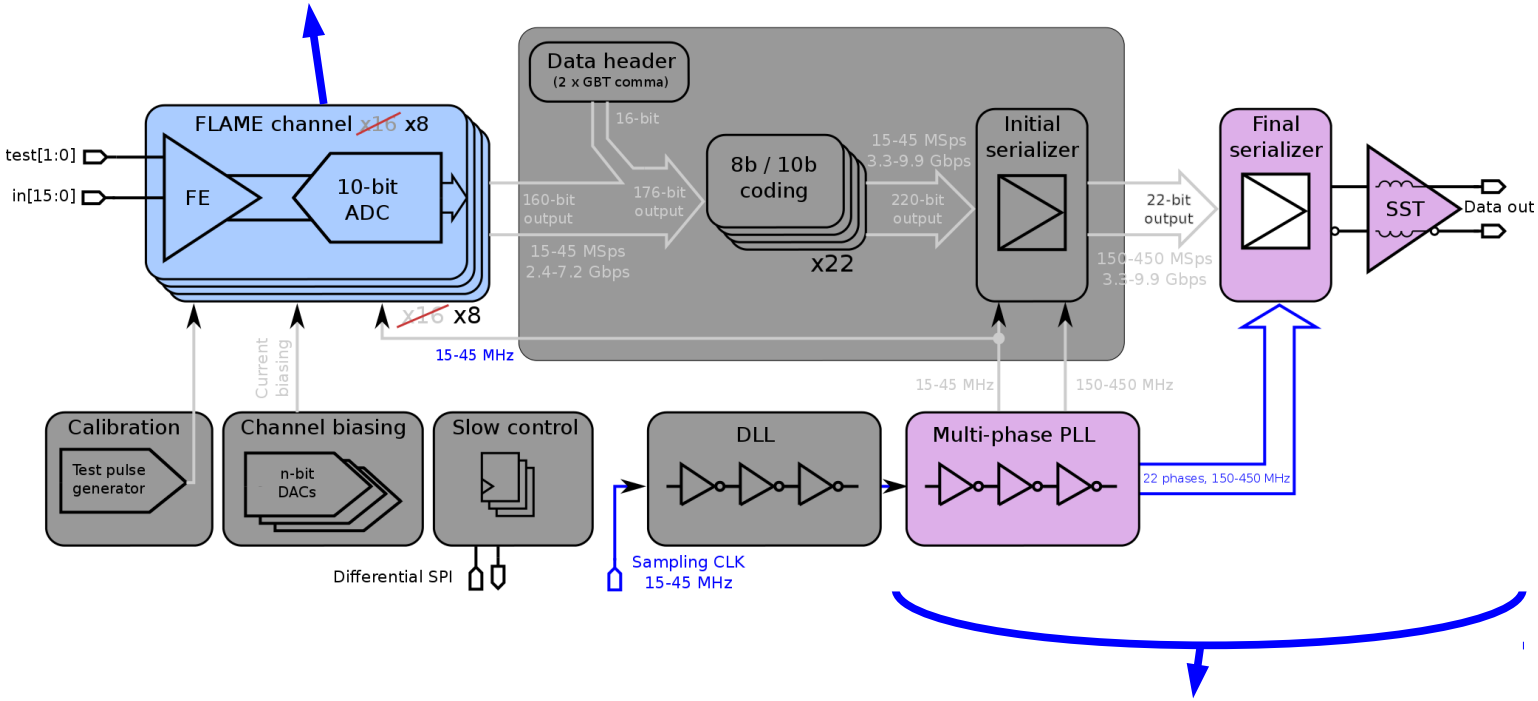

Prototypes submitted on November 2015, test board developed, tests should start within month...

- Prototype serializer ASIC comprising:
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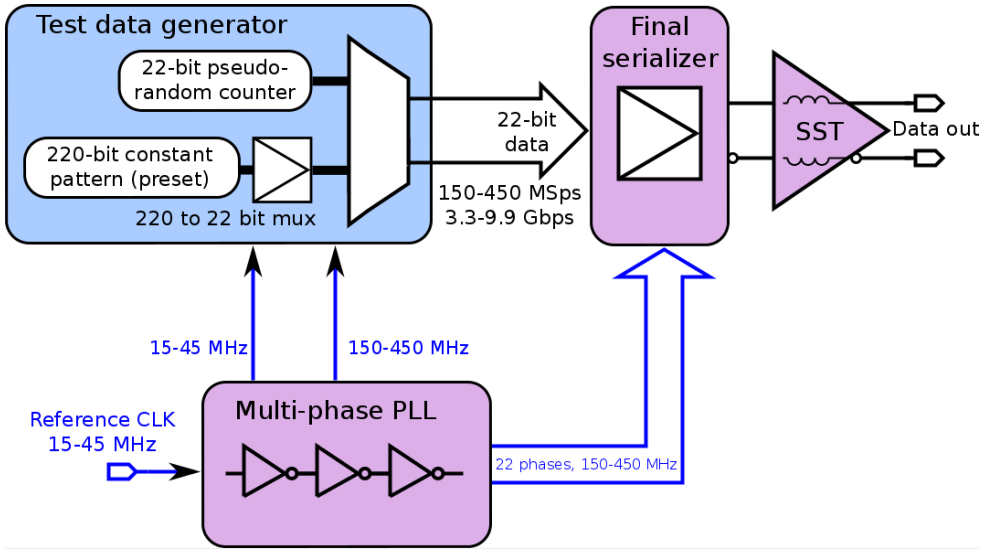
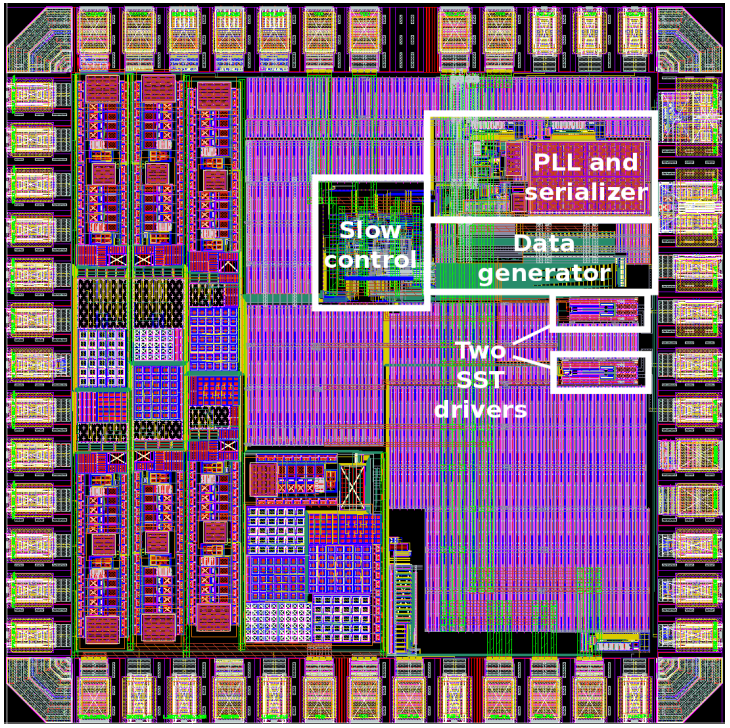
  - Fast serializer 22b → 1b
  - Fast SST driver

Current development in CMOS 130nm
Fast serializer





1250 µm x 1250 µm

FLAME serializer prototype:

- Ultra low power, ultra low jitter multi-phase PLL
  - Output frequency range 150-450 MHz
  - 22 phases for serializer
- 22b → 1b serializer with fast SST driver (3.3 – 9.9 Gbps)
- Power consumption < 15 mW at 9.9 Gbps
- Test data generator
  - 22-bit pseudo-random counter for eye diagram analysis
  - 220-bit preset pattern (via slow control) – constant during transmission – one complete FLAME package

Design submitted on November 2015, tests already started, first results are promising...

Summary and future plans

Summary

• Development of new readout ASIC for LumiCal – FLAME – started

• Simplified 8-channel FLAME v0 ASIC and fast serializer ASIC designed and fabricated

• Test already started...

Future plans

• In case of positive test verification we plan a complete 16-channel FLAME submission at the beginning of the 2017.

Thank you for attention