BeamCal readout - proof of concept and some extras

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29th FCAL Workshop

Outline

Recent activities at PUC around Beamcal

- Configurable front-end proof-of-concept

And some extras:

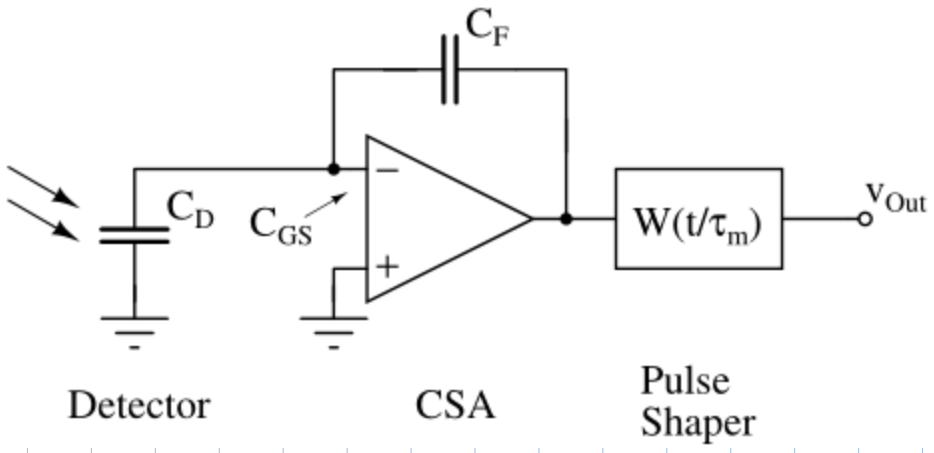
- The Bean V2 testing
- BeamCal specifications revisited
- Future chip design for BeamCal

CONFIGURABLE FRONT-END PROOF-OF-CONCEPT

Motivation

- BeamCal detector segmentation still under study
- Chip cannot be optimized without a definite design
  - Pixel size impacts capacitance, speed and noise
- What if the front-end chip could be designed to accommodate different pixel sizes?

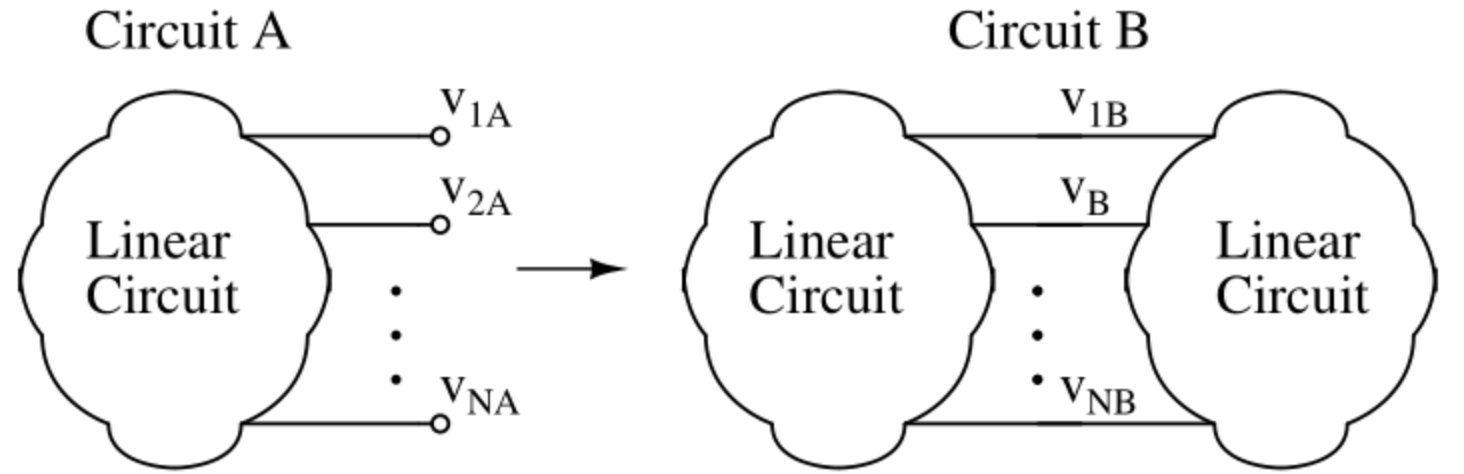
Noise and detector capacitance



$$ENC^2 = (C_{GS} + C_F + C_D)^2 \left(\frac{N_W}{\tau_p} \overline{V^2_{Amp,W}} + N_F K_F \right) + \tau_p N_P \overline{I^2_{Det}}$$

Readout noise is a strong function of detector capacitance C_D

Configurable front-end concept



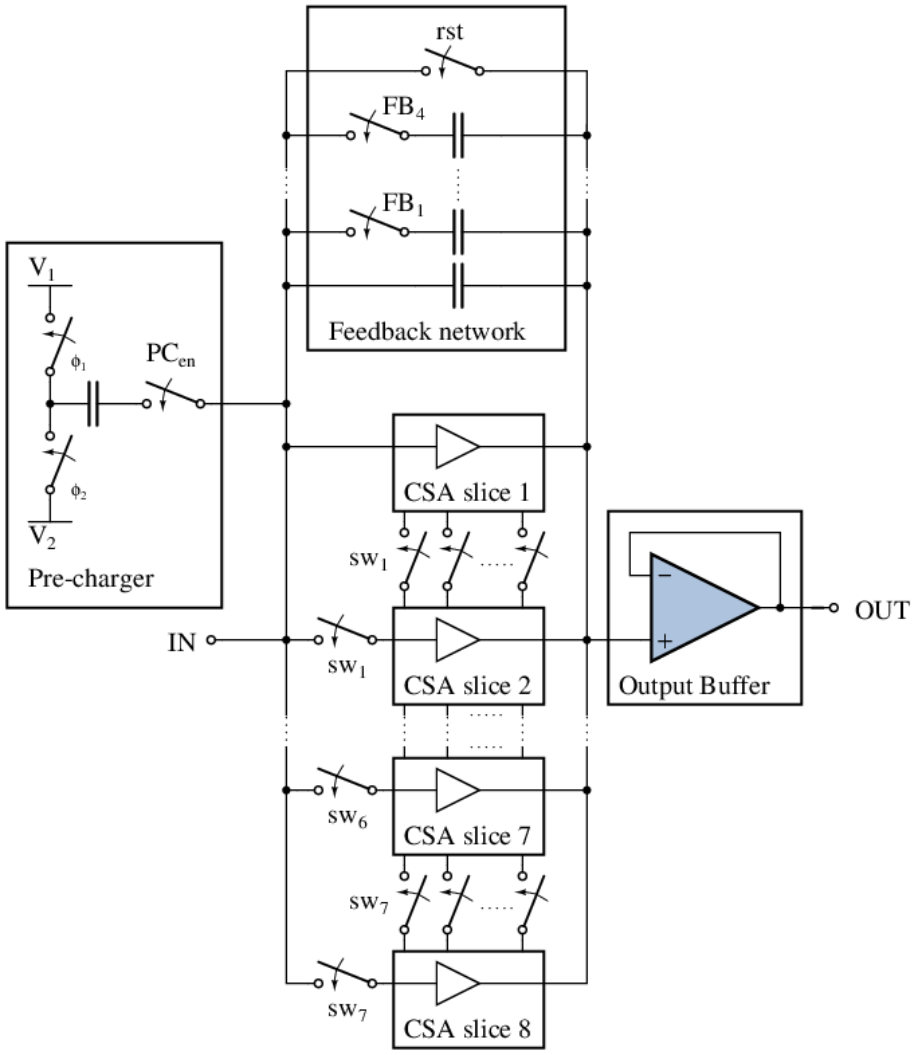
Things that don't change

- Bandwidth
- Gain

Things that do change

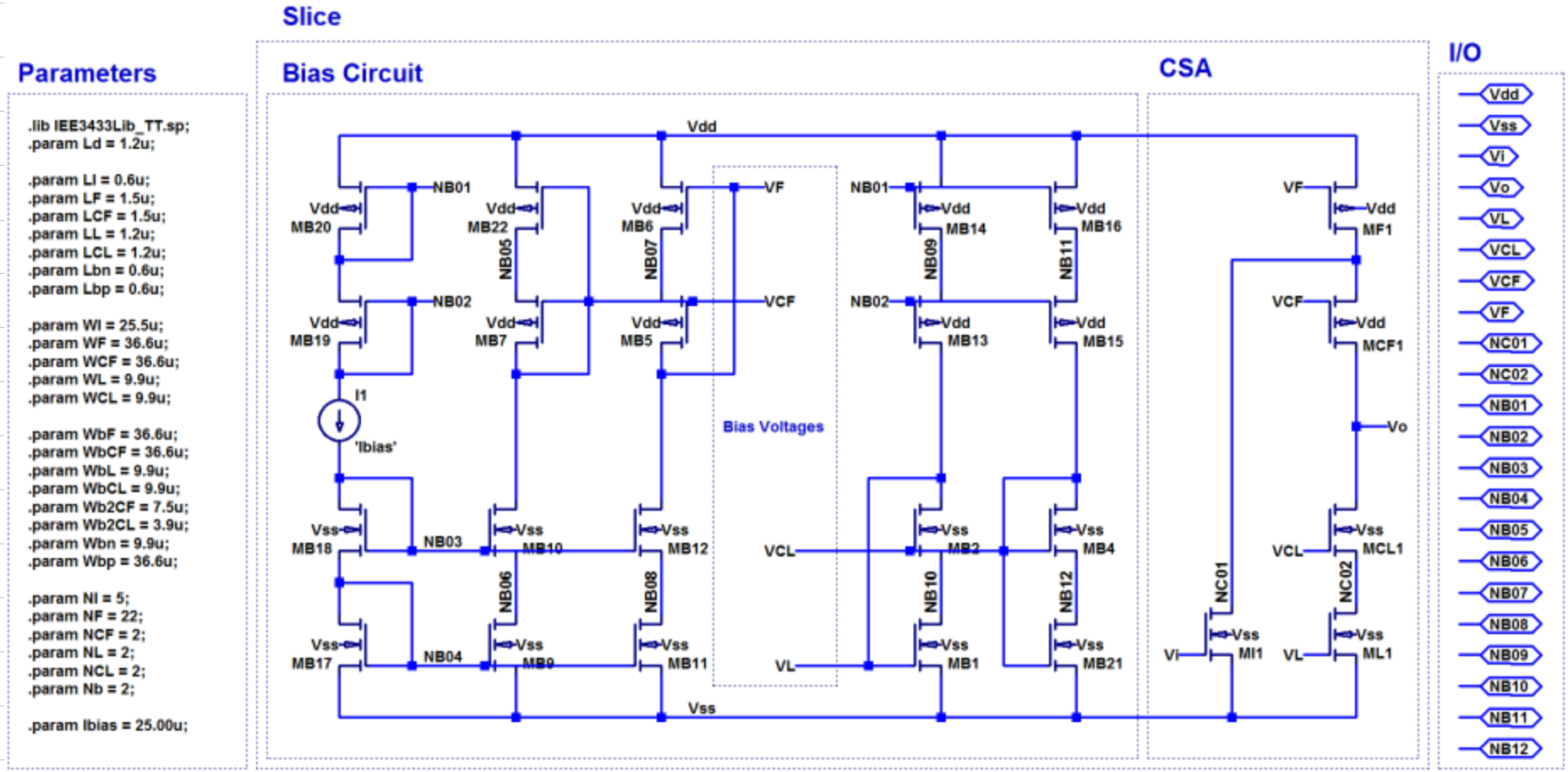
- Drive capability
- Noise
- Mismatch

Configurable front-end: Heisenberg Chip (0.5μm)

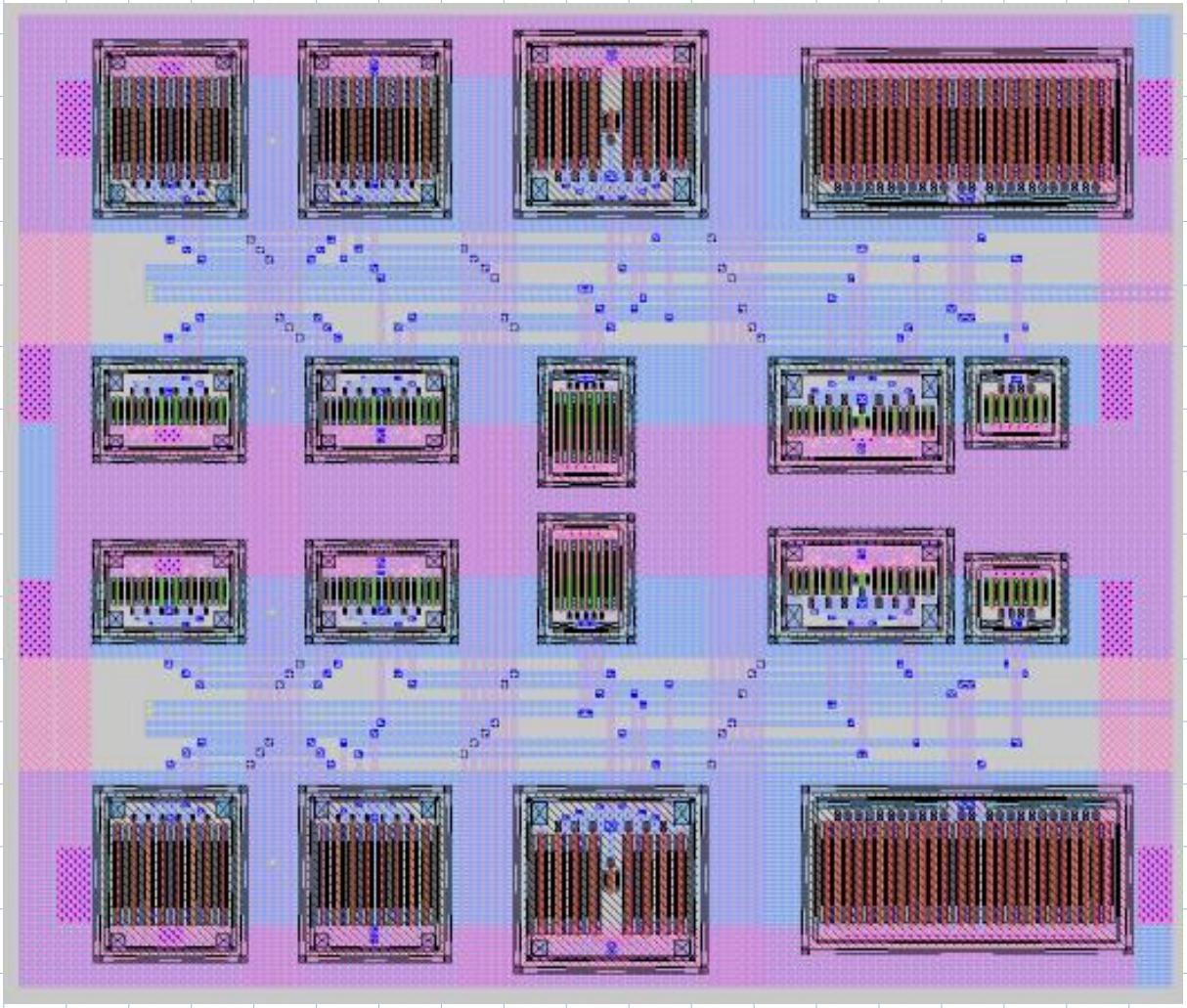


- Charge amplifier split into parallel slices
  - Configuration through switches
- Feedback capacitance is configurable, too
- Chip includes pulser and buffer

Front-end slice design

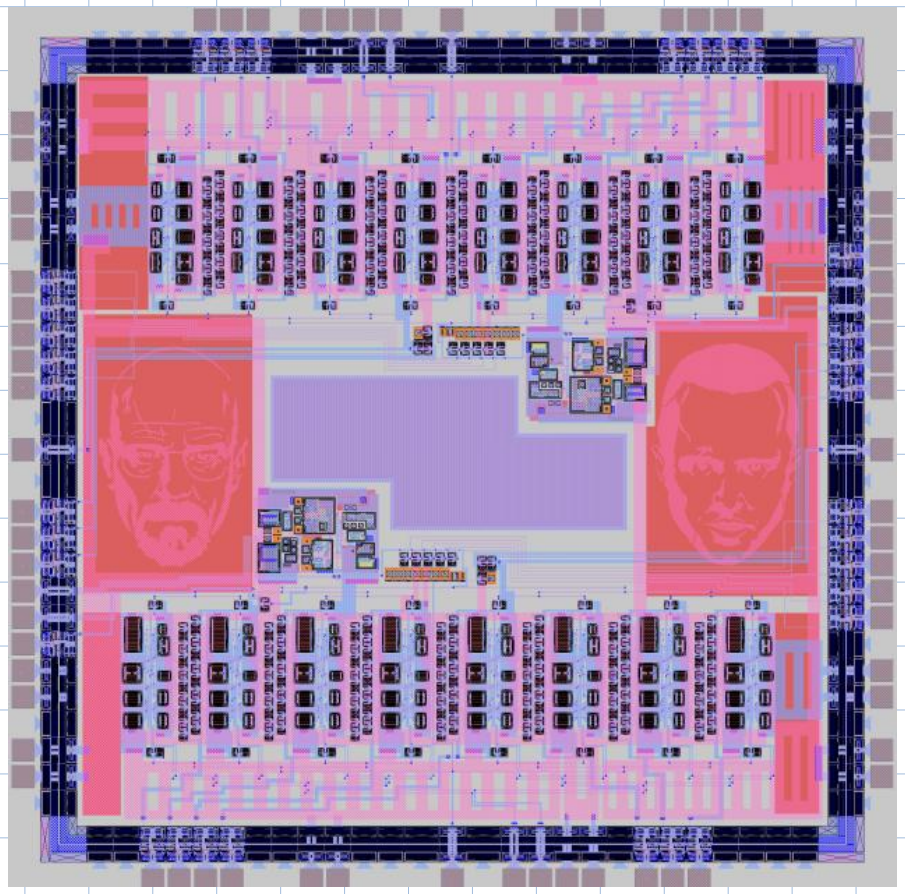


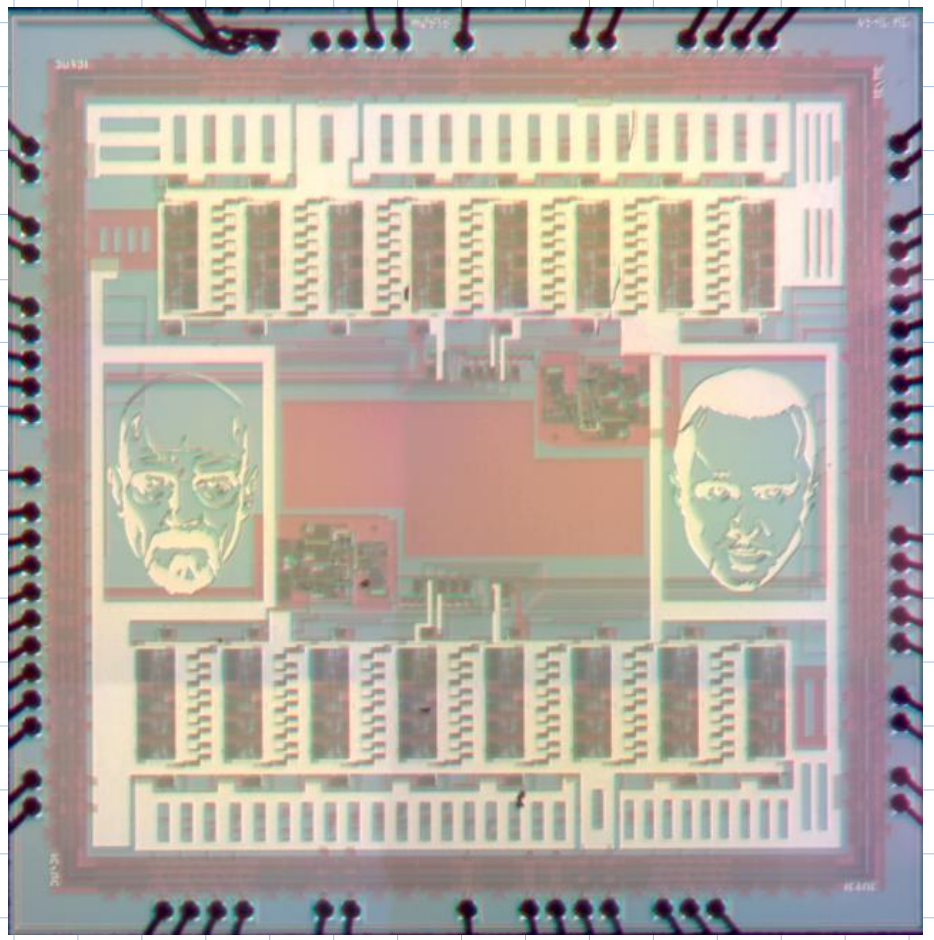
Slice layout



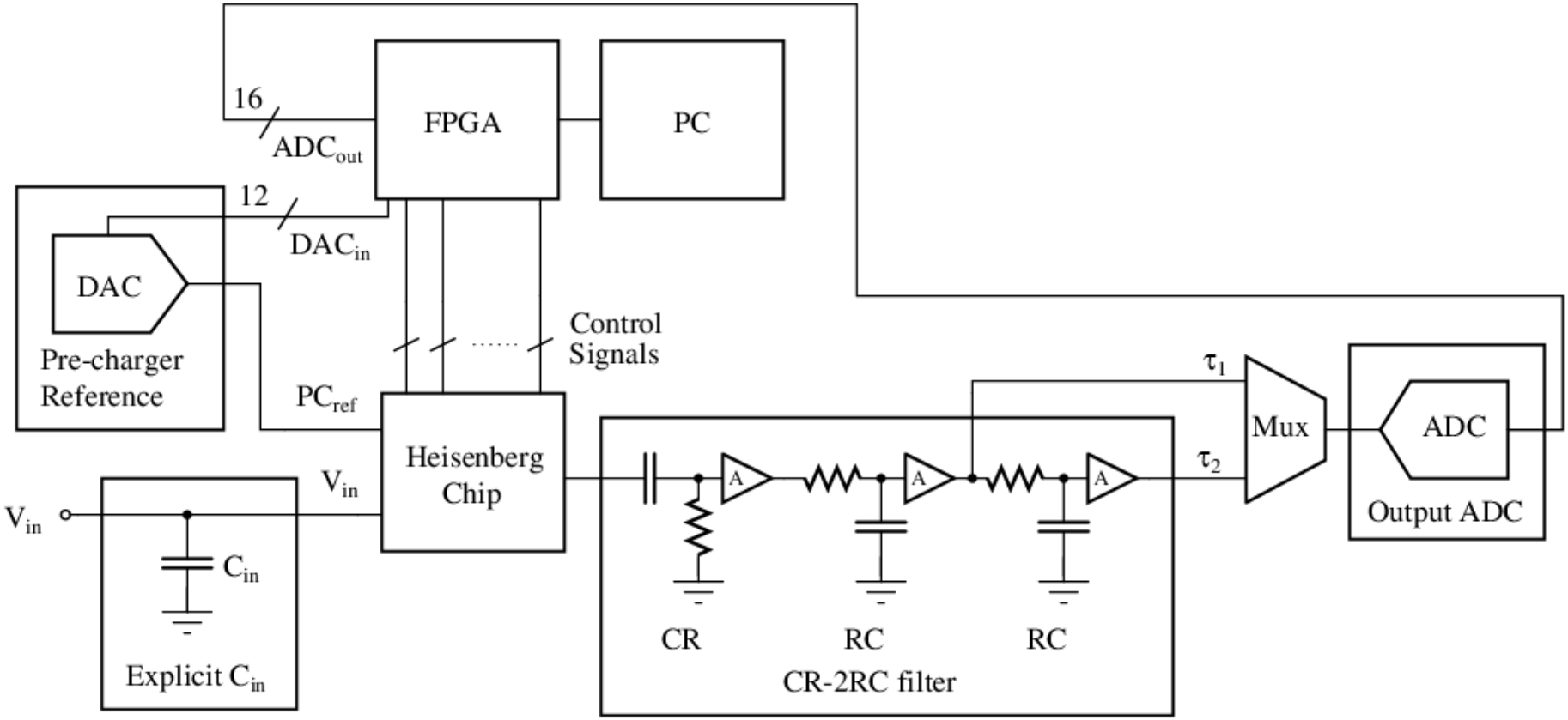
- In future revisions, slices can be connected by abutment

Chip layout and micrograph



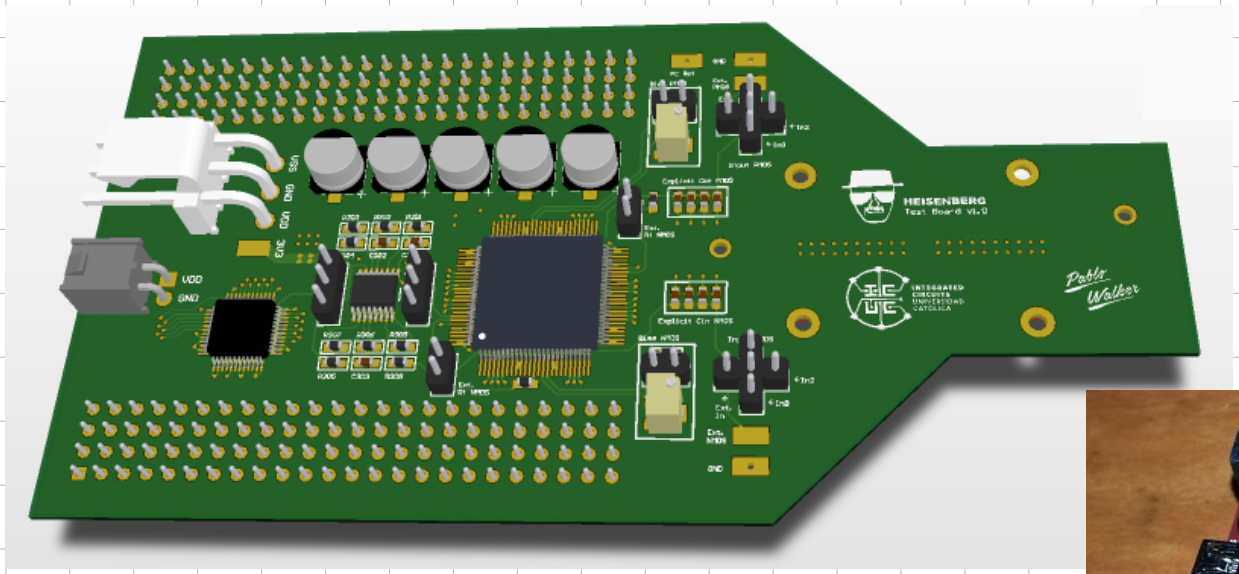


Test setup – Block diagram



Test setup – Board design

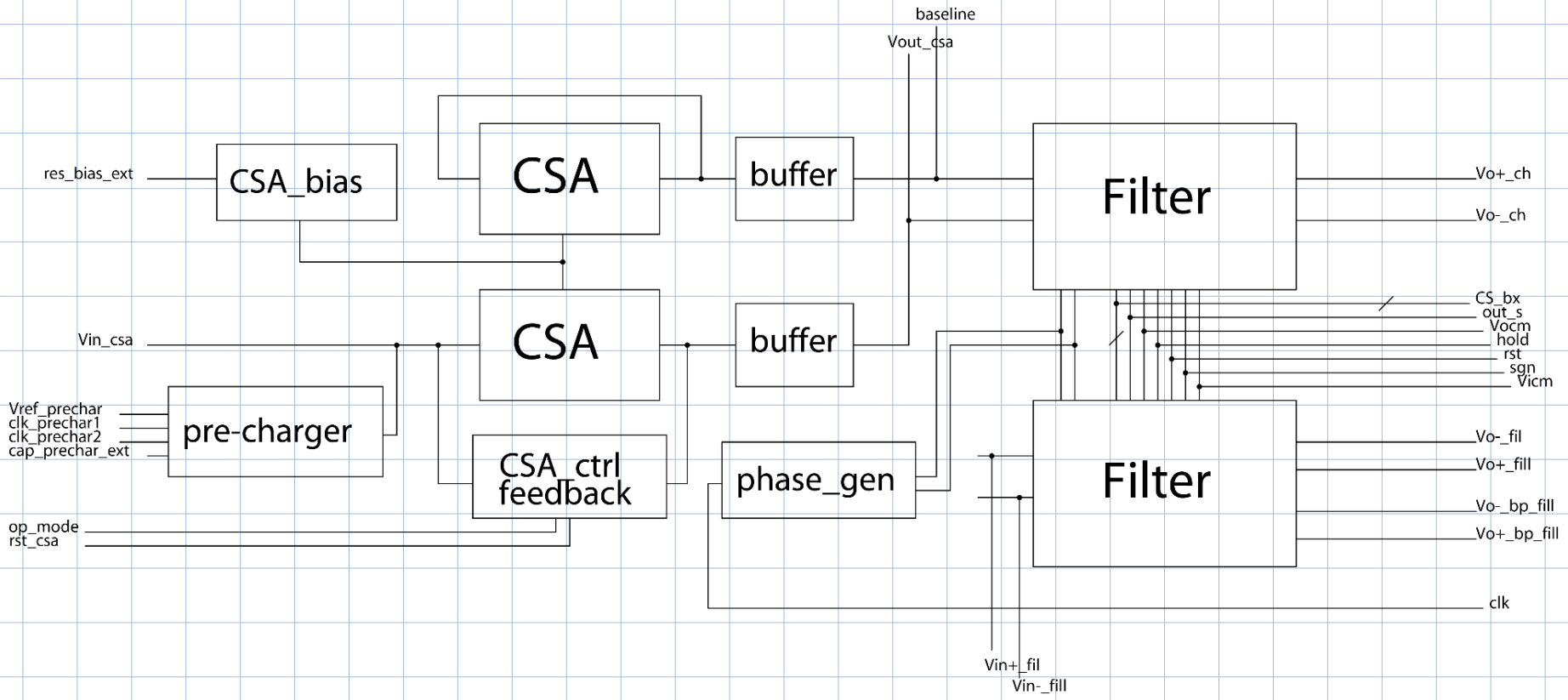
Board is placed on top of FPGA



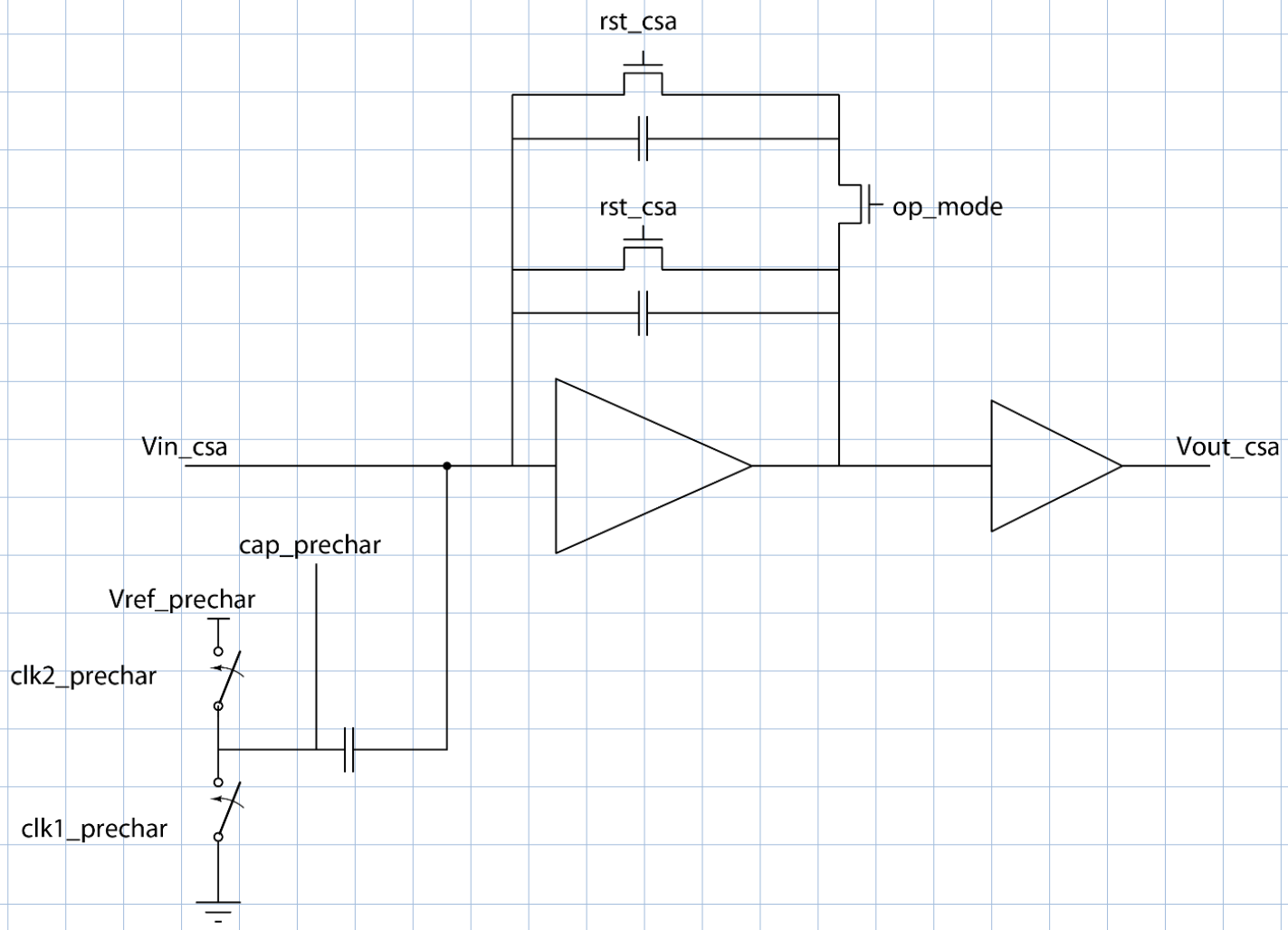
Right now board is being populated…
Preliminary results are promising…
Full results should come soon…

THE BEAN V2 TESTING

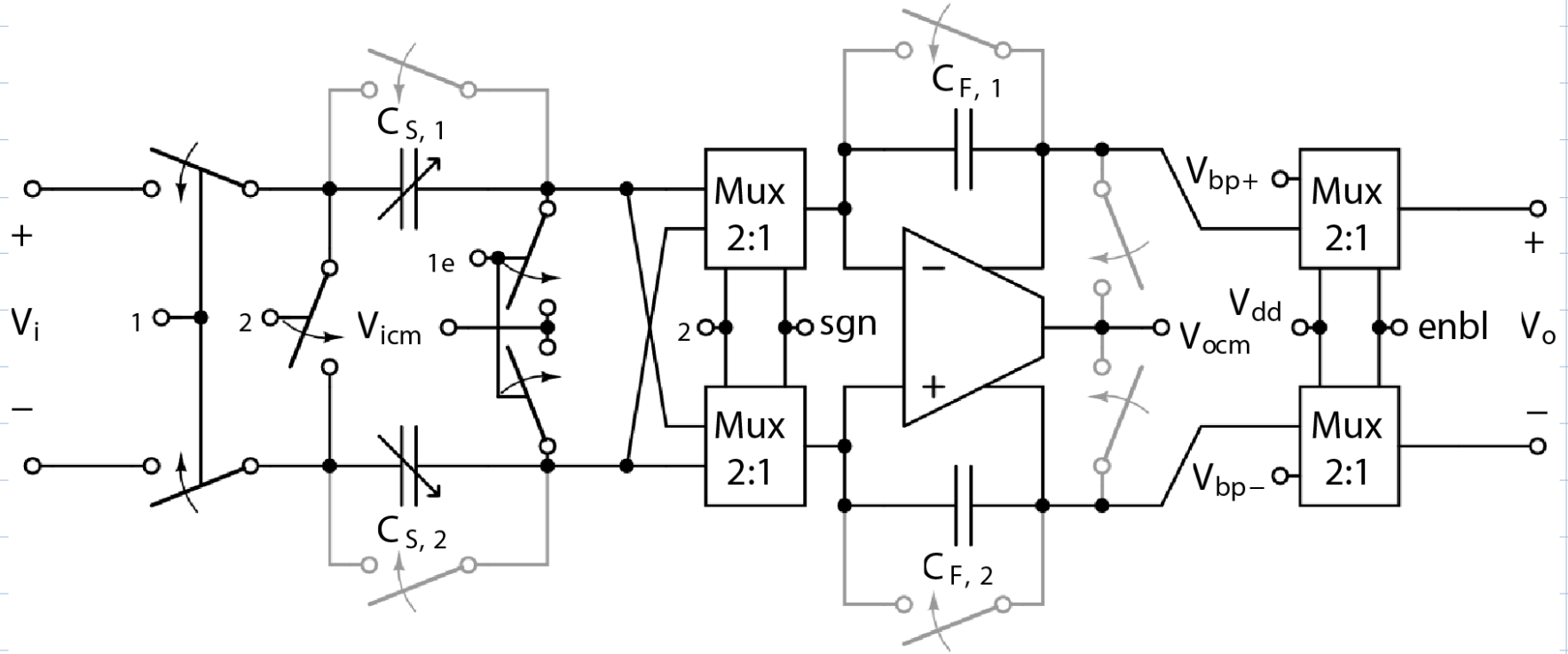
The Bean V2: Block diagram



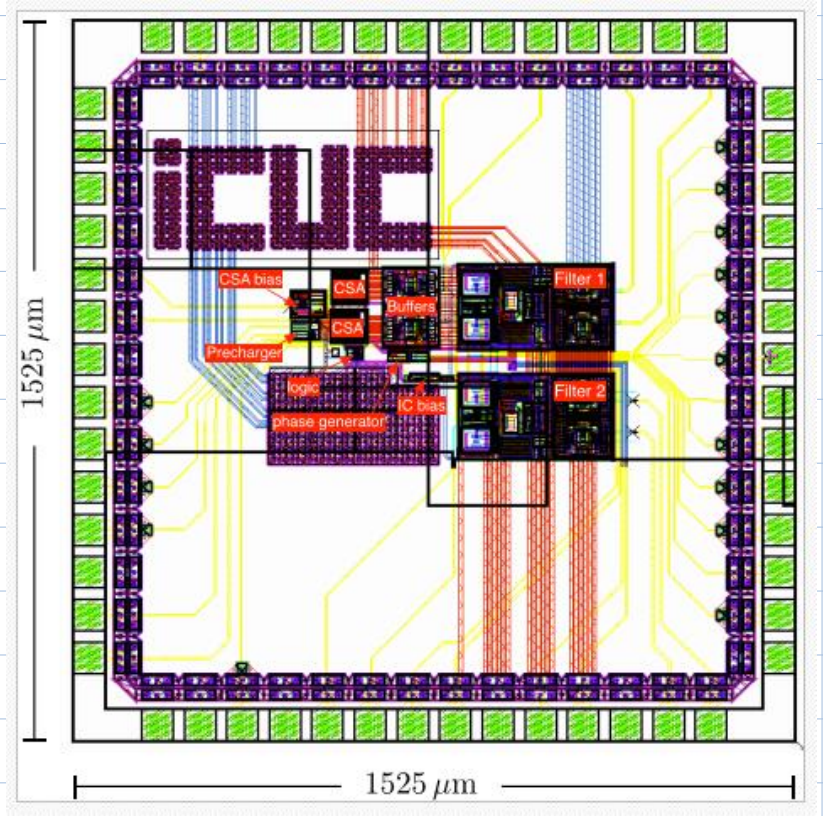
The Bean V2: CSA

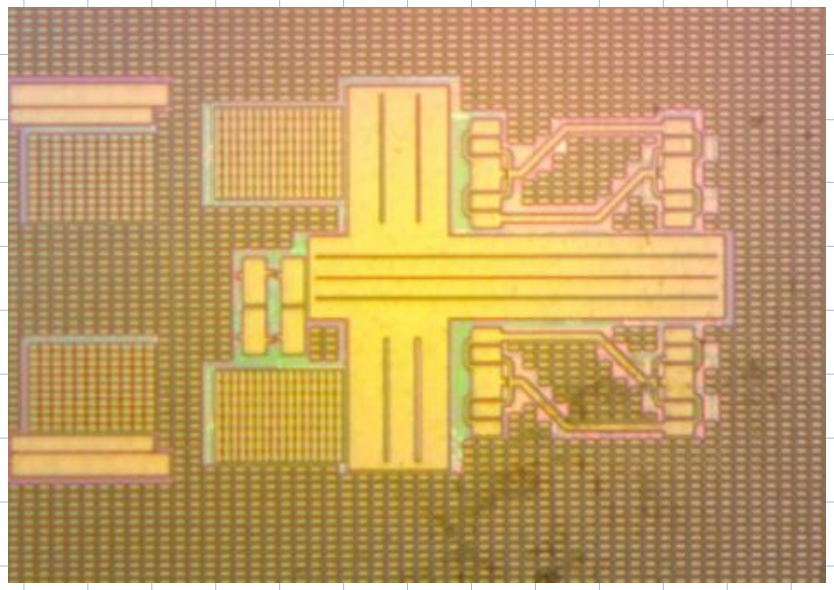


The Bean V2: Configurable filter



Bean V2 Chip (180nm CMOS process)

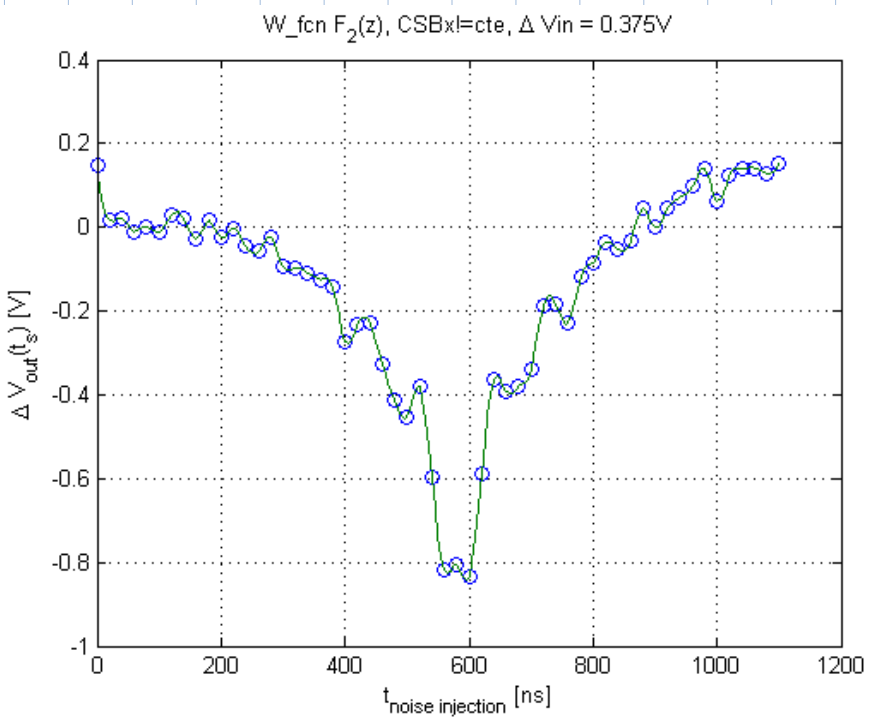




Test setup picture

Preliminary test results:

- Weighting function measurement

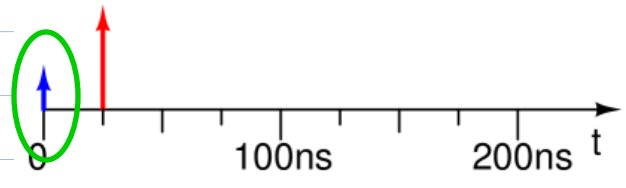


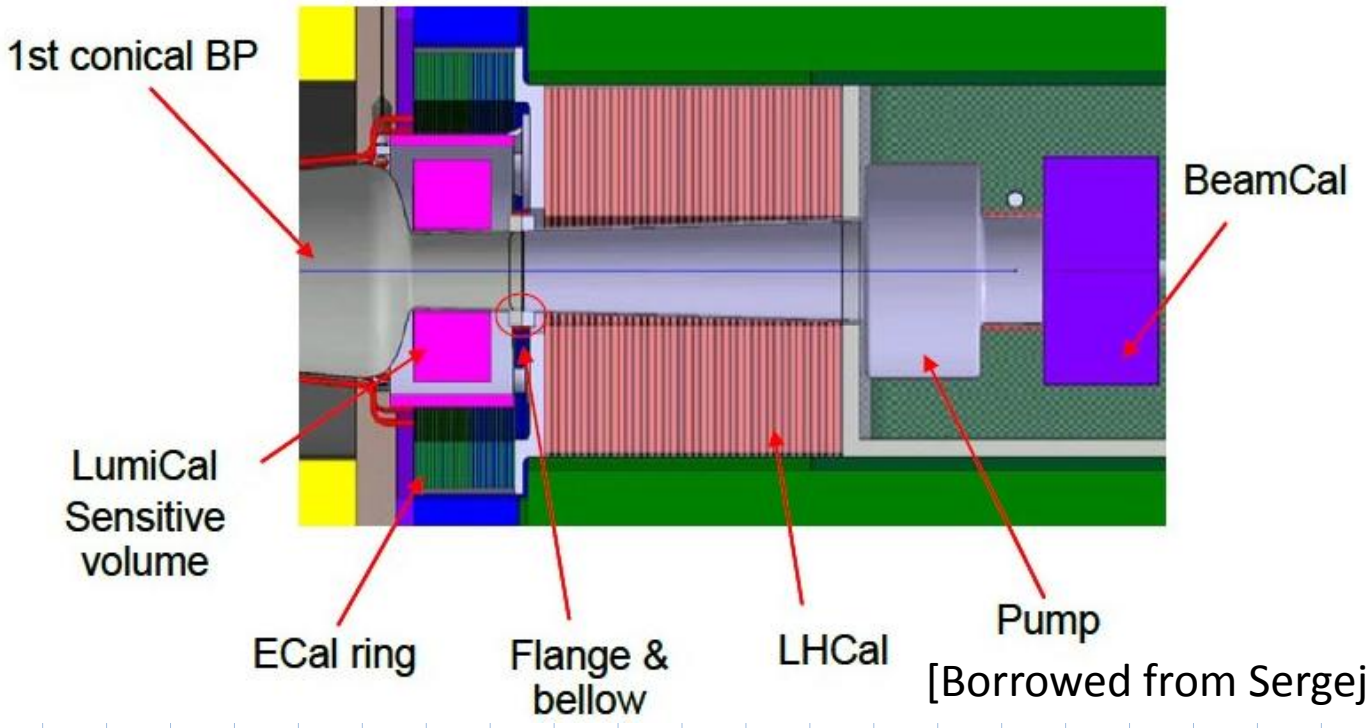
- Still some timing issues…

BEAMCAL SPECIFICATIONS REVISITED

Dual hits per BX?

- Firstly, BeamCal is hit by beam halo
  - ~MIP deposition, low noise required
  - clean environment
  - Great for calibration

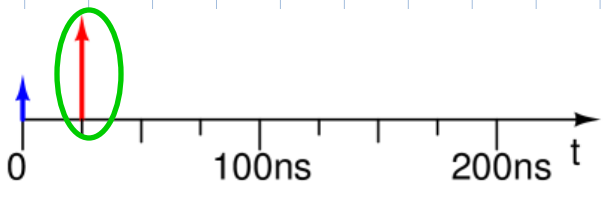


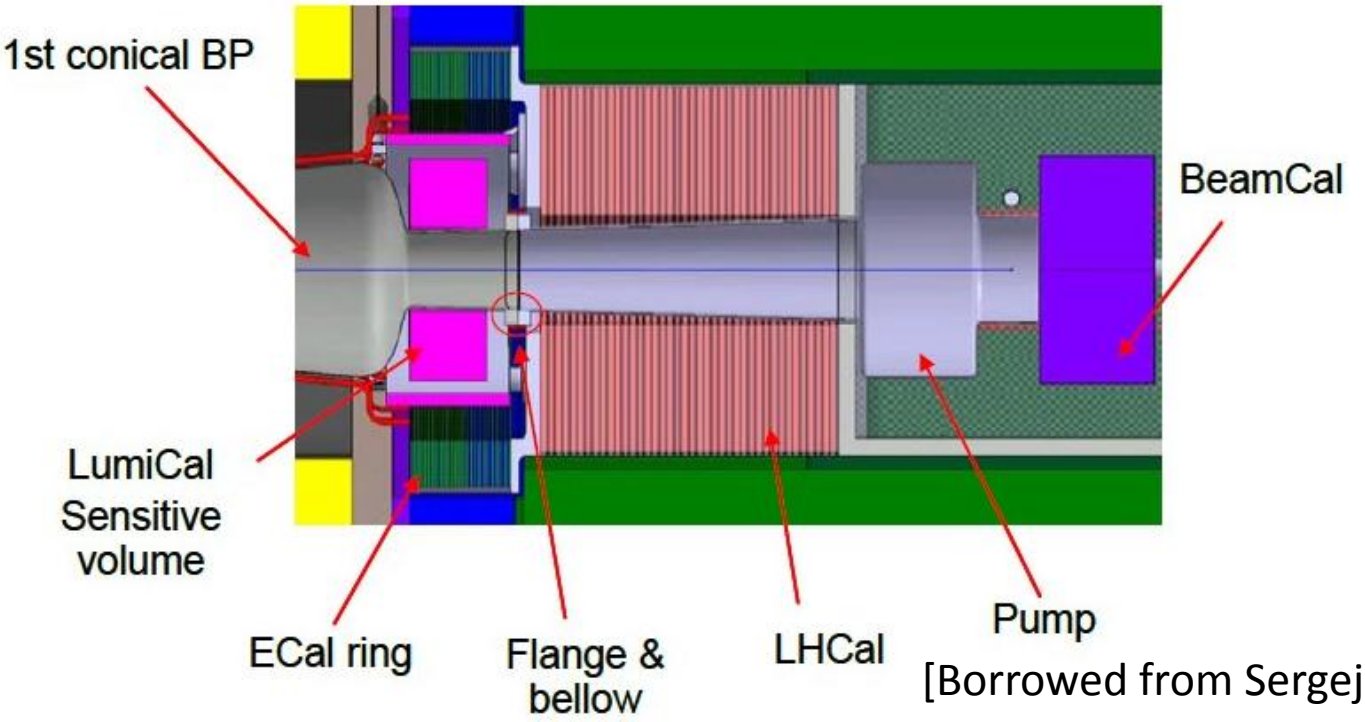


[Borrowed from Sergej slides]

Dual hits per BX?

- ~25ns later, BeamCal is hit by collision results
  - Large deposition, noise is not a problem
  - Physics readout
- Physics and calibration within same BX
- Interesting idea. Now is this possible?



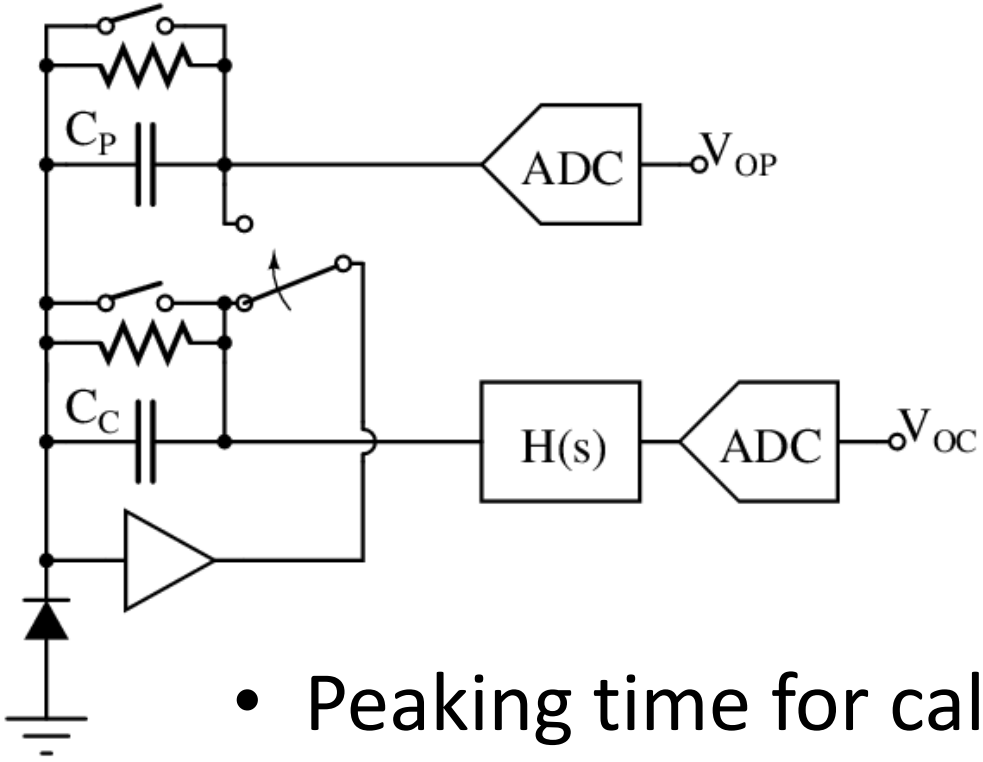


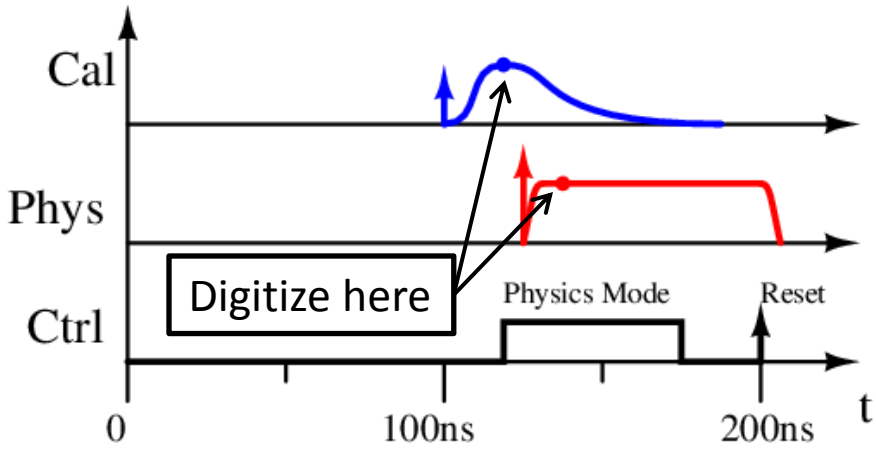
[Borrowed from Sergej slides]

Electronics for dual hits

- Digitization
  - Very fast ADC, or
  - Analog memory
- Fast analog electronics
  - Switch between modes really quick, or
  - Very large dynamic range
    - Not easy for calibration (only 25ns peaking time)
      - Need huge current on input device!!!
      - Or some trick instead (e.g. negative capacitance?)

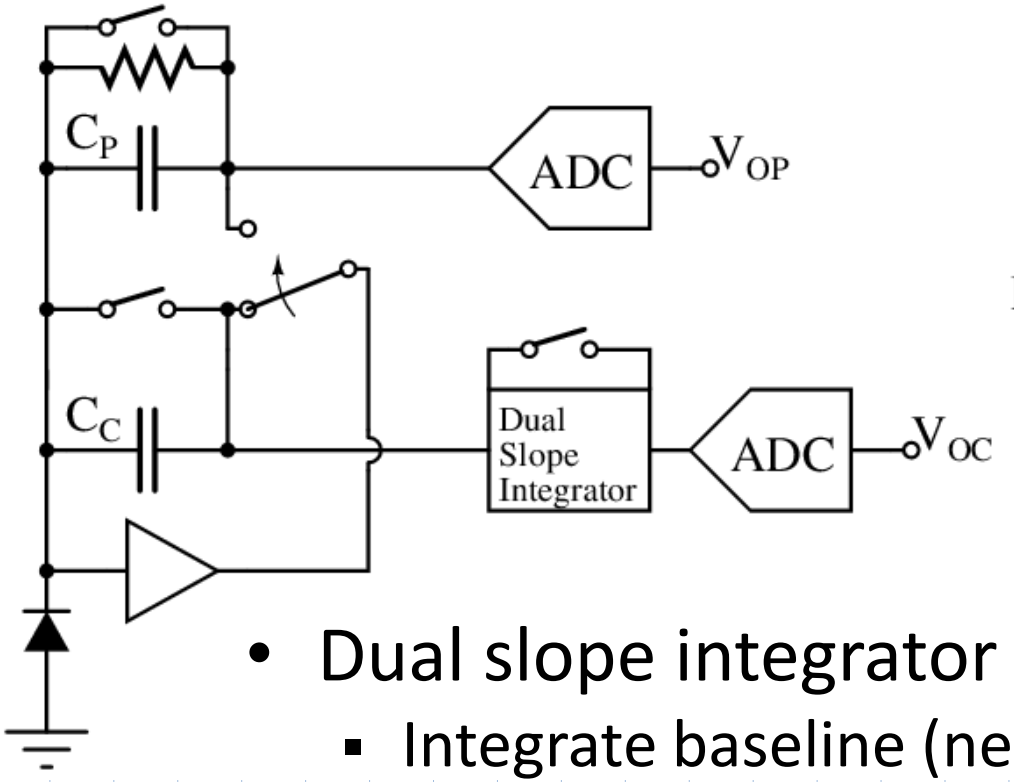
A first approach: Output mux

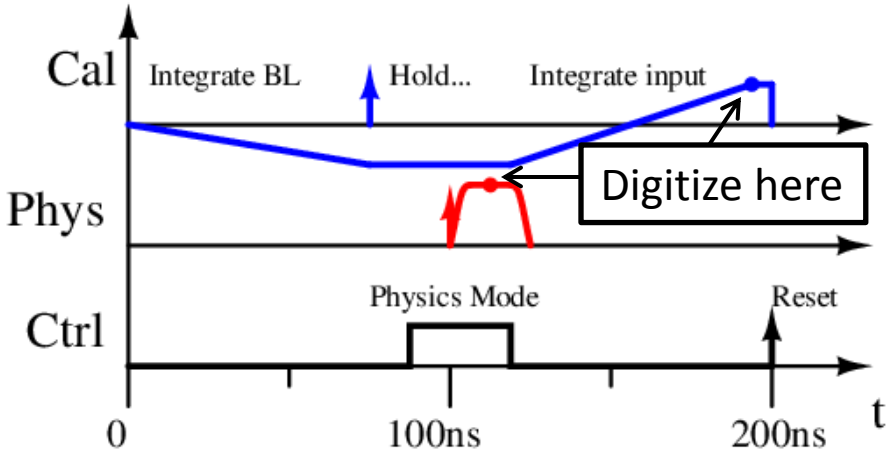




- Peaking time for calibration is <25ns
  - Will require very large CSA current (~5mA)
- Physics signal is then sampled

Another idea: time allocation





- Dual slope integrator for calibration signal
  - Integrate baseline (negative gain)
  - Calibration signal is produced, but held…
  - Switch to physics mode, process output quickly
  - Then Integrate calibration signal and sample

Yet another, much simpler idea

- Beam halo is really convenient for calibration
  - MIP behavior, constant energy deposition per particle
- Over time, beam halo should cover the whole detector area
- Then we can measure the deposited energy for each pixel many times
- This allows noise reduction by oversampling
  - This lowers the stdev of measurements
- But this doesn't work if noise is way too large or if multiple halo particles hit pixels
  - Cannot tell how many particles hit a pixel in a certain event
  - This is particularly true if beam halo is too dense…

FUTURE CHIP DESIGN FOR BEAMCAL

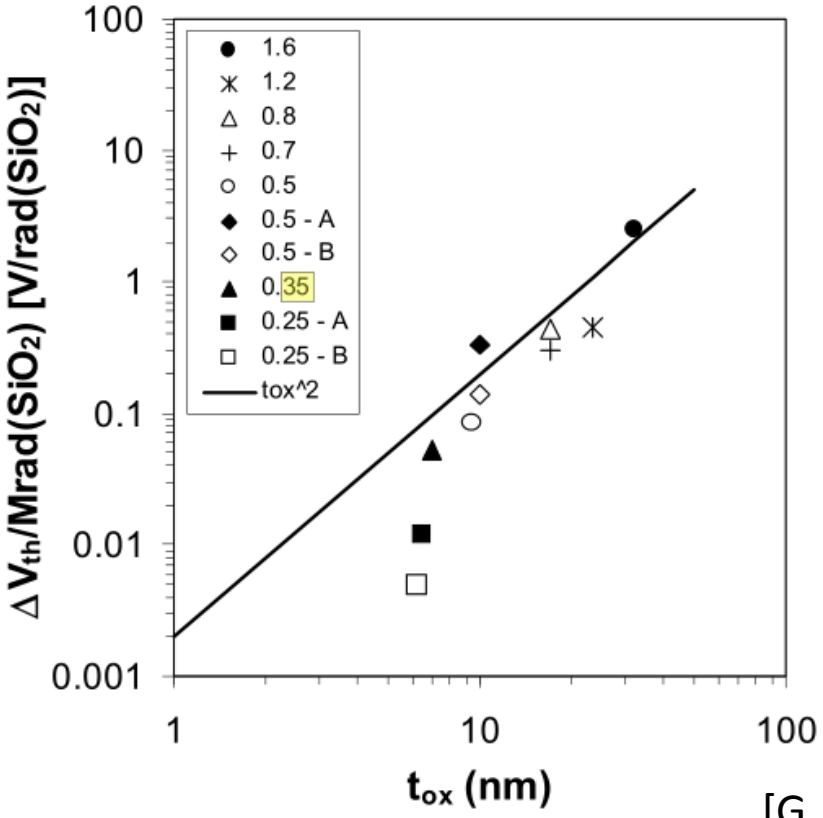
Future plans

- Things are moving slowly…
  - No luck with funding
    - Now waiting for results from **four** proposals
  - No luck so far with CADENCE
  - No luck with CERN MPW runs
  - No luck with new students
- But I have interesting news
  - I just joined a project that may have some $$...
  - I may choose a process that does not require CADENCE
  - I will design the electronics myself, period
    - If I had decided this 2 years ago…

Other processes?

- TSMC 250nm: many EDA tools, not too expensive (USD ~$10.000/25mm^2)
- ON Semi 350nm: many EDA tools, cheap (USD ~$1000/mm^2)
- Radiation tolerance could be a problem…
  - But new BeamCal structure places electronics under lower radiation dose…
  - How bad is 350nm?

On radiation tolerance



[G. Anelli Thesis, 2000]

Figure 2.8: Threshold voltage variation per Mrad dose as a function of the oxide thickness. The points are taken from measurements done in the Microelectronics Group at CERN [Ane97] (except for four points, whose data are taken from [Osb98]). The legend gives the minimum gate length for the technologies in microns. It is also shown the $\Delta V_{th} \propto t_{ox}^{2}$ trend (solid line).

Conclusion

- Specs for BeamCal front-end? **To be discussed**…
- Readout board? **To be discussed**…
- Dual hit per BX? **To be discussed**…
  - Negative capacitance for noise reduction? **To be discussed**…
  - Time allocation scheme? **To be discussed**…
  - Multi sampling noise reduction? **To be discussed**…
- New process for chip design? **To be discussed**…

Thanks for your attention