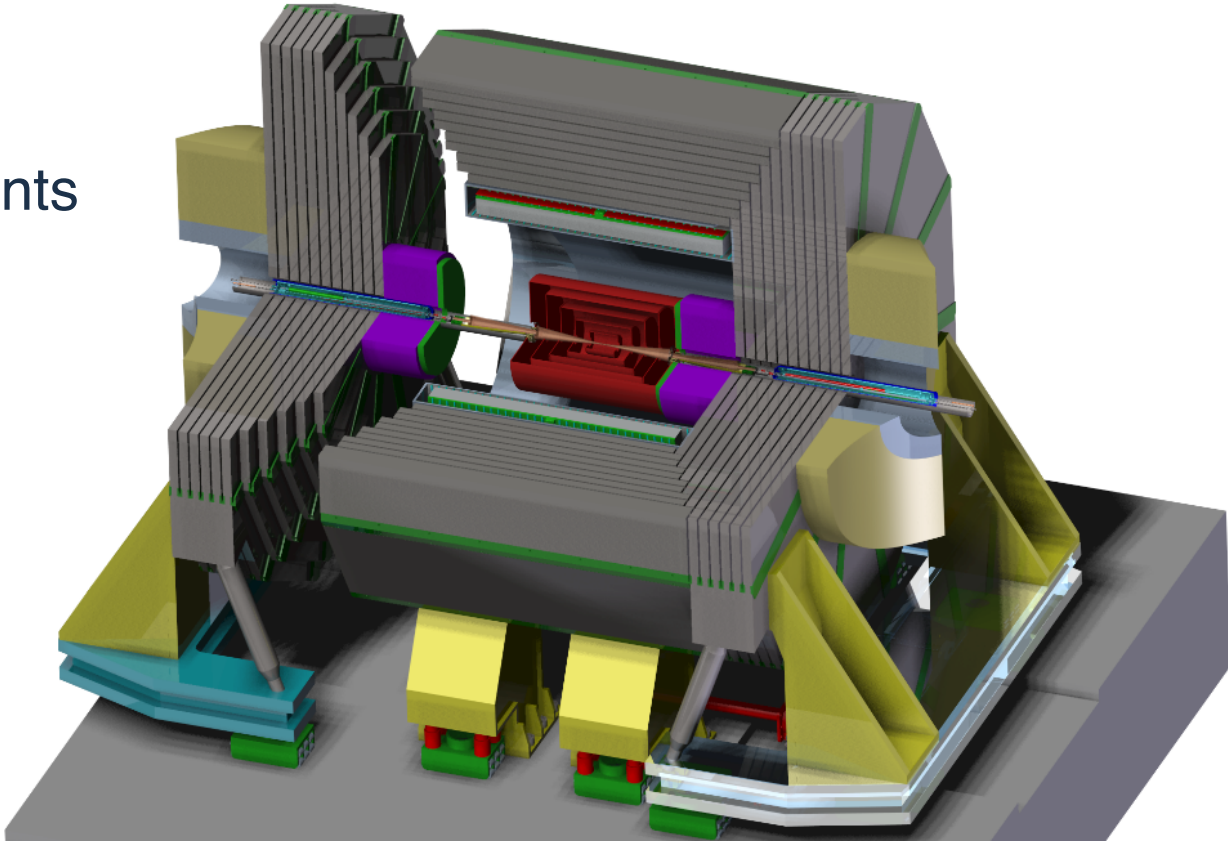
SiD Status and Plans

International Workshop on Linear Colliders
Morioka, 5 Dec 2016

- Overview
- R&D and software developments
- Collaboration activities
- Outlook



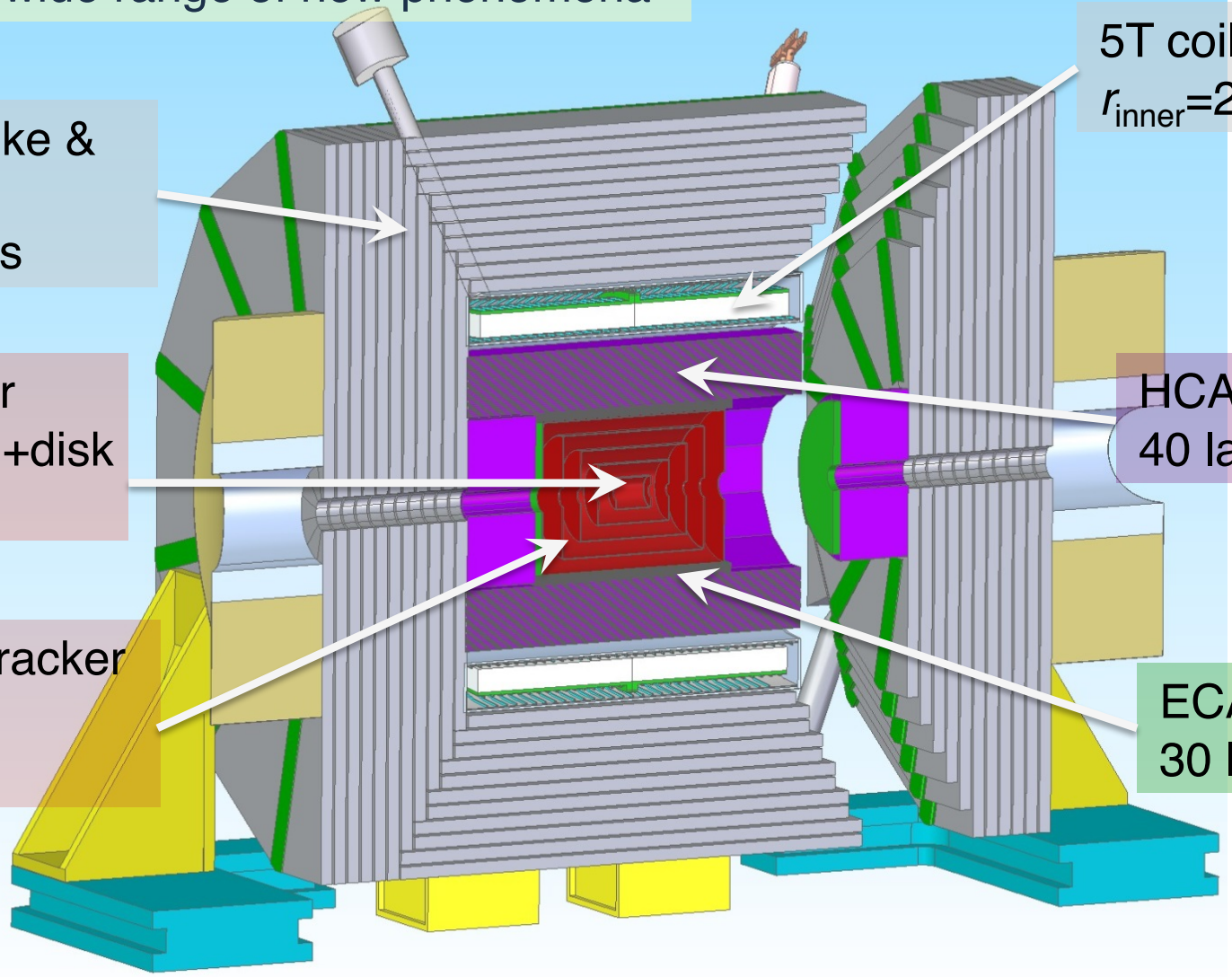
Aidan Robson
for the SiD Consortium

University of Glasgow | Experimental Particle Physics

SiD

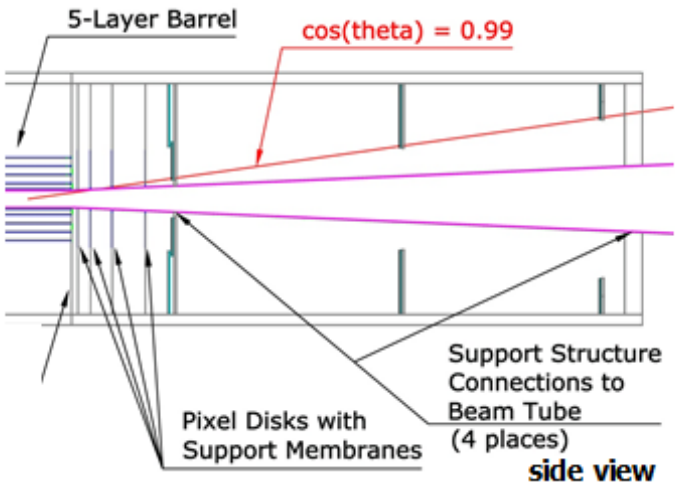
A compact, cost-constrained detector

designed to make precision measurements and be sensitive to a wide range of new phenomena



SiD tracking

A robust, low-material, high-precision silicon system



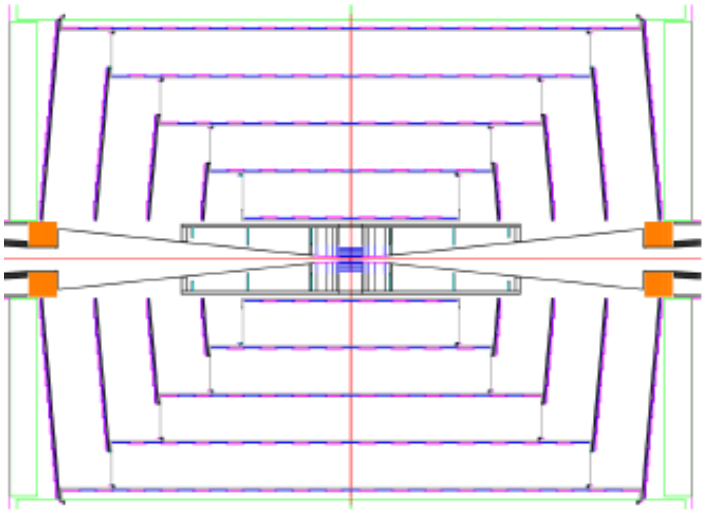
Vertex Detector

Challenging requirements:

- <3μm hit resolution
- Feature size ~20μm
- ~0.1% X_0 per layer material budget
- <130μW/mm^2
- Single-bunch timing resolution

Technology choice comes later:

- Si diode pixels ('standard' tech)
- Monolithic designs (MAPS, Chronopix)
- Vertically integrated ('3d') approaches (VIP chip)
- High-Voltage CMOS



Silicon strip tracker

- Silicon microstrips, 25μm pitch / 50μm readout
- 5 barrel layers / 4 disks
- Tracking unified with vertex detector – 10 layers in barrel
- Gas-cooled
- Material budget <20% X_0 in active region
- Readout using KPiX ASIC bump-bonded to module

MAPS development

Baseline readout for SiD tracker and ECal is KPiX

CMOS monolithic approach
Integrate sensors and front-end electronics on the same substrate

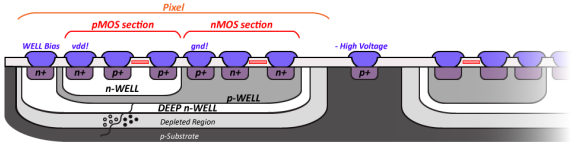
Potential for:

- Lower material budget
- Smaller pixel size
- Lower costs

	kPixM-Trk	kPixM-Cal
Pixel size	40x500 μm^2	1000x1000 μm^2
Array	200x2400	100x94
Full Size	Stitched 5x5 reticles	Stitched 5x5 reticles
Max. Signal	1fC	1pC
Effective ENC	<200e^-	<1000e^-
Filtering	LP + CDS	LP + CDS
S/N	>20	>4
In pix mem. depth	1 bucket	16 buckets
ADC resolution	12 bits	12 bits
DC Power cons.	~ 20μW/pix	~ 20μW/pix
Power pulsing	Yes	Yes

kPixM Test structure submission:

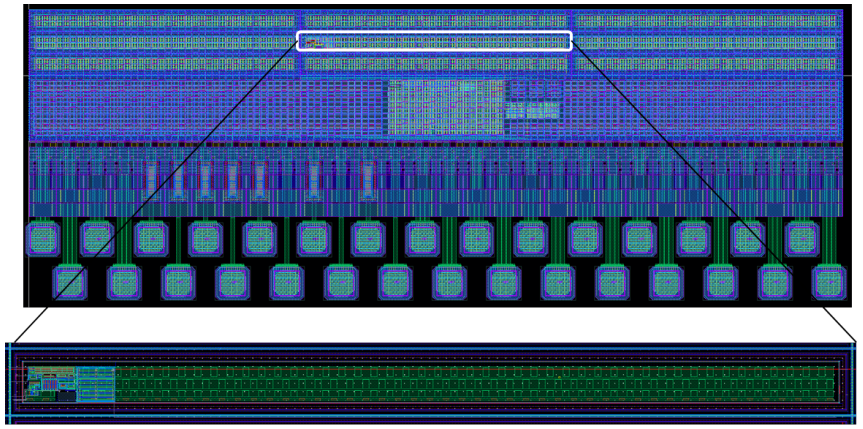
Technology LFoundry 150nm on high resistivity substrate (2kΩcm) thinned to 150μm (fully depleted with 80V)



- Passive pixels (40μm x 500μm)
- Active pixels (8 variants of 40μm x 500μm)
- Mosfet arrays for technology characterization

=> Being produced now

SLAC, Oregon



Chronopix

Baseline readout for SiD vertex detector

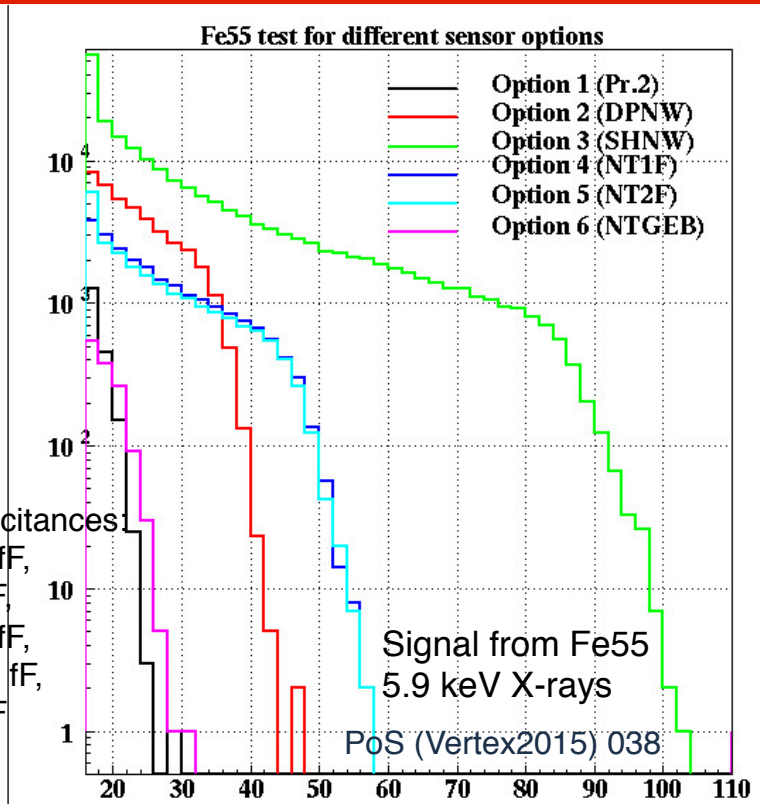
- Series of three Chronopixel prototypes:

  Timestamping (300ns period)
  Sparse readout
  Pulsed power
  } demonstrated with v1

  NMOS electronics with acceptable power consumption
  Comparator offset calibration works
  } v2

- Many problems solved; concept proven valid

- Sensor diode capacitance an issue for 90nm process
  Prototype 3 had six sensor options to study sensor diode capacitance – large sensor capacitance in 90nm technology appears solved



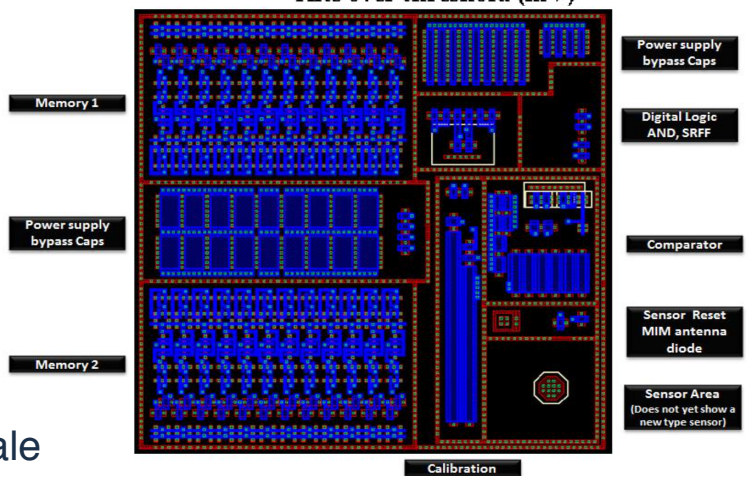
Derived capacitances:
Opt 1 – 9.04 fF,
Opt 2 – 6.2 fF,
Opt 3 – 2.73 fF,
Opt 4 & 5 4.9 fF,
Opt 6 – 8.9 fF

- Need to fully understand sensor operation details, measure sensor efficiency for MIPs

- Cross-talk issues have been addressed by separating analogue and digital power and adding small decoupling capacitor. Some minor cross-talk persists – will try to minimise more

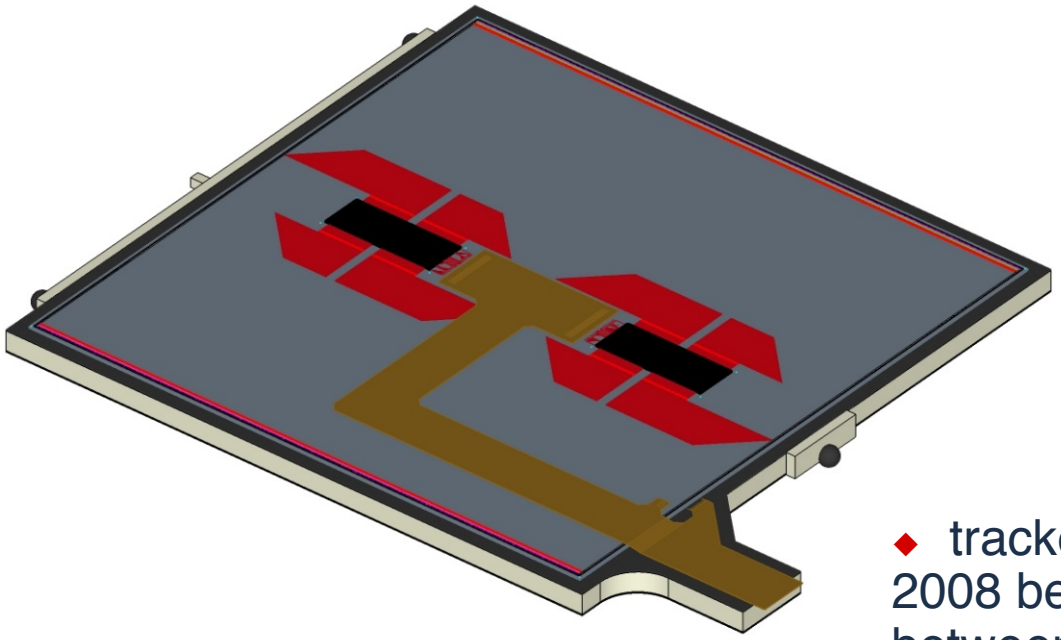
- Prototype 3 chips at Yale

=> MIPs and rad-hardness measurements in progress



Oregon, Yale

Tracker sensors



- tracker sensor prototypes from Hamamatsu from 2008 became damaged by wirebonding (oxide layer between Metal 1 and 2 inadequate)
- not pursued for several years
- renewed interest in 2016 (both SiD and ILD) and favourable negotiations with Hamamatsu; oxide layer thickness will be increased and Under Bump Metallization will be provided

=> going ahead

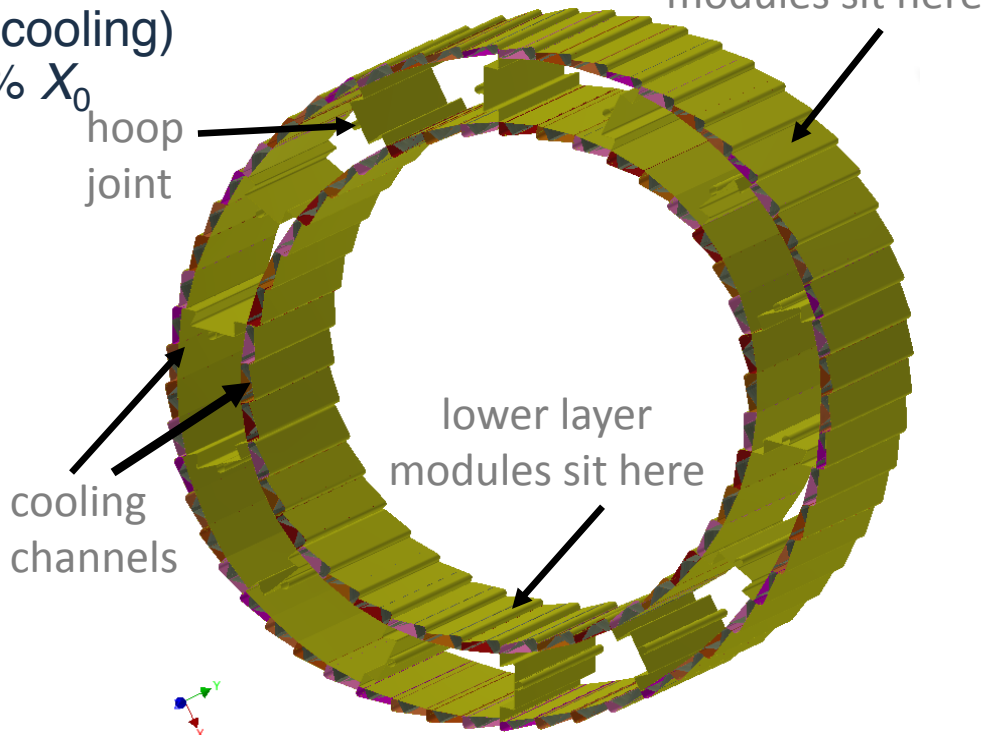
Working towards full prototype test:
sensor + KPiX + cables

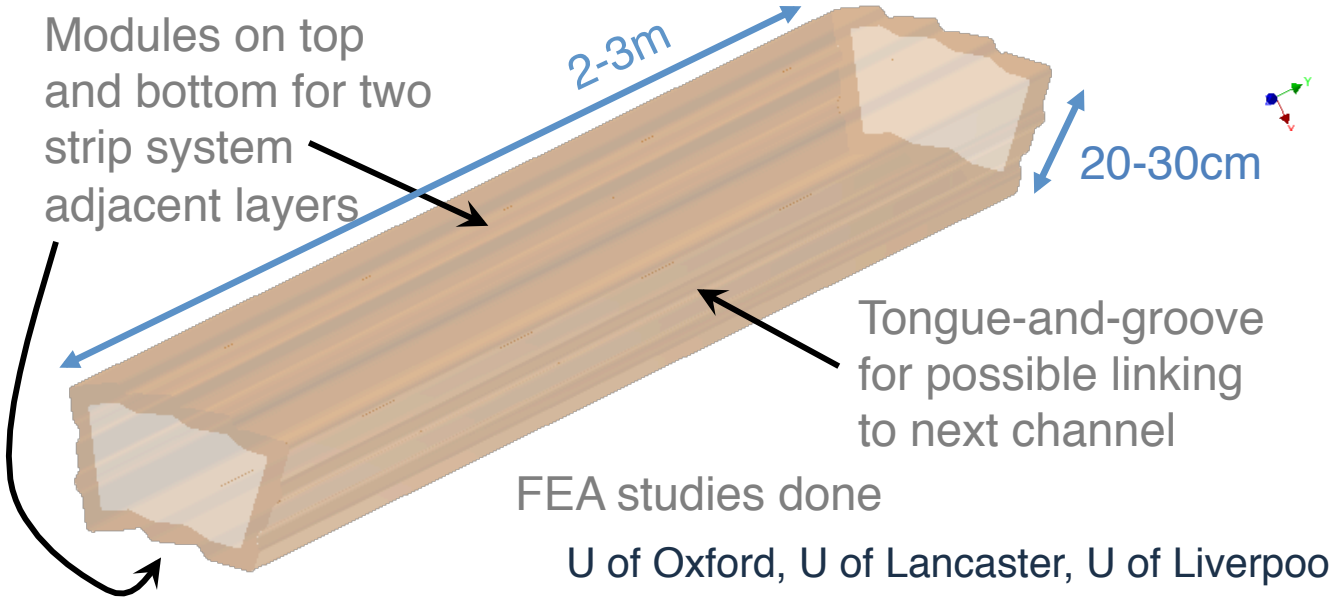
SLAC, Oregon, Davis, UNM, DESY

Tracker support structures

New effort!

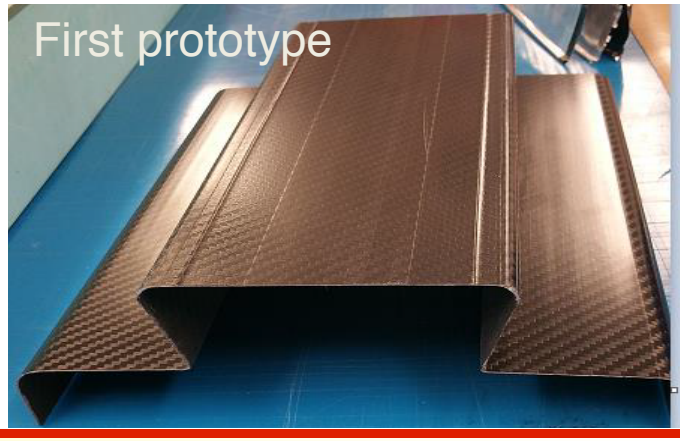
- Aim to build structures (including services and cooling) with lengths of several metres and less than 1% X_0
- Supports consist of CFRP box channels
  - ultra-high modulus skins
  - high moment of inertia
  - manageable dimensions
- Services are co-cured into the structure
- Also investigating possibilities for linking the box channels



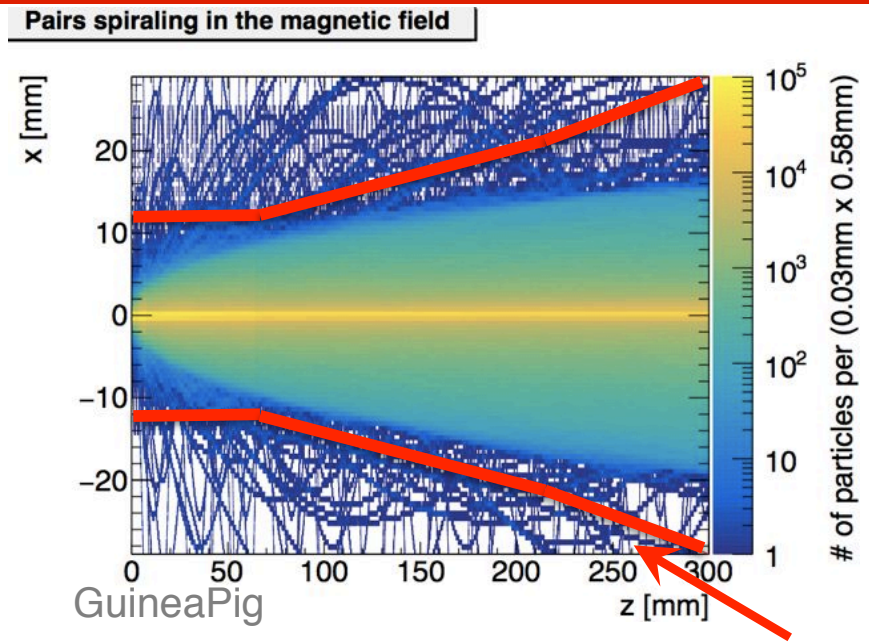


FEA studies done

U of Oxford, U of Lancaster, U of Liverpool



Pair background envelope

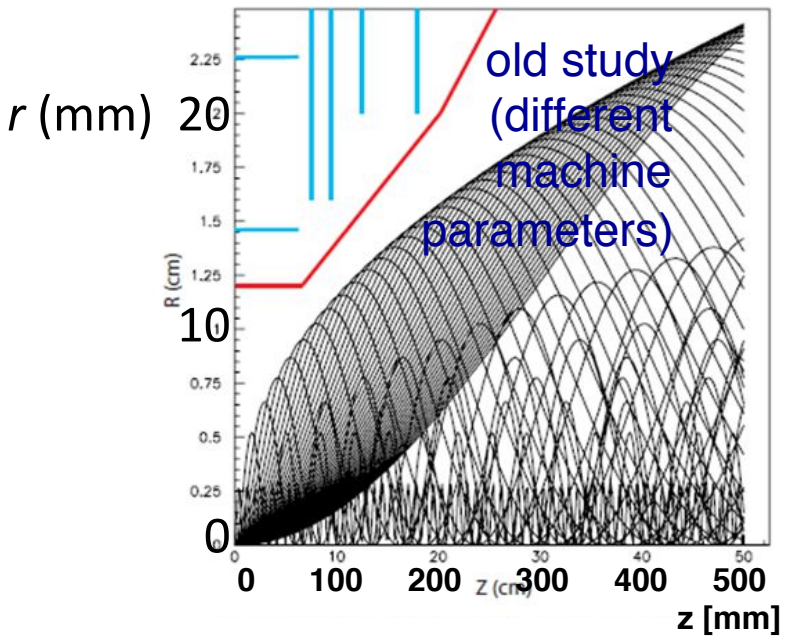


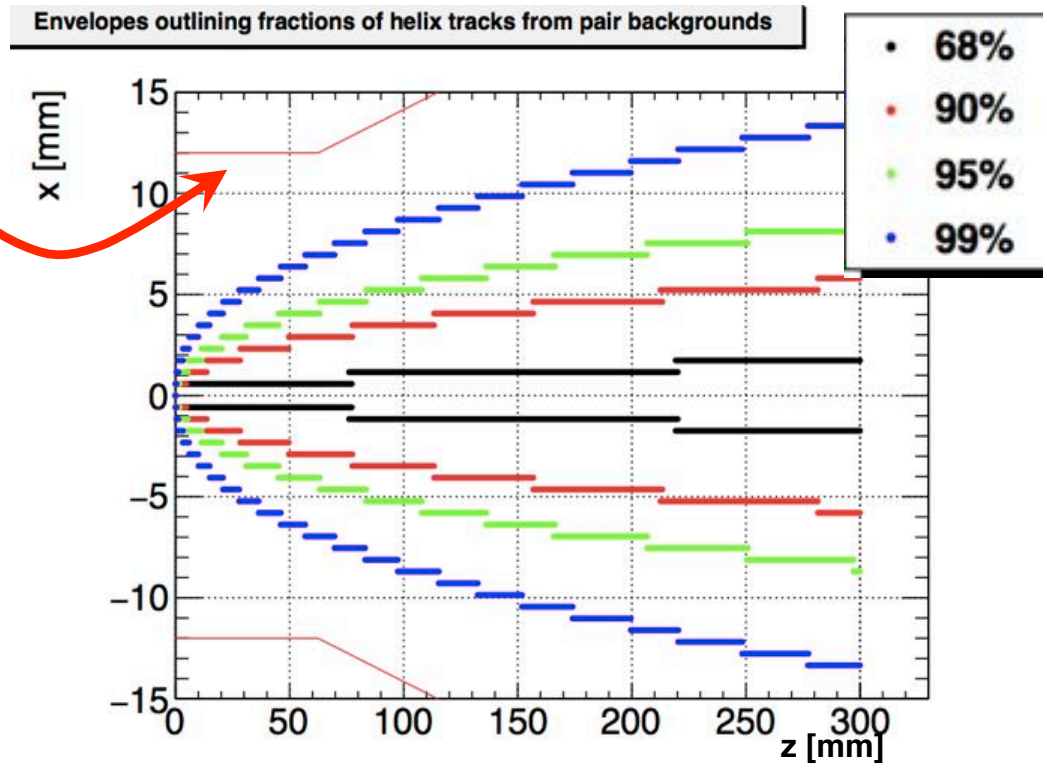
Re-analysed pair background envelope in beam pipe

New analysis!

- with current beam pipe design, around 0.45% of all particles leave tracks outside the beam pipe
- could consider reducing beam pipe radius by 2mm
- could consider an additional vertex detector layer for SiD

beam pipe



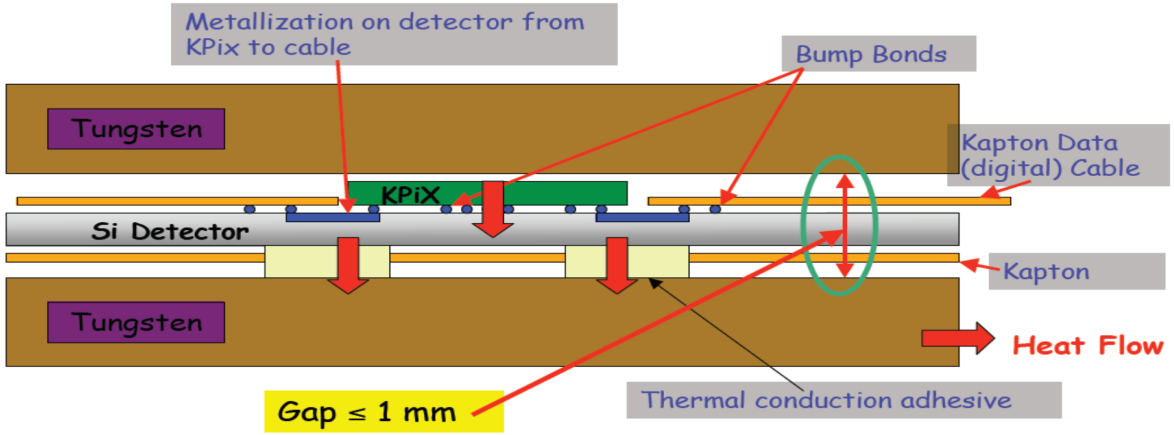


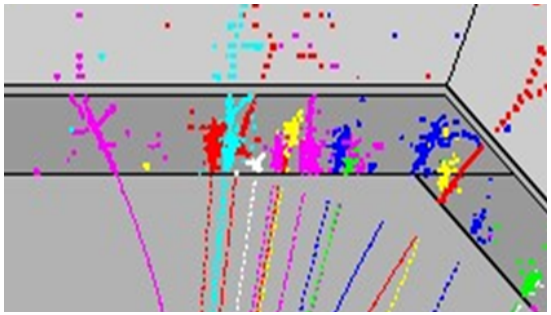
DESY

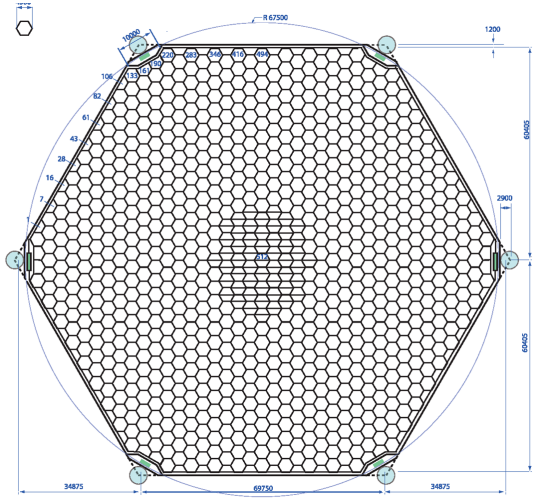
ECal

Highly granular 'imaging' calorimetry essential for ILC physics programme:

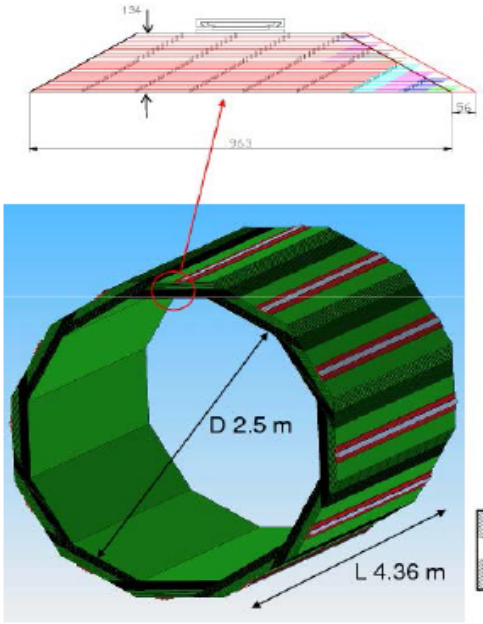
- Particle ID/reconstruction
- Tracking charged particles
- Integral part of Particle Flow detector design

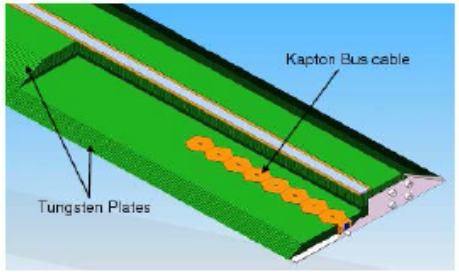


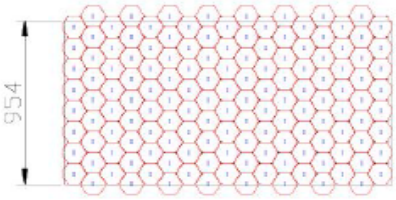


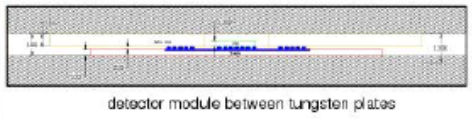


- Baseline design: silicon / tungsten









Baseline configuration:

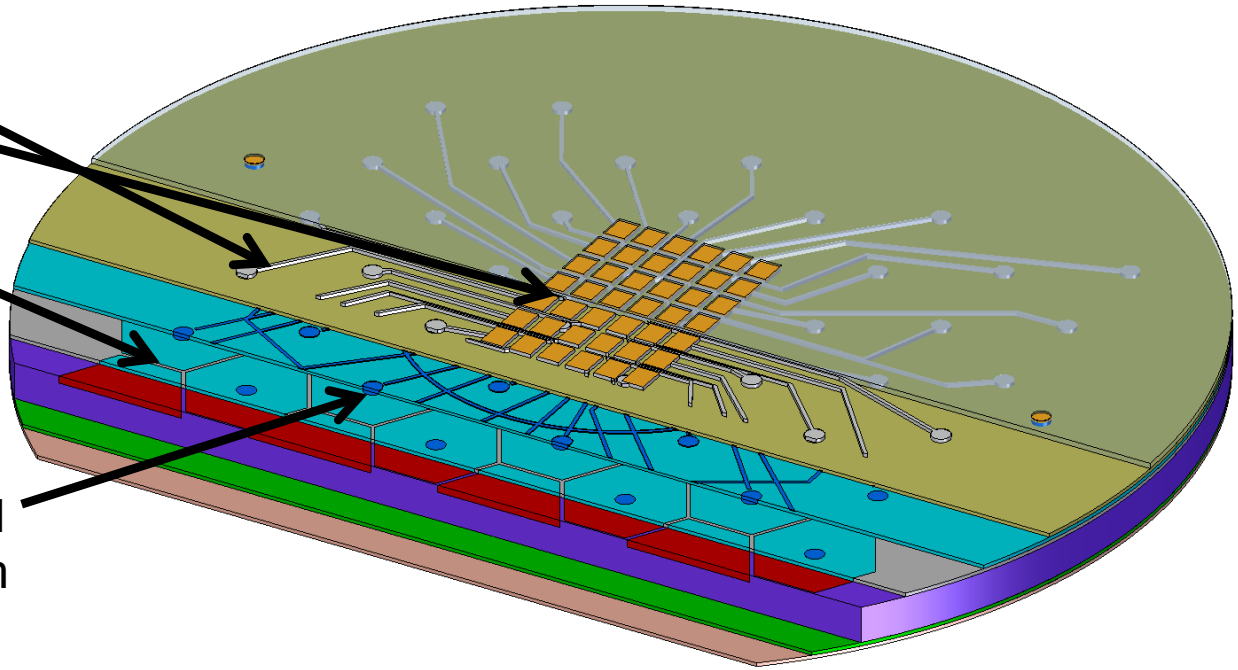
- transverse: 12 mm² pixels
- longitudinal: (20 x 5/7 X_0) + (10 x 10/7 X_0) ⇒ 17%/sqrt(E)
- 1 mm readout gaps ⇒ 13 mm effective Moliere radius

ECal sensors

Major lessons so far…:

- Bump bonding to sensors with Al pads can be very difficult
  – sensor foundry build final pad stack – Under Bump Metallization
- Sensors with ROCs can have issues with parasitic couplings
  – shield pixel traces

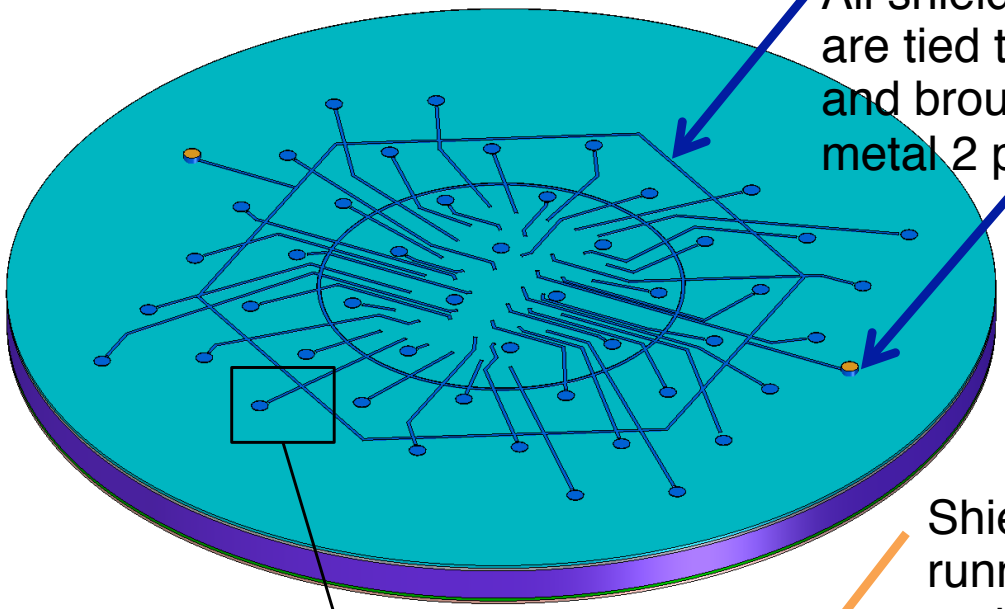
In present design, metal 2 traces from pixels to pad array run over other pixels: parasitic capacitances cause crosstalk.



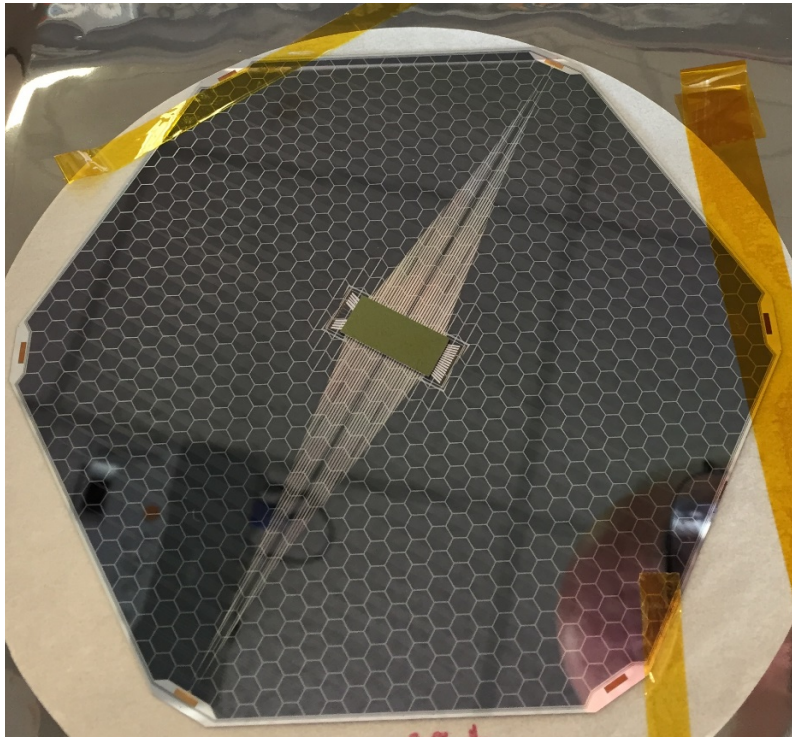
New scheme has “same” metal 2 traces, but a fixed potential metal 1 trace shields the signal traces from the pixels.

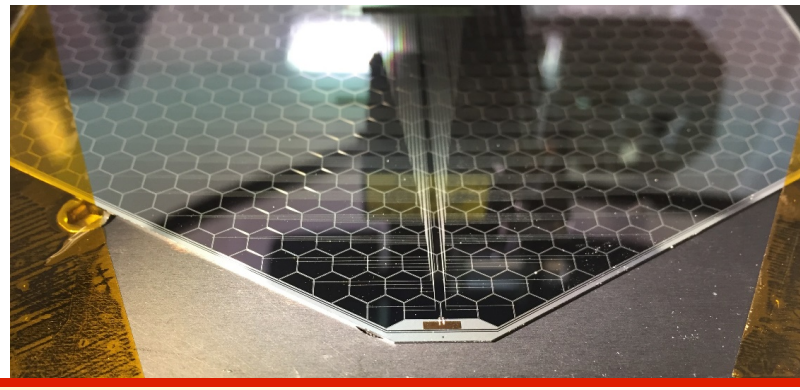
SLAC, Oregon, UC Davis

ECal sensors



New prototypes with KPiX attached

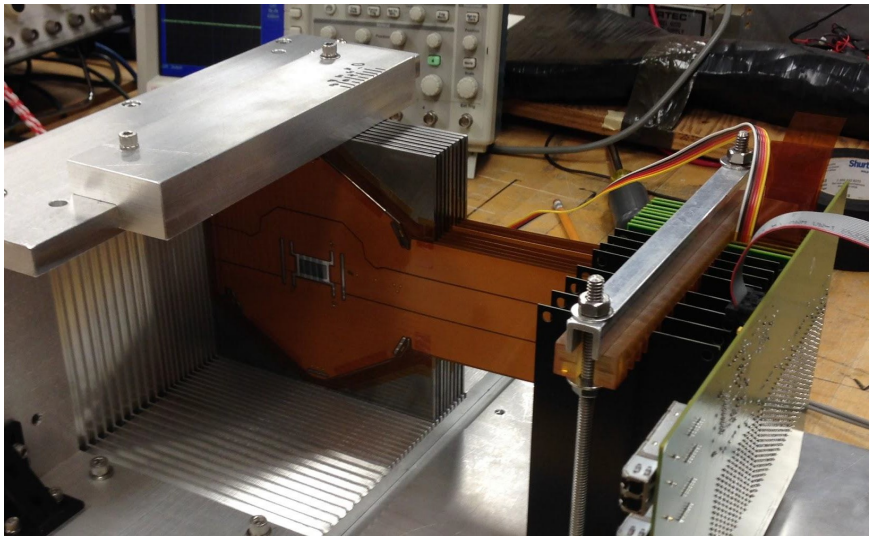




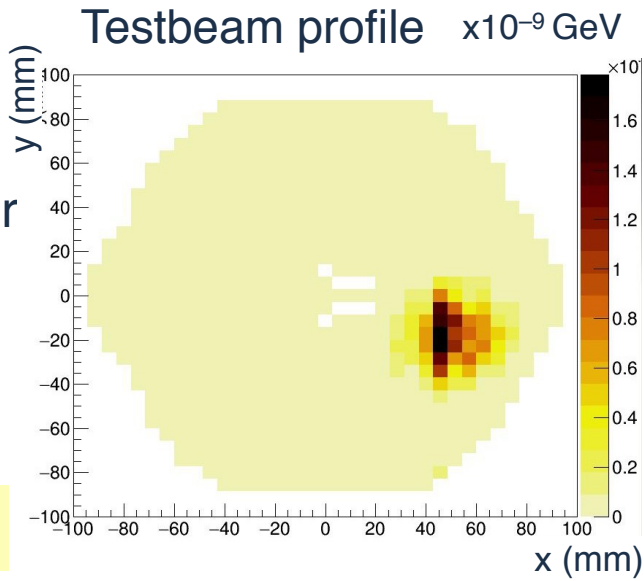
Testing underway, preparing for cable attachment →

SLAC, Oregon, UC Davis

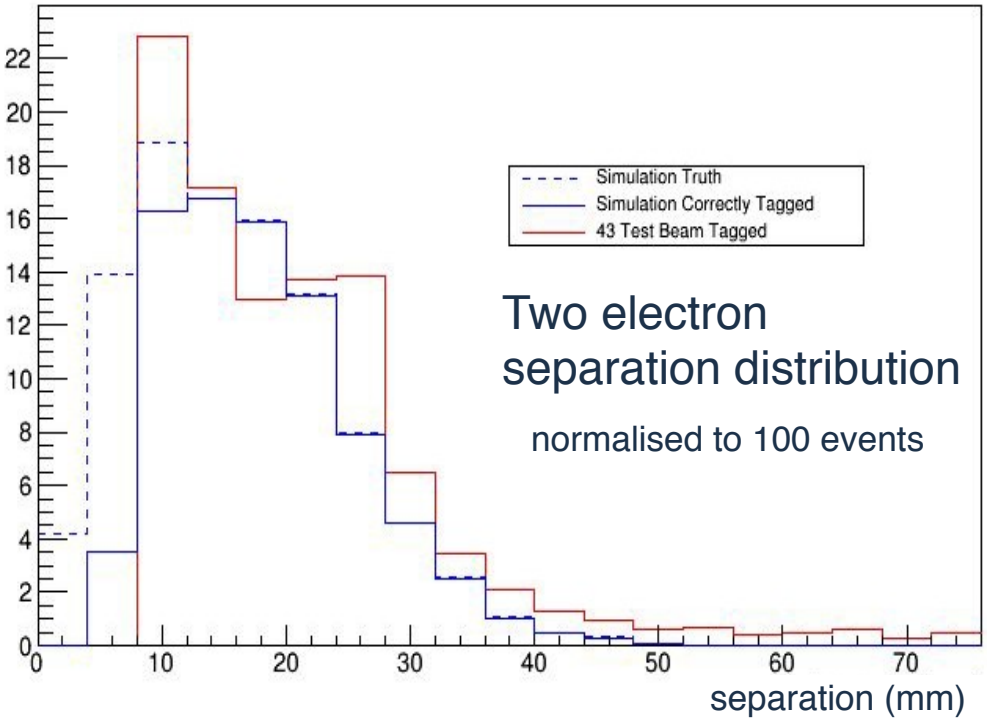
SiW ECal testbeam analysis

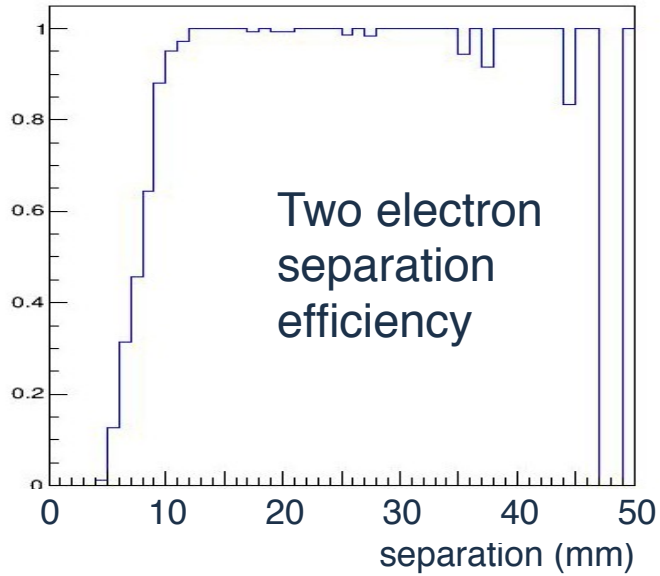


- 9-layer Si/W calorimeter
- ~6X_0
- 13mm^2 pixels
- 12.1GeV electrons



New analysis!

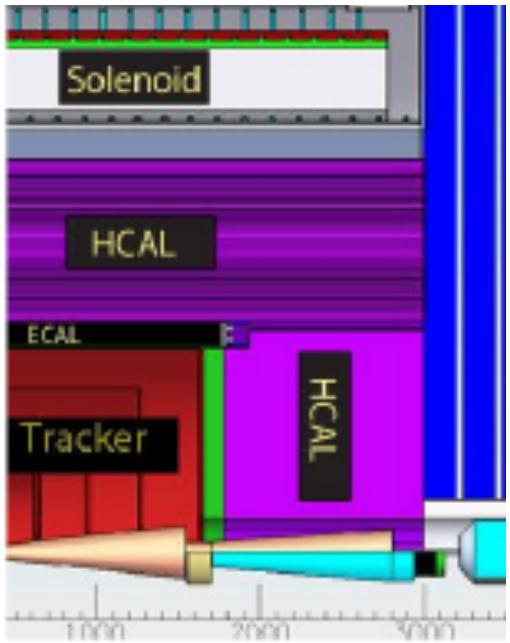




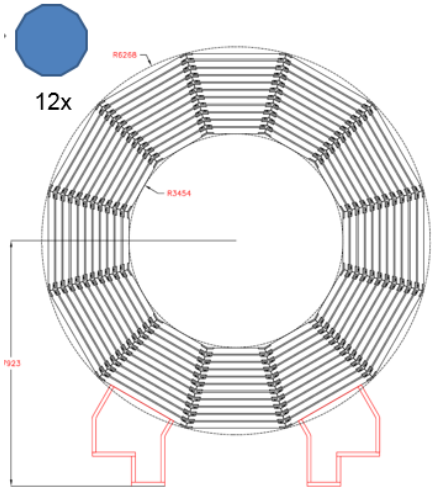
Oregon, SLAC, UC Davis

-> See talk by A. Steinhebel in Cal session (Wed pm)

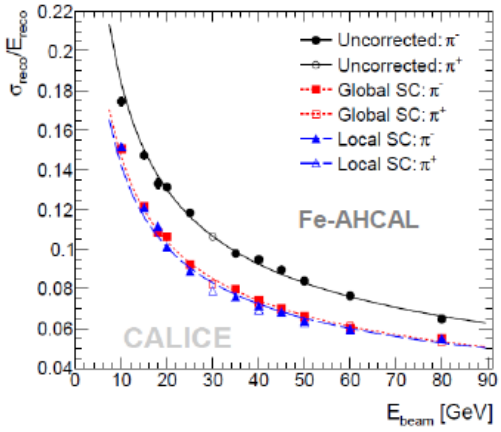
HCal

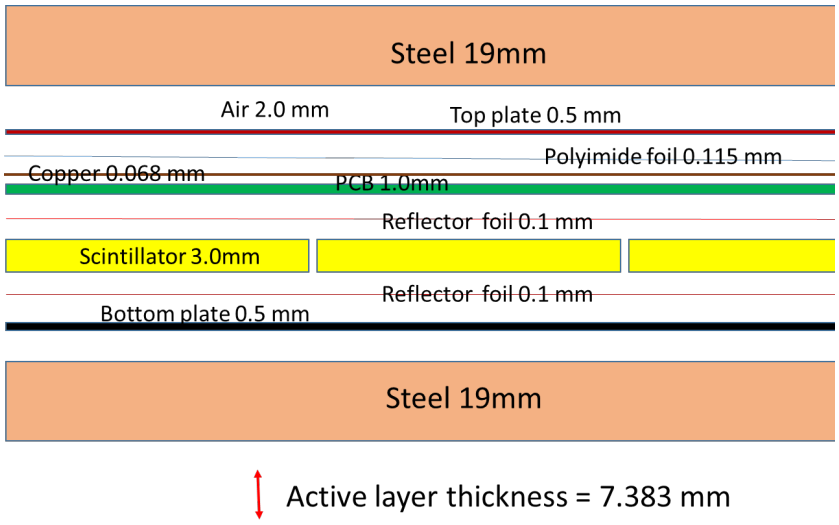


Following a review, new baseline technology for the SiD HCal is Scintillator / SiPM / Steel



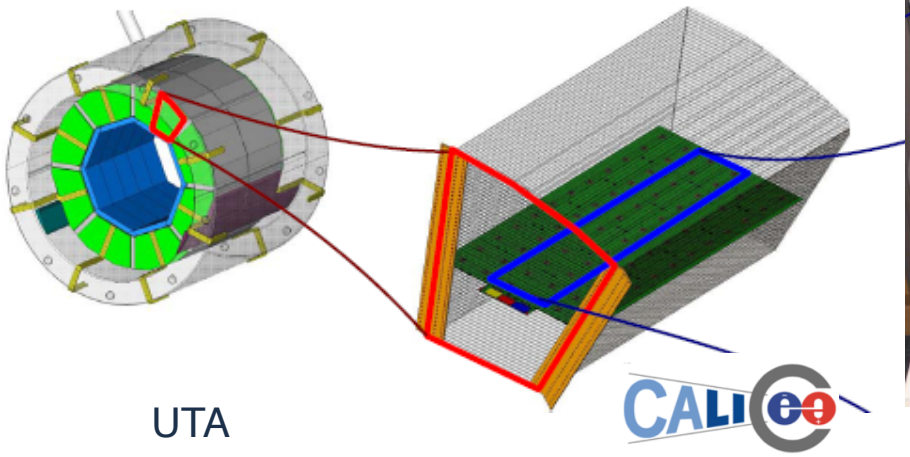
Work ongoing to compare simulated single-particle energy resolution with CALICE testbeam results



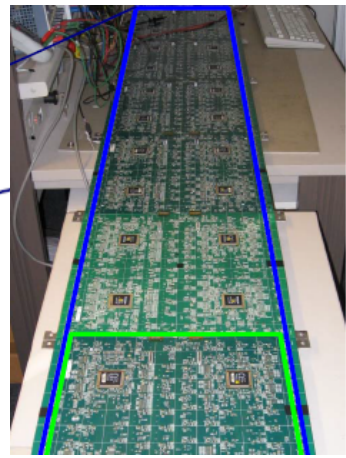


Active layer thickness = 7.383 mm

To come: mechanical design work following rebaselining

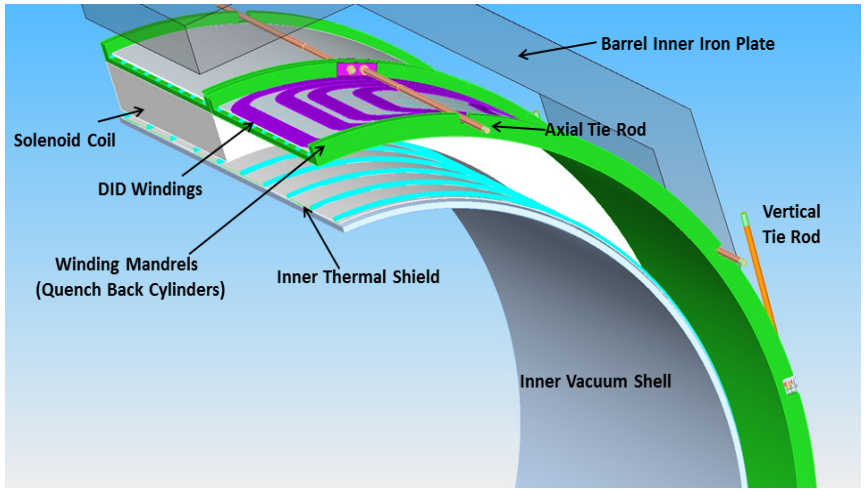


UTA

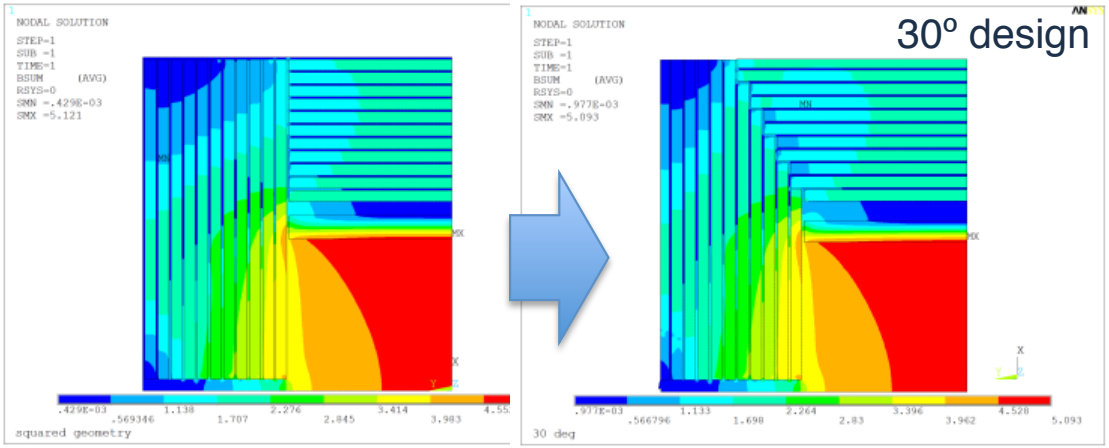


Solenoid

5T field

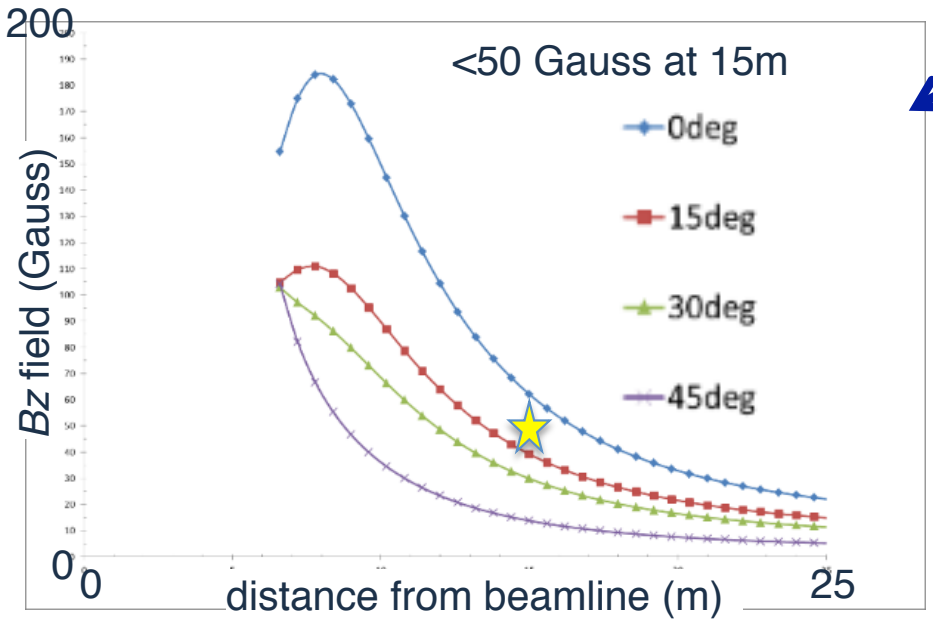


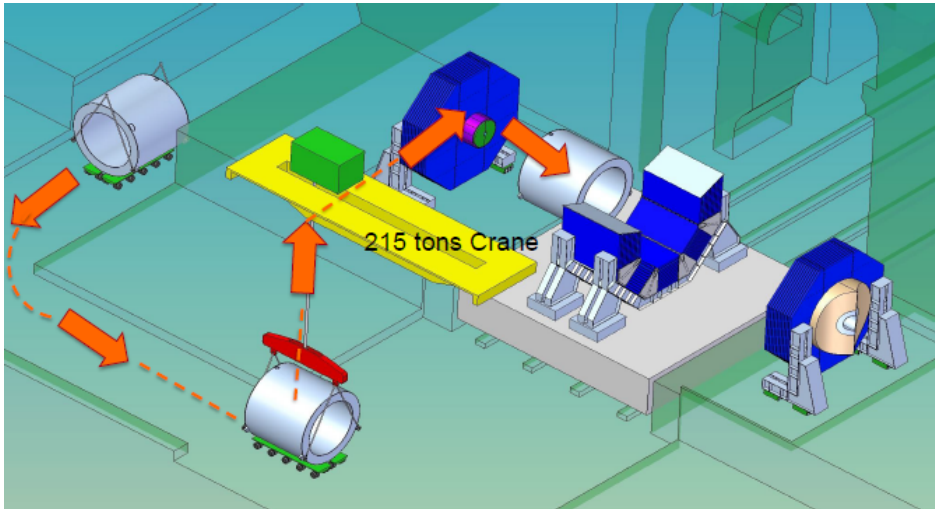
Baseline CMS conductor



Recent redesign of barrel / door junction:

- More efficient flux return
- Easier transport / handling



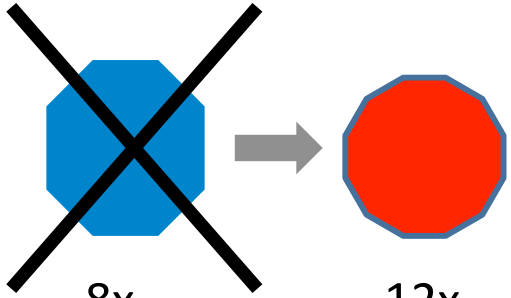


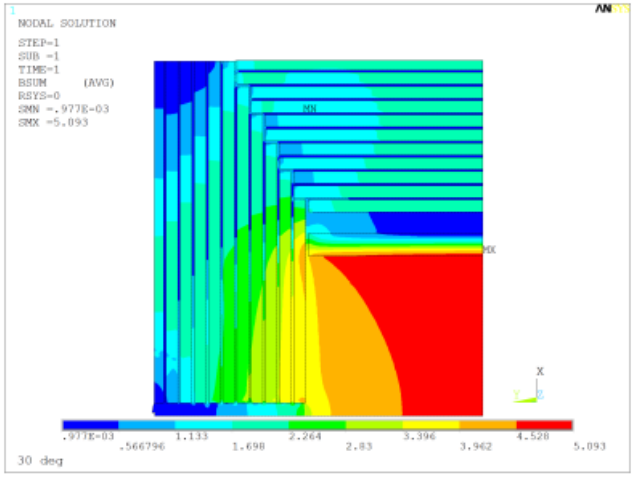
SLAC

Muon identifier / calorimeter tail catcher

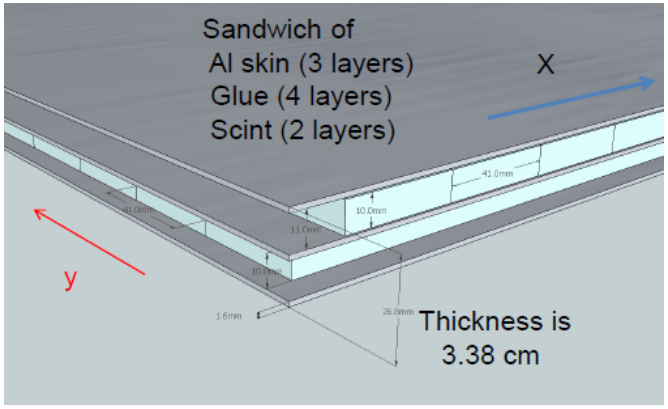
SiD baseline: long scintillator strips with WLS fibre and SiPM readout

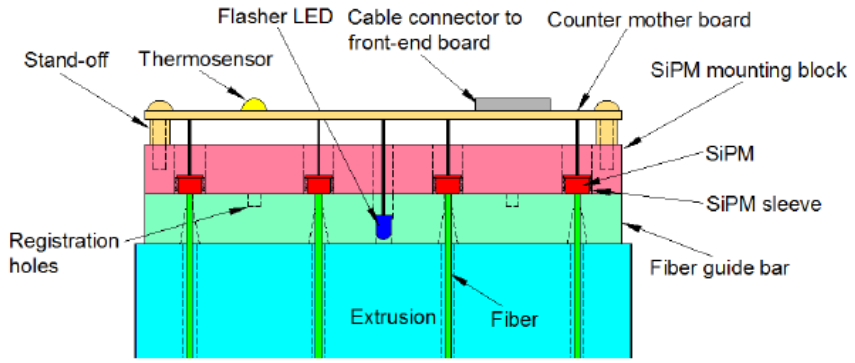
Yoke/Muon system changes since DBD:





- Consistent extension of the baseline HCal scintillator technology
- Need to optimize number of layers, strip dimensions



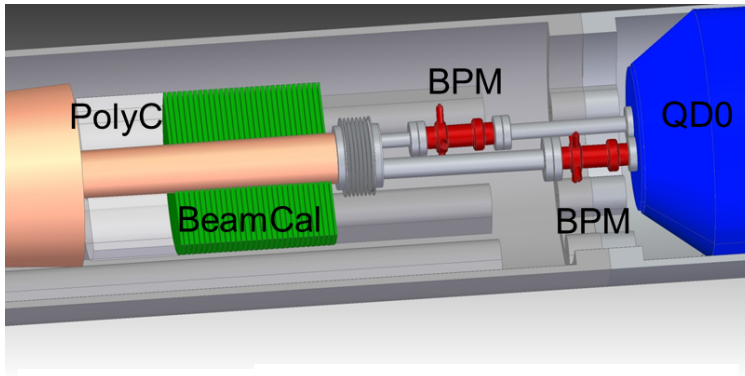


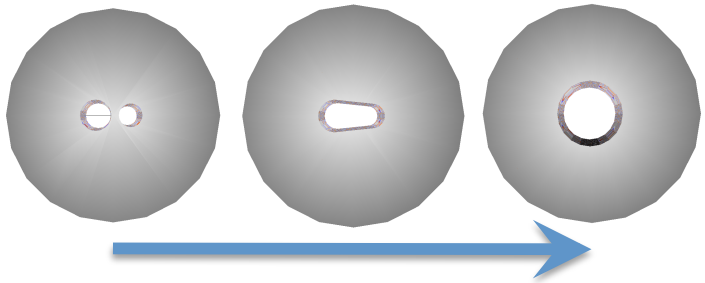
Forward region layout

Recent studies have looked at different aspects of the forward region layout

Set of related questions:

- Is the anti-DID necessary?
- What is the optimum forward calorimeter (BeamCal) shape?
- What buffer depth is required for forward/ inner detectors?

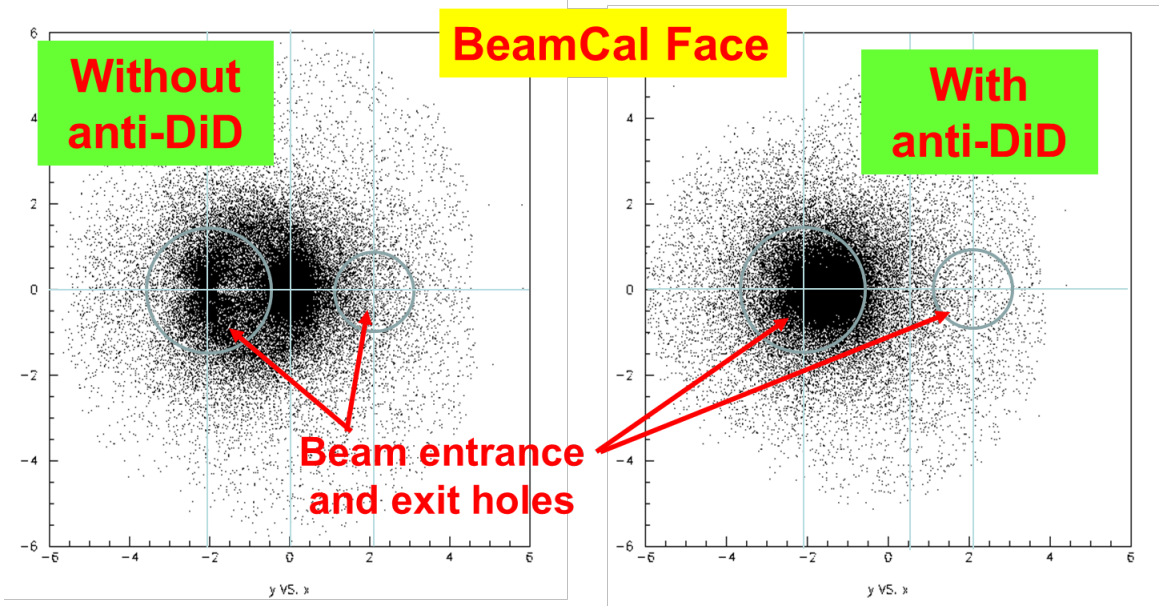




More aggressive approach to removing material from the path of backgrounds

Trade-off between BeamCal reconstruction efficiency and albedo effect

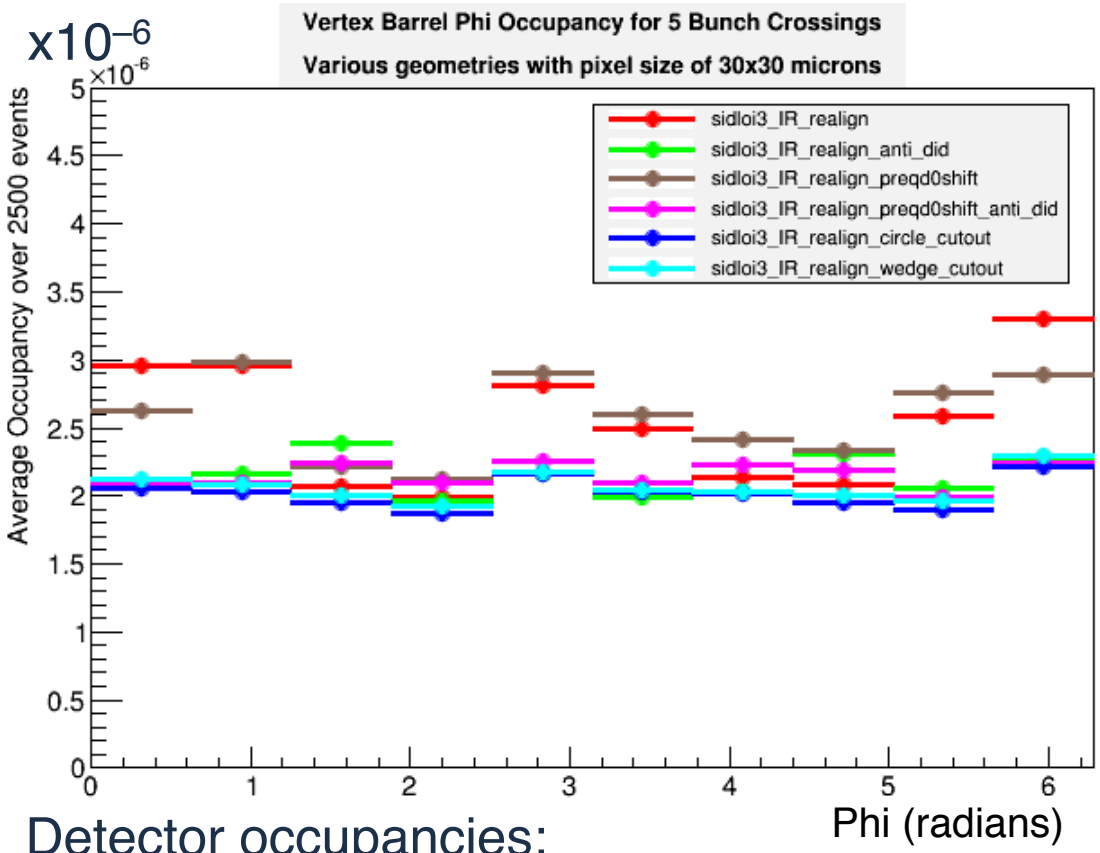
DID: Detector-integrated Dipole



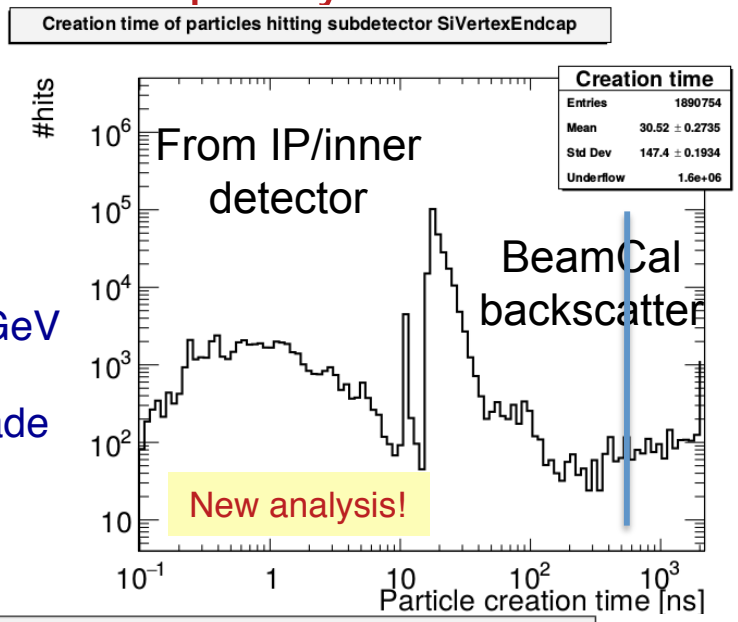
UCSC, SLAC

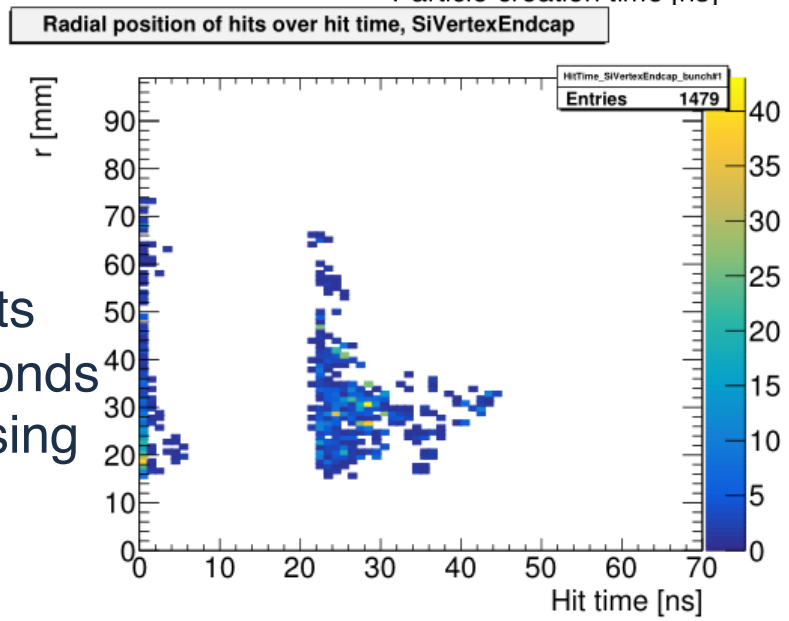
Vertex detector occupancy

Forward region design can affect vertex detector occupancy:



using 500 GeV lumi upgrade





Detector occupancies:
- with/without anti-DID
- different beam holes

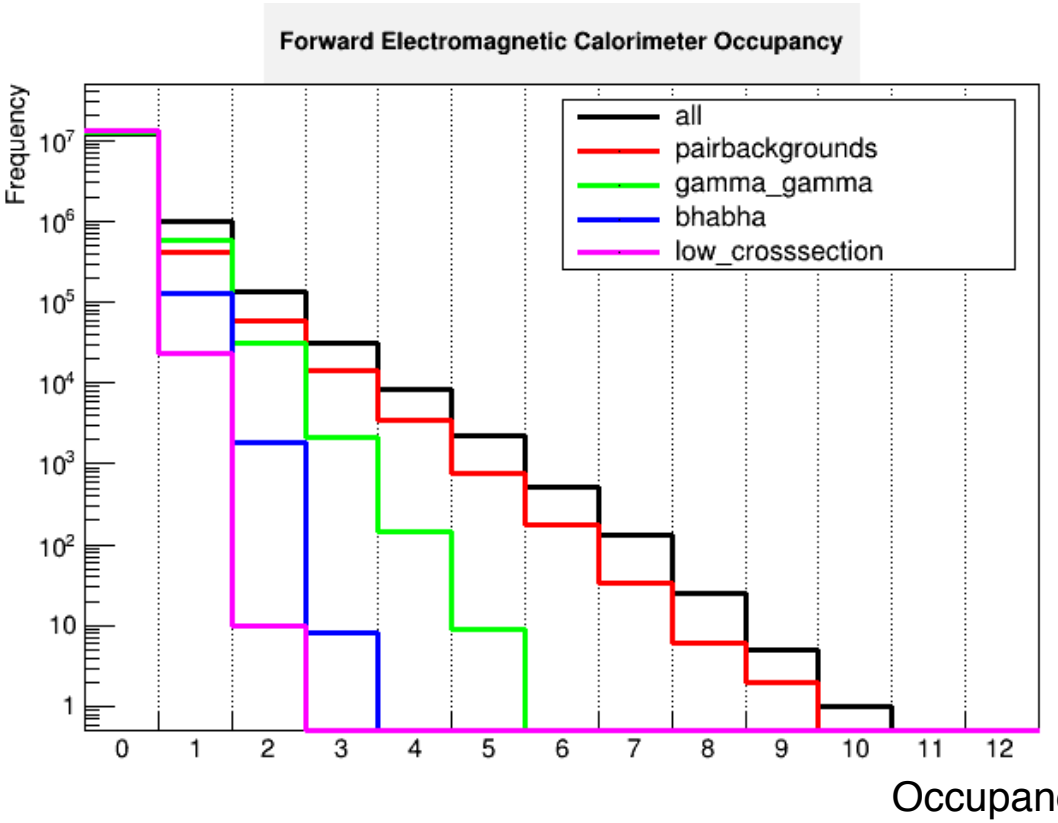
-> robust

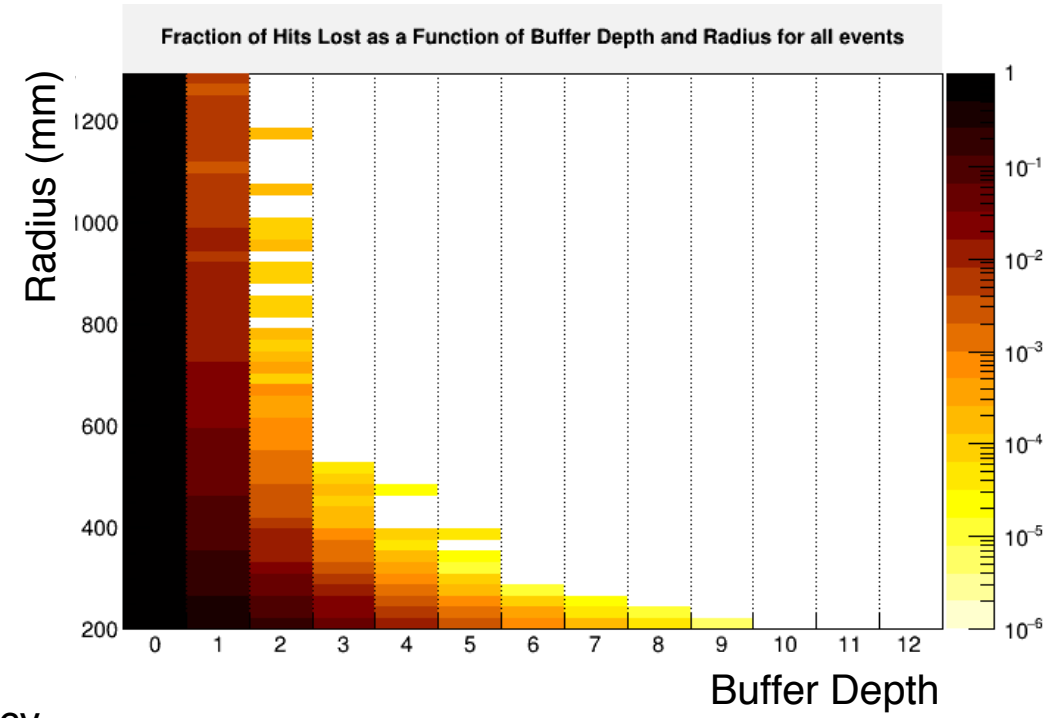
Background pairs hits can arrive microseconds after the beam crossing -> able to reject with timing cuts

DESY

see arXiv:1609.07816

Forward calorimeter buffer size





Detailed study of dominant low-angle backgrounds
using latest beam parameters
Many channels in forward ECal have ~10 hits per train

Depth of 4 buffers -> lose around 10^{-3} of hits
Depth of 6 buffers -> lose around 10^{-4}
-> need 8 buffers to maintain losses below 10^{-4} for innermost radii

see arXiv:1609.07816

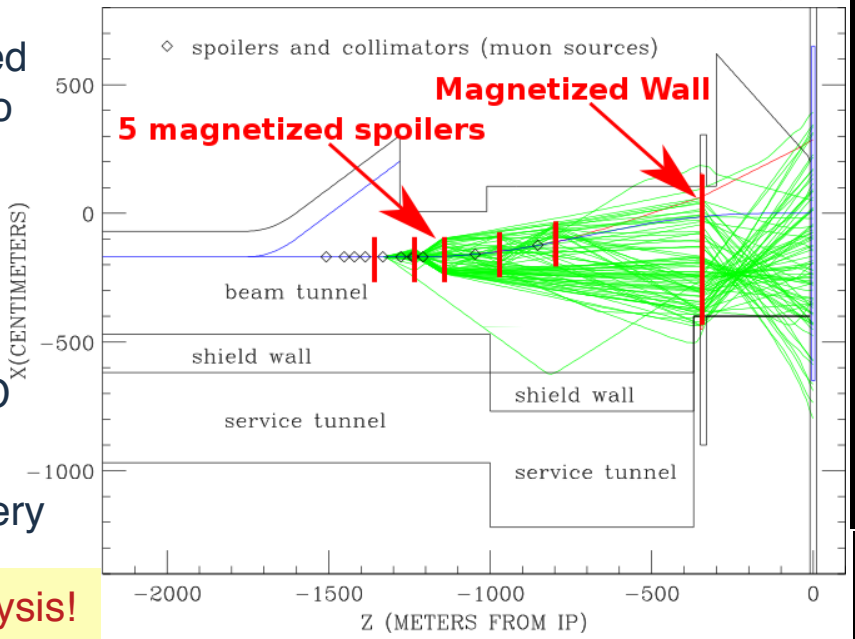
UCSC

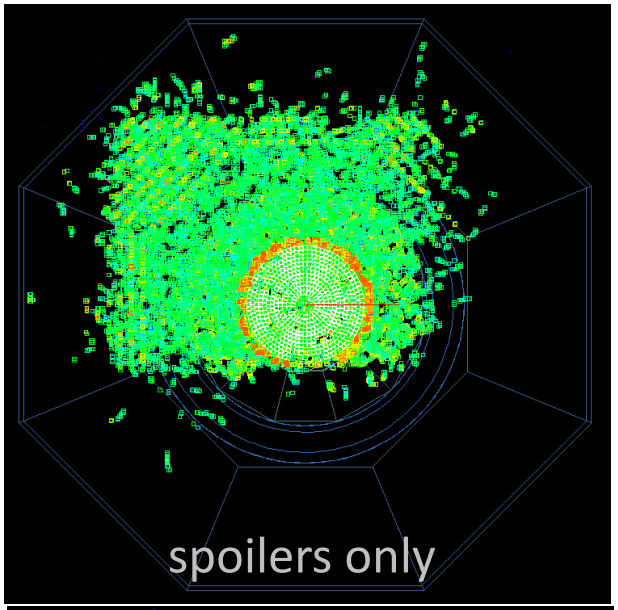
Beam-related muon background

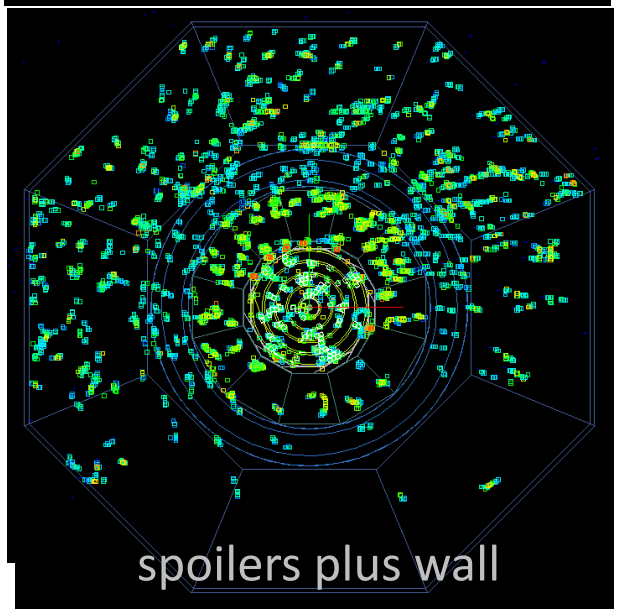
Shield detectors from muons from beam delivery sys

- Magnetized spoilers intended to sweep muons from BDS into tunnel walls
- Is magnetized wall also necessary?
- Simulated with MUCARLO from BDS plus full Geant 4 SiD detector simulation
- ECcalEndcap occupancy very high without wall

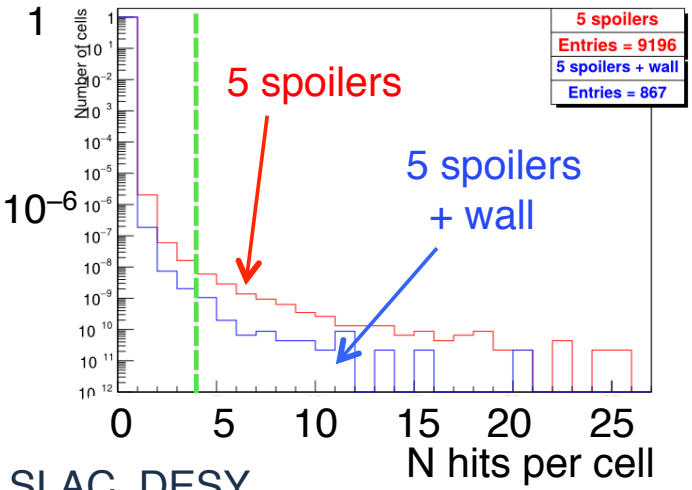
New analysis!



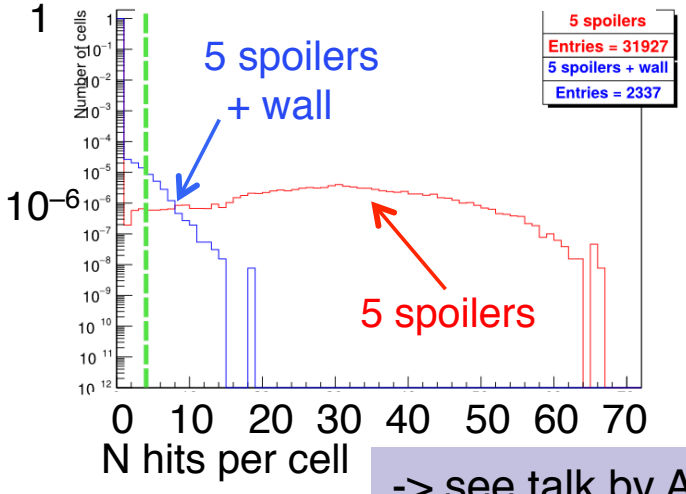




Occupancy, SiTrackerEndcap



Occupancy, ECalEndcap

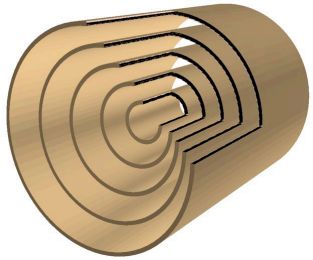


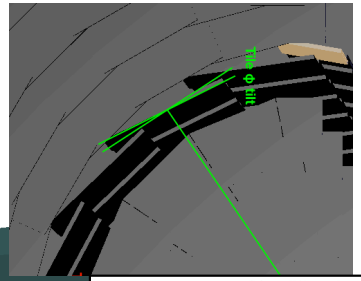
SLAC, DESY

-> see talk by A. Schuetz in MDI session (Thurs)

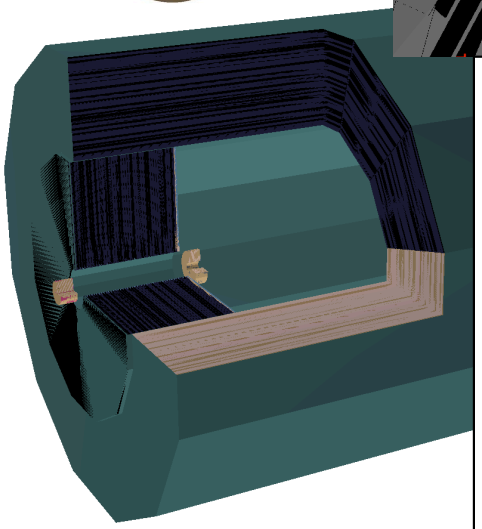
Simulation & reconstruction

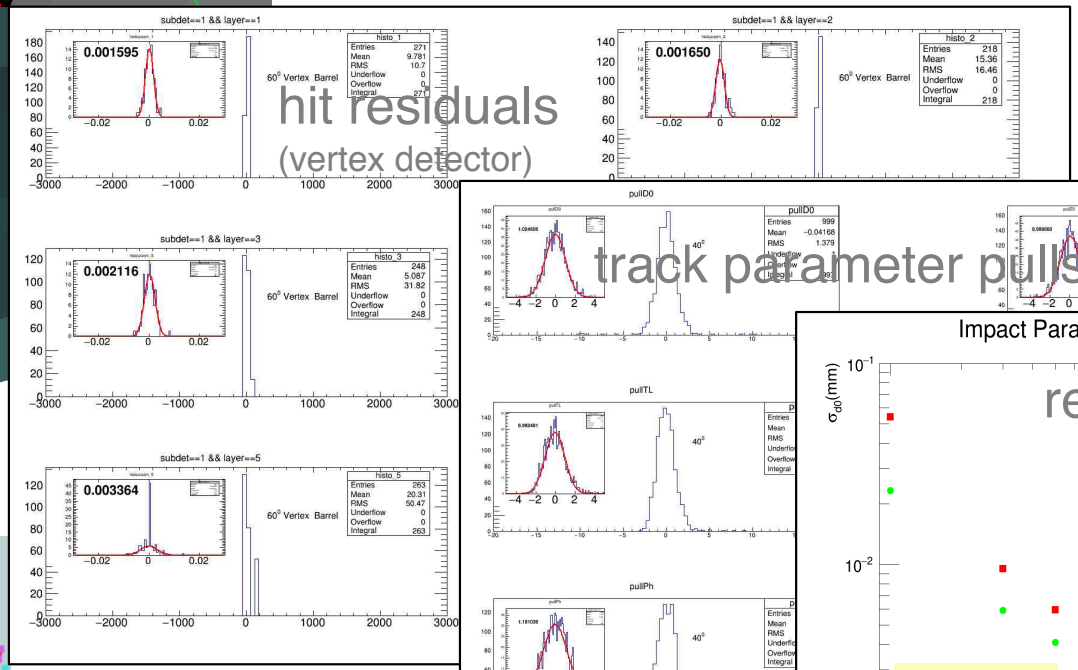
At LCWS15, SiD decided to implement DD4HEP simulation and common reco



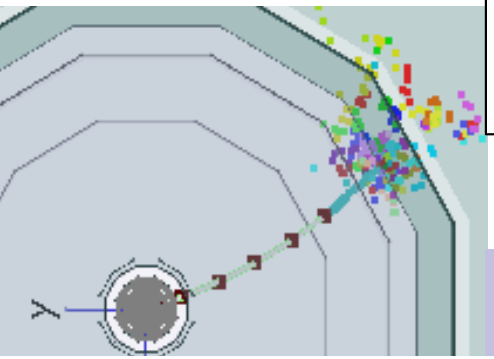


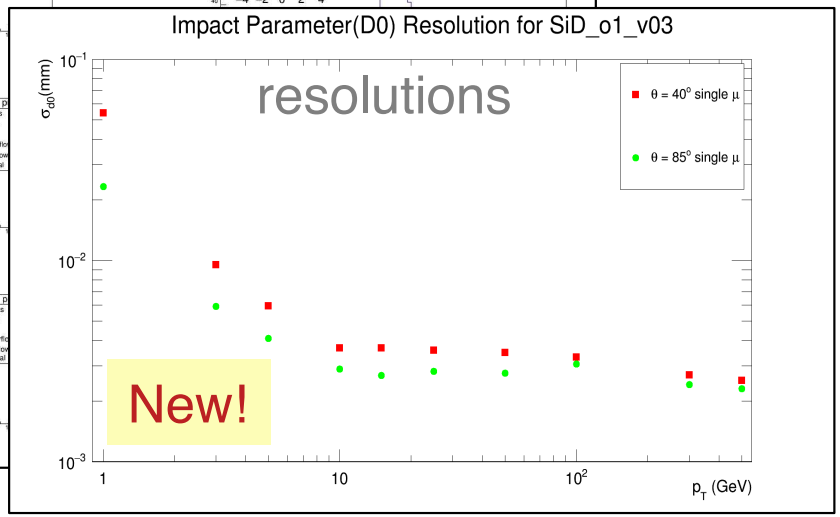
- Implemented geometry and drivers
- Updated to latest digitizers
- Developing performance benchmarking tools
- Currently commissioning full conformal pattern recognition (as implemented by CLICdp) & Pandora PFA





Relies on close collaboration/support from CLICdp and ILD developers





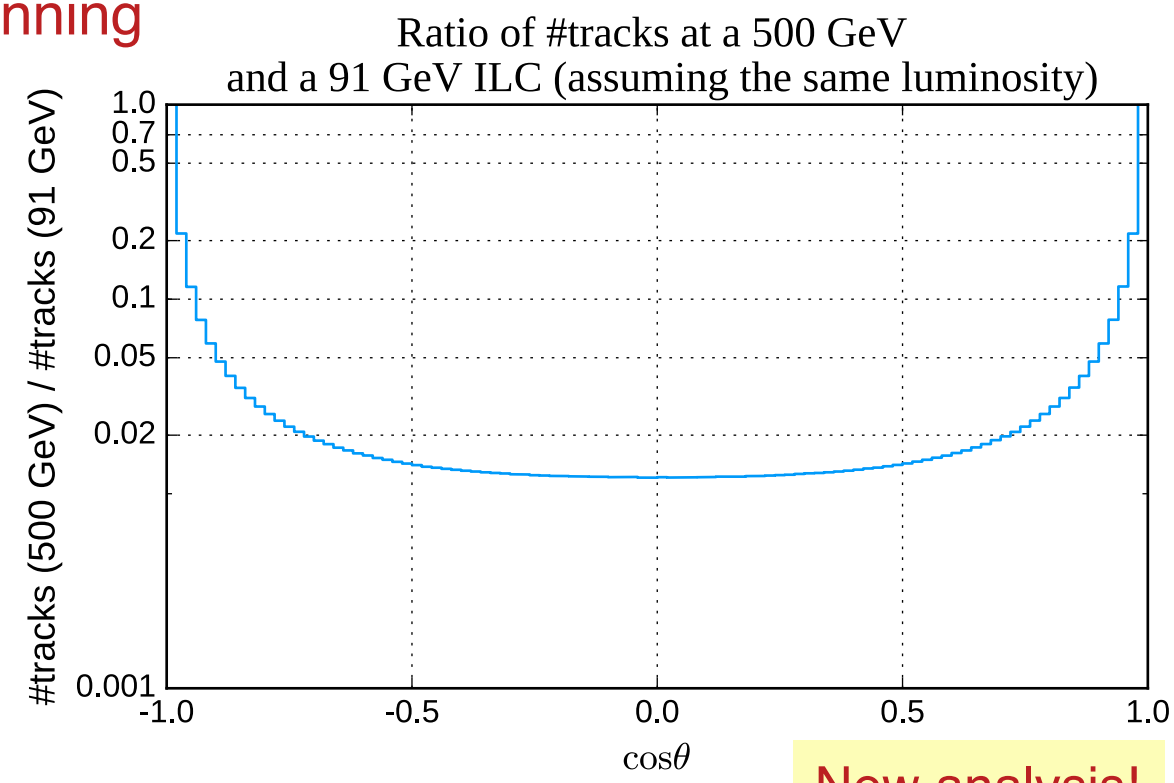
-> See talk by B. Mishchenko in Sim/Reco/Perf session (Tue am)

Glasgow, UTA, Oregon, UCSC

Alignment and Calibration strategies

Considering question of Z-pole running

- Track-based alignment essential for high-precision tracking
- Low cross-section of relevant processes => limited high-pT tracks
  - currently, SiD has no reason to believe this will improve by running the machine at the Z pole
- Rough estimation: 1000 tracks / month / module in outer tracker during ramp-up in the first year



New analysis!

- SiD has started to look at different strategies to augment alignment
  - ATLAS-like FSI
  - changes to electronics to increase efficiency for cosmics
- Currently back-of-the-envelope calculations only
- Discussions in the dedicated session tomorrow

Bristol, PNNL

-> see talk by J. Strube in ZPole session (Tue pm)

Collaboration activities

Excellent SiD software/optimization workshop at PNNL in September

ILC NEWSLINE
THE NEWSLETTER OF THE LINEAR COLLIDER COMMUNITY

CURRENT ISSUE
3 NOVEMBER 2016

Calorimeter under telescope scrutiny
Strasbourg steers ILC towards ESRFI roadmap
Construction completed: ILC in Roppongi
Download the current issue as a full .pdf

ANNOUNCEMENTS

LCWS2016 early registration deadline extended

The early registration deadline for LCWS2016 in Morioka, Japan, has been extended to 7 November.

CALENDAR

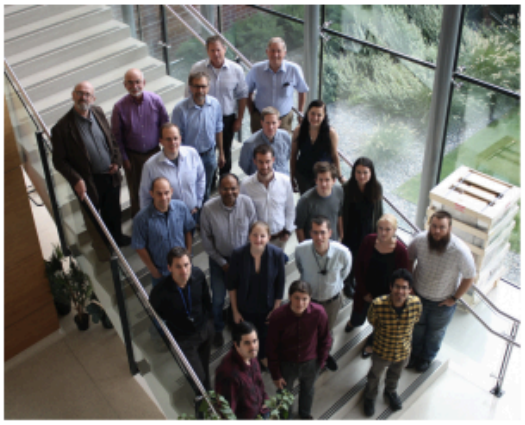
Upcoming Events

International Workshop on Future Linear Colliders

FEATURE

SiD optimisation group moves towards new detector model after PNNL meeting

Jan Strube, PNNL | 20 October 2016



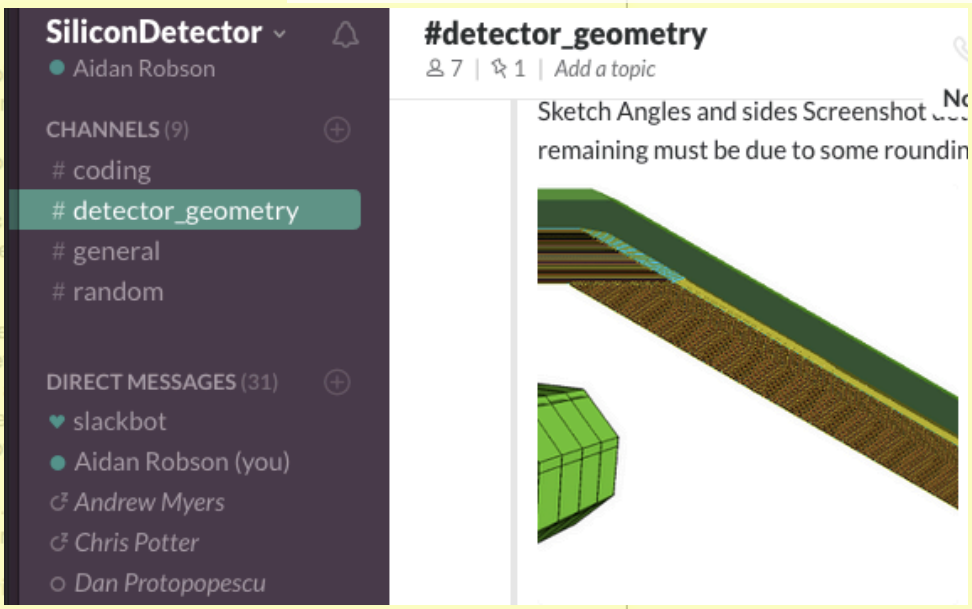
Participants of the 2016 SiD optimisation workshop at PNNL.

With LCWS in Mori… students from the U… Cruz and University… SiD optimisation gr… dedicated to getting… framework. The Pac… event, and 20 peopl… WA, about 14 miles…

While the ILC accel… have a way to go be… consortium decided… reconstruction to the… partially supported b… disruptive, as users… based infrastructure… support for SiD's co…

The benefits of having a common event data model like LCIO became obv… the old framework could easily be read in the new framework.

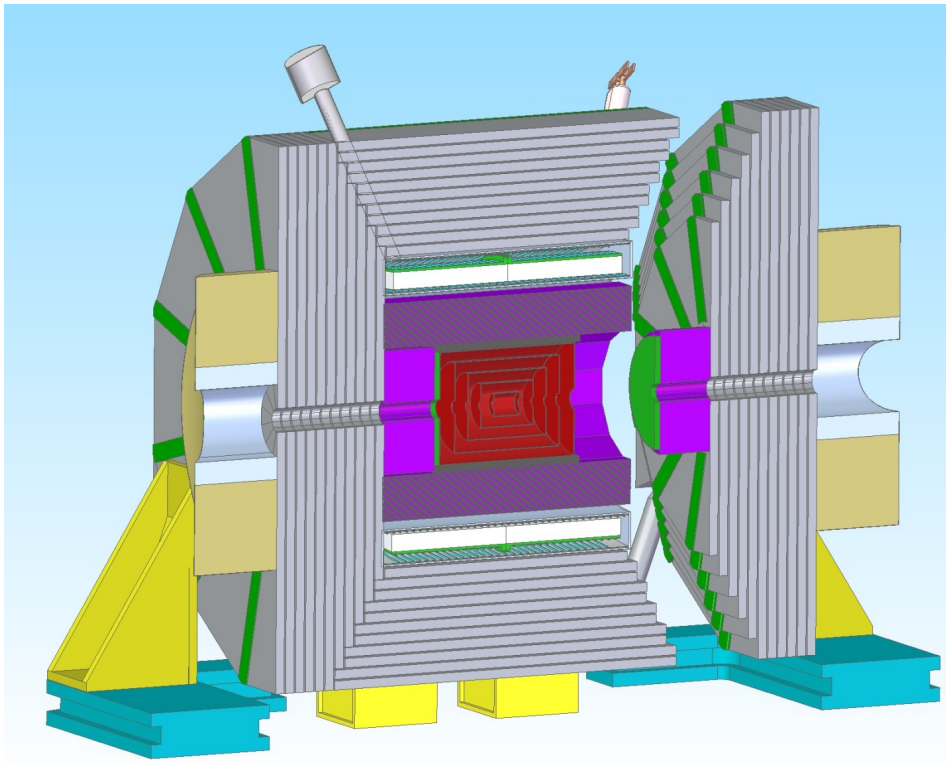
Work continuing via weekly meetings and collaborative tools e.g. slack channels



Outlook

- SiD is a compact, capable detector
- Well-defined baseline that exceeds physics requirements
- Evolving: a lot of activity in detector R&D and in optimization
  - readout
  - sensors
  - structures
  - layout
  - simulation and reconstruction
- …but limited effort available.

So if you have ideas for the application of new technologies, software development, or new physics studies, we welcome to you consider joining the SiD Consortium!



-> all welcome to come to SiD session (Wed am)

Backup

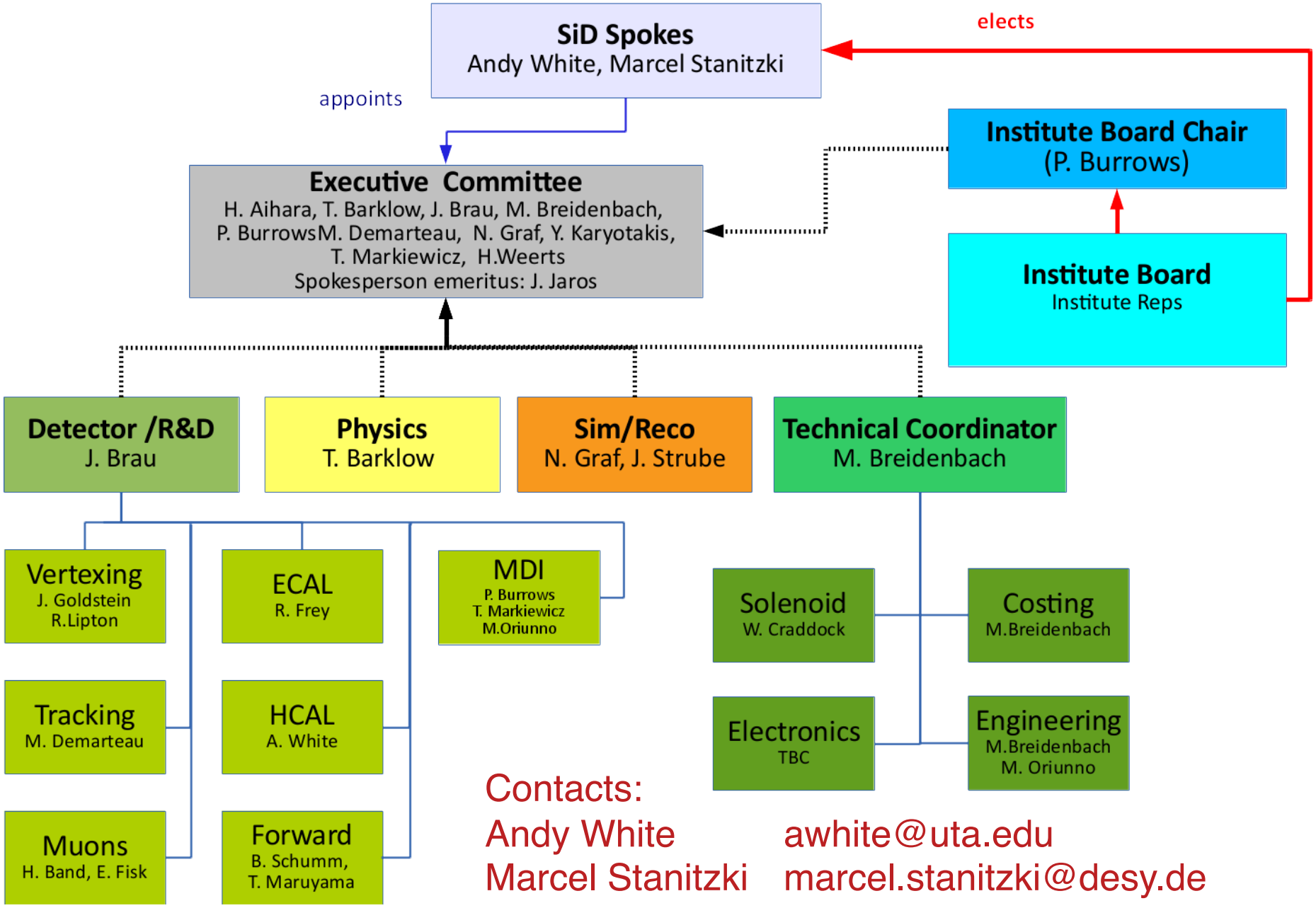
SiD Consortium

SiD Consortium Member Institutions

- Argonne National Laboratory
- Universitat de Barcelona
- University of Bergen
- Bristol University
- University of California, Davis
- University of California, Santa Cruz
- Cornell University
- Fermi National Accelerator Laboratory
- University of Glasgow
- University of Iowa
- LAPP Annecy
- Lawrence Livermore National Laboratory
- University of Manchester
- The Open University
- University of Oregon
- Oxford University
- Pacific Northwest National Laboratory
- Queen Mary University of London
- Rutherford-Appleton Laboratory
- SLAC National Accelerator Laboratory
- University of Texas, Arlington
- Tohoku University
- University of Tokyo
- Yale University

Spokespeople:
Andy White awhite@uta.edu
Marcel Stanitzki marcel.stanitzki@desy.de

SiD Organisation



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