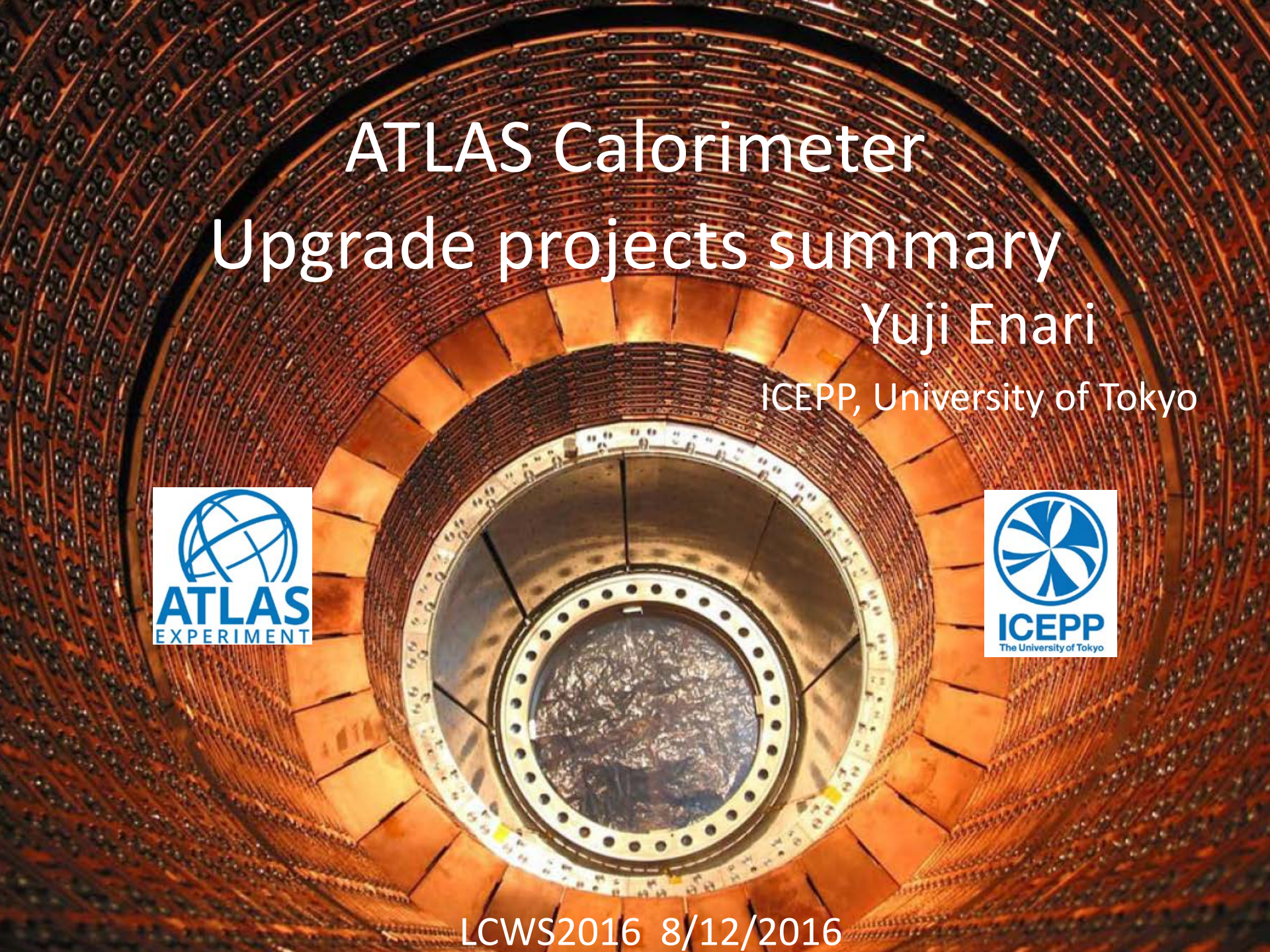


ATLAS Calorimeter Upgrade projects summary

Yuji Enari

ICEPP, University of Tokyo

LCWS2016 8/12/2016

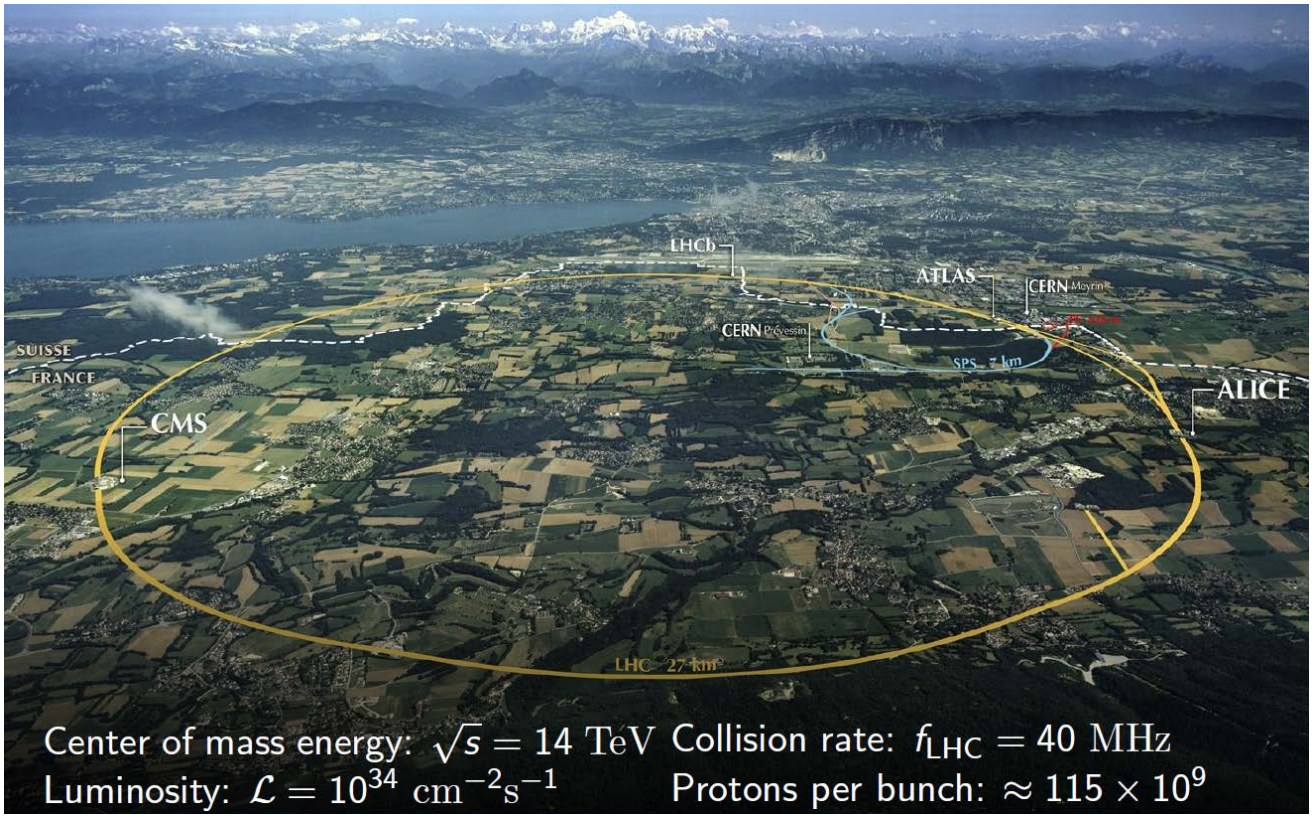
Contents

- Introduction
  - LHC schedule
- ATLAS calorimeter upgrade project
  - High Granularity Timing Detector
    - Concept and first beam test results
  - Readout Electronics R&Ds
    - ASIC & system
- Summary

LHC upgrade schedule

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2035
LS1		Run-2			LS2		Run-3			LS3		Hi-Lumi	

Run-2	Run-3	Hi-Lumi
$\sqrt{s}$ = 13-14 TeV	$\sqrt{s}$ = 14 TeV	$\sqrt{s}$ = 14 TeV
L = 1×10^{34} cm^{-2}s^{-1}	L = 2×10^{34} cm^{-2}s^{-1}	L = $5\sim7 \times 10^{34}$ cm^{-2}s^{-1}
$\int$Ldt = 100~120 fb^{-1}	$\int$Ldt = 300 fb^{-1}	$\int$Ldt = 3000 fb^{-1}



LHC upgrade plan

2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2035

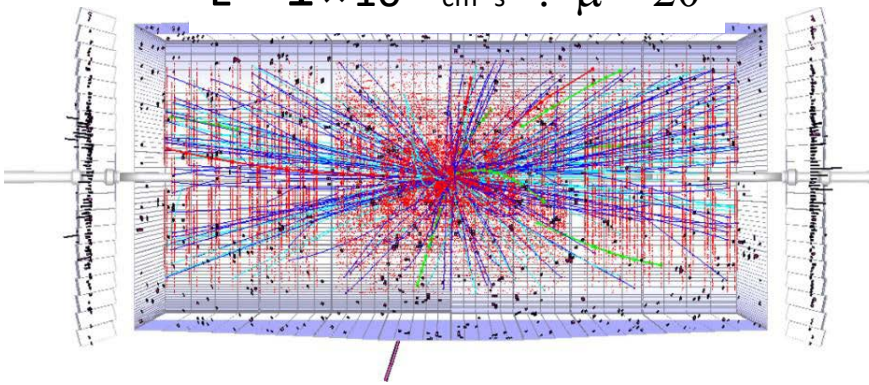
LS1	Run-2	LS2	Run-3	LS3	Hi-Lumi

Run-2	Run-3	Hi-Lumi
$\sqrt{s}$ = 13-14 TeV	$\sqrt{s}$ = 14 TeV	$\sqrt{s}$ = 14 TeV
$L = 1 \times 10^{34}$ cm^{-2}s^{-1}	$L = 2 \times 10^{34}$ cm^{-2}s^{-1}	$L = 5\sim7 \times 10^{34}$ cm^{-2}s^{-1}
$\int Ldt$ = 150 fb^{-1}	$\int Ldt$ = 300 fb^{-1}	$\int Ldt$ = 3000 fb^{-1}

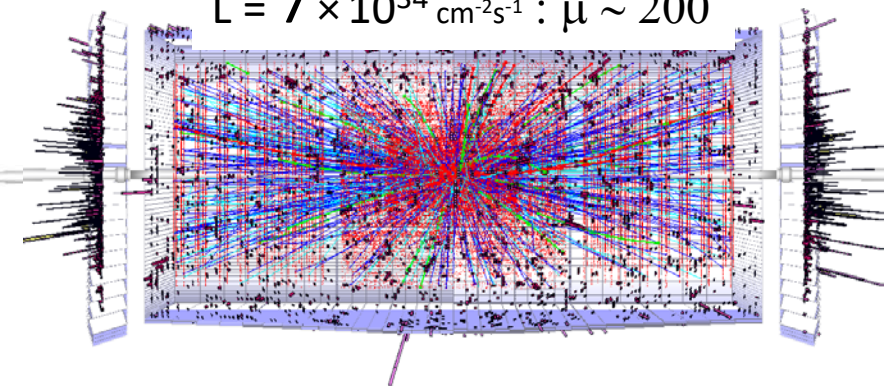
Accelerator, Detector upgrades.

Simulation for Z→ μμ

$L = 1 \times 10^{34}$ cm^{-2}s^{-1} : μ ~ 20



$L = 7 \times 10^{34}$ cm^{-2}s^{-1} : μ ~ 200



- Challenge at high luminosity: Pileup
  - Trigger and detector performance.

LHC upgrade plan

2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2035

LS1 | Run-3 | LS3 | Hi-Lumi

14 TeV

2×10^{34} cm^{-2}s^{-1}

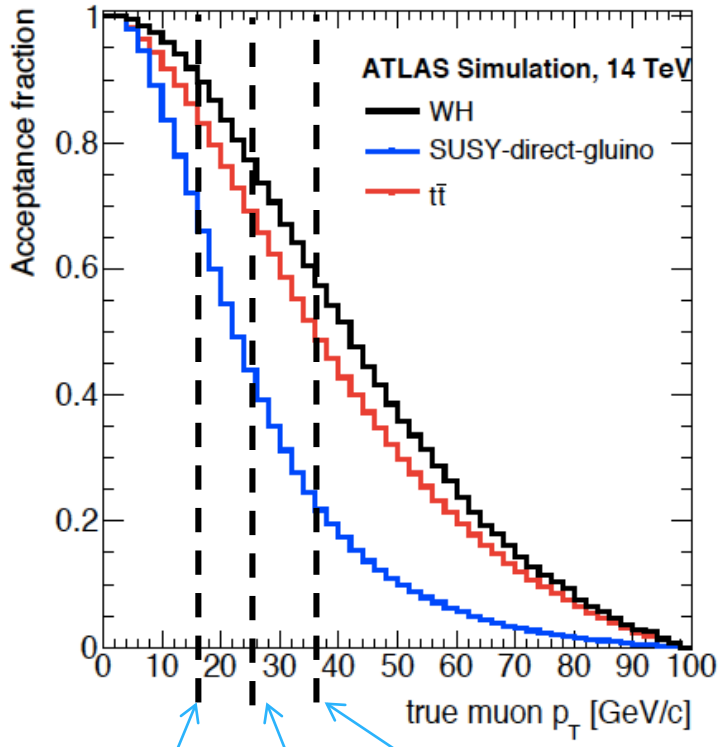
= 300 fb^{-1}

)etector upgrades.

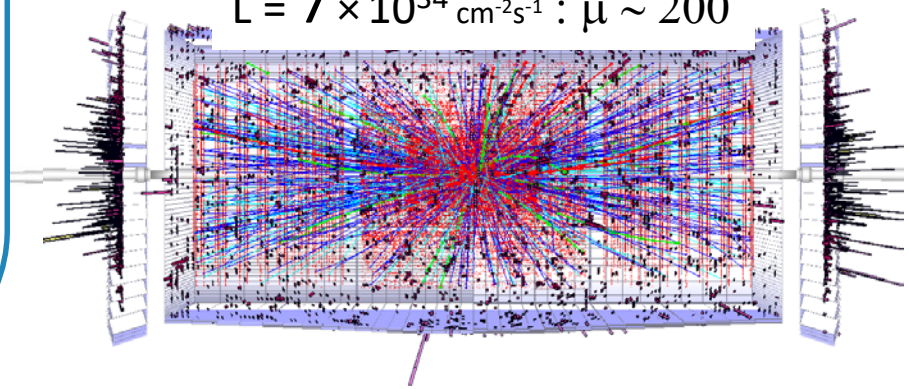
$\sqrt{s}$ = 14 TeV

L = 5~7 $\times 10^{34}$ cm^{-2}s^{-1}

$\int$Ldt = 3000 fb^{-1}

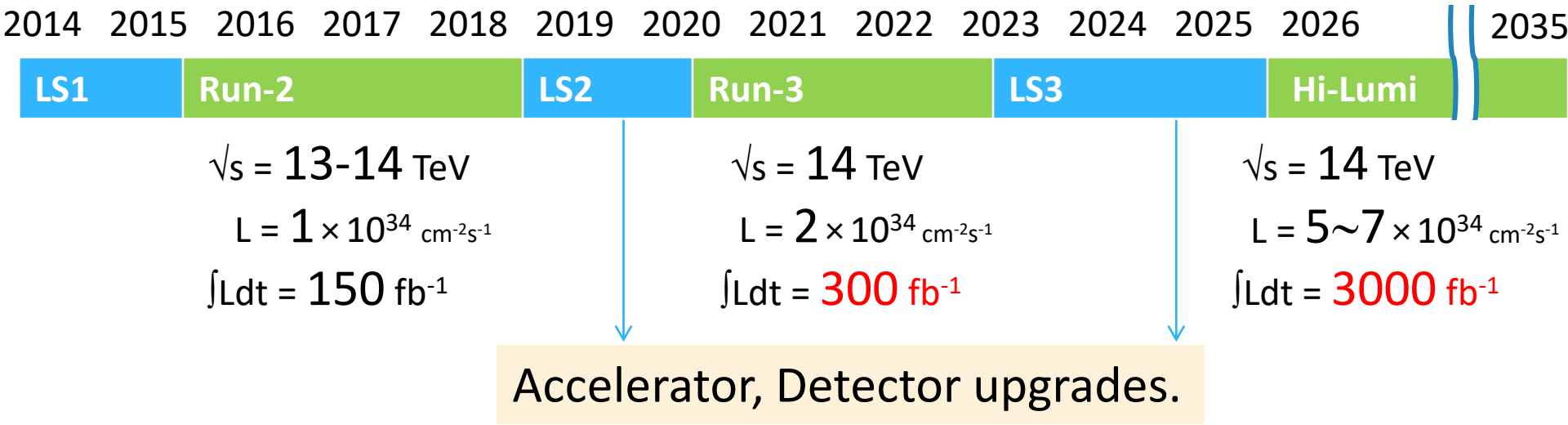


L = 7 $\times 10^{34}$ cm^{-2}s^{-1} : $\mu \sim 200$



- Challenge at high luminosity: Pileup
  - Detector performance, Trigger.

LHC upgrade plan



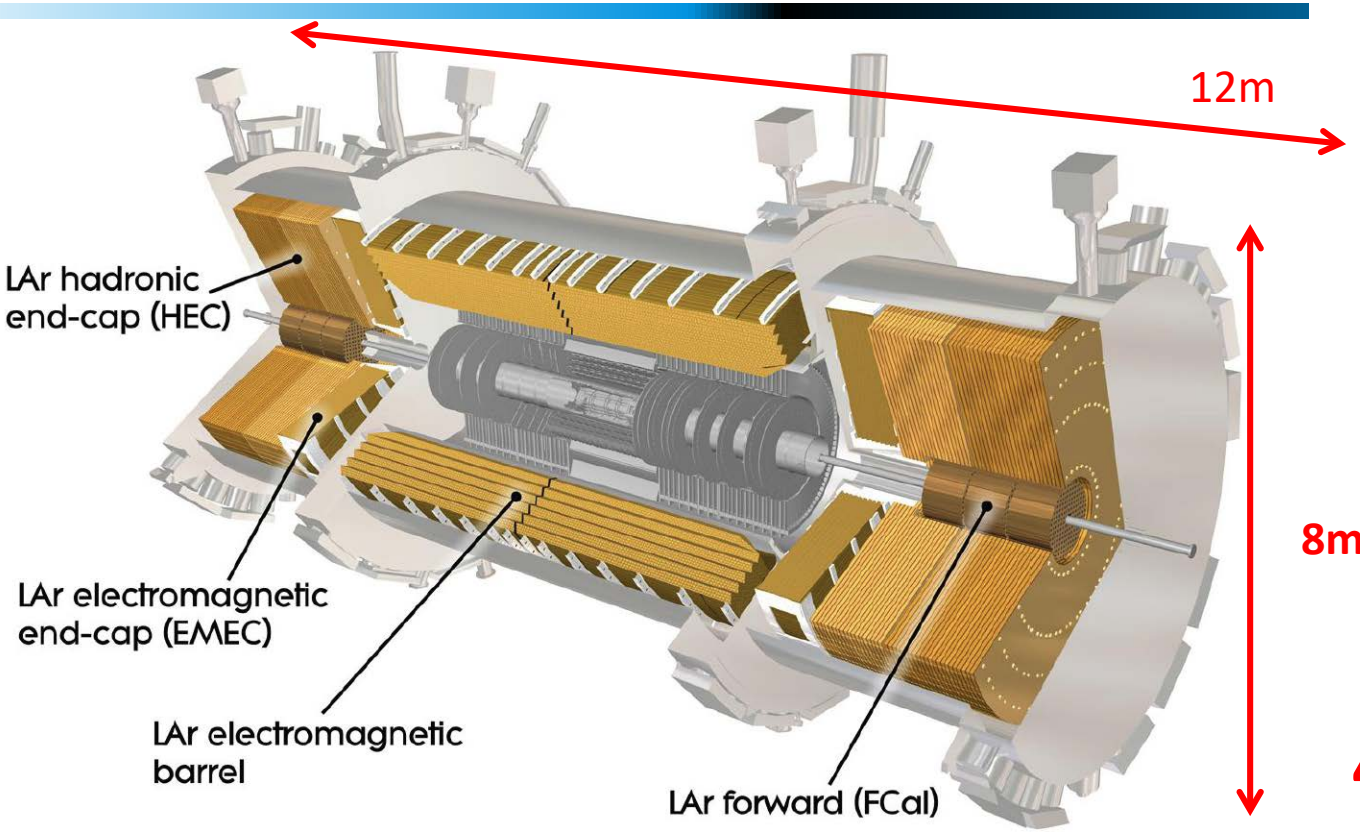
LS2: Phase-1 upgrade

- Trigger readout upgrade
- Level-1 trigger
  100 kHz == latency 3 μs
- data recording rate
  a few hundreds Hz.

LS3: Phase-2 upgrade

- Main readout upgrade
- Forward part detector upgrade
- Level-1 trigger
  1 MHz == latency 10-20 μs
- data recording rate

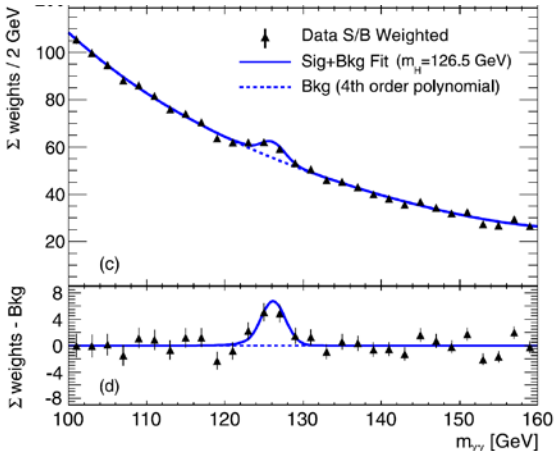
ATLAS Calorimeter: Now and Future



4000 tons

LAr-Pb EM calorimeter (|η|<3.2):

- e/γ trigger, identification; measurement
- **σ/E ~ 10%/√E ⊕ 0.7%**
- Granularity: 0.025x0.025 ; $22X_0$
- 3 long. layers + presampler(0 <|η|<1.8)
- $180x10^3$ channels

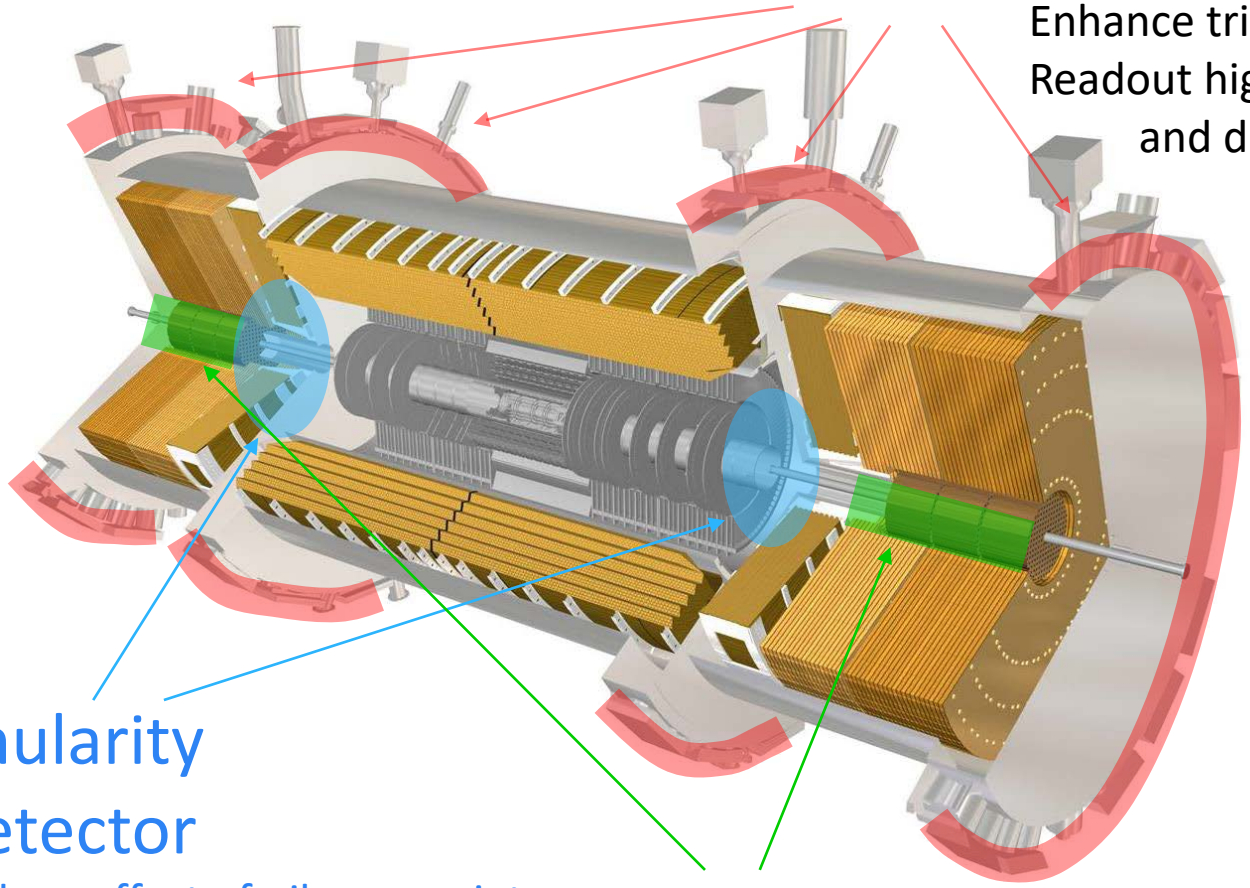


ATLAS Calorimeter: Now and Future

- LAr/Absorber itself is radiation tolerant

LAr Readout Electronics

Enhance trigger capability,
Readout higher frequency
and due to radiation.



High Granularity Timing Detector

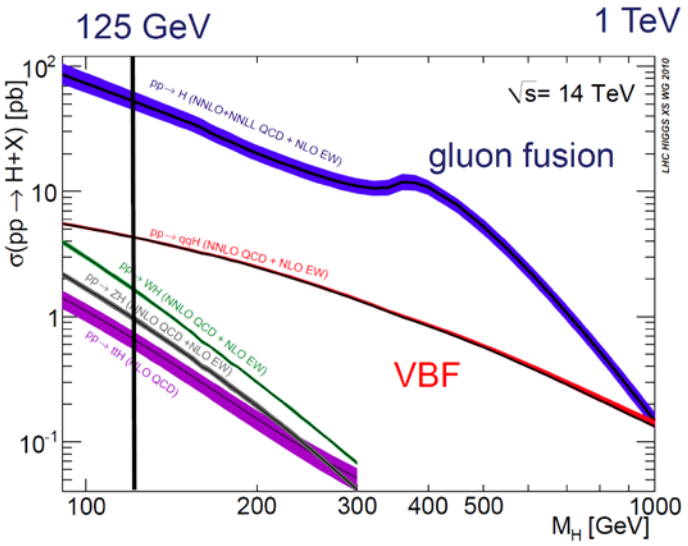
In order to reduce effect of pile-up on jets

LAr forward Calorimeter

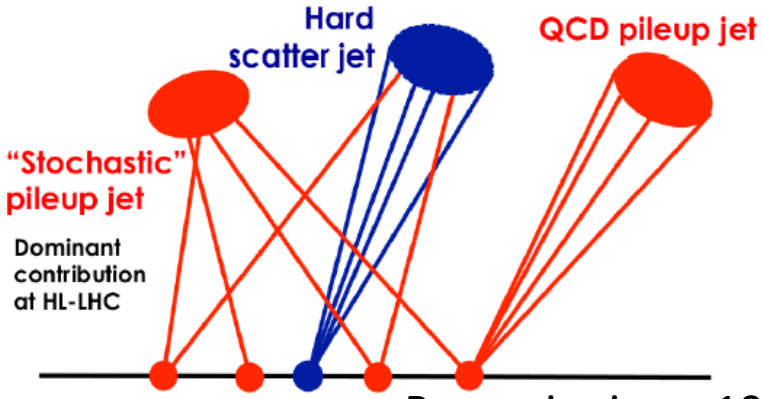
Potential risk of “boiling” Liquid Argon.
Decided no replacement. (To avoid Risks for permanent damage in cryostat)

Forward region is important!

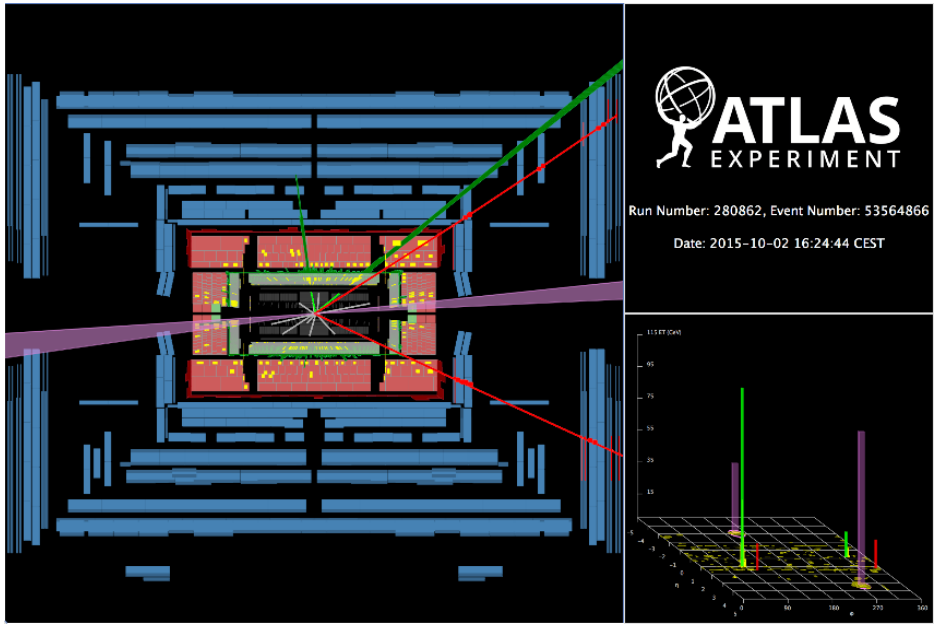
- Vector Boson fusion production
  - SM Higgs, BSM signatures
  - Vector Boson Scattering
    - One of major physics goal @ 3 ab^{-1}



Forward region: more contamination of PileUps.
Now: no tracker
Future: extension of coverage possible.
→ Resolved vertices in Z.



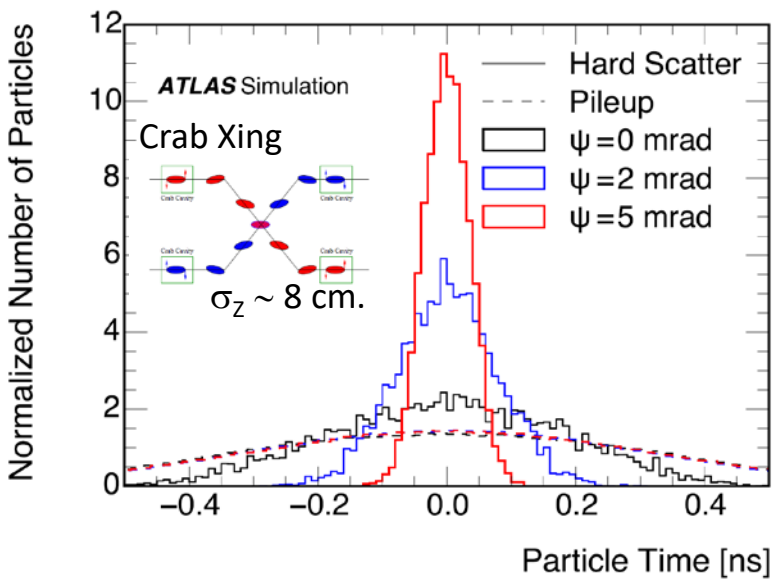
Beam size in z:~10 cm

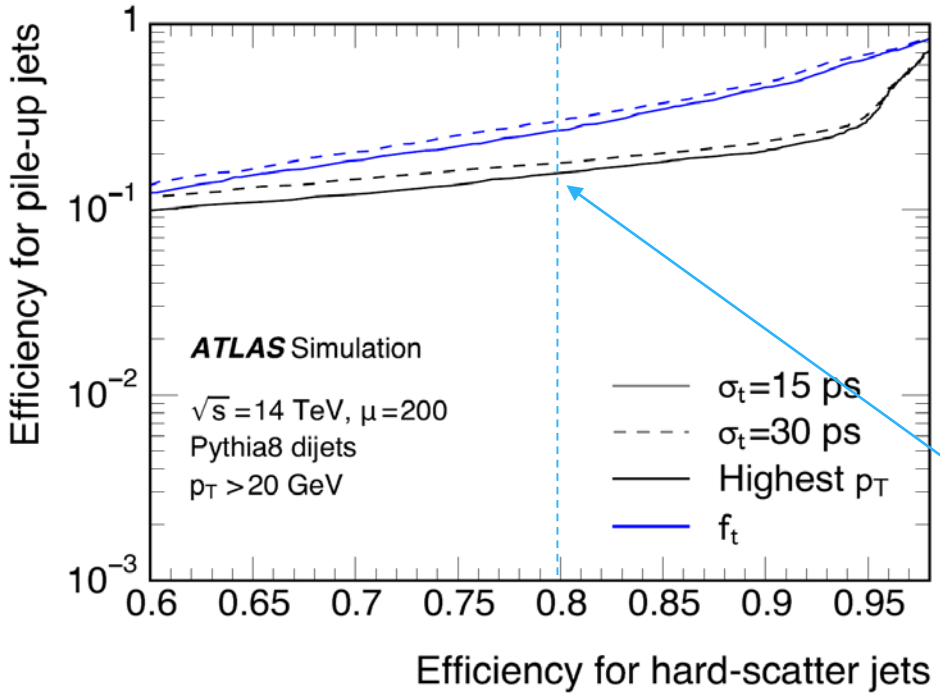


Can we add more information??
→ YES! Let's use timing information.

Timing information to resolve Z vertex

- Pileup jet is from other Z-vertex.
- Particle arrival time in calorimeter is as function of time (TOF).
- If we could have very good timing resolution, a jet can be assigned the vertex.

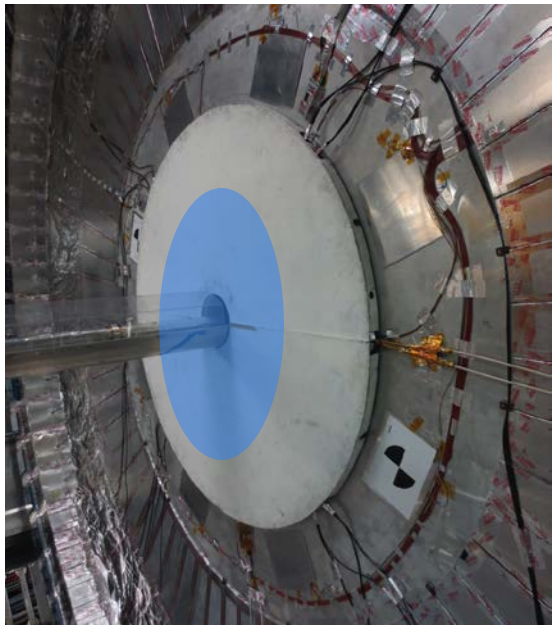




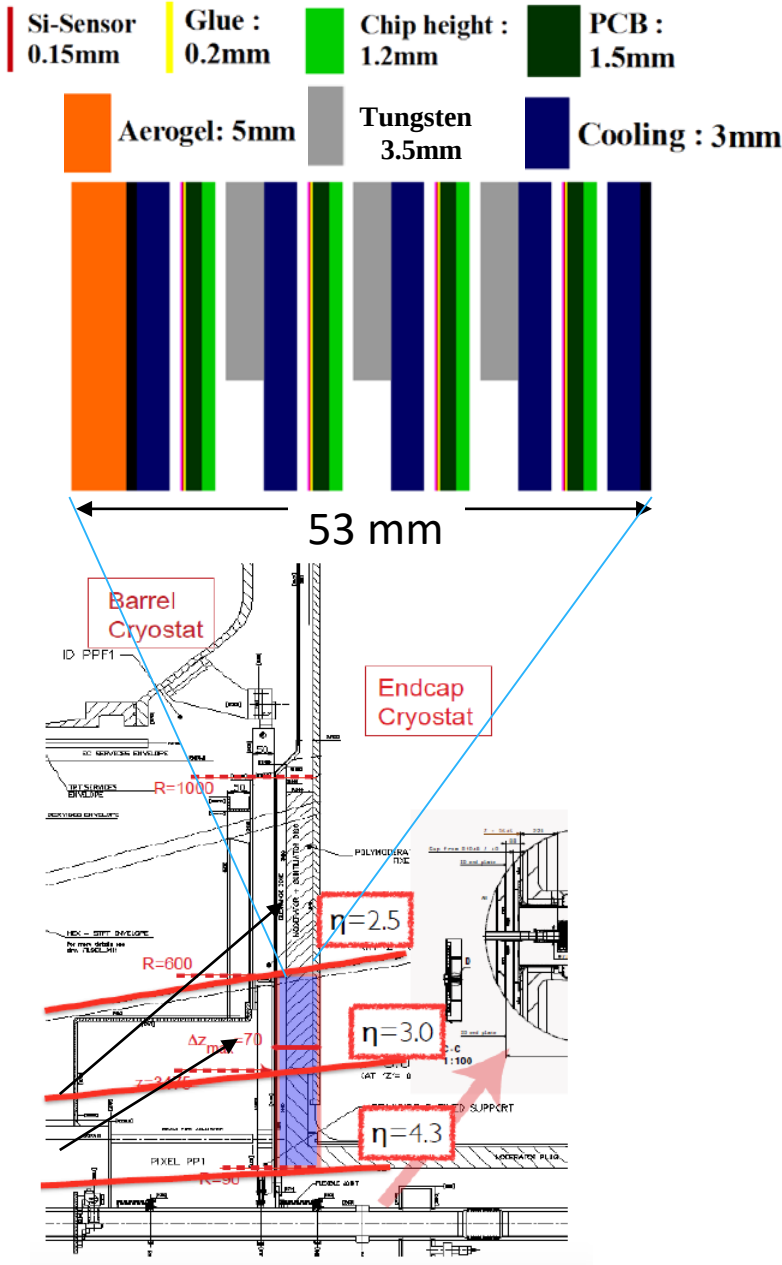
Simulation study for 7 x 10^34 $cm^{-2}s^{-1}$
- With 30 ps resolution per particle
- Preliminary algorithm
  Use Timing of the highest pT track
  Rejection of pileup jet: 85%
  Efficiency of HS jet: 80%

Detector design

- On front of End Cap region
  - Z=3500 mm
  - $2.4 < \eta < 4.2$
- Thin detector (5-6 mm)
  - 4 layers of silicon sensor.
- Option
  - With / without W absorber



Inner surface of the endcap cryostat



Detector design

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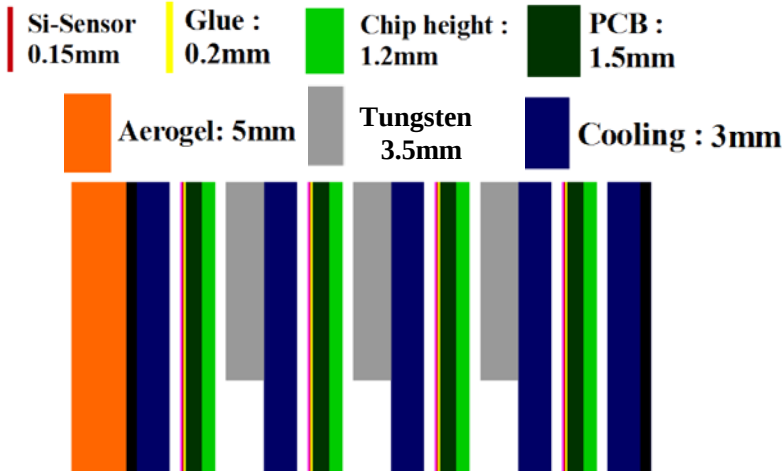

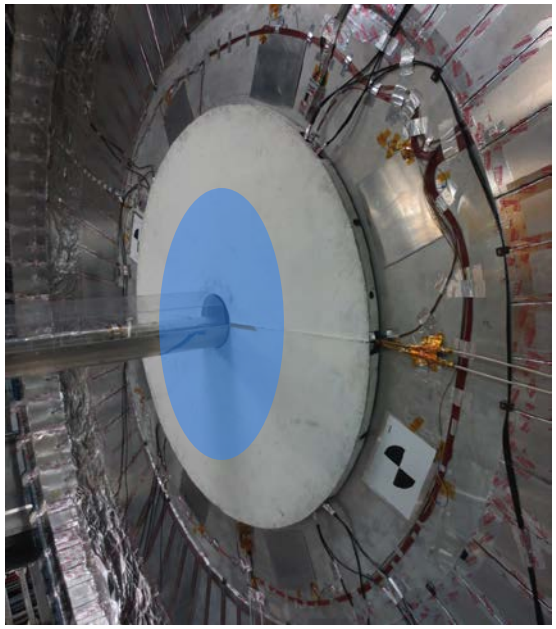

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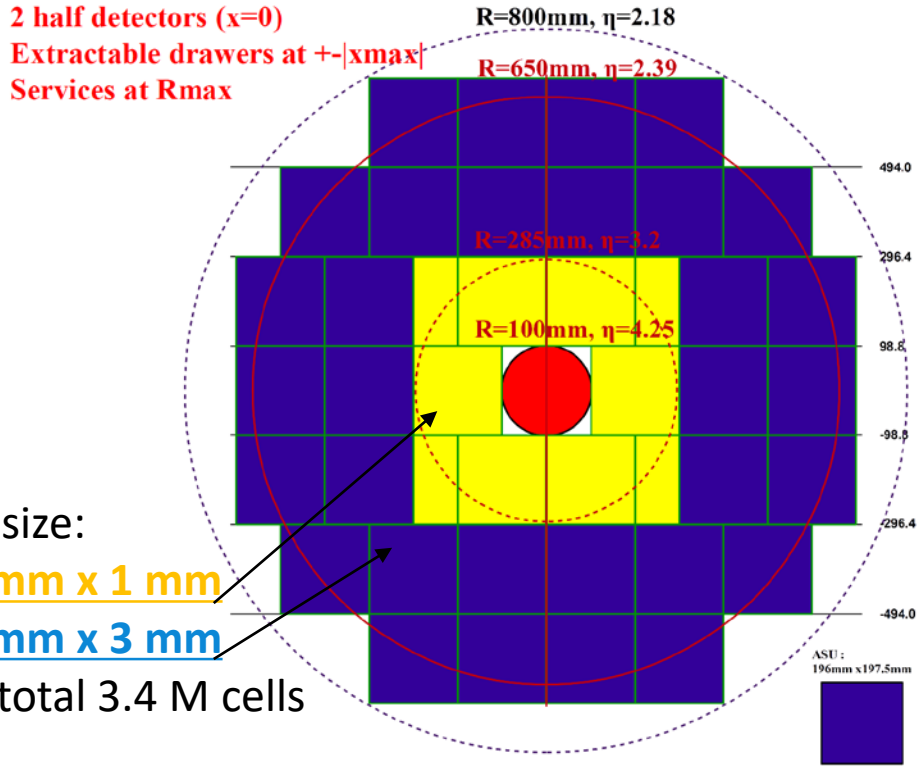


Cell size:

1 mm x 1 mm

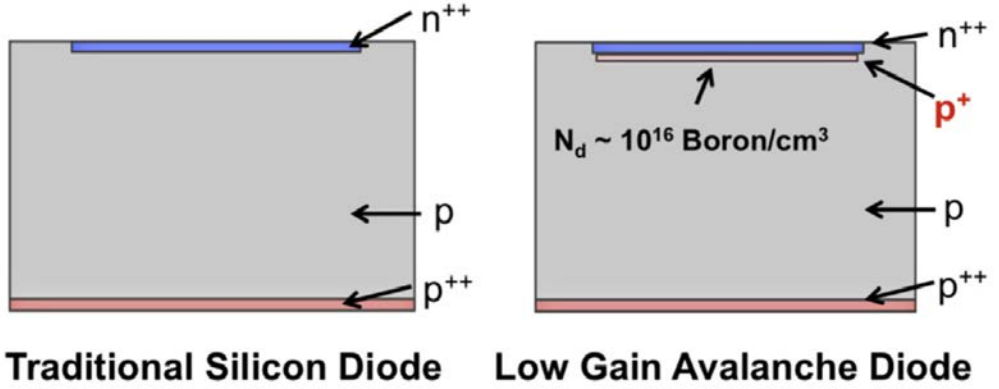
3 mm x 3 mm

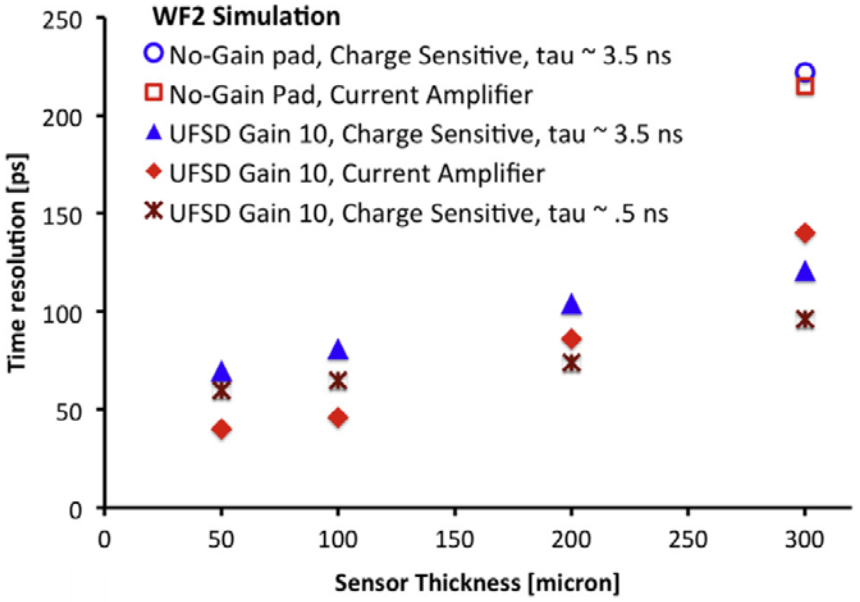
total 3.4 M cells

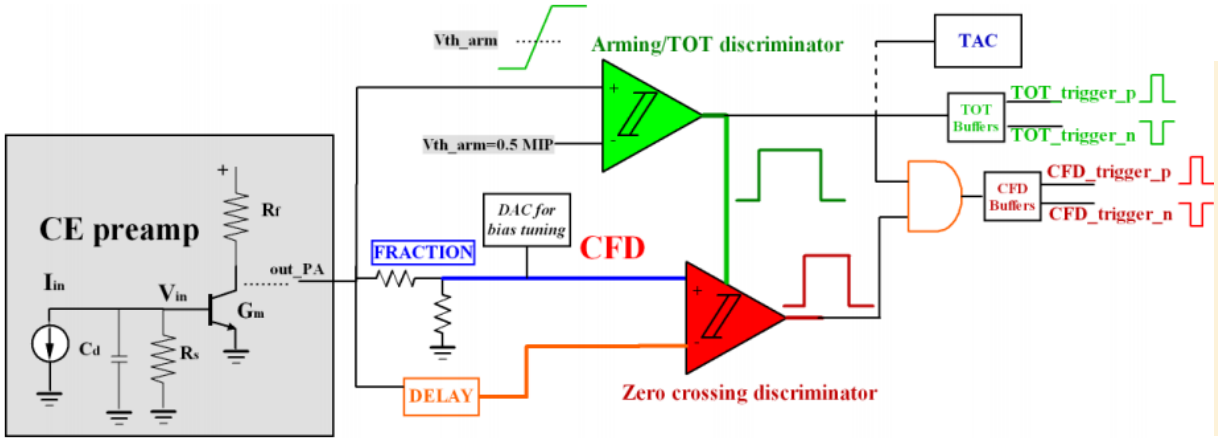
Sensor and readout

- Low Gain Avalanche Diode (LGAD)
- Developed by CNM under RD50 project.

NIM A 765(2014) 12, NIM A 796 (2015) 141







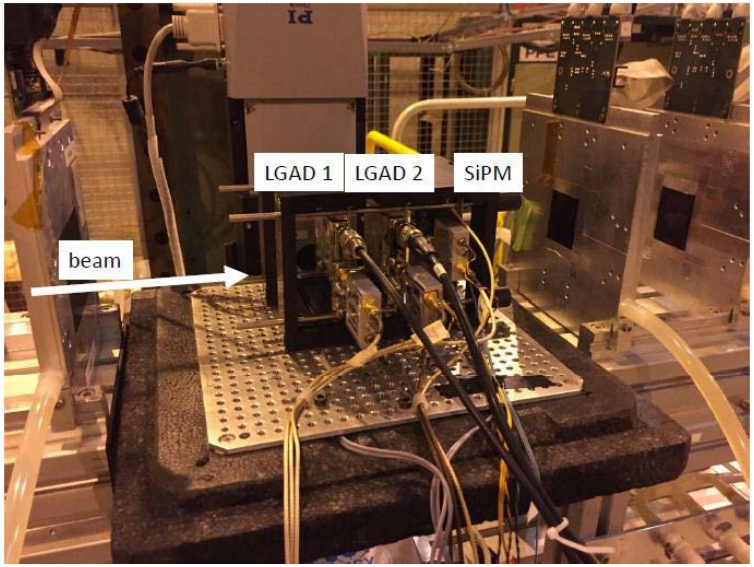
Timing measurement

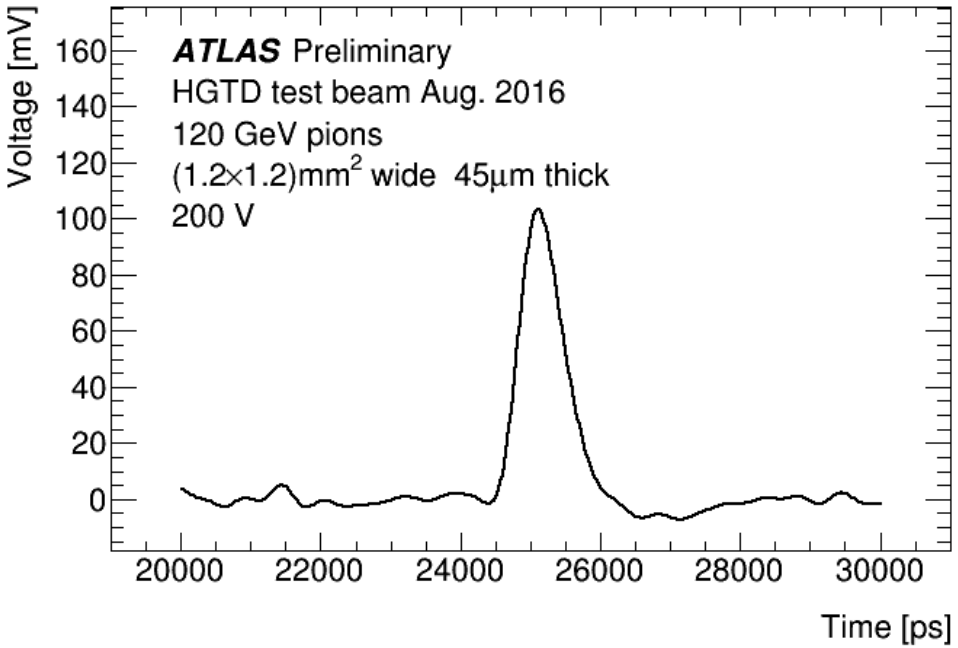
- Time over Threshold (TOT)
- Constant Fraction Discr. (CFD)

→ Time walk correction.

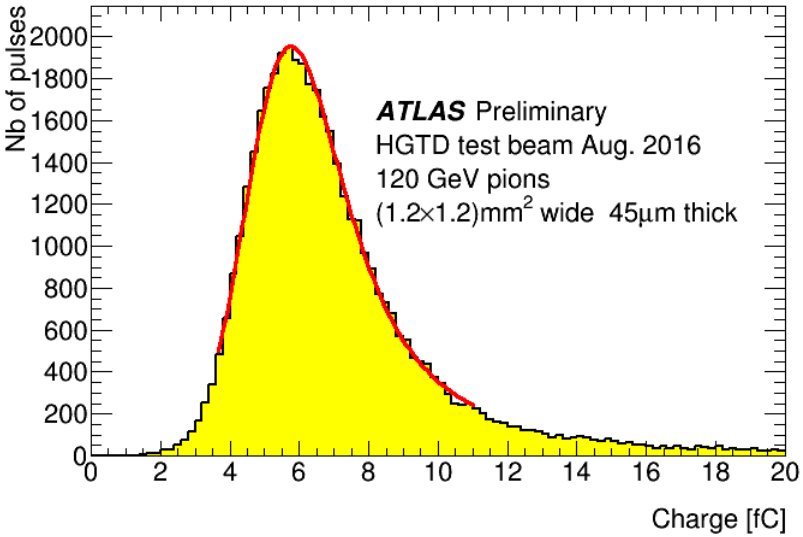
Readout system time resolution <10-20 ps

Beam test (CERN 120 GeV pion beam)

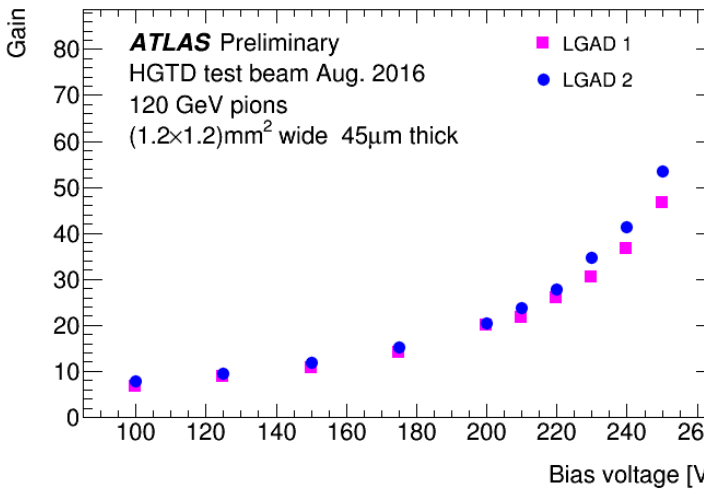


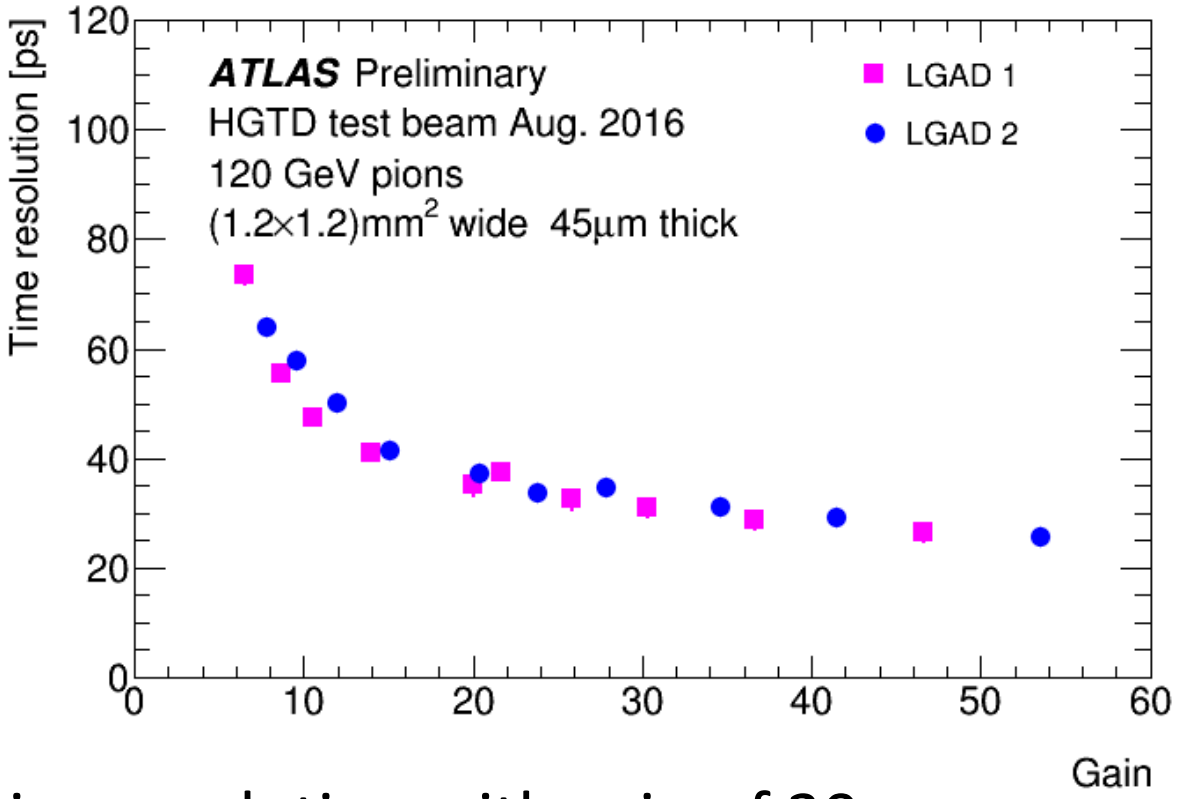


- First beam test.
  - 2016 August
- Nice signal pulse observed!



Beam test result

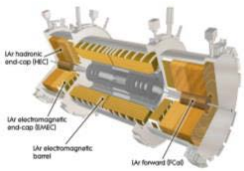


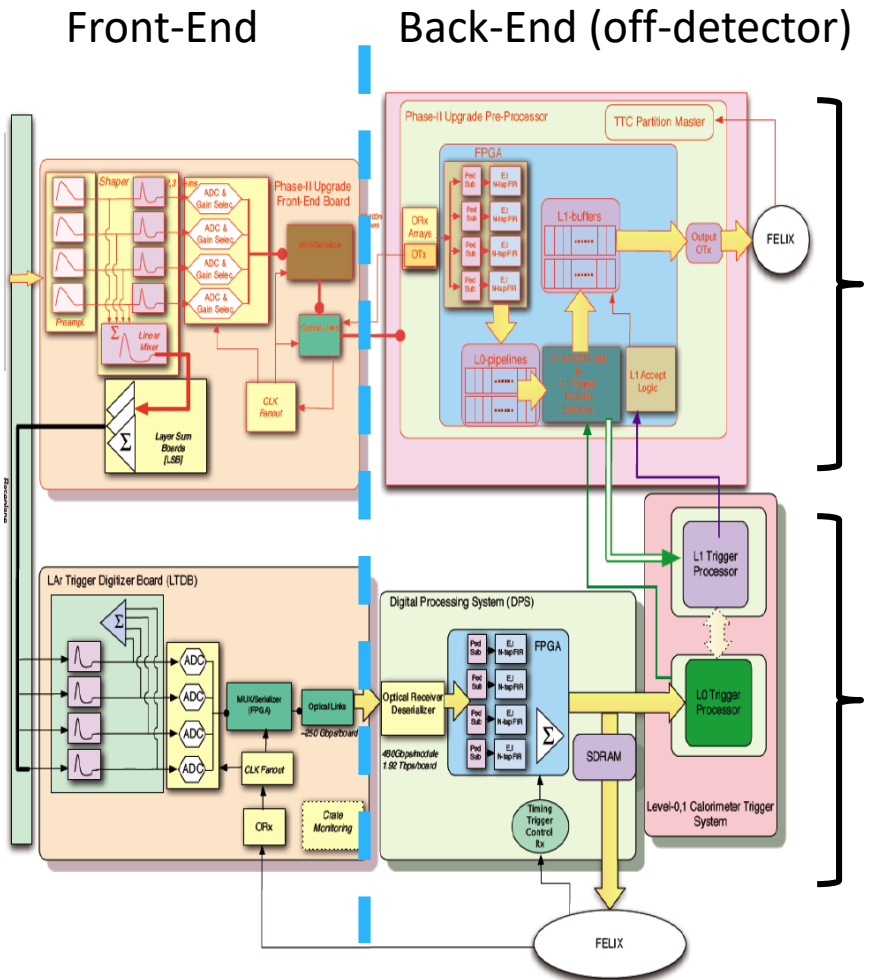


- Achieved 30 ps timing resolution with gain of 30.
  - Bias voltage of ~ 230 V.
- Result consistent for two modules.
- Very promising result at the first beam test.
- Technical Design Report will be released in 2017.

LAr Calorimeter readout system

- Phase-1(2019-2020) : Trigger readout upgrade
- Phase-2(2023-2025) : Main readout upgrade

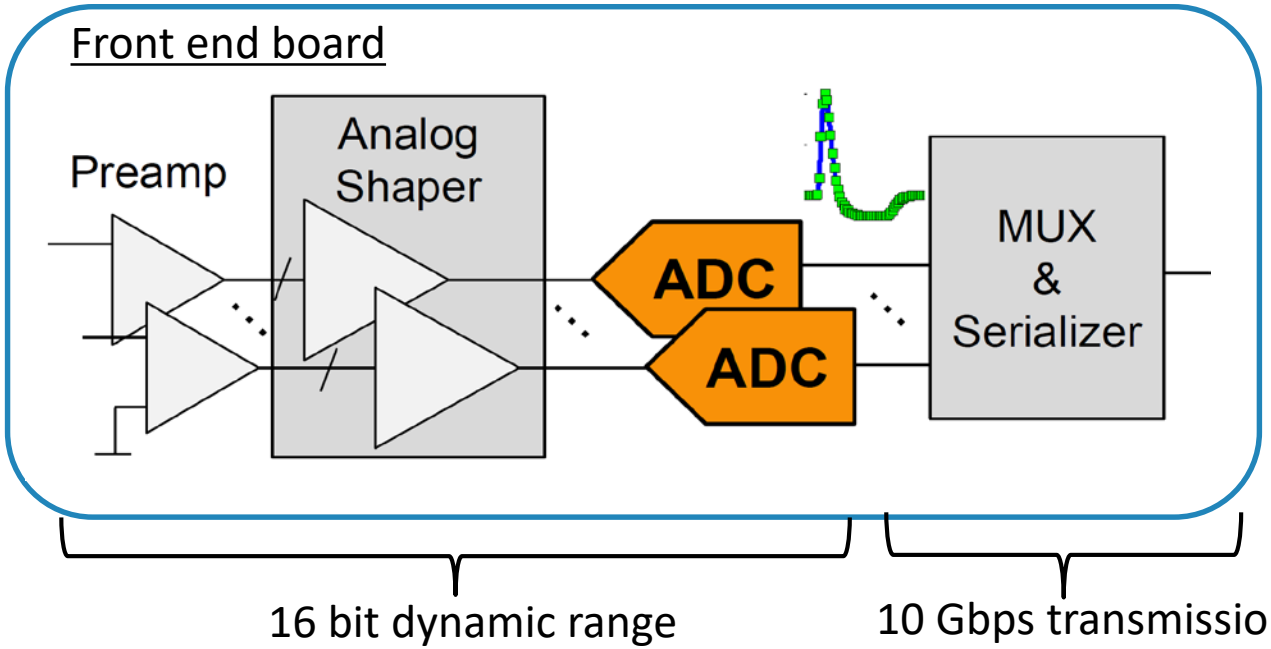




Main readout (Phase-2)
- Precise full readout with 40 MHz sampling (180 k channels)
- Input to high level trigger
- Radiation hardness

Trigger readout (Phase-1)
- Super-cell readout (34 k channels)
- x 10 better granularity to current system
- 40 MHz sampling

LAr Calorimeter Front end electronics

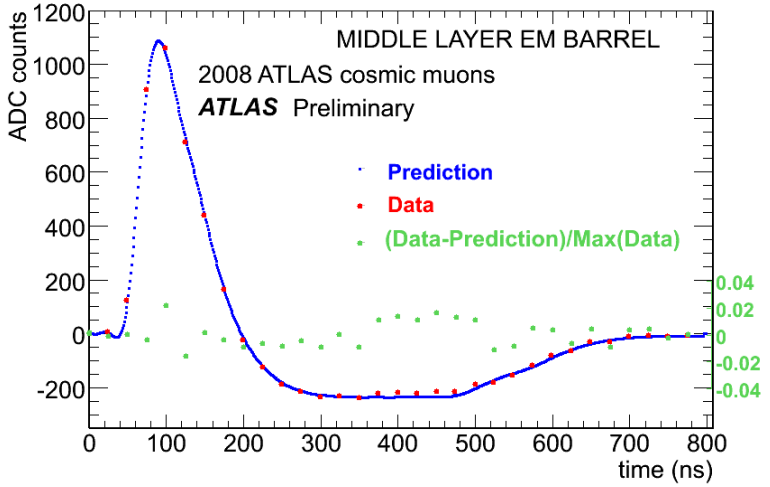


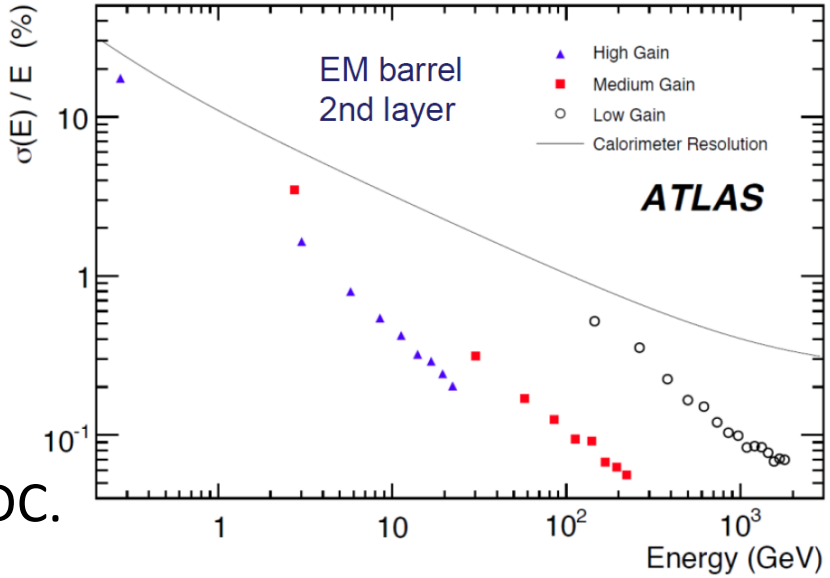
- Functionalities in Front-End
  - Shaper and preamp
  - Analog to digital conversion
  - Serialize and transmission.
- Realize with tough condition of
  - All bunch crossing of 40 MHz
  - Large dynamic range of 16-17 bits.
  - Radiation hardness and long term stability

Target:
All functionality on a chip
FE System **O**n **C**hip (FESOC)
→ reduced power consumption
no need to water cooling?

Overall design: shaper, gain and ADC

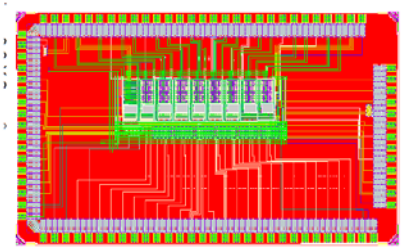
- Shaper
  - Now: bi-polar shaping(CR-RC^2)
    - Avoids baseline shift
  - Uni-polar is under consideration
    - No need to have negative part.
      → good for ADC dynamic range
- Gain and ADC
  - Now: 3 gain ranges.
  - Makes minor shift in transition.
    - Mass measurement on H→γγ
  - Plan
    - 2 gain ranges with 14 bit ADC.
    - Alternative is 1 gain with 16 bits ADC.



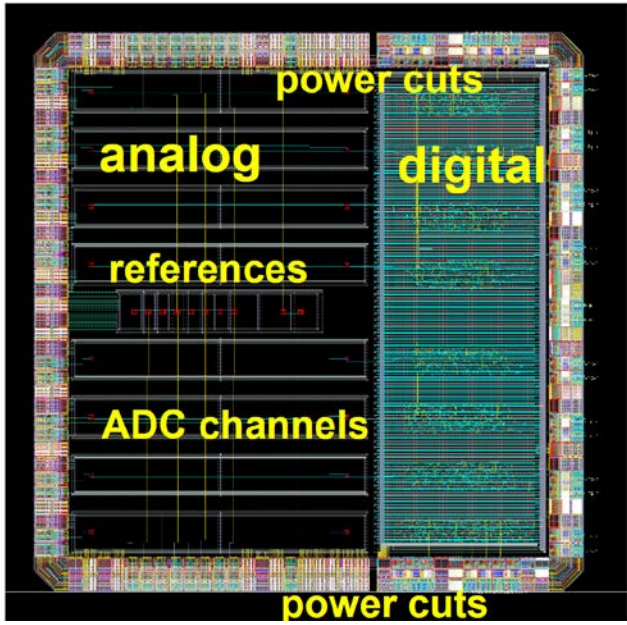


ASIC developments

- ADC for Phase-1
  - 130 nm CMOS, 65 nm CMOS.
  - Ready for mass production.
- ADC for Phase-2
  - 8ch 14-bit ADC with 65 nm
  - With Serializer with 320 MHz
    - Analog and digital.
      → two different ground in a chip
  - Yearly test chip submission will be started next year. Aiming for full prototype in 2020.
  - Also various commercial ADCs are under test for radiation hardness. (See backup slides.)



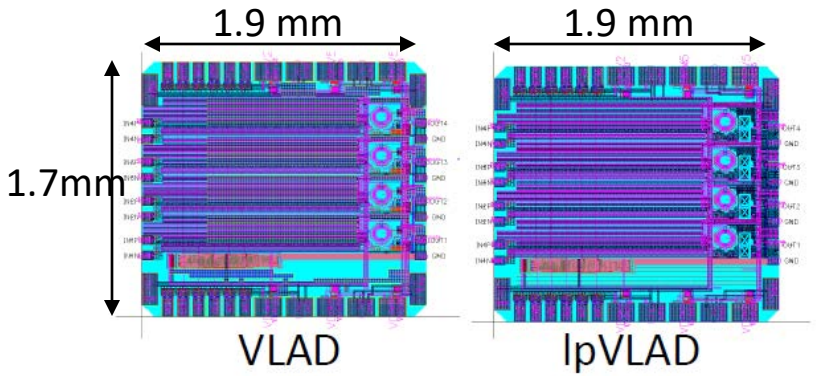
Chip size : 3.3 X 2 mm^2
Packaging in PGA144 cavity 10x10mm2
Pad opening : 72X58 μm2 pitch 100μm



Transmitter: optical link driver

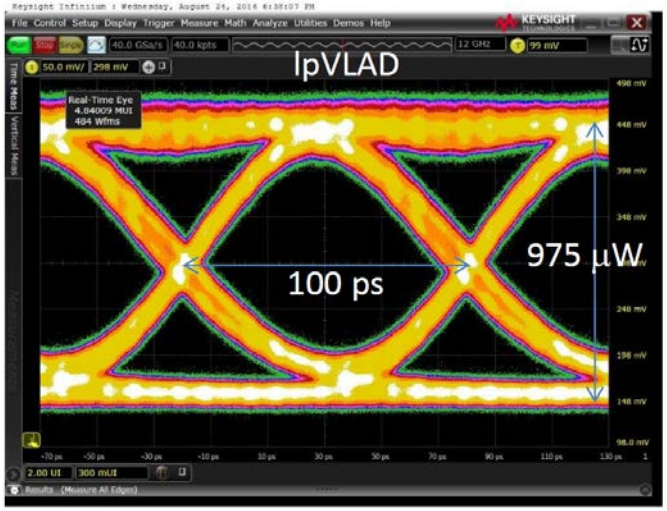
- Baseline: lpGBT in 65 nm CMOS.
- Development of laser array drivers and optical transmitter module within VL+ project
  - VCSEL Array Driver (VLAD and lpVLAD)
  - 4-channel 10 Gbps with 65 nm

low power



lpVLAD:
- 35 ps jitter
- 22 mW/channel

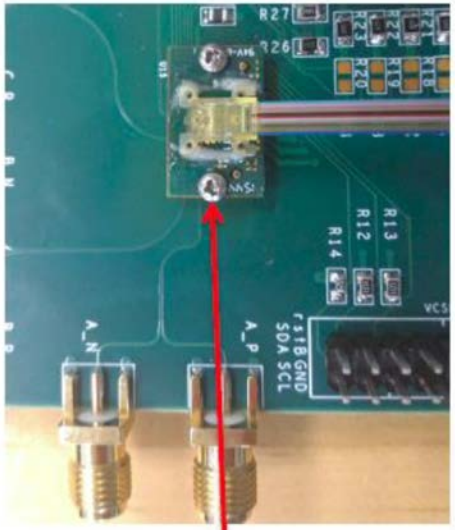
→ World record now!



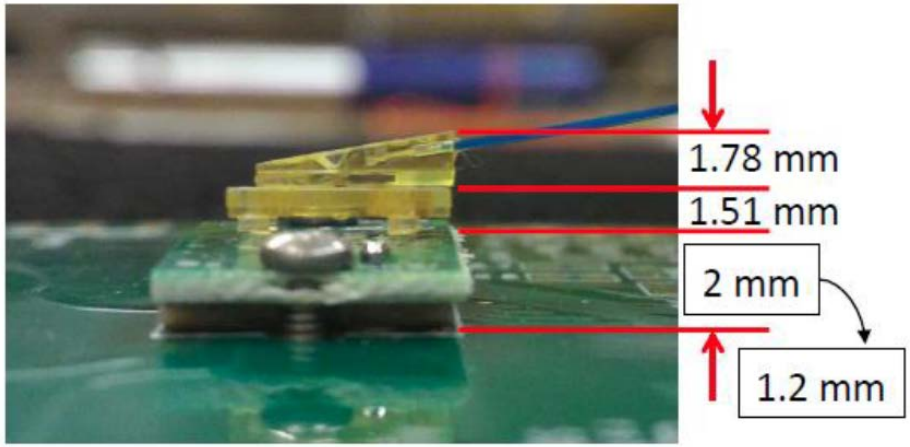
Measured eye diagram lpVLAD @ 10 Gbps w/ Agilent J-BERT N4903B, DSA91204A (Signal source, Oscilloscope)

Optical transmitter

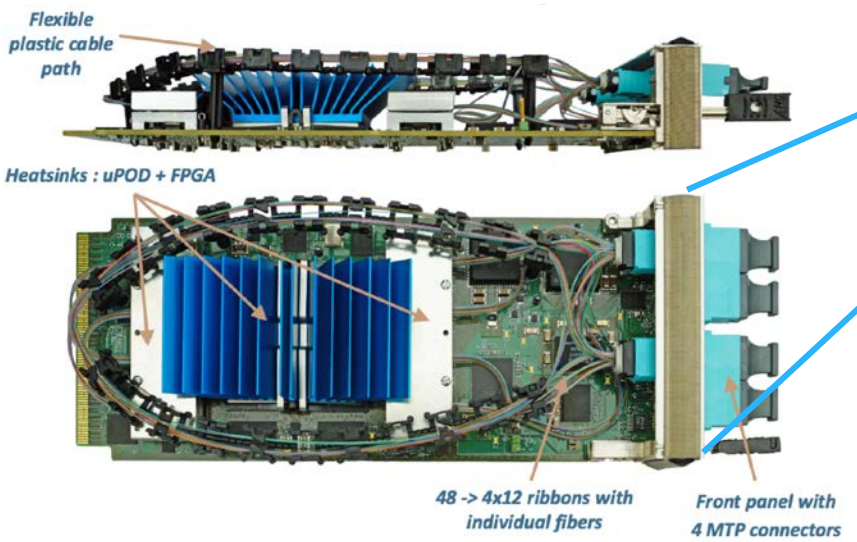
- 12-channel optical transmitter
- Very compact connecter from Samtec.
- Tested with IpVLAD/VLAD
- Commercial VCSEL+transmitter arrays are also investigated. Initial test works.



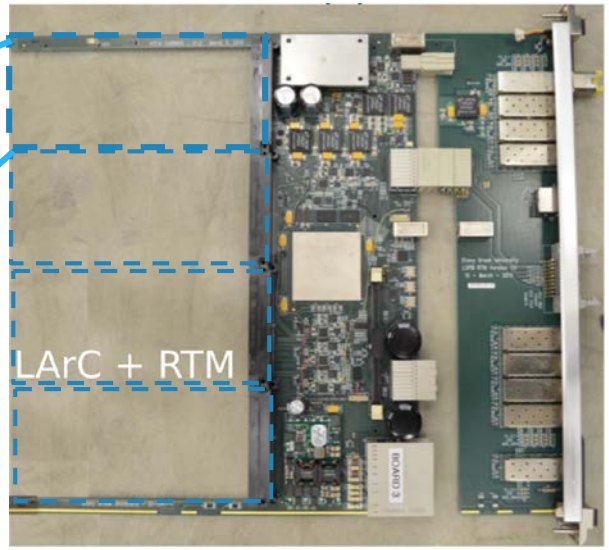
ATx foot print: 10 mm x 15 mm.
MOI with a Prizm connect to a 12-way fiber ribbon.



Backend electronics



Advanced Mezzanine Card（LATOME）for Phase-1 project.
→ total 124 LATOMEs



ATCA carrier blade and RTM
→ Total 32 blades.

- Backend electronics(each LATOME)
  1. Receive 48 data stream (fiber @ 5.12 Gbps)
  2. Remap channel
  3. ET and BC assignment (Filtering)
     - Accurate Energy at proper bunch crossing
  4. Energy Summing ($\Delta\eta \times \Delta\phi$ =0.1x0.1 and 0.2x0.2)
  5. Transmit 48 data stream (fiber @ 11.2 Gbps)

FPGA
Altera
Arria-10

About filtering algorithm

- Calculate the energy at fixed Latency
  - The energy is proportional to peak value of pulse.
    - The 3rd point is the peak
  - FIR calculation
    - a_i, b_i are the key points.

$$E_T = \sum_{i=1}^{4} a_i S_i$$

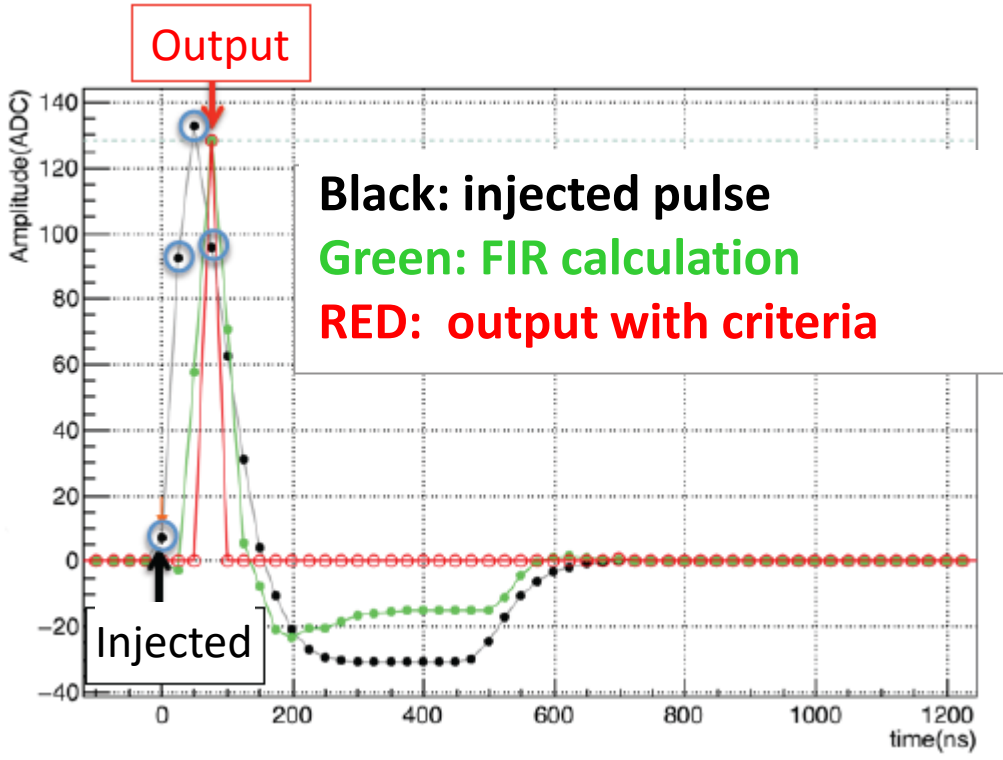
$$E_T\tau = \sum_{i=1}^{4} b_i S_i$$

Criteria

$E_T > 0$ & $|\tau| < 12.5$ ns

An energy with fulfilling the criteria is the energy at the right BC.

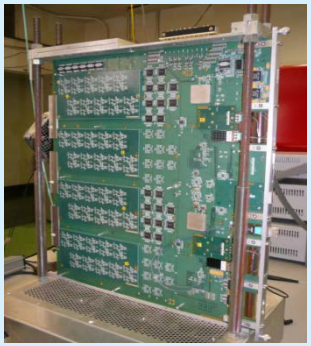
Options for alternative filter:
Wiener filter, Extended Optimal filter



In-Situ Demonstrator for Phase-1

Front End

Demonstrator LTDBs installed in UX15 crate I06

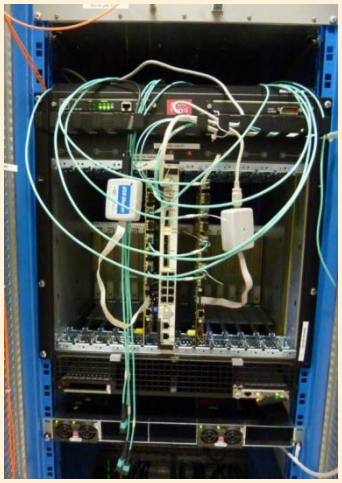


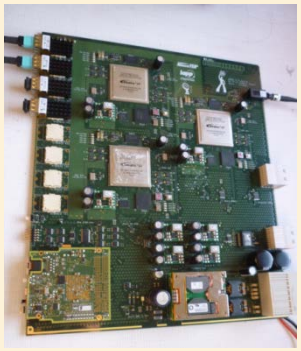
70m

x100

Back End

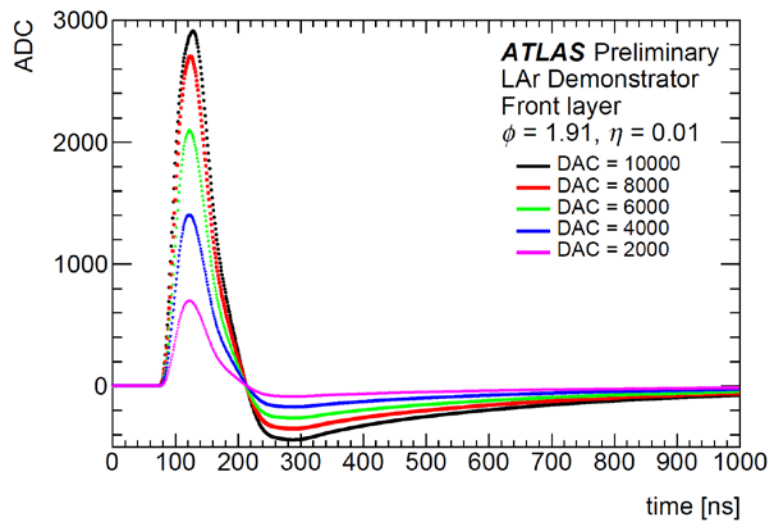
Demonstrator LDPS installed in USA15

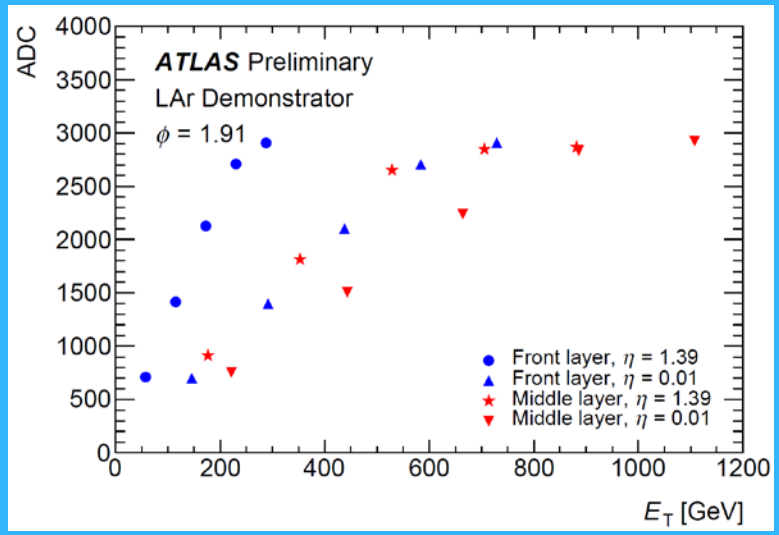




- Installed Summer 2014
  - $0<\eta<1.4$, $1.8<\phi<2.2$
- Readout being developed
  - L1Topo is used for readout.

In-Situ Demonstrator





Data taking with collision data.

Collected data have been using to have detailed understanding of pileup effect.

Make feedback to the filtering algorithm developments.

- Installed Summer 2014
  - $0<\eta<1.4$, $1.8<\phi<2.2$
- Readout being developed
  - L1Topo is used for readout.

Summary

- Long term main program at CERN: HL-LHC
  - High luminosity makes high pileups condition.
  - Enhance performance on trigger and pileup rejection.
- ATLAS calorimeter upgrade projects
  - Phase-1 (LS2:2019-2020): Trigger electronics
  - Phase-2 (LS3:2023-2025): Main readout electronics
    - Various ASICs developments are on-going.

      Target: all in one: **FE S**ystem On Chip (FESOC)

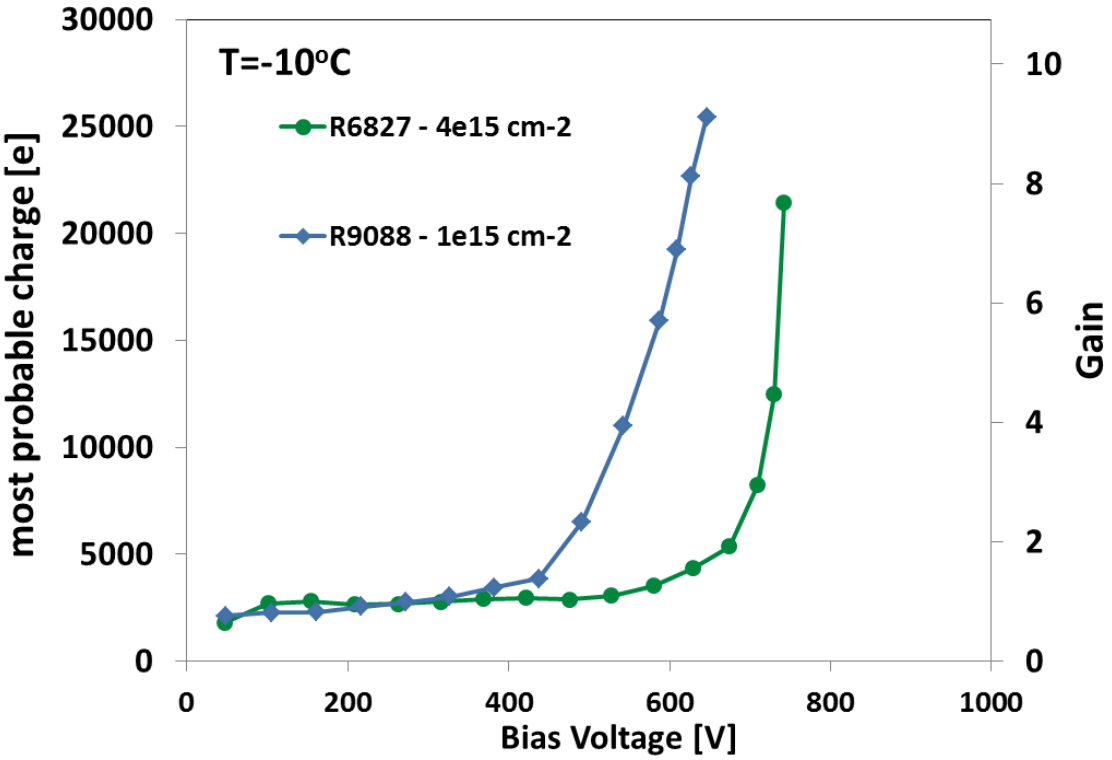
      → Low power consumption and radiation hardness
  - Forward region for Phase-2 upgrade
    - Concluded no upgrade on the LAr calorimeter.
    - High Granularity Timing Detector

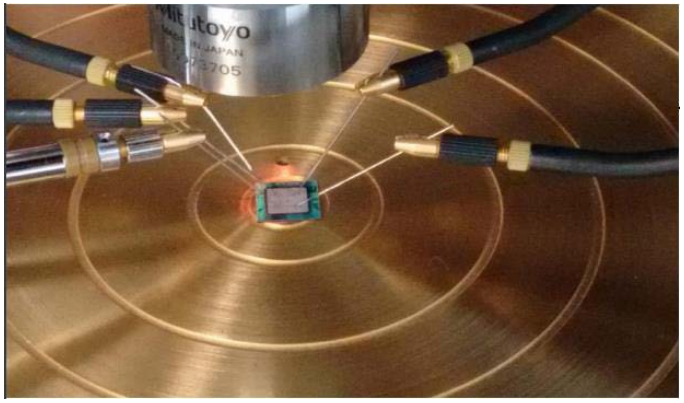
      → First beam test shows promising results.

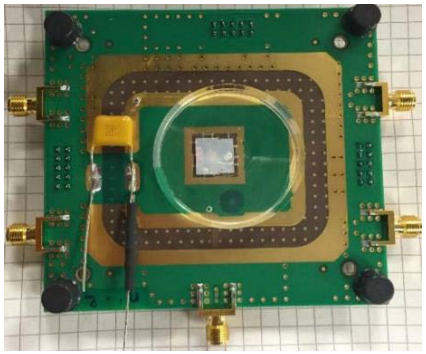
      TDR will be released in 2017.

Backups

Radiation tolerance on LGAD





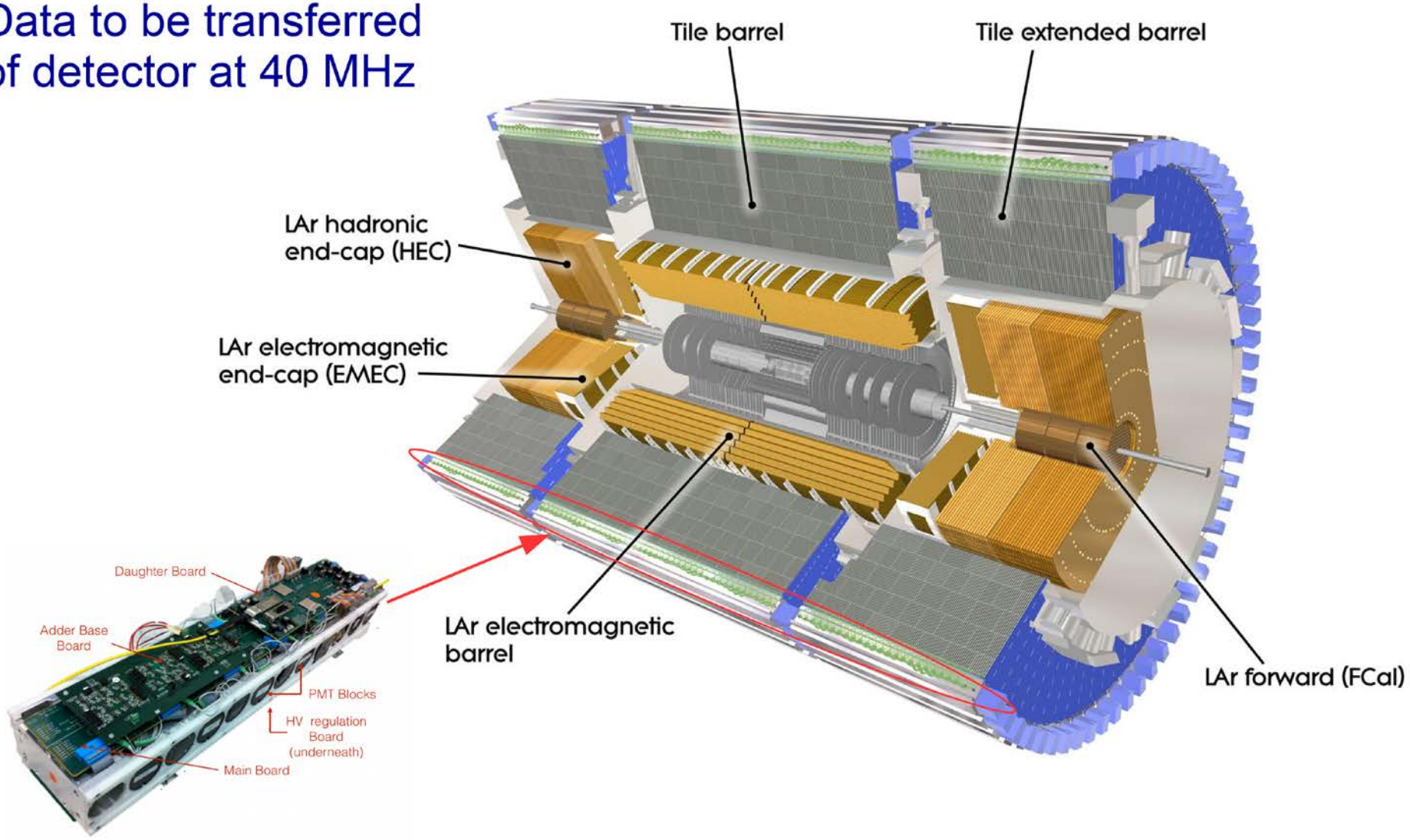


- Neutron irradiation upto $4x10^{15}$ cm^{-2}.
- Responses measured with SR90 electron
- Bias voltage increase is necessary to compensate the radiation damage.

ATLAS Tile calorimeter upgrade

No upgrade to detector or optics required for HL-LHC
All FE and BE electronics including power supplies to be replaced

Data to be transferred of detector at 40 MHz



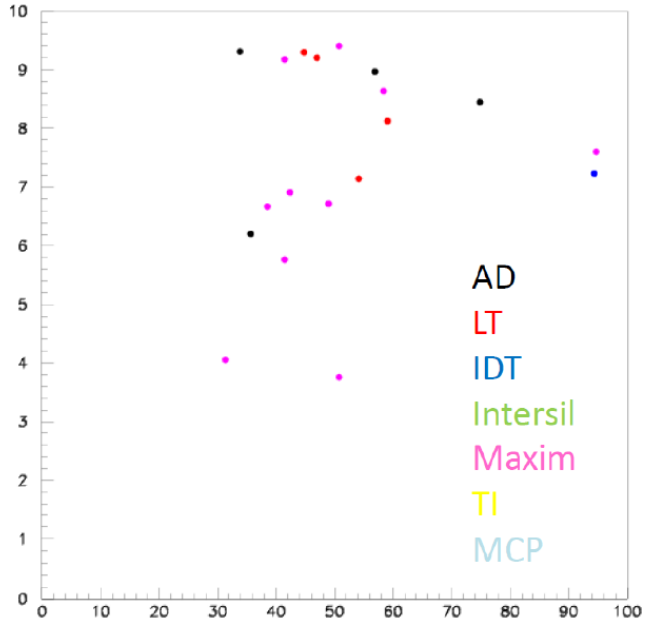
Evaluation on commercial ADC chips

- Evaluation of commercial ADCs - selection of promising chips according to power and costs
  - 20 candidates for 14-bit ADC
  - 7 candidates for 16-bit ADC
- Different vendors, different sampling rates
- Irradiation tests are planned to be done in the coming months

For Phase-2 R&D

14 bits (zoom on interesting region)

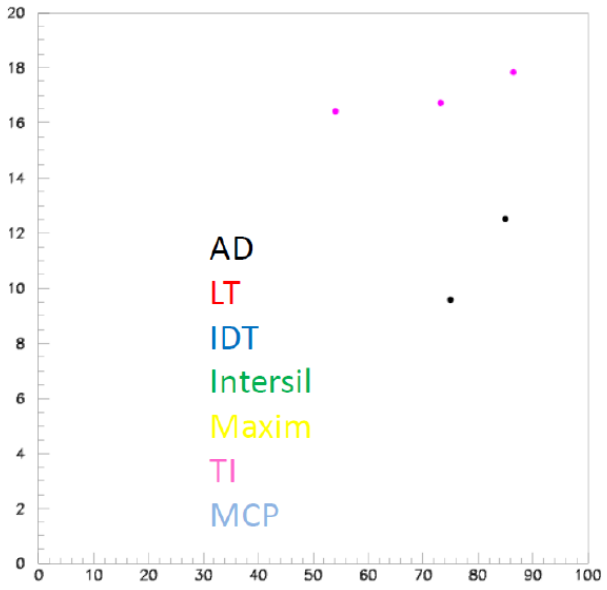
Cost per channel (US$)



Power per channel (mW)

16 bits (zoom on interesting region)

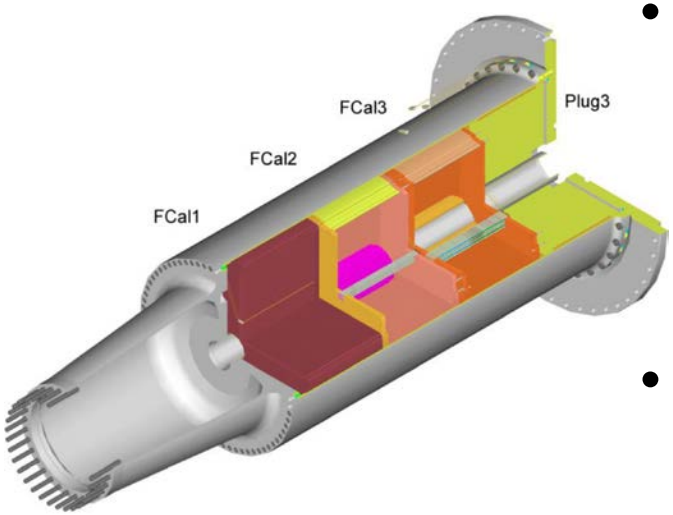
Cost per channel (US$)



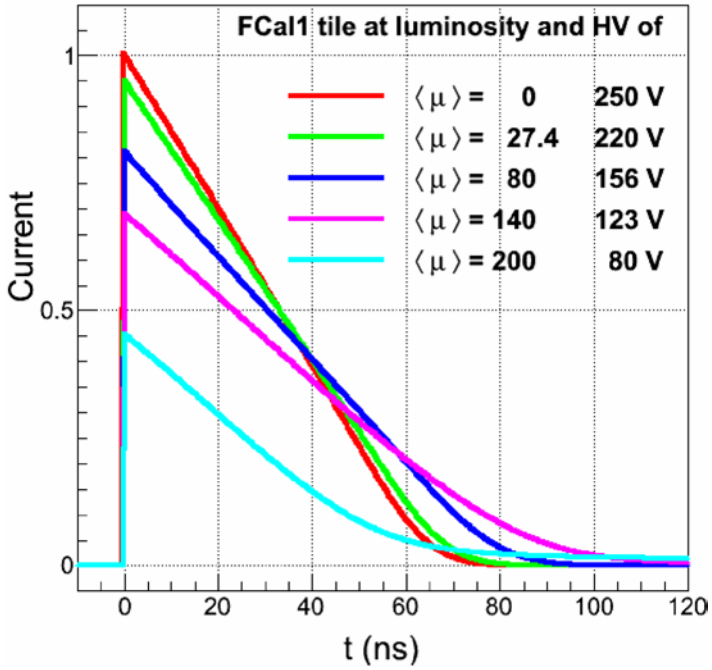
Power per channel (mW)

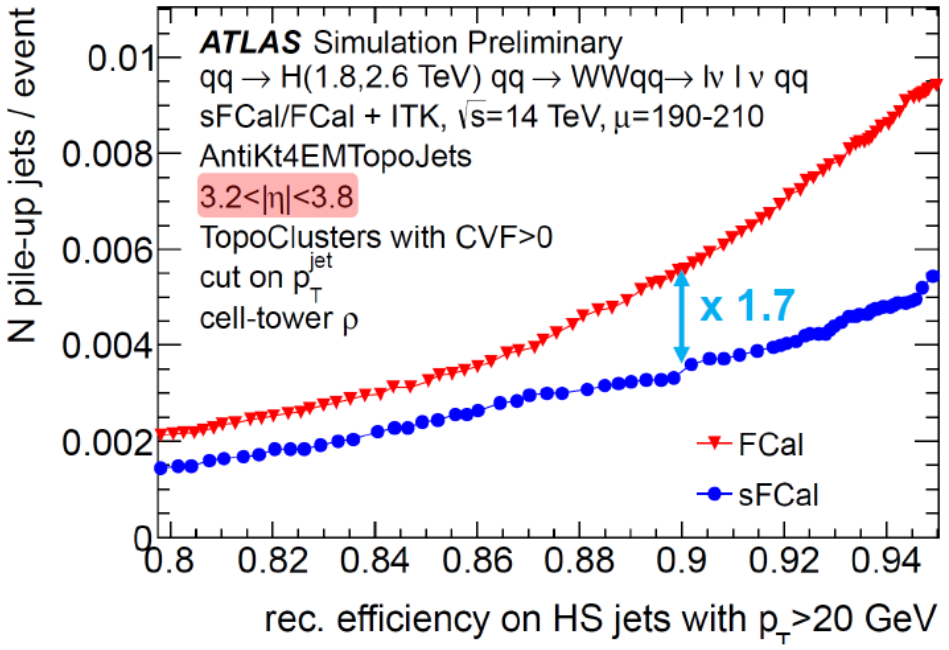
Forward Calorimeter

For Phase-2 R&D



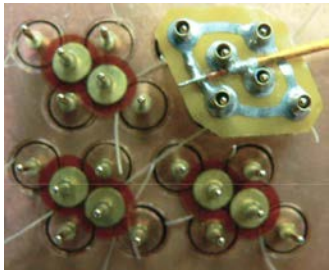
- Many studies have been done.
  - Liquid Argon boiling (28 TeV energy deposited in FCal) → 110 W heat
    → turned out we can manage.
  - Space charge effect.
    - Turned out we can operate
- In order to avoid risk of permanent damage.
  - Physics gain is not enough to pay risk..
  - Decided no change in forward section of detector.





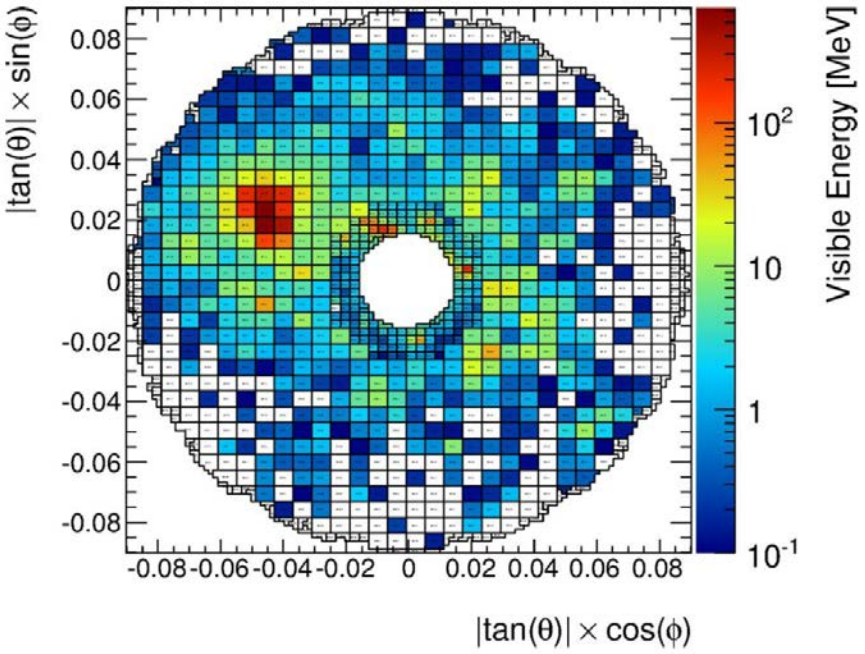
High granularity Forward detector

- Current system

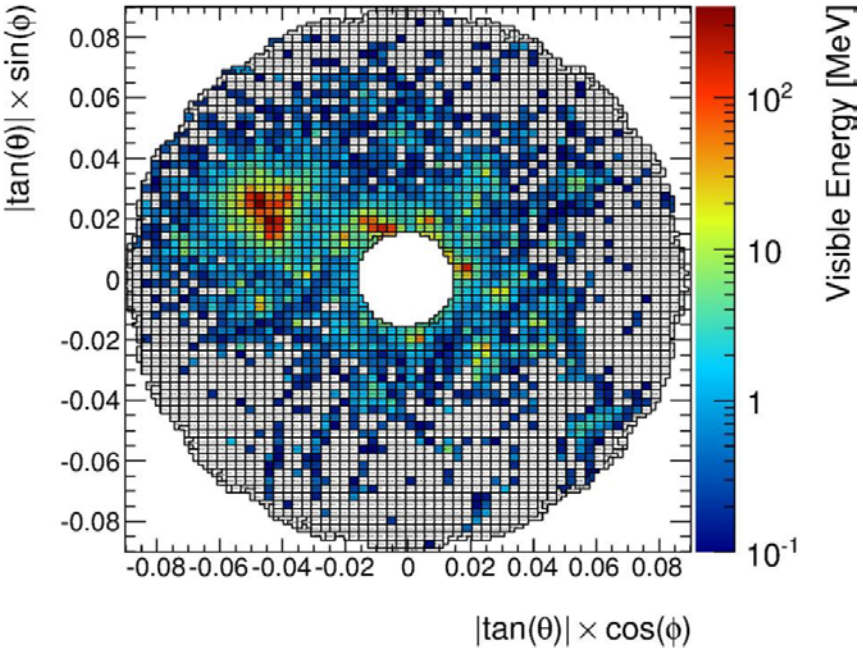


Proposed system

Single jet with current system

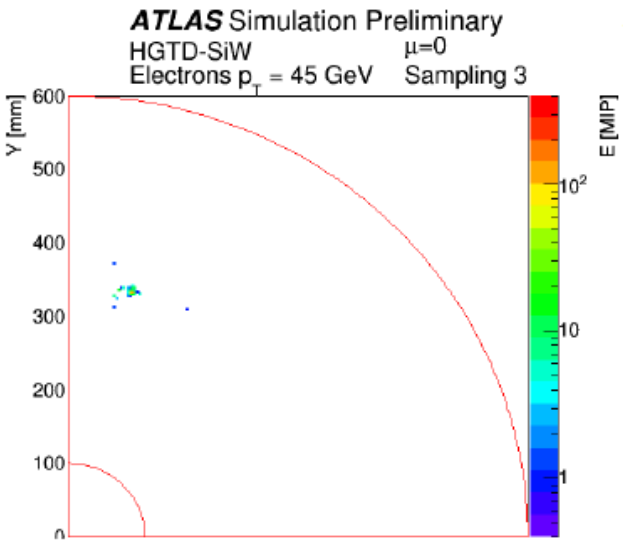


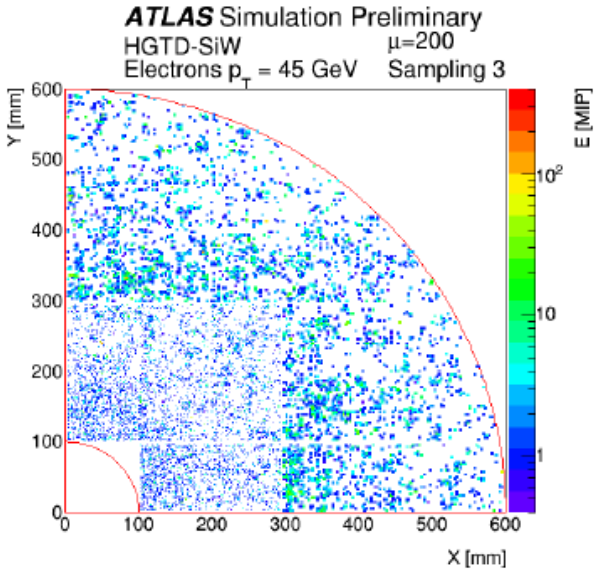
Single jet with proposed system

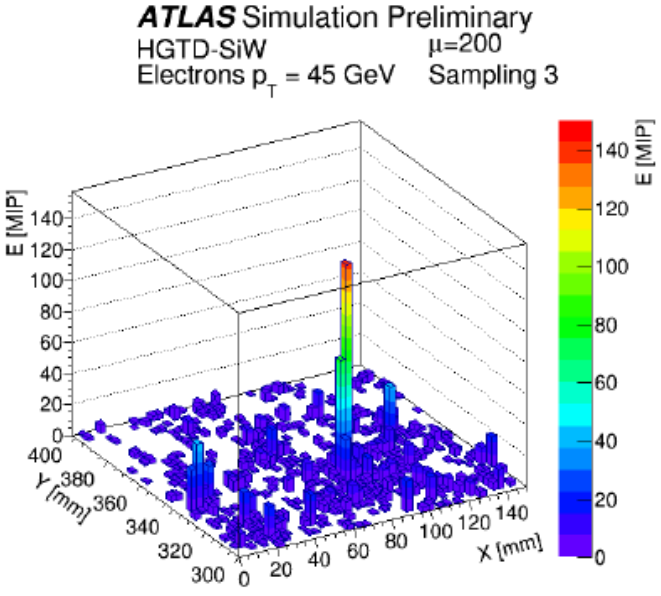


How does electron look like w/ HGTD

Electrons





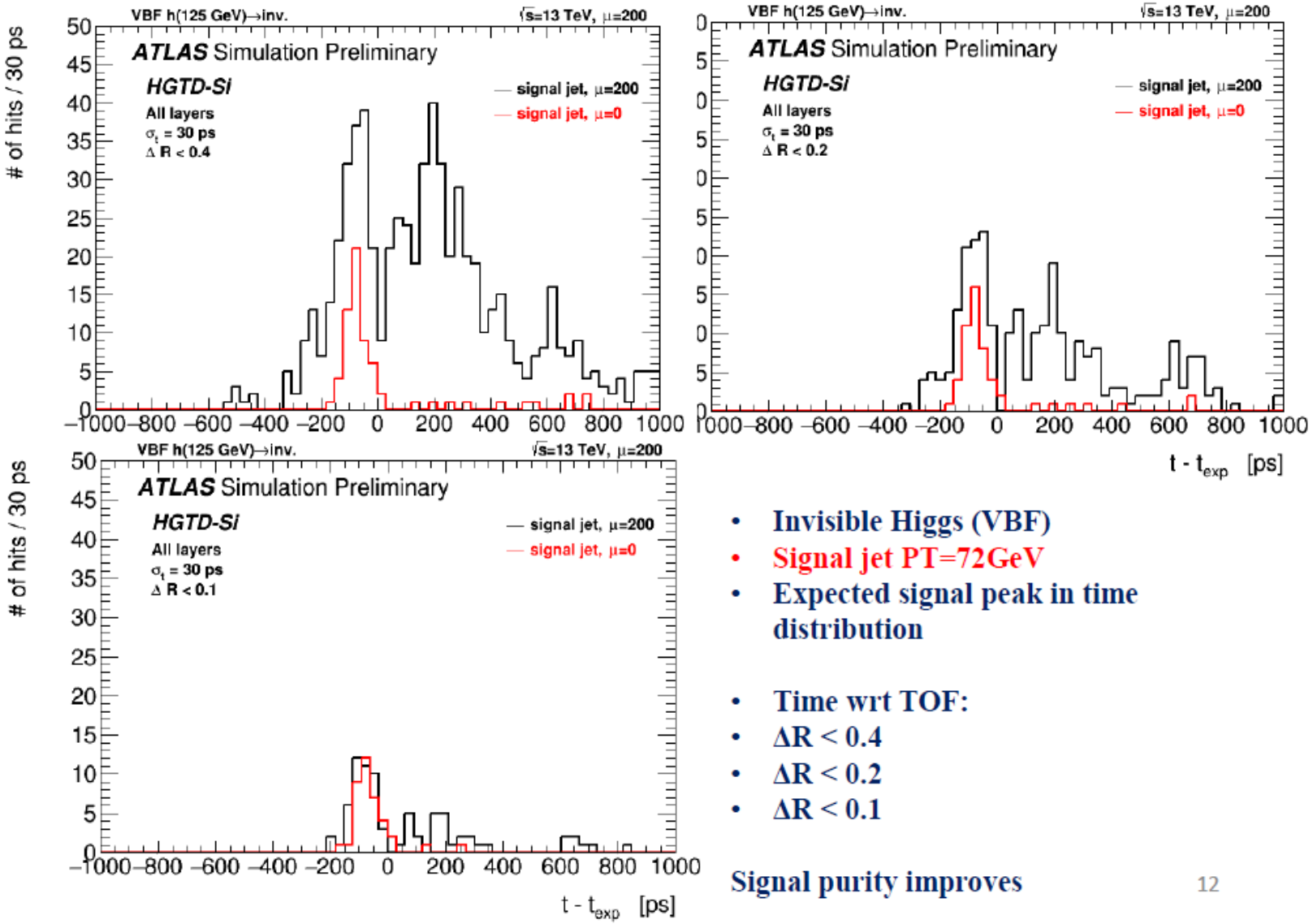


- **Electrons: PT=45GeV (Z boson)**
- **dynamic range:**
  - **HGTD-Si : 22xMIP**
  - **HGTD-SiW: 563xMIP**
- **shower development**
- **With pileup: challenging**

How does jet look like w/ HGTD

For Phase-2 R&D

Jets



- Invisible Higgs (VBF)
- Signal jet PT=72GeV
- Expected signal peak in time distribution

- Time wrt TOF:
- ΔR < 0.4
- ΔR < 0.2
- ΔR < 0.1

Signal purity improves

Phase-1 upgrade: Trigger readout

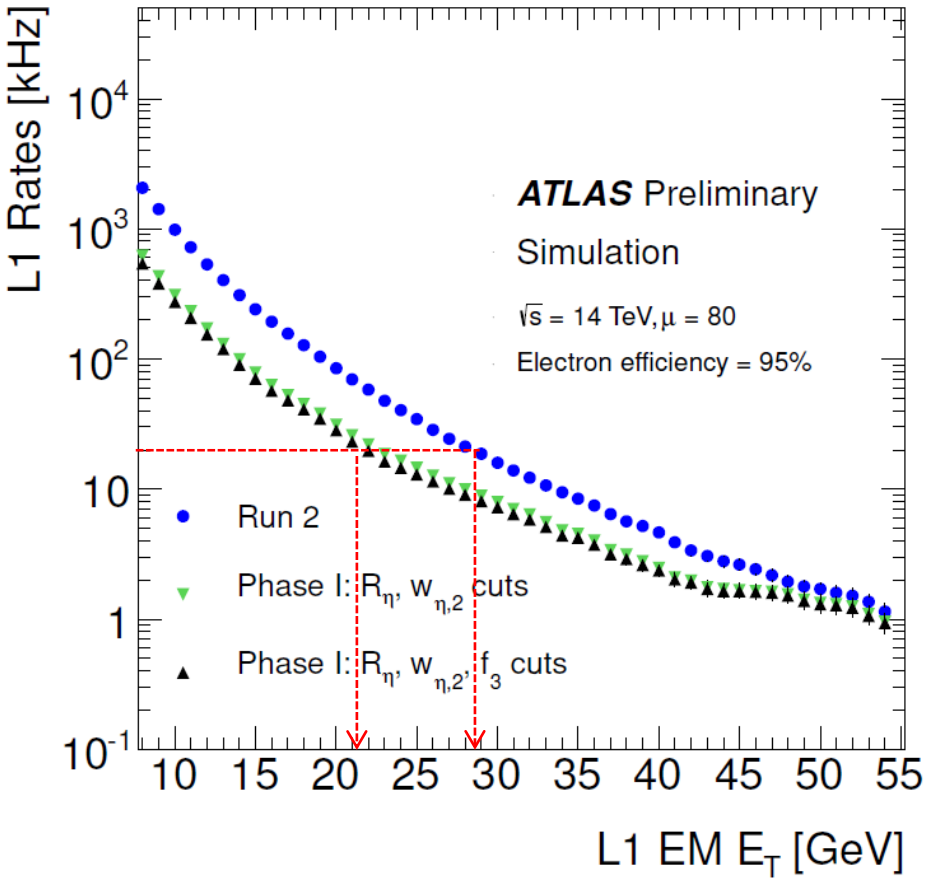
For Phase-1 R&D

- LHC Run-3 and beyond
  - High energy upto 14 TeV
  - High Luminosity up to 3 x 10^{34} with 25 ns bunch spacing (Phase-I).

  → Trigger system needs to be upgraded to preserve the acceptance to events with low pt objects (electron, photons and taus).

- ATLAS **L**iquid **Ar**gon Calorimeter provides the **inputs** to the calorimeter trigger (**L1Calo**)

  → Upgrade Electronics in long shutdown (LS2, 2018-2019).

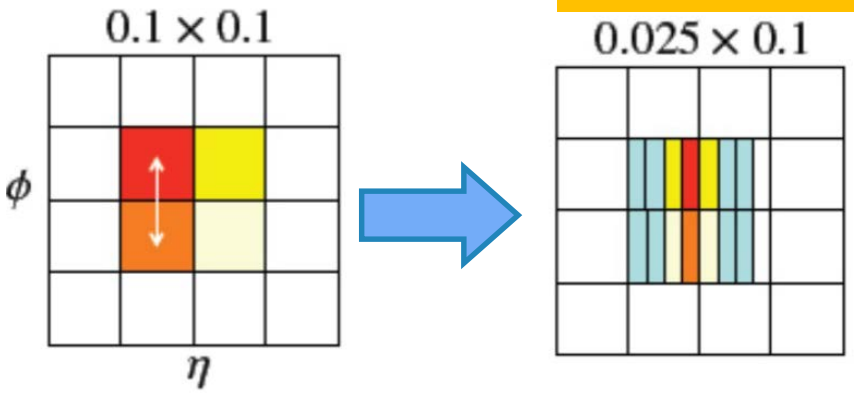


Single EM object can use up to 20kHz bandwidth in L1.

How to reduce the trigger rate?

For Phase-1 R&D

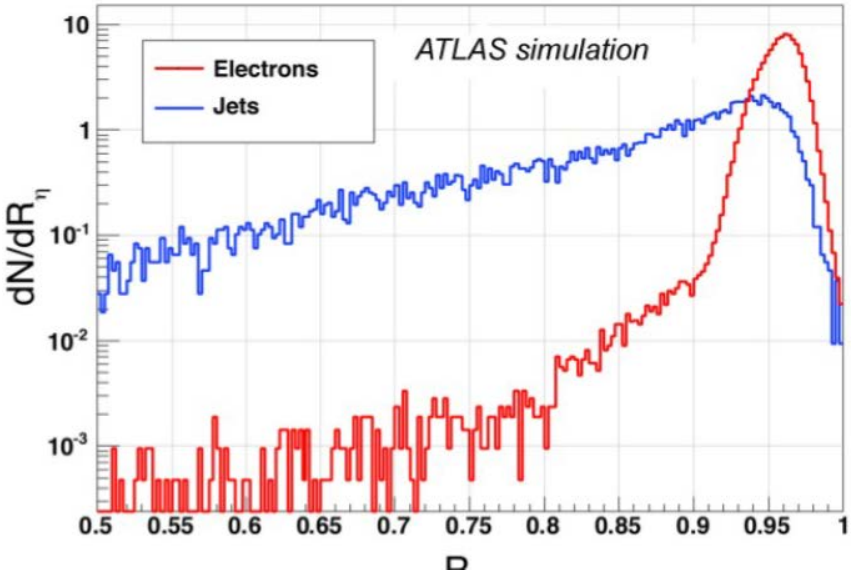
- **Current system**
  - Trigger tower size: $\Delta\eta \times \Delta\phi = 0.1 \times 0.1$
    (Shower width ~0.08)
  - 1 Tower in EM calorimeter
  → Shower shape is not fully used.



- **New system**

Introduce "Super Cell" already at level-1
  - Longitudinal segmentation
  - Lateral segmentation down to 0.025
  → Utilize narrow EM shower against Jet objects

Digitize trigger signal on detector
→ Robust energy reconstruction by Digital signal processing (Filtering) against large pileup under high luminosity environment.



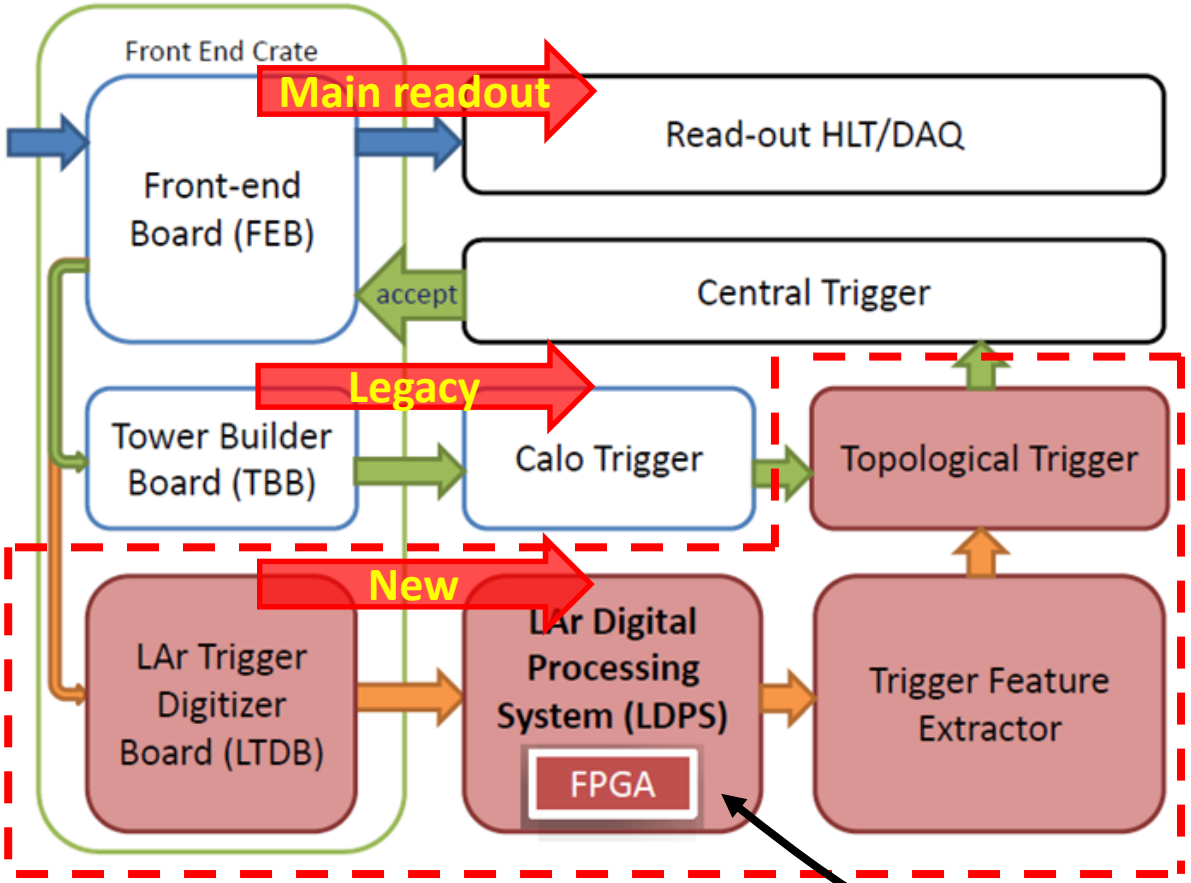
$$R_\eta = \frac{E_{T3\times2}}{E_{T7\times2}}$$

Phase1 LAr trigger readout scheme

Y. Enari
ATLAS Calorimeter Upgrade

For Phase-1 R&D

- Electronics upgrade for Trigger at Phase-I (2018)
  - Introduce new components while keeping legacy electronics
- Introduce Super-Cells (**10 times finer granularity**)
  - $\Delta\eta x\Delta\phi$ = **0.1x0.1** → 4 layers with **0.025x0.1** in middle layers.



Phase-1 components shown by the red dashed lines.

New components:

- Super-Cells are digitized at Front-End (FE).
- Converted to E_T by Digital signal processing at Back-End with FPGA (BE).
  - Sent to Feature extractor (FEX) to make L1-Trigger.

Fast data transfer is key

- **25 Tbps (FE→BE)**
- **41 Tbps (BE→FEX)**

Tokyo's activities

Detailed description LAr Phase-1 TDR

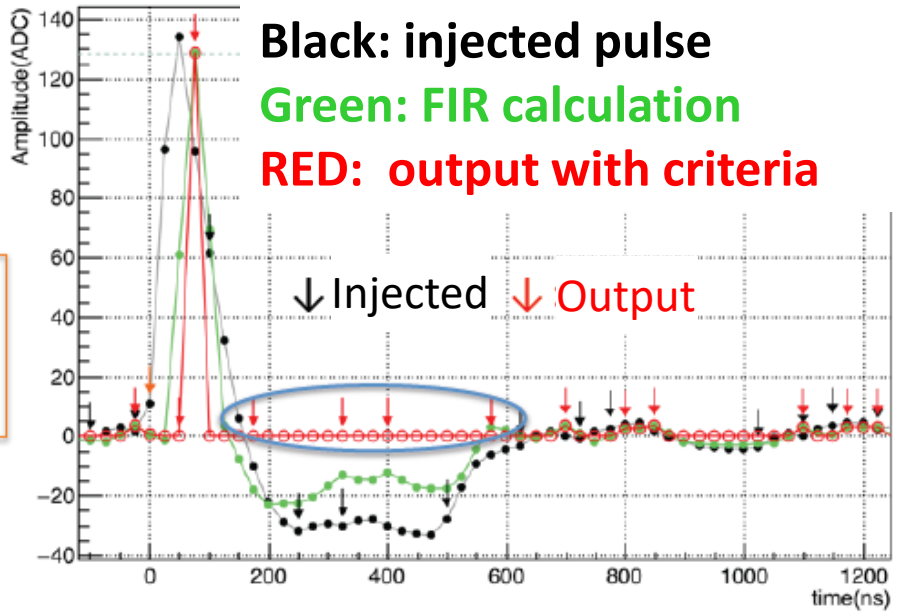
R&D on Filtering algorithm

- Default

Optimal Filter

$$A = \sum_{i=1}^{4} a_i S_i$$

$$A\tau = \sum_{i=1}^{4} b_i S_i$$



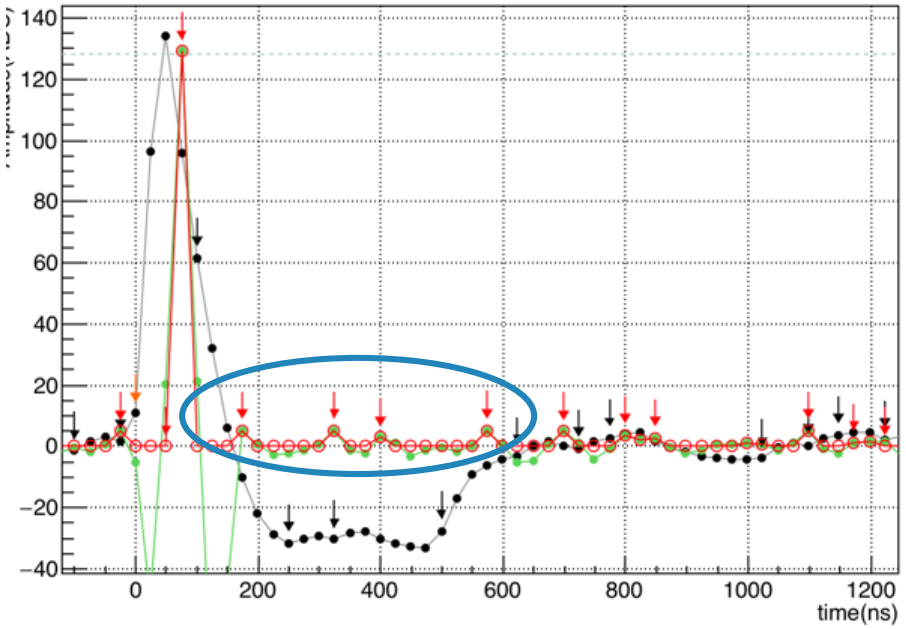
Need to have proper pedestal.
→ BCID dependent correction.

New Filter

Extended Optimal Filter

$$A = \sum_{i=1}^{24} a_i S_i$$

$$A\tau = \sum_{i=1}^{8} b_i S_i$$



Pedestal is always same.
→ only one pedestal per channel.

Given Latency for LAr system

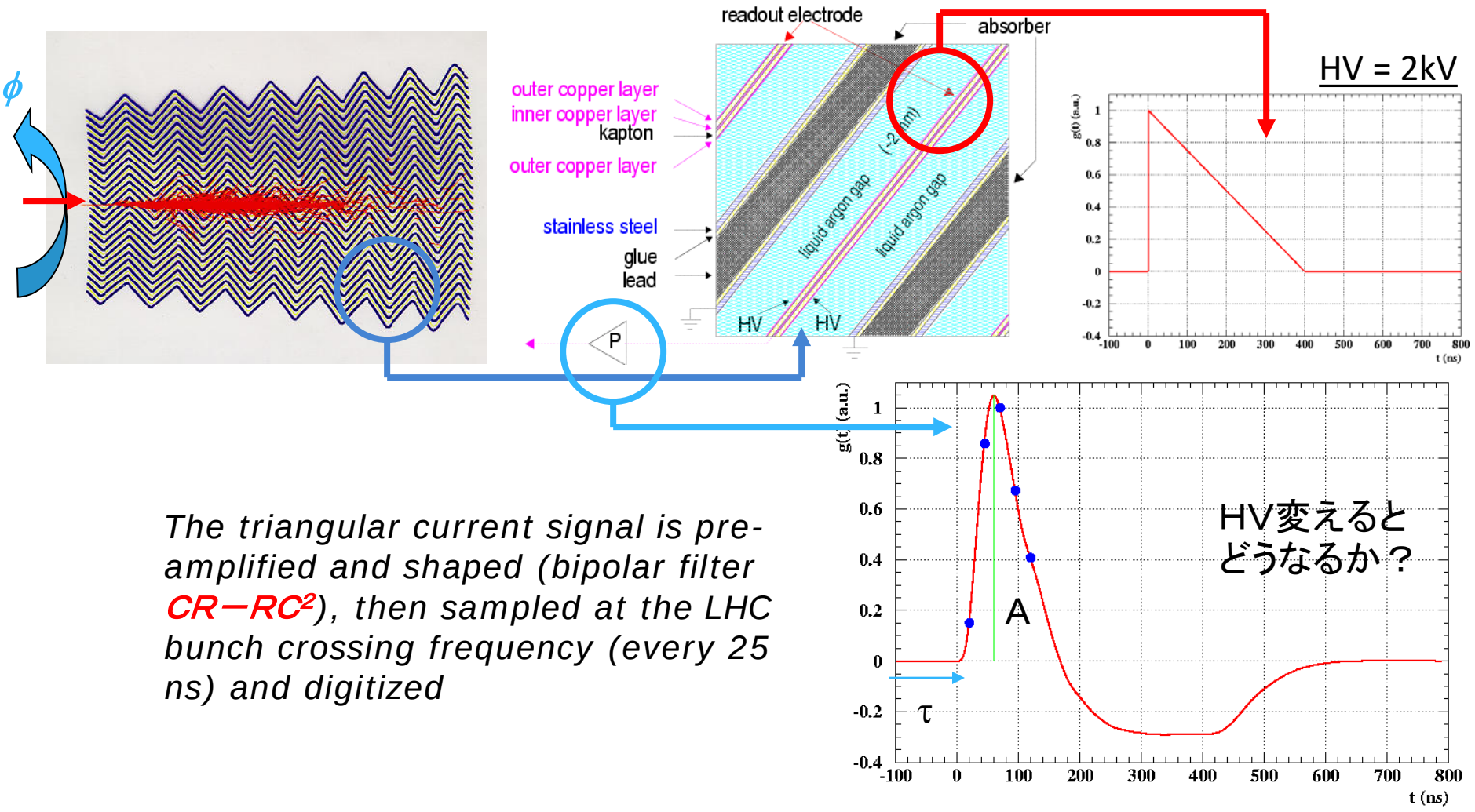
For Phase-1

Table 1: Latency estimates (in units of BC) for a LTDB - LDPS system up to entry into FEX. Elements in the table which have been calculated (not measured) are shown in *italics*

	BCs	Sub Total	Total	
Time-of-flight to endcap at eta = 2	0.6			
Cable to pulse preamplifier	1.2			
Pulse preamplifier and shaper	0.4			
		2.2	2.2	
Digitization on LTDB	*8*			Front-End
Multiplexing on LTDB	*1*			11x25ns = 275 ns
Serializer on LTDB	*2*			
Optical cable (70 m) from LTDB to LDPS	14			
		25	27.2	
Deserializer on LDPS	2			Back-End
Channel demultiplexing on LDPS	1			14x25ns = 350 ns
Pedestal subtraction	1			
E, t, Q, N-tap FIR, BCID Calculations	5			
Digital summation	*2*			
Multiplexing on LDPS	*1*			
Serializer on LDPS	2			
Optical cable (15 m) from LDPS to e-jFEX	3			
		17	**44.2**	

Without cabling, FE part:275ns, BE part: 350ns

Cell structure and signal shape



The triangular current signal is pre-amplified and shaped (bipolar filter $CR-RC^2$), then sampled at the LHC bunch crossing frequency (every 25 ns) and digitized

The peak of the ionization current is proportional to the energy released in LAr.