

The EUDET TPC Project

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Goal:

- design, develop and build a field cage for a "Large Prototype" (LP) to be used for studies and development work towards a TPC at the ILC.
- develop readout electronics to be used in conjunction with the LP

Members of the fieldcage group:

DESY, University Hamburg for the field cage
CERN, Lund, Rostock for the electronics

The fieldcage

Size and boundary conditions:

defined through PCMAG (see presentation by Tobias on JRA1)

Main parameters:

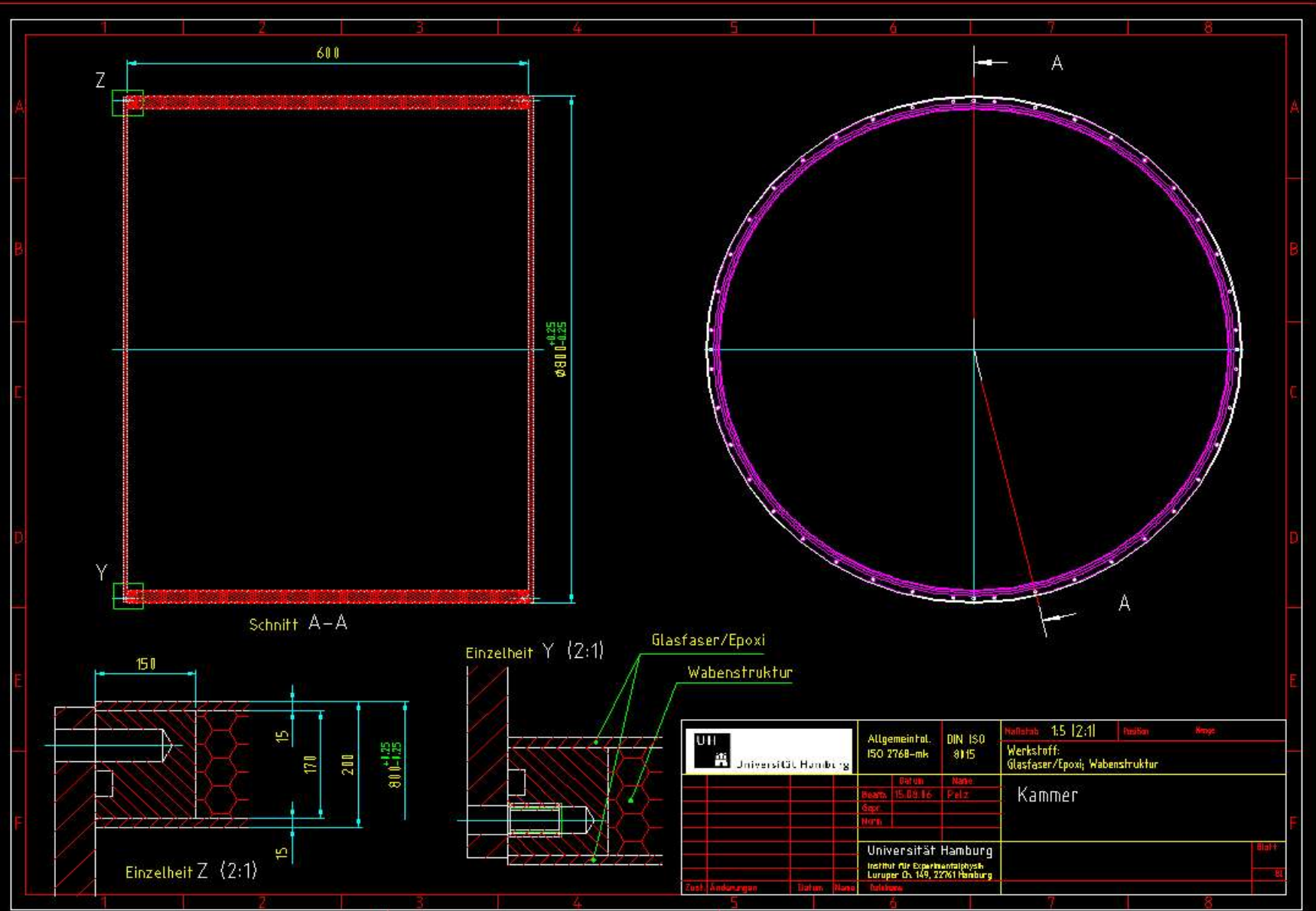
Length: 60 cm drift

Radius: 80 cm (to allow external Si detectors, if wanted)

Lightweight, stable, flexible

support more than one endplate with different readout technologies and ideas.

The Prototype



Plans:

Field cage design has started in earnest,

negotiations with industry to build the field cage have started
(but there are no results yet: difficult financial planning)

End 2006: freeze the final design, including all interface questions and
material questions

mid 2007: have the fieldcage available

Electronics development

Main contributors:

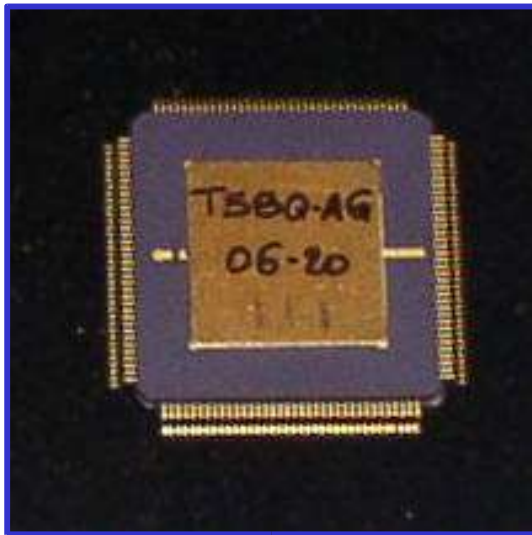
CERN/ Lund (readout electronic based on Altro chip)

Rostock (TDC based readout electronics)

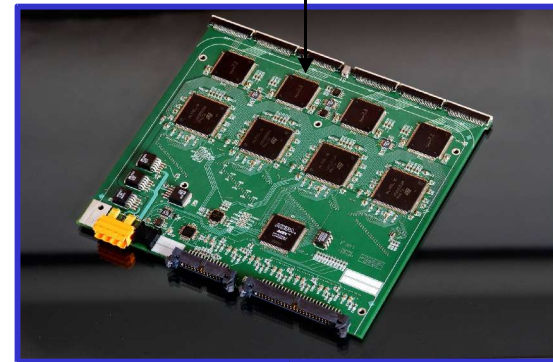
Basis for the main LC-TPC development:

ALTRO based solution,

Programmable Charge Amplifier



- The CQFP 144 package has the same pin-count and similar pinout as the ALICE TPC PASA
- In the near future the new chip will be tested on a ALICE TPC FEC



Next Step

- Milestone I (Q4 2006) Programmable Charge Amplifier (prototype)
 - 16 channel charge amplifier + anti-aliasing filter
 - Programmable peaking time (50ns – 500ns) and gain
 - Submission (?? To be discussed with Sandro)

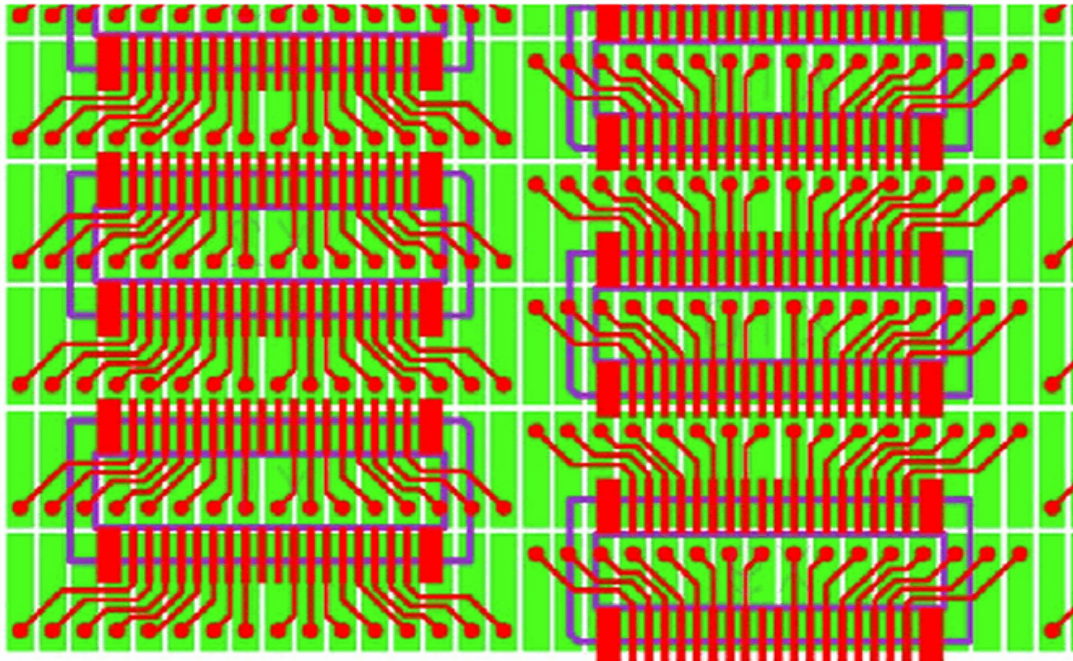
Endplate Logistics

Problem: find a correct mapping between Pads ($O 1 \text{ mm}^2$) and electronics

Current development:

connectors on the back of the endplate

flexible circuit connection to the electronics (this is not the final version)



circuit layout
for the endplate

main contributor Lund

Milestones of ALTRO development

- Milestone I (Q1 2007) Programmable Charge Amplifier (prototype)
 - 16 channel charge amplifier + anti-aliasing filter
- Milestone II (Q2 2007) 10-bit multi-rate ADC (prototype)
 - 4-channel 10-bit 40-MHz ADC. The circuit can be operated as a 4-channel 40-MHz ADC or single-channel 160-MHz ADC
- Milestone III (Q2 2008) Charge Readout Chip (prototype)
 - This circuit incorporates 32 (or 64) channels.
- Milestone IV (Q2 2009) Charge Readout Chip (final version)

EUDET and LC-TPC

Work of this tasks is closely integrated into LC-TPC group

Regular discussion meetings with the other members of the LC-TPC group

Specifications and design is developed together with LC-TPC

Financial information

University of Hamburg:

1 position filled as of 15. September 2006

DESY

position has been advertised, offer has gone out, hope to fill position by November 1st

CERN

budget for 2006 nearly all allocated / spent

Lund

information will be forthcoming (my fault)

Rostock

one person being paid by EUDET funds

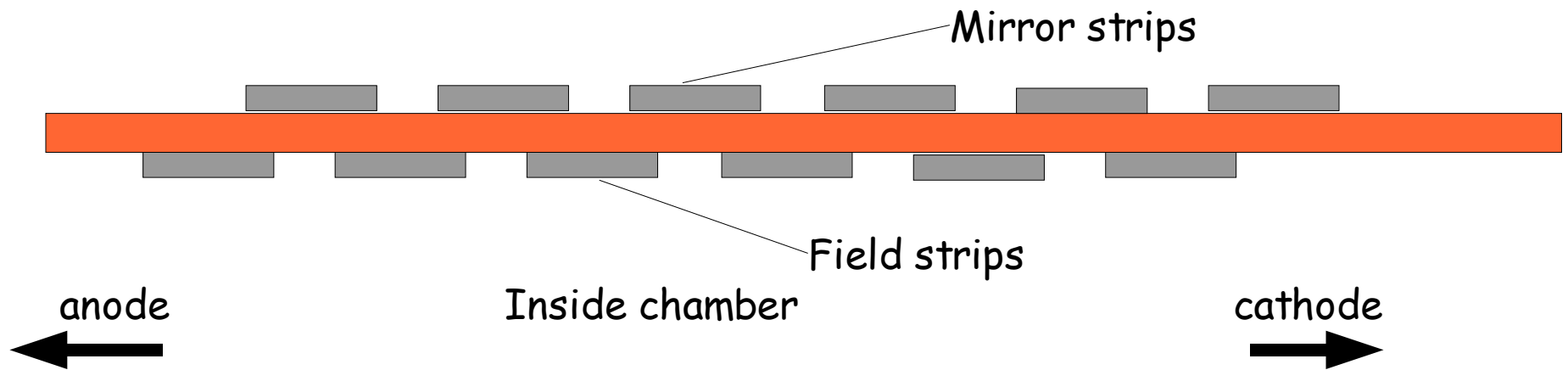
We expect to be able to spend the allocated budget for 2006 in full.

Backup

Optimization of Layout

Work by Peter Schade, DESY

Configurations of different field strips:



Questions:

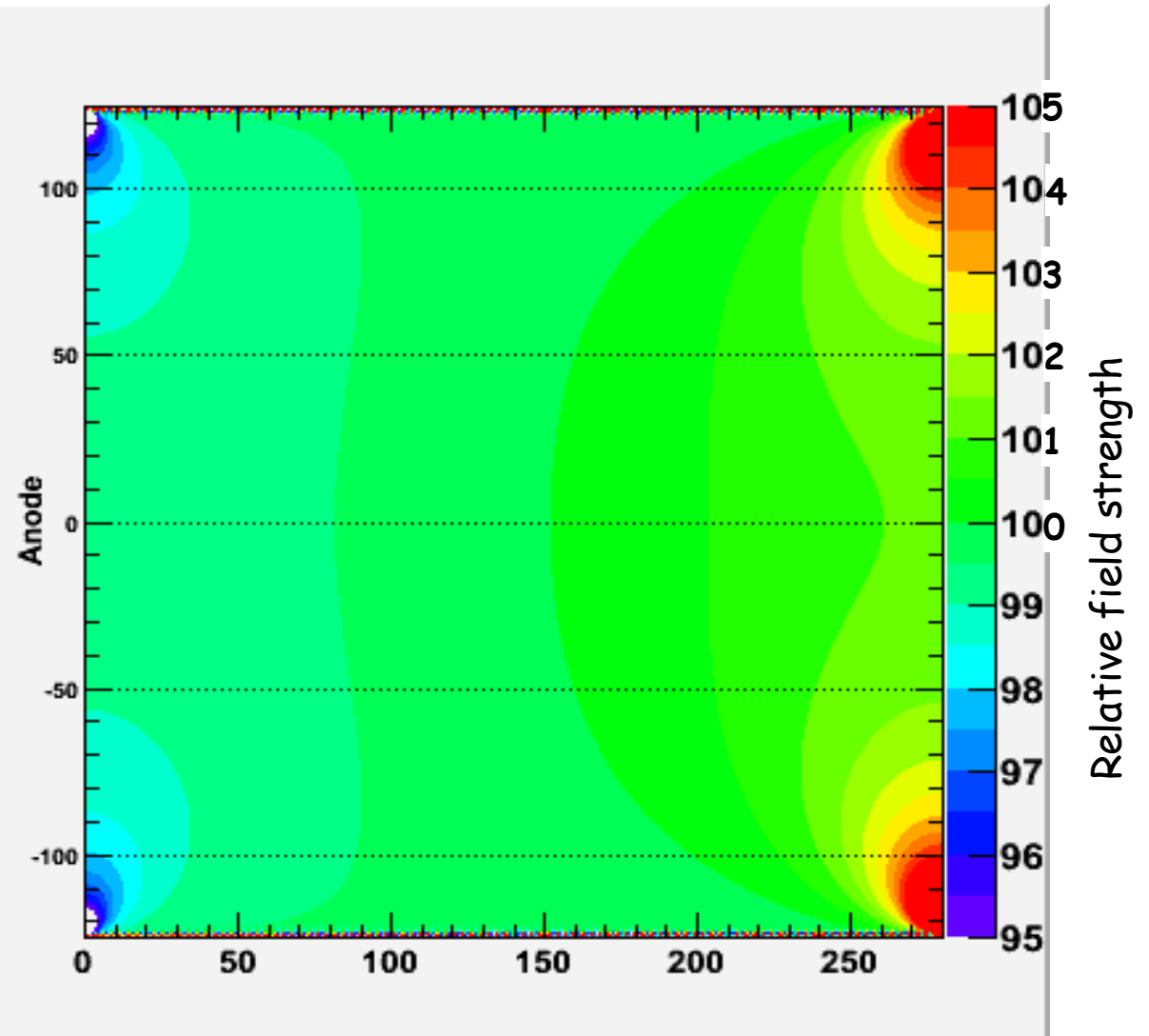
mirror strips, yes or no?

Arrangements of mirror strips

Field Optimzation

No mirror strips

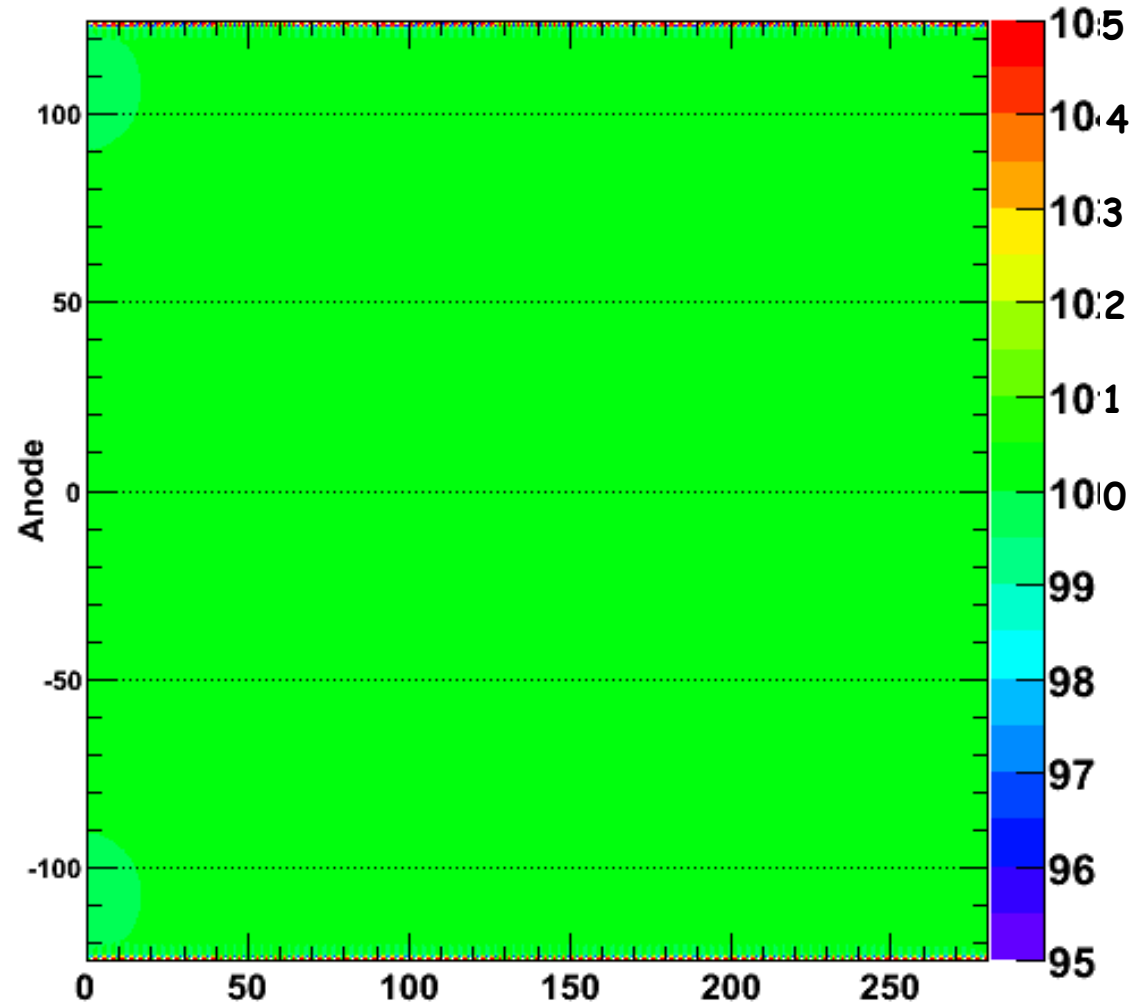
- Large field distortions, particularly at cathode ($>5\%$)
- Inhomogeneous field for main drift region of $O(1.5\%)$



With optimised mirror strips

Mirror strips,
at intermediate potential

- Deviations in field volume small ($< 0.5\%$)
- Some residue deviations at anode of $O(<1\%)$ (need optimization of interface endplate - drift volume)



Material Studies

Field cage wall:

composite structure,
HV insulation through Kapton layers
mechanical strength through GFK - NOMEX - GFK structure

Plans:

HV studies of the wall material this fall
investigate several "new" materials in place of Kapton
discussion with industry on ways how to wind the LP field cage are ongoing