News from KLauS (4)

- New chip & test setup
- Characterization measurements
  - Front-end
  - ADC
  - Full chain
- Next steps & further plans

Konrad Briggl,
KIP, Uni Heidelberg

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KLauS4: New multi-channel prototype

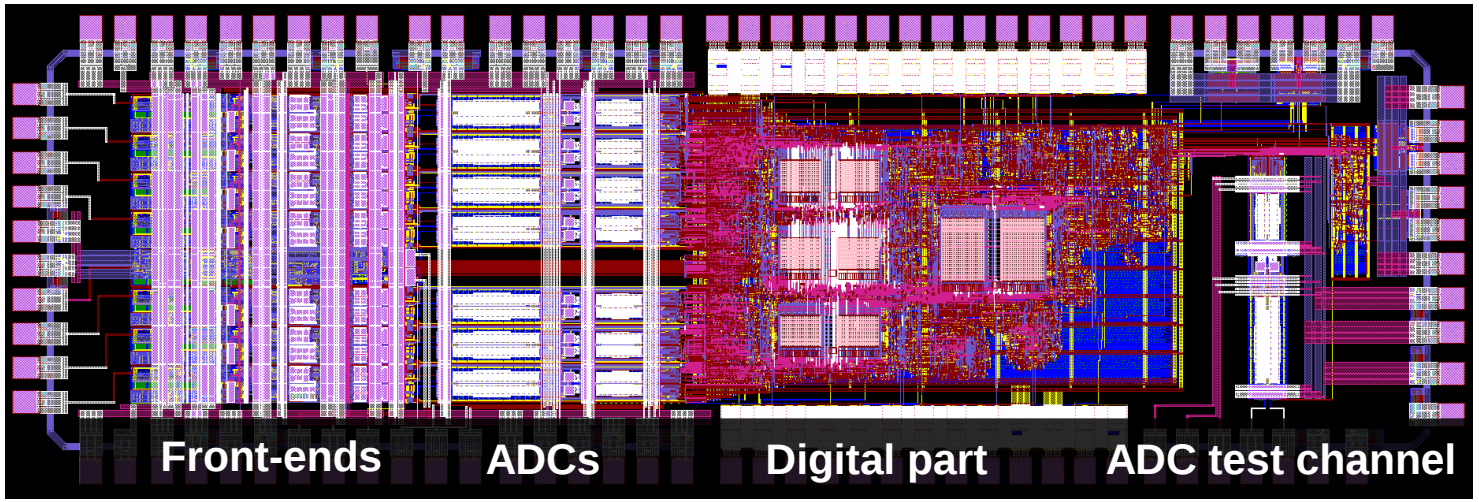
Taped out first multi-channel prototype in May 2016
1.5 x 4.5 mm² miniASIC, UMC180 (Final 36 channel chip size 5x5mm²)
Under test since few weeks

7 Front-End + ADC + digital channel control modules
1 TDC-only channel (external time reference)
25ns binning of all time-stamps (Fine-time TDC under development)

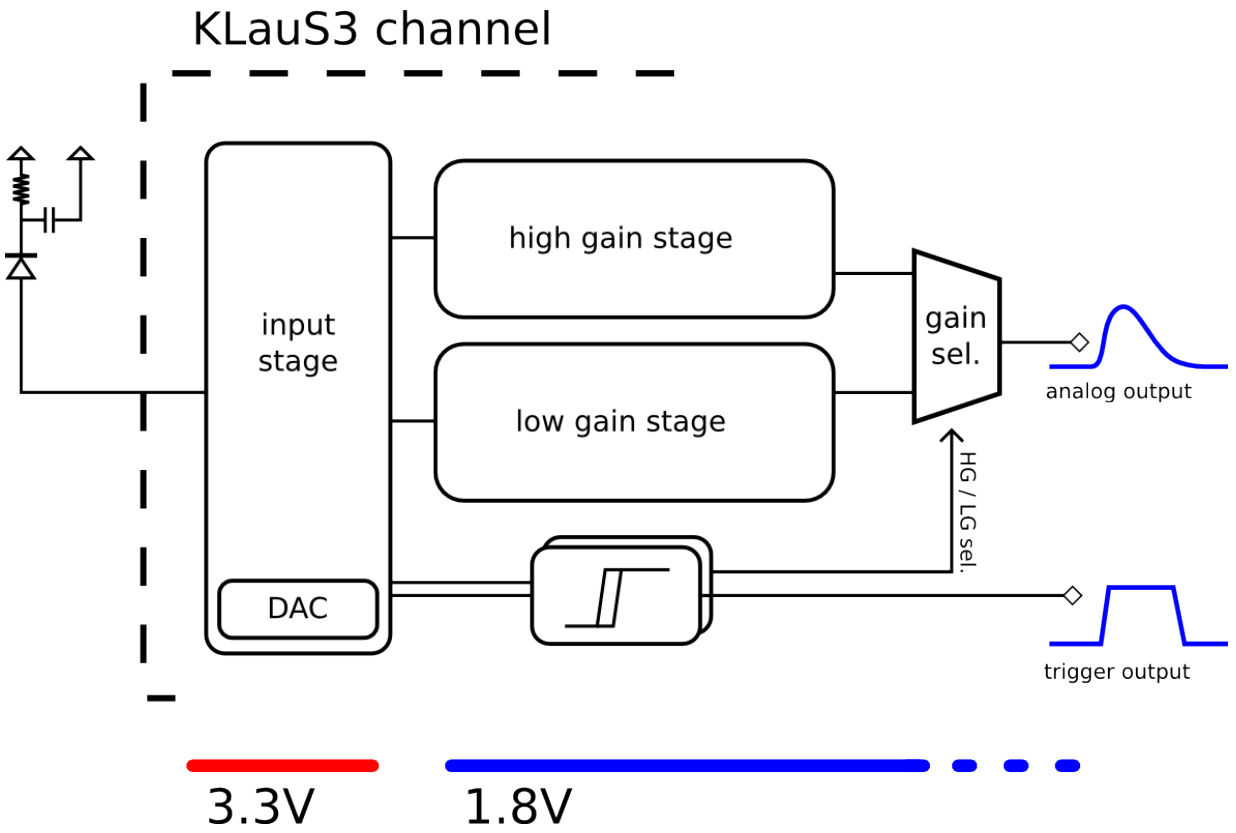
1 ADC test channel (separate)

Digital part

Structured as future 36 channel version
Different readout options: Fast LVDS (160Mbit/s), slow I^2C link



Front-end: Blocks



Input stage:

- Low input impedance
- SiPM bias voltage DAC

High gain stage:

- Single pixel spectra
- O(10ths of pixels)

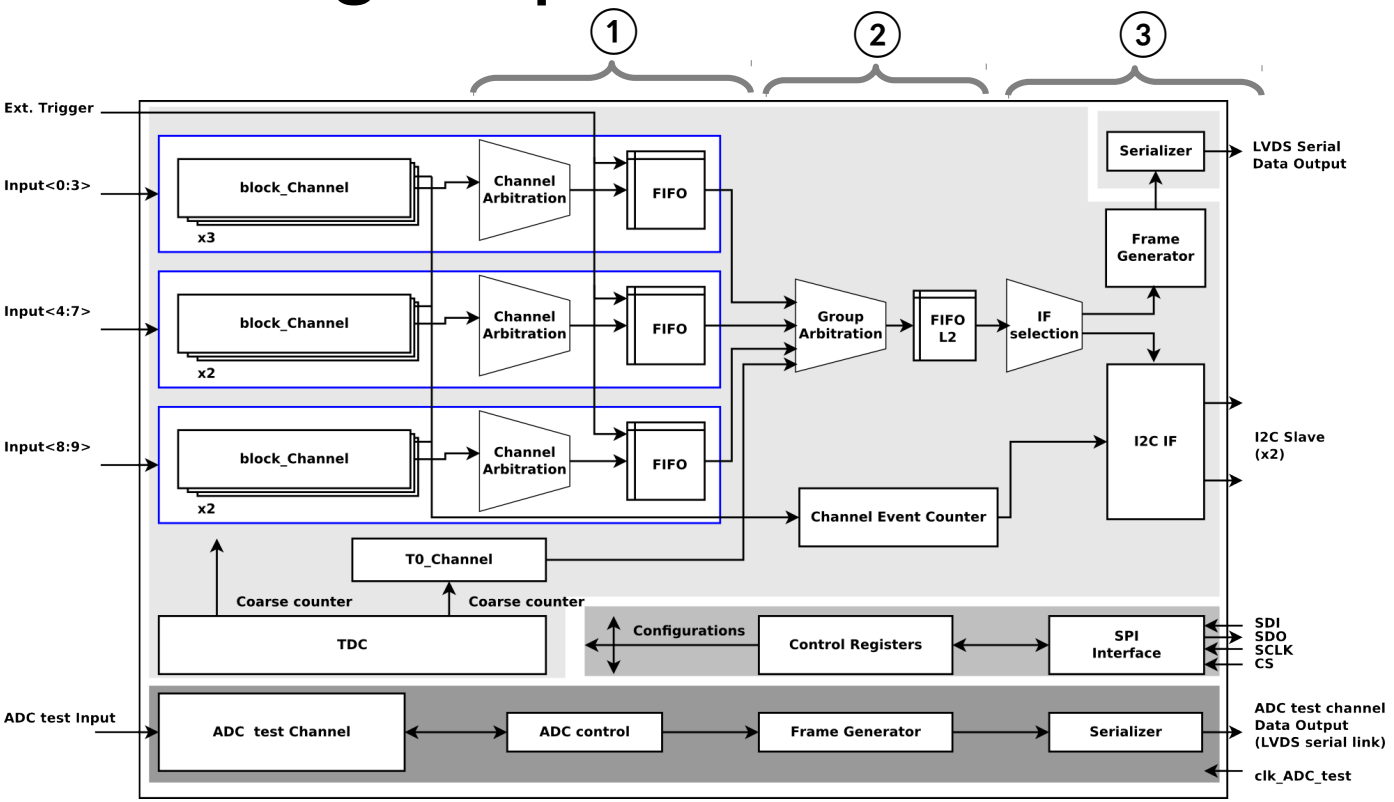
Low gain stage:

- Full SiPM dynamic range

2 Trigger branches:

- Event trigger
- HG/LG selection

Digital part: Overview



Two levels of data concentration:

L1 & L2 arbiter+FIFO (①, ②)

Event data Serialization

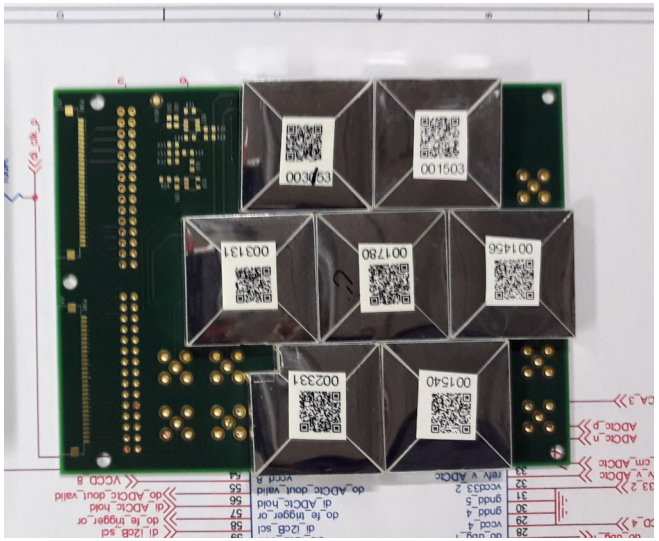
LVDS or I²C interfaces (③)

Hit validation in ADC control logic & L1 FIFO
8bit channel hit counter read out by I²C transaction (SMBUS block read)
Slow control using SPI, will be replaced by I²C (SMBUS block r/w)

KLauS4 test board

Compatibility with requirements for Testbeam

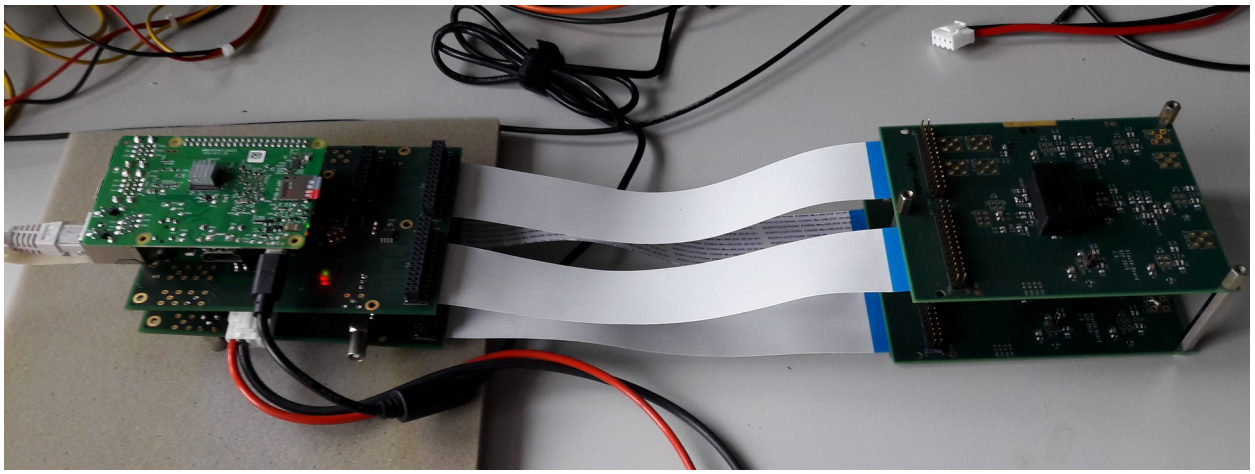
Possibility to participate in future testbeam campaigns
SMD MPPC pads distribution similar to HBU
→ Scintillating tiles can be placed on top



To allow insertion into absorber stack

Form factor & overall height *adopted*
→ *Total thickness <7mm*
→ *1mm PCB, 6 layers*

DAQ outside of absorber
→ *Flex cable connection*



Interface Connections
SPI & LVDS & I2C
↔ interface board
↔ DAQ

SiPM DAC scans

8bit voltage DAC for each channel:

Tuning of voltage at input terminal
Always on: Low power (1-2nA/LSB)

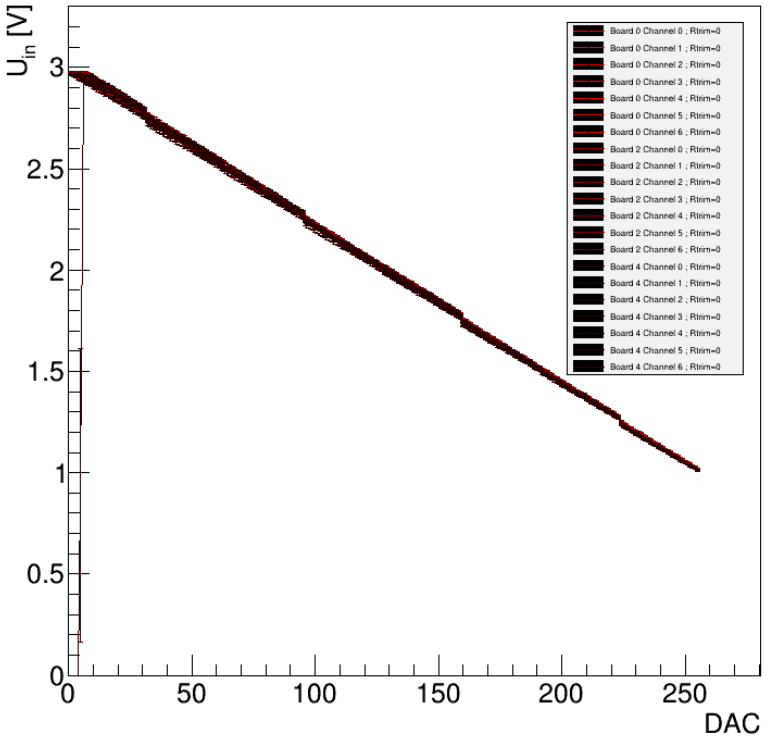
Measure 3 boards, 7 channels each

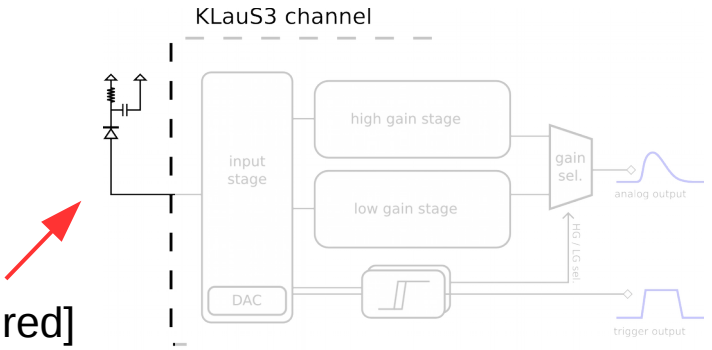
Tuning range of 2V as expected

Some slope dispersion:
Mostly channel-to-channel,
chip-to-chip dispersion small

DNL pattern visible,
withing expectations of MC simulations

Scanned voltage
3 ASICs,7 channels each





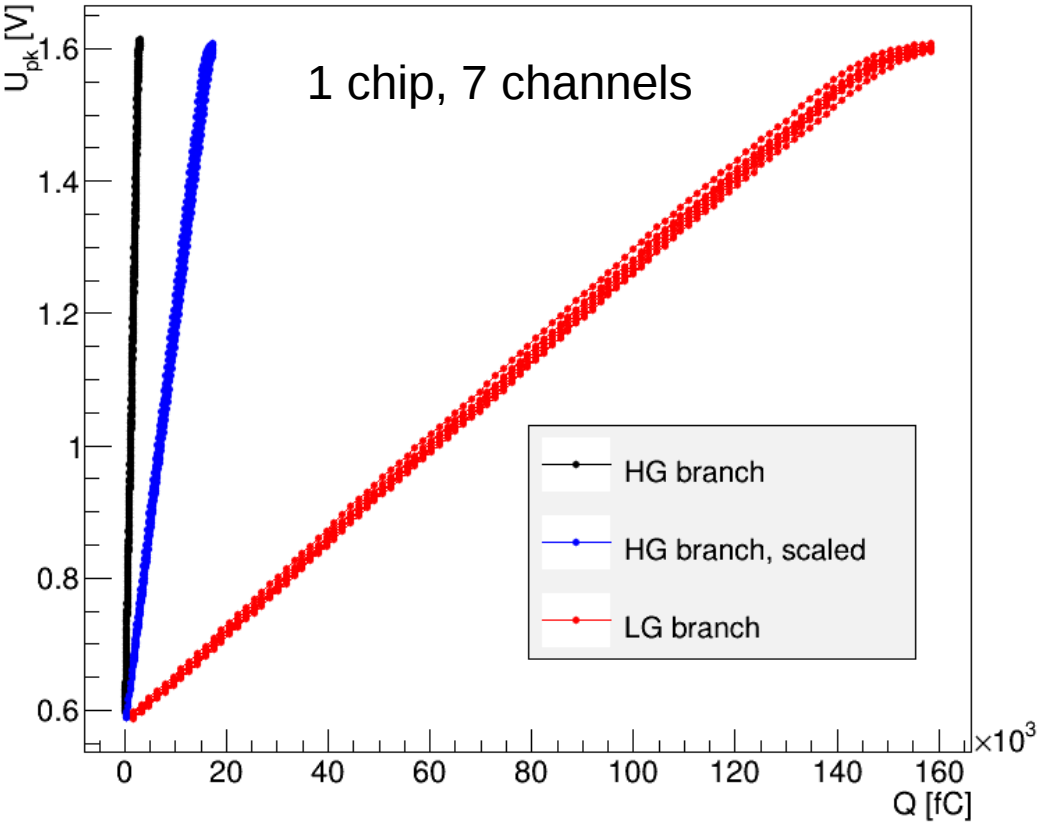
[DC voltage measured]

Charge integration

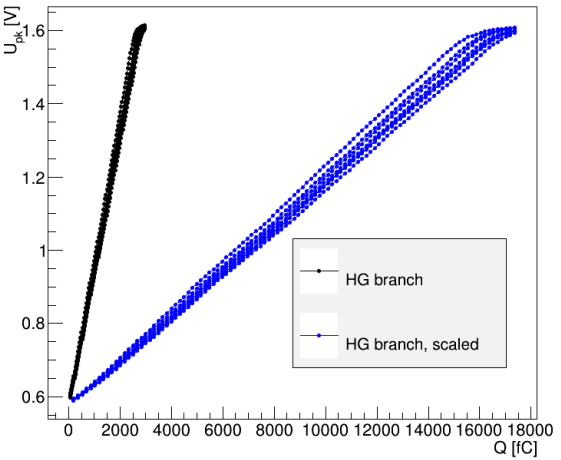
Charge injection using 33pF capacitor

3 Scale settings, 2 separate Branches

High gain branch → 1:1 or 1:7 (exclusive)
Low gain branch → 1:48

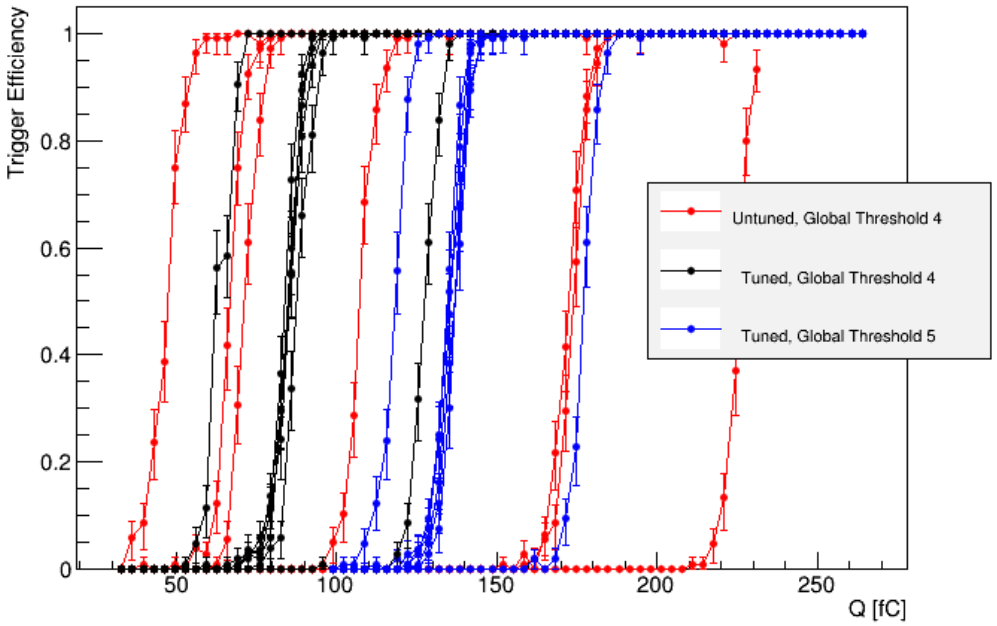


All scale ranges available



HG branch configurations

Comparator: Threshold setting



Comparator s-curves, 7 channels:
- No threshold tuning (same finetune setting)
- 2 global threshold settings after finetuning

Two DACs to adjust threshold:

- **Global 6 bit DAC**:
  Coarse setting
  ~50fC / LSB
- **4 bit DAC per channel**:
  Fine-tuning,
  ~5fC/LSB
  Threshold Dispersion mitigation

Dispersion reduced after fine adjustment
  60fC RMS → 17fC RMS
  (Some outliers)

Satisfactory for >=25 um pixel SiPMs,
To be tested for 10um pixels
@ low light yield/MIP

Full chain: first checks

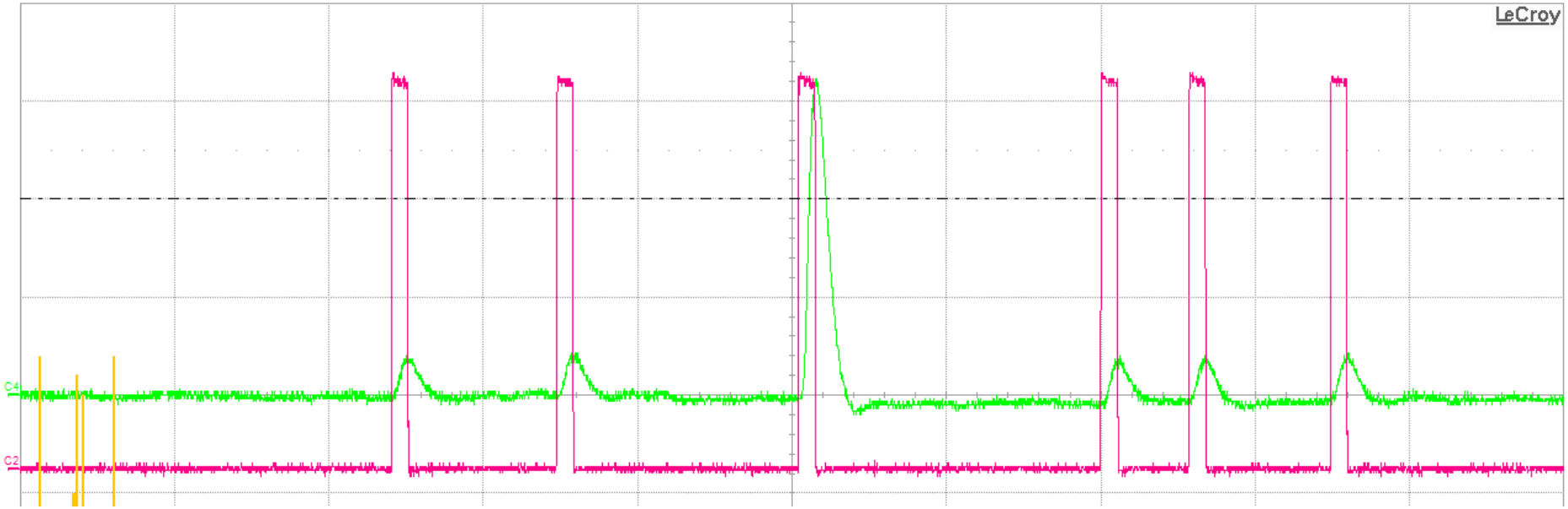
After proper Threshold and hold time settings:

Behaviour as expected

→ Comparator fires (Trigger signal set)
→ Hold swich opened at peak
→ ADC takes over conversion (Trigger signal reset)

Waveforms: DCR + LED light pulse on 25um MPPC

- Analog outputs
- Comparator output



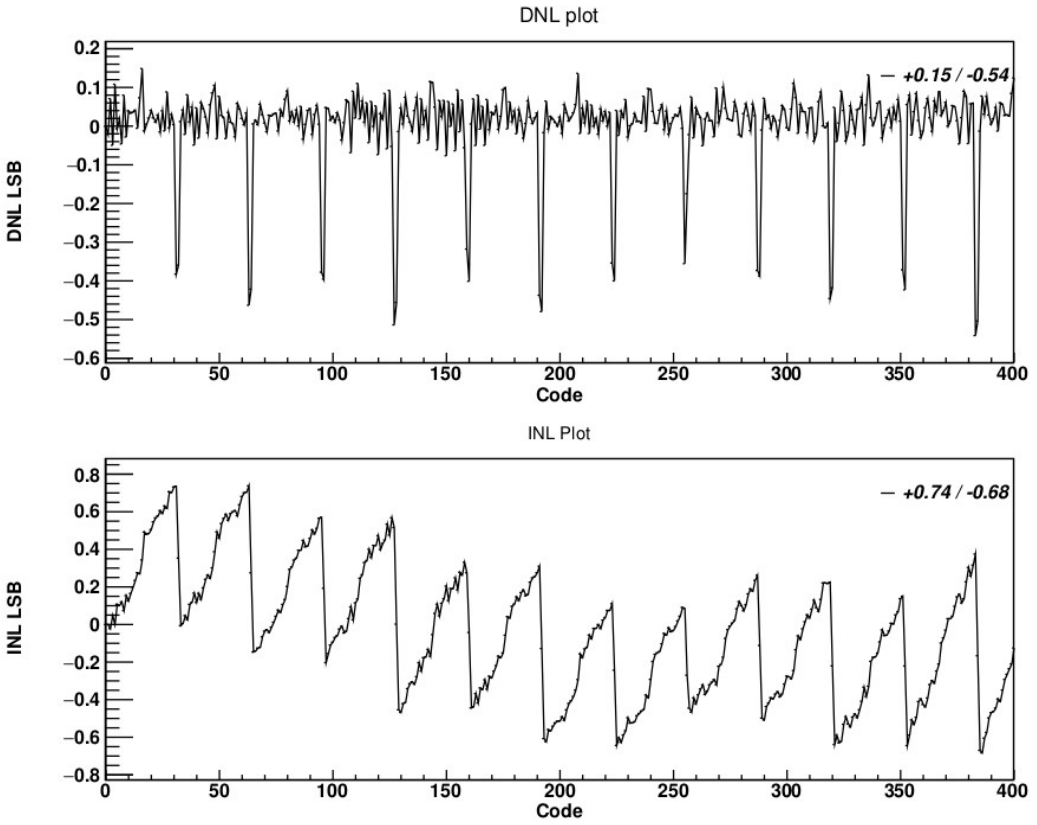
ADC: 10bit operation

For linearity measurements:

External DC signal, sweep voltage

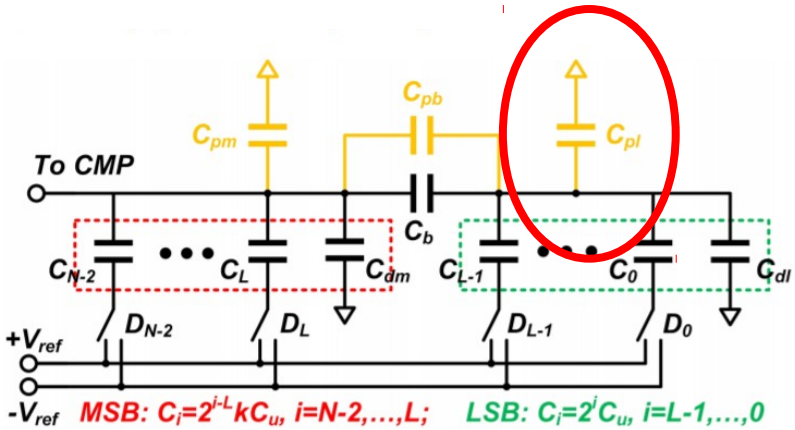
DNL pattern: every 32, pair of two
- → Parasitics on bridge capacitor
- → Easy to correct in software:
  Simple rebinning,
  no calibration runs needed

Much better than previous prototype!

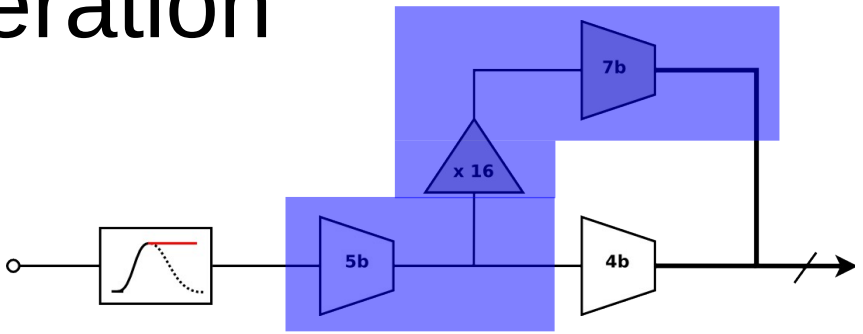


Performance satisfactory
→ ***Next 36 channel prototype will use this ADC***

Expect to improve in separate Test chip to be submitted in Q1/2017



ADC: 12bit operation



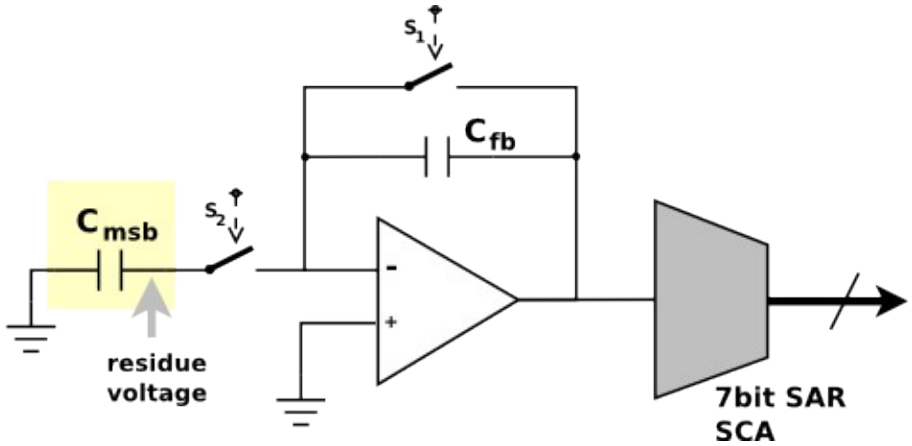
12b resolution operation mode
for SiPM spectrum digitizaton

<u>3 digitization steps:</u>

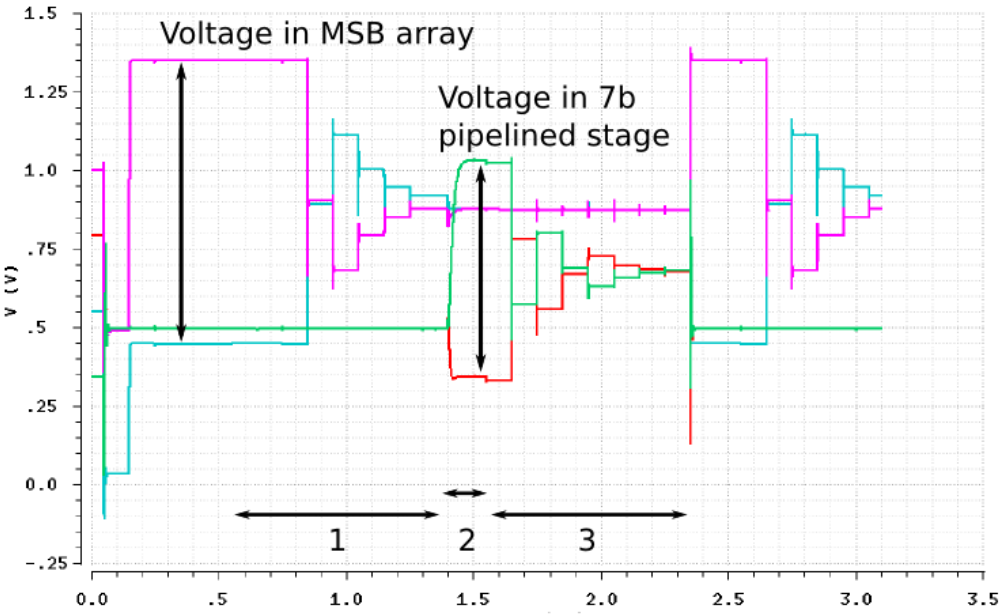
(1) 6b digitization in main SAR

(2) Amplification of residual error

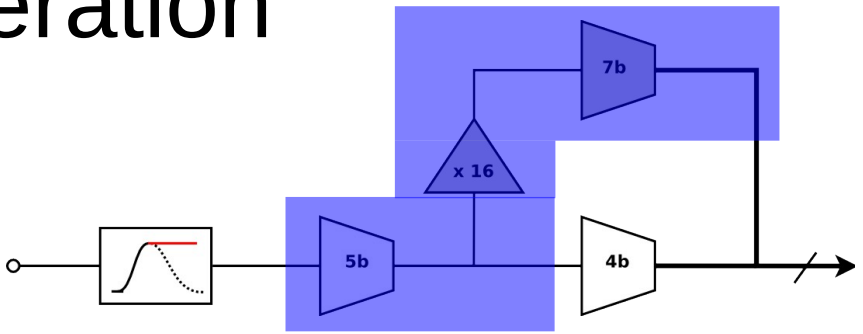
(3) 8b digitization in pipelined stage
remaining bits saved for redundancy



(1) (2) (3)



ADC: 12bit operation



12b resolution operation mode
for SiPM spectrum digitizaton

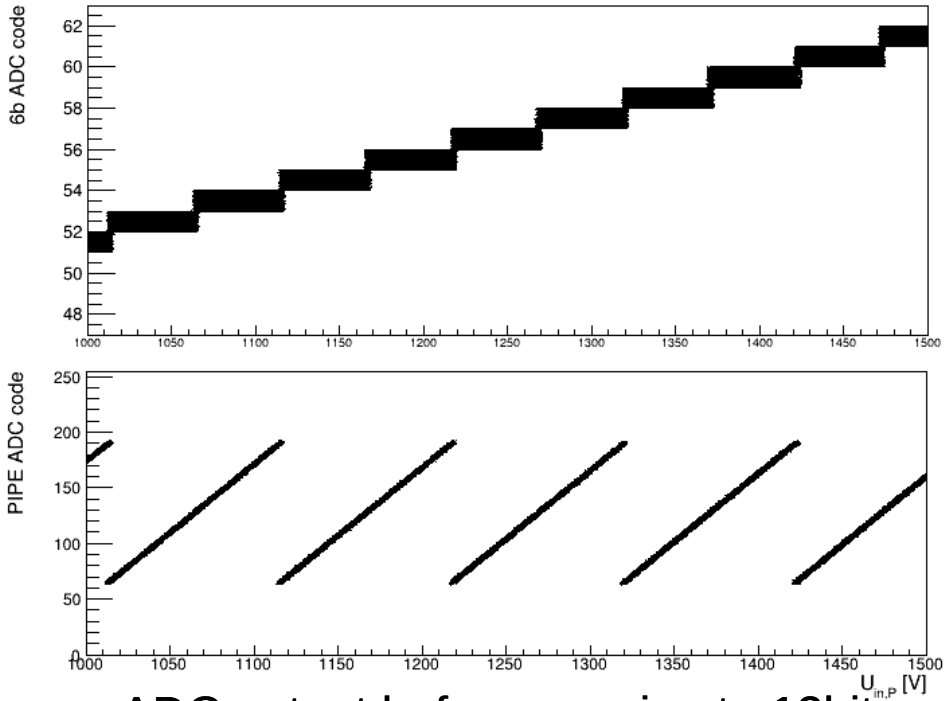
<u>Scan results:</u>

Very satisfactory:

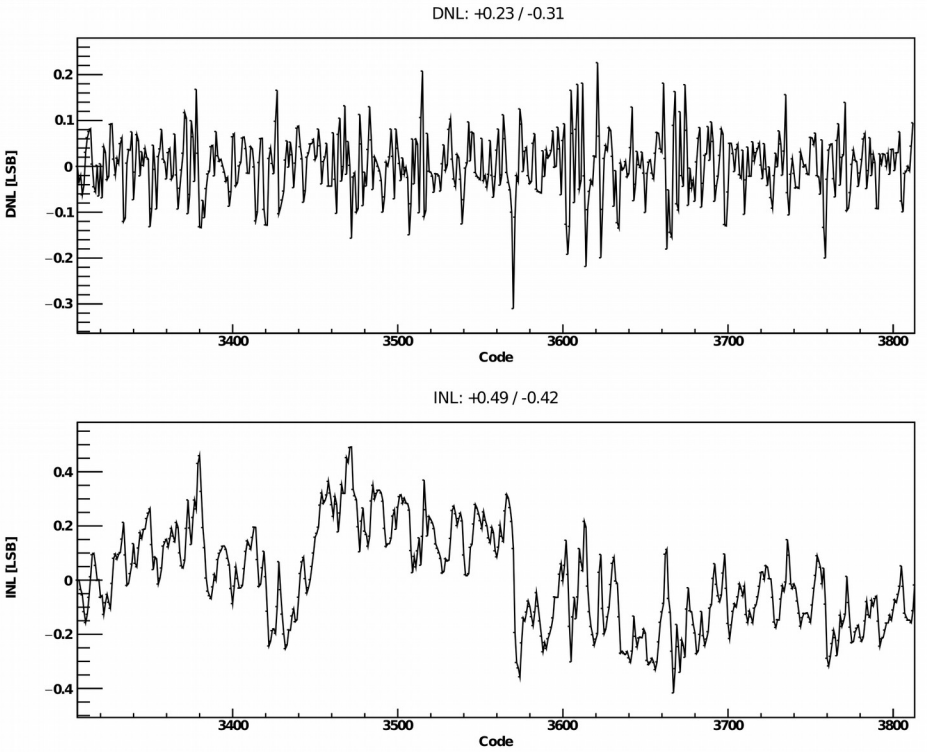
DNL < 0.31 LSB

INL < 0.50 LSB

(Note: not the full dynamic range!)



ADC output before merging to 12bit



Combined 12b ADC nonlinearity

Full chain: MPPCs & 10bit ADC

25um & 50um Pixel MPPCs: Large single pixel signals
10bit ADC resolution sufficient to see single photon spectra

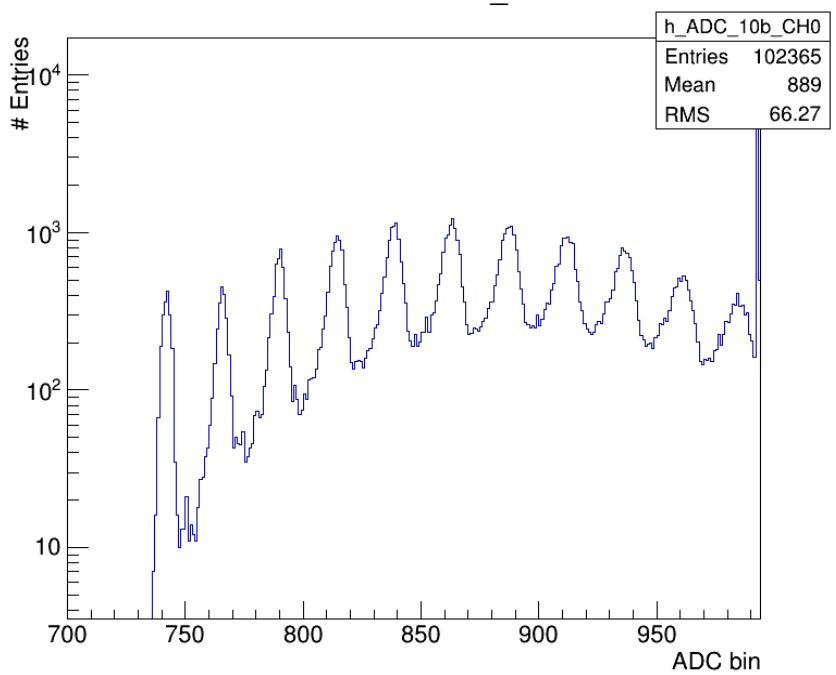
Both spectra:

- Internal trigger, ~15ns LED pulse
- Threshold at 1-2 p.e.
- Fixed to 1:1 scaling (HG branch)

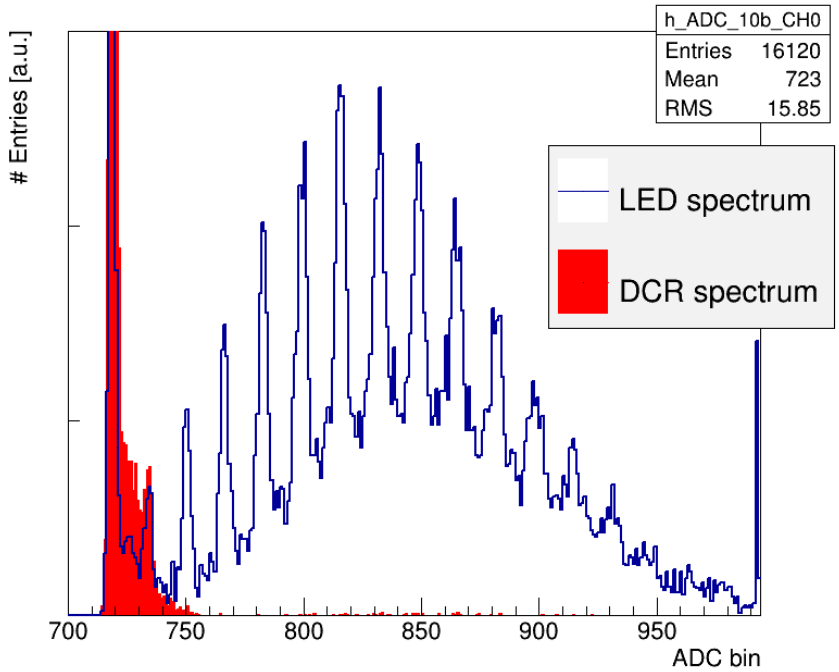
External trigger / validation features not tested yet:

- Would remove DCR hits

→ Backup slides:
50um MPPC spectra
at different thresholds



50um pixel MPPC *[log scale]*



25um pixel MPPC: LED+DCR, DCR only

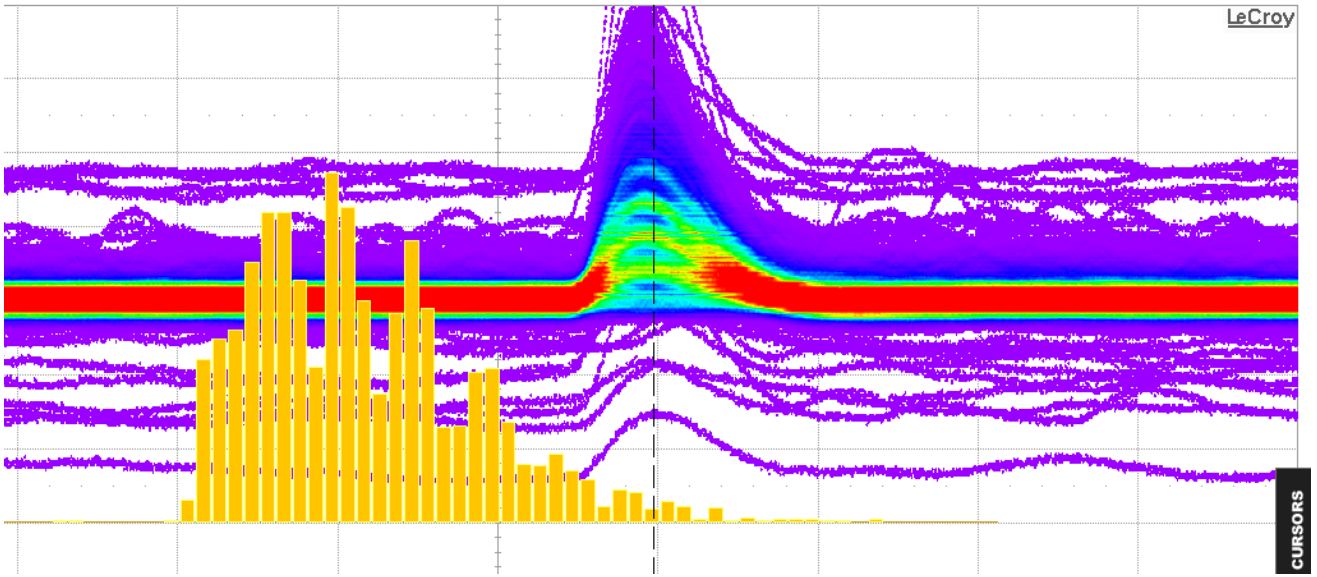
Front-end only: 10um MPPC

10um Pixel MPPCs:
12bit ADC needed for single photon spectra

To be done next...

Here: 10um MPPC at datasheet bias (gain: 1.35e5),
Measured with analog monitor of front-end & Fast DSO

- Decent peak separation
- Most ASIC parameters not touched



Summary & further development

Current prototype
- KLauS4 7 channel prototype operational
- 2V SiPM bias tuning range
- ADC shows promising results
- SPS for full chain using larger gain SiPMs

Next steps
- Qualitative characterization of front-end parameters
- Full chain measurements of 10um SiPM
- Test Power gating and remaining digital features

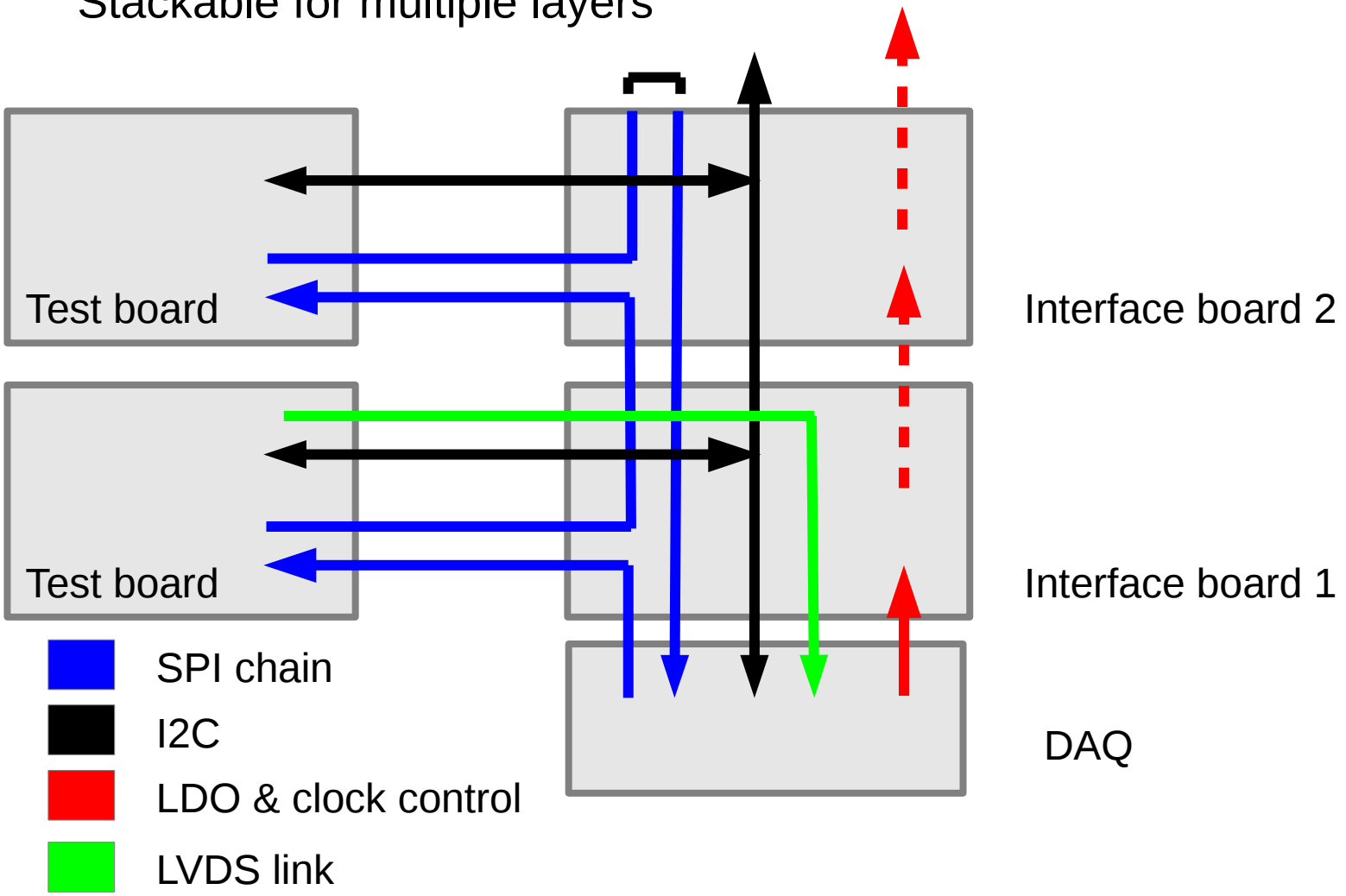
- Participation in test beam in near future seems feasible!
- 36 Channel version planned to be submitted in Q2 2017

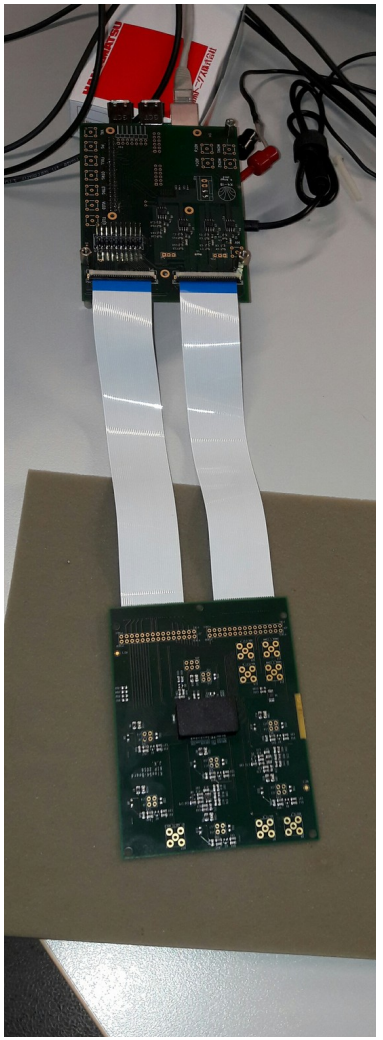
Backup slides

KLauS4 Test setup

Signal routing in System:

Stackable for multiple layers

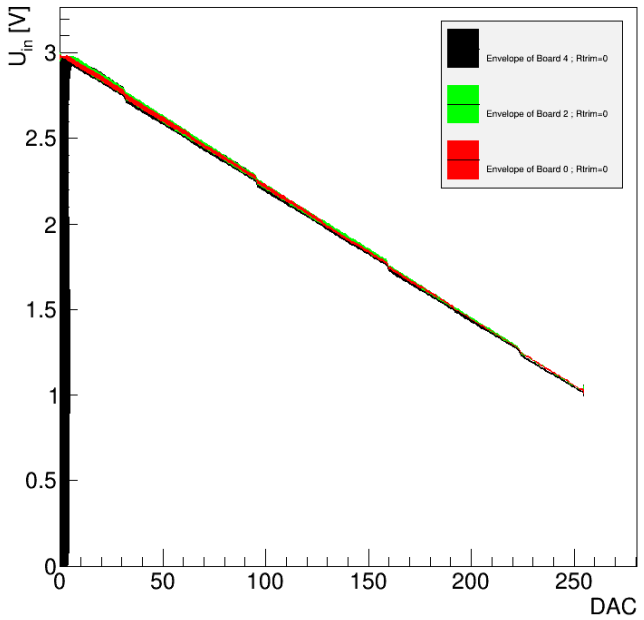




SiPM DAC scans

8bit voltage DAC for each channel

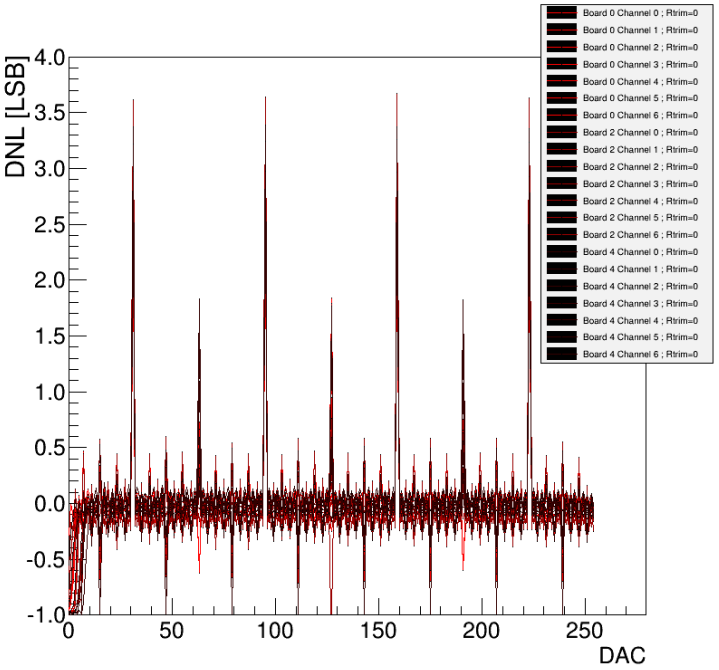
Tuning range of 2V as expected
Some slope dispersion:
Mostly channel-to-channel,
chip-to-chip dispersion small



3 ASICs, 7 channels each:
Envelope per chip

DNL patterns

Low power → Large DNL expected:
Up to 4 in MC simulations
Similar pattern for all chips&channels
→ Layout can be tuned eventually



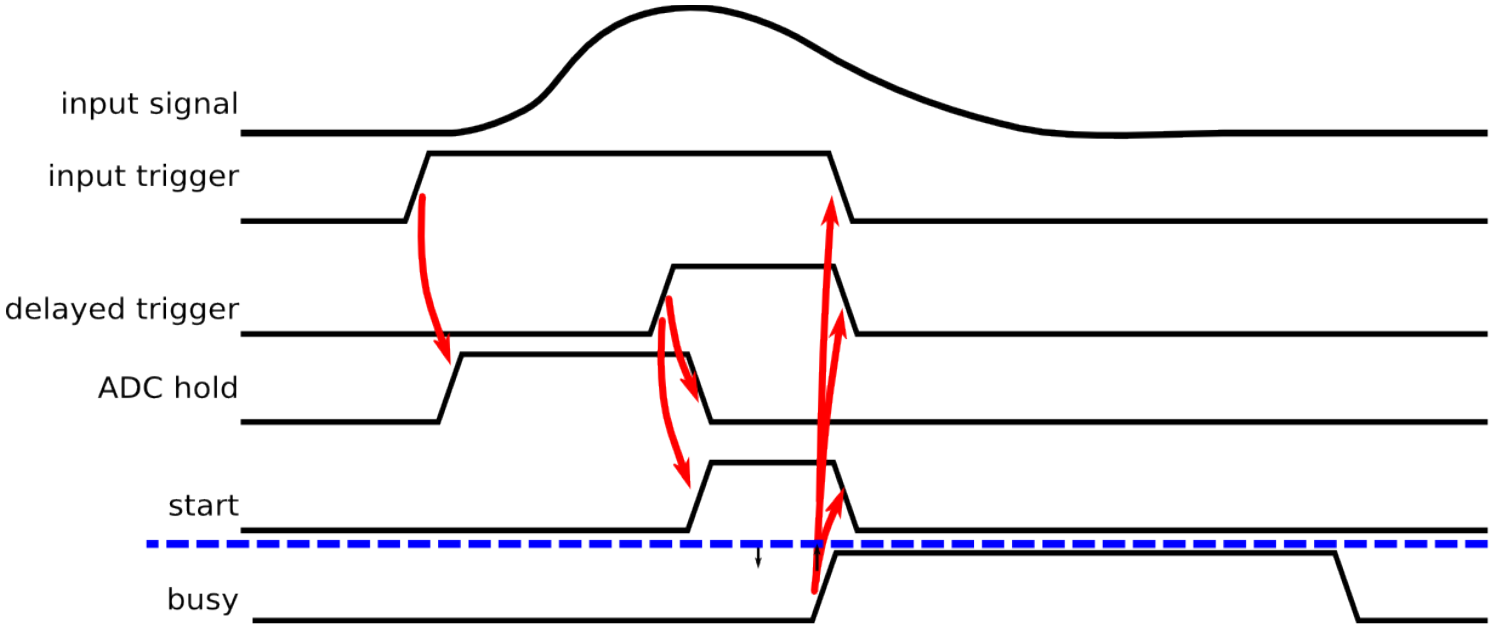
DAC DNL: 21 Channels

Interface: Front-end, ADC & control logic

Hold switch controlled by Front-end
→ Initiated by Comparator

Synchronized pass-over to ADC
→ ADC starts conversion (Trigger signal reset & blocked)

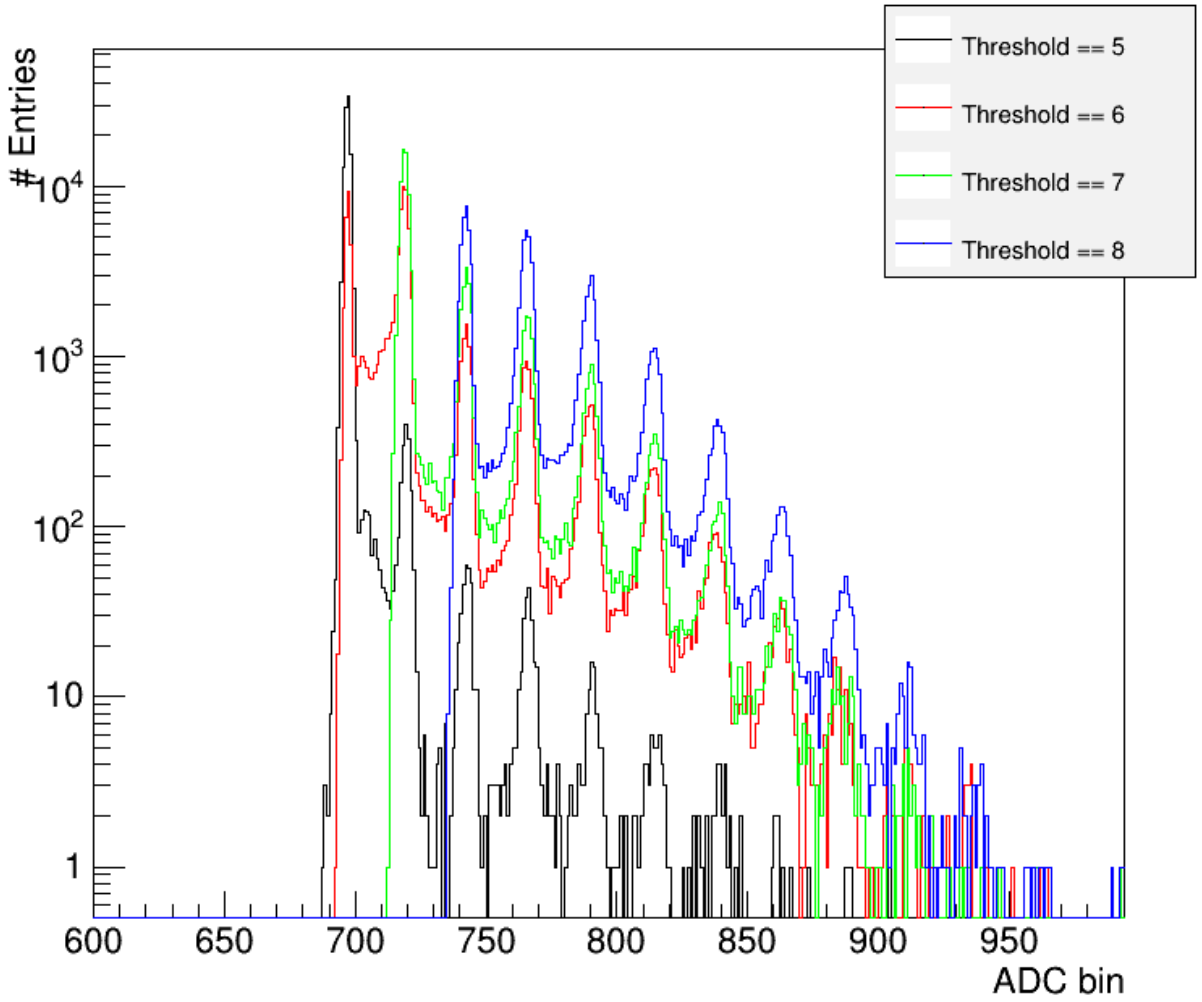
Synchronized unblocking of comparator
→ ADC conversion finished
→ New comparator triggers allowed to pass



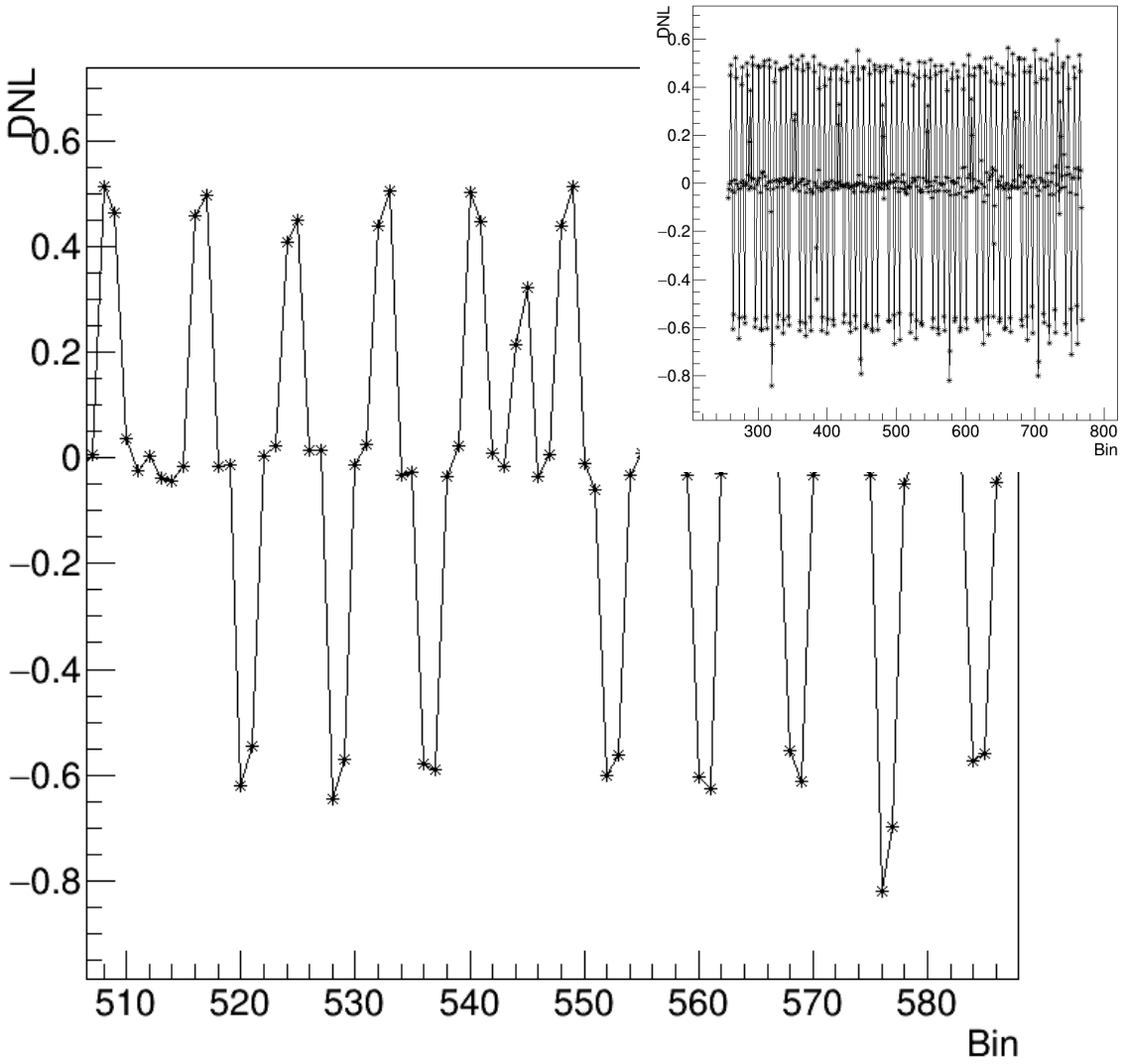
Full chain: MPPCs & 10bit ADC

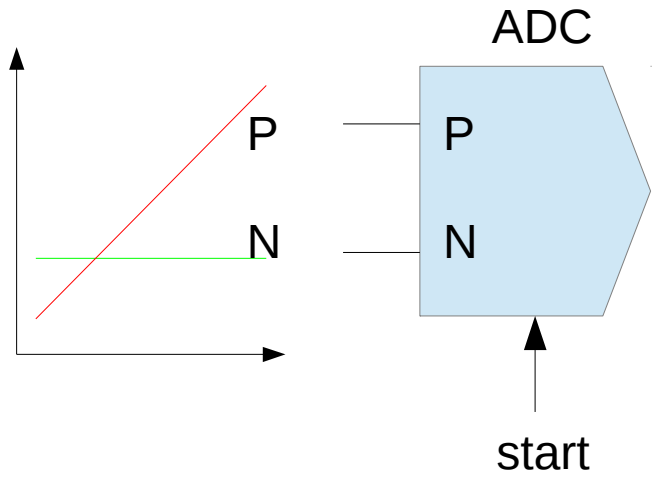
50um Pixel MPPCs

LED spectra at different thresholds (Auto trigger)
Lower thresholds: Higher DCR contributions
Same statistics for all runs: Different acquisition times



Previous protoype:
ADC DNL estimations





Negative terminal fixed to 0.9V
Positive Terminal swept [0 ; 1.8V]

Code density test used for DNL estimation