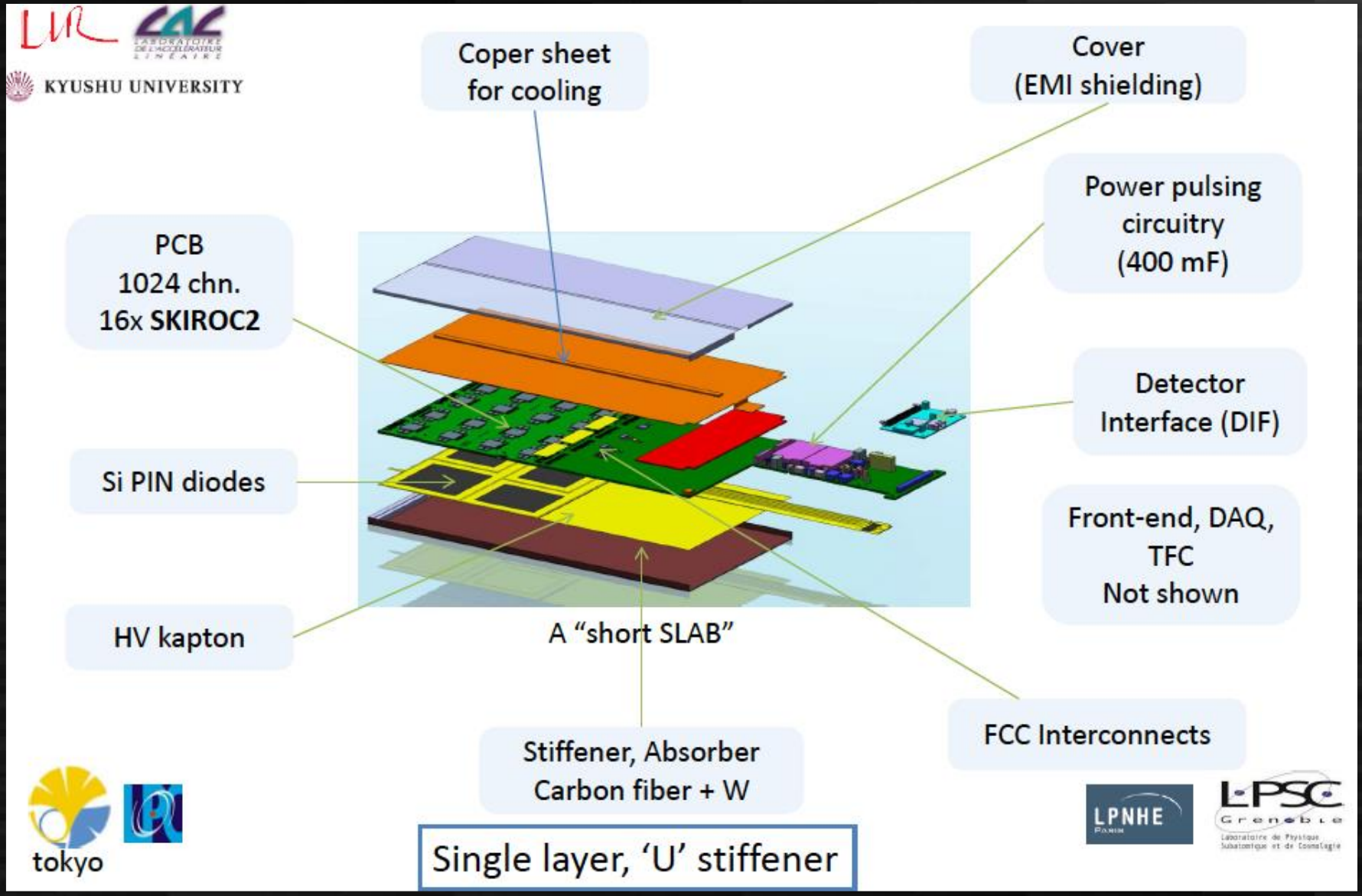
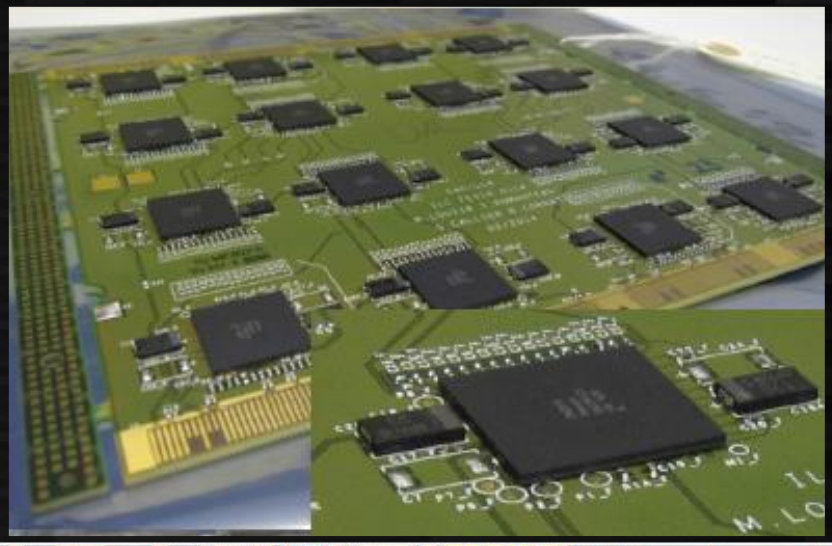
SKIROC2/2A study in Kyushu

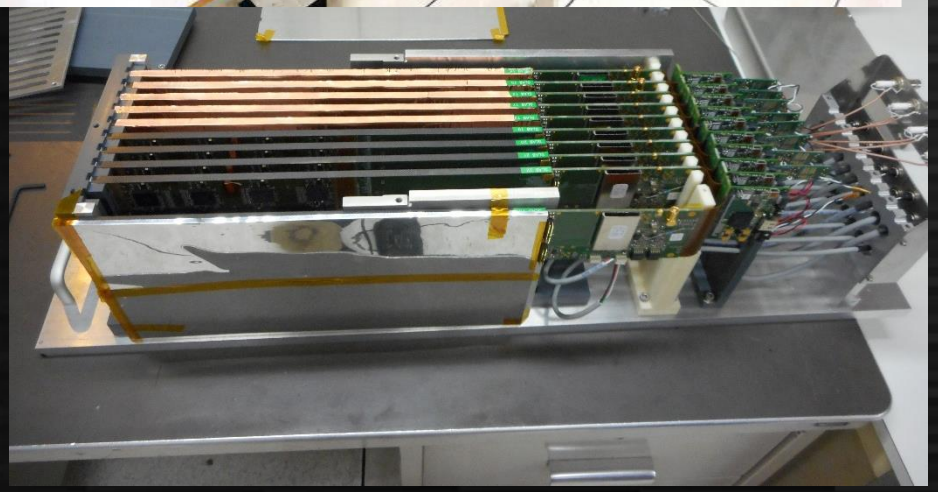
I. Sekiya, T. Suehara, T. Yoshioka, K. Kawagoe
(Kyushu University)
with support of Omega, LLR, ILD SiW-ECAL group

Detector module of ILD SiW-ECAL

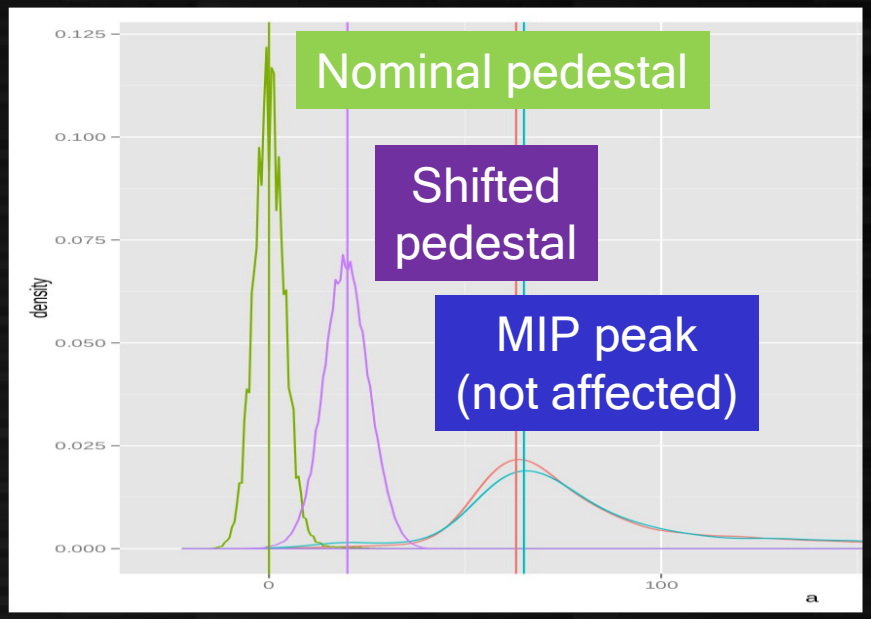


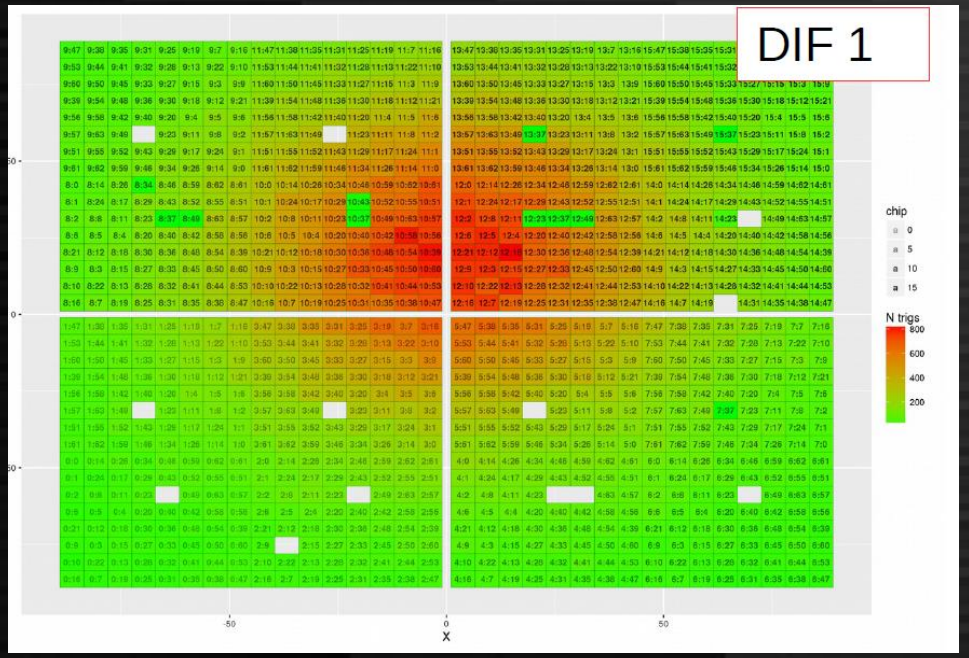
Slab in bench and testbeam





Issues in slabs of test beam





Pedestal shift at some condition occurred

Some fixed channel (37?) is always noisy

Investigation of dedicated setup may help

SKIROC2

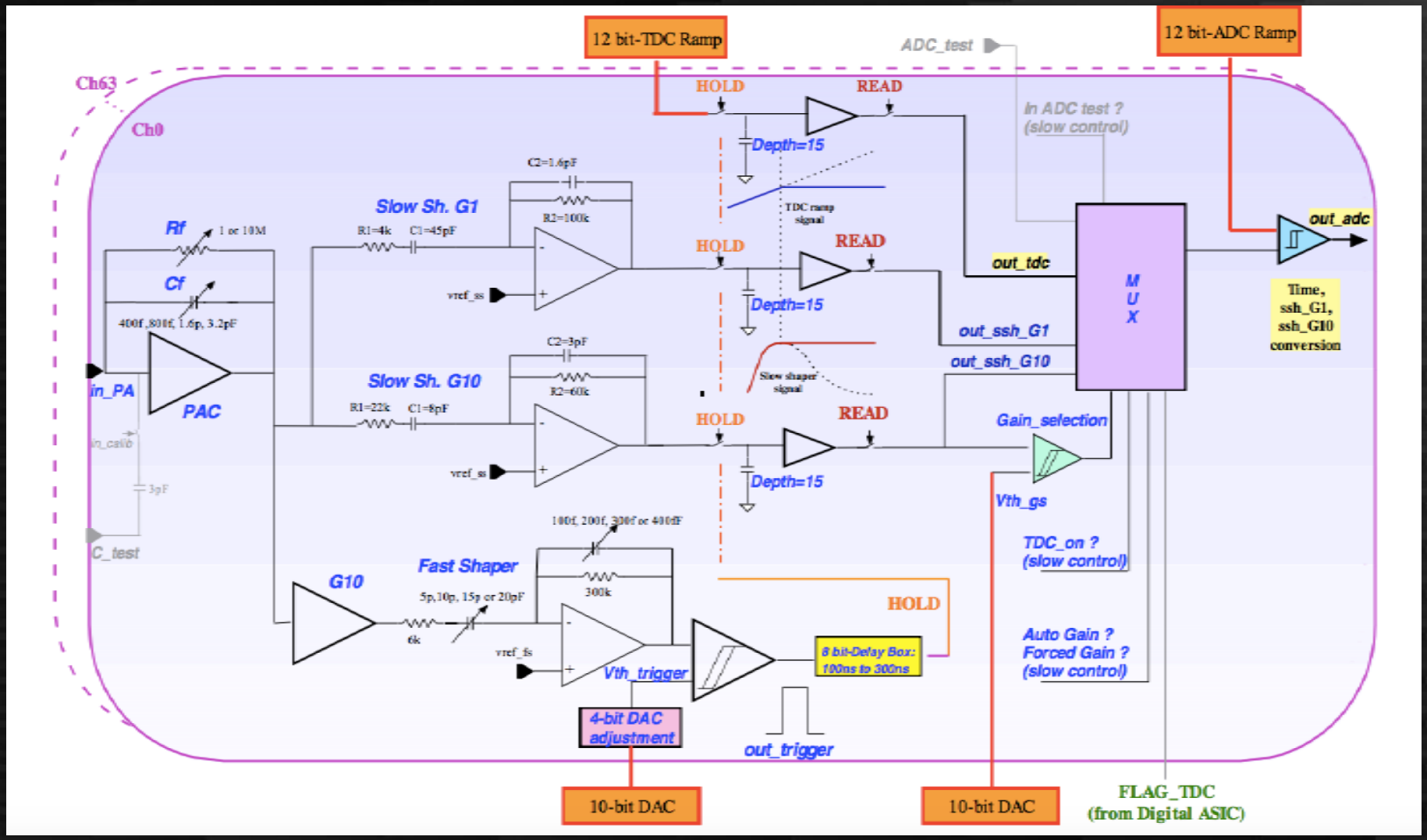


Diagram of analog part of SKIROC2

SKIROC2

SKIROC2 features

- 64 ch / chip
- 15 analog memories / ch
- 12 bit BX counting
- Two 12 bit ADC (G1 and G10)
- Internal trigger with DAC threshold adjust
- Power pulsing

Modification on SKIROC2A

- Threshold adjustment on individual channels
- TDC
- Auto gain selection
- External trigger

etc.

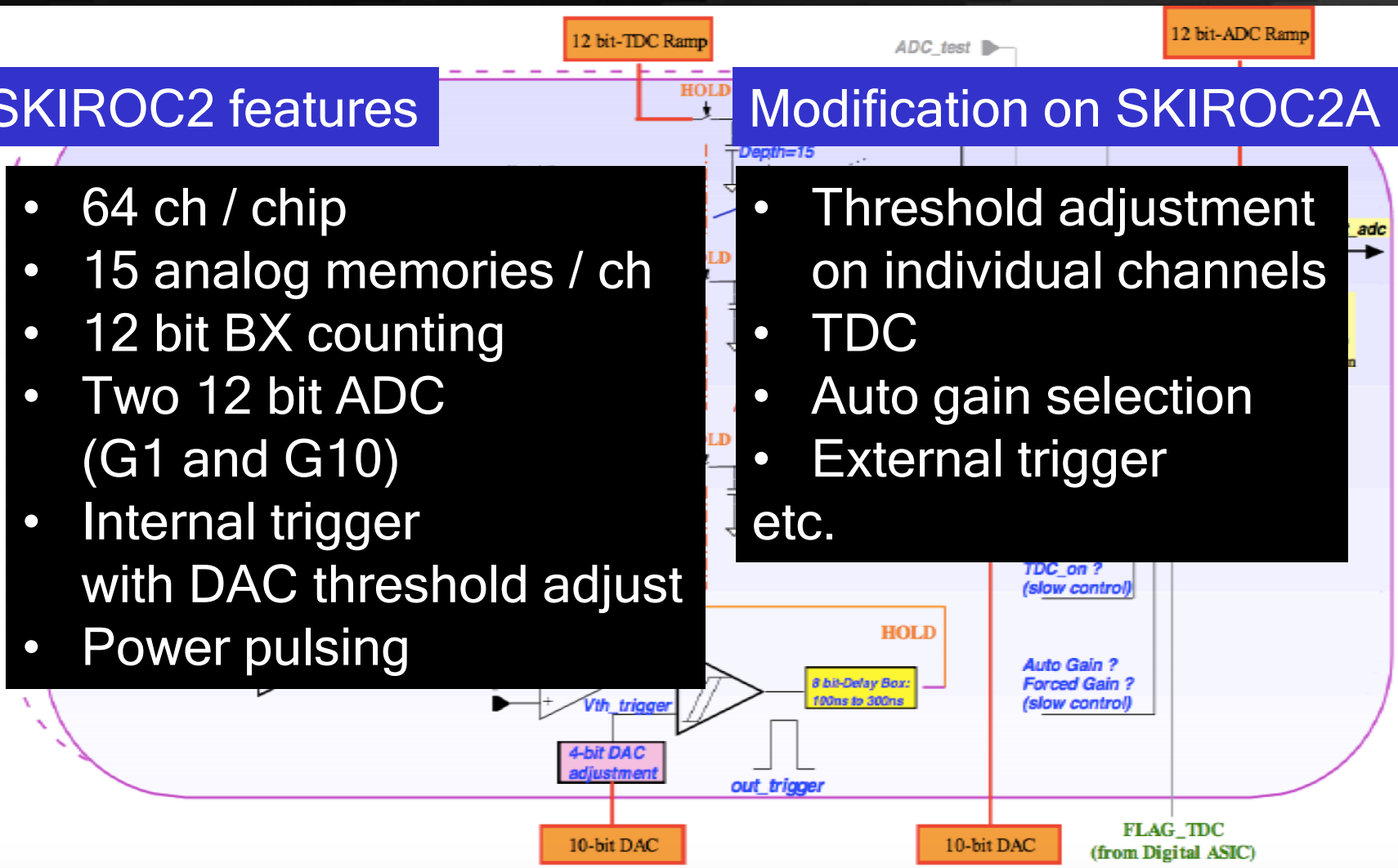


Diagram of analog part of SKIROC2

SKIROC2/2A testboard

With soldered SKIROC2A
(Thanks to OMEGA)

Analog probe

Slow clock in

Connector
for detector
connection

BGA400 socket
SKIROC2/2A

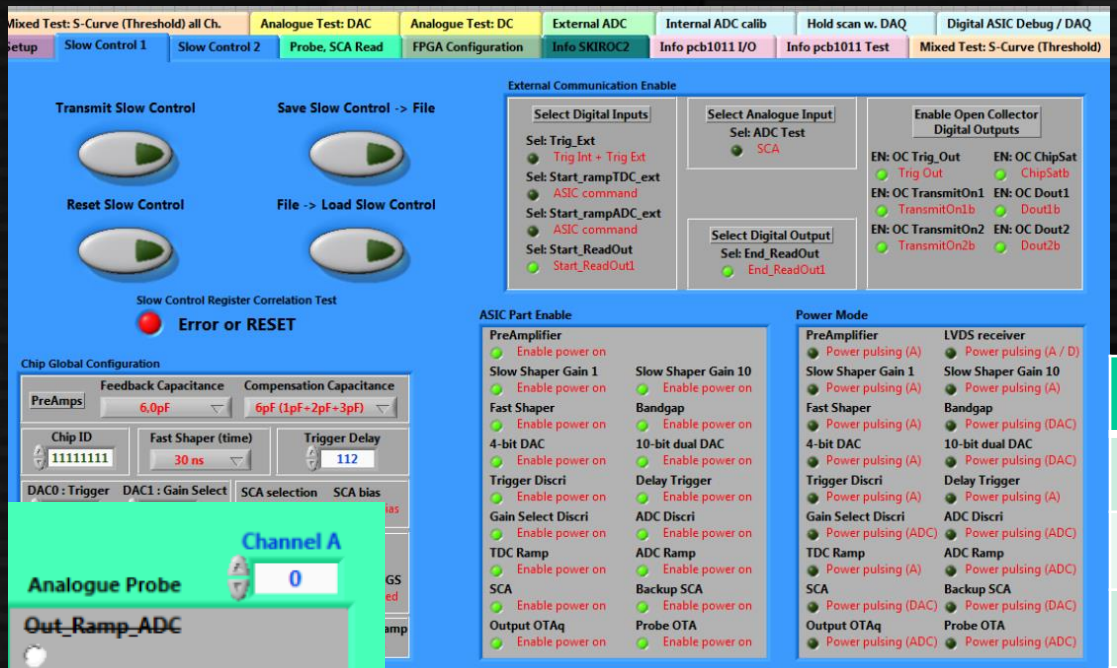
Control
PP/TDC etc.

Test pulse in

USB readout

DIF interface

Readout and DAQ



C++ DAQ (original)

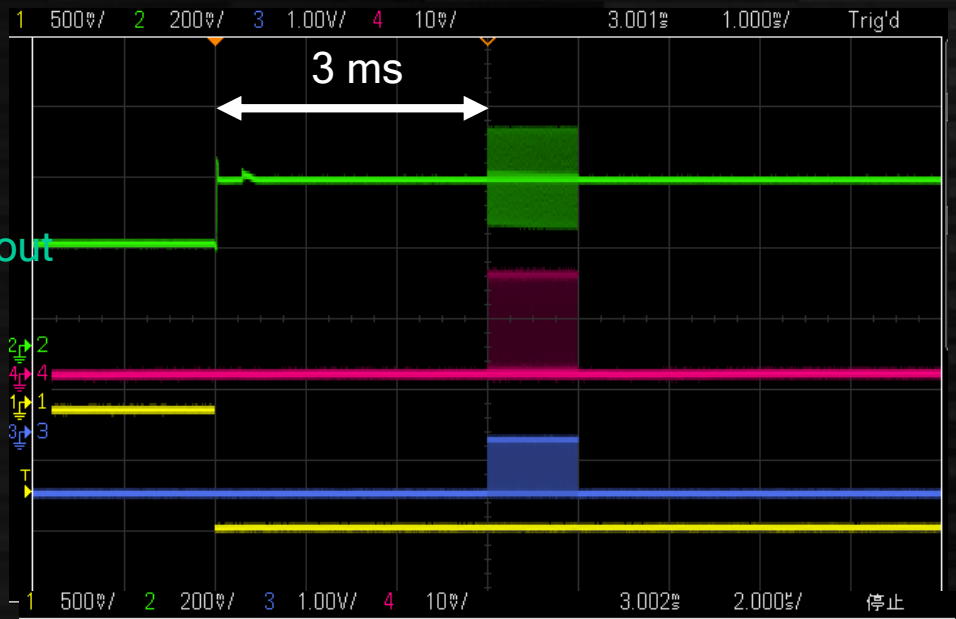
- Based on labview DAQ (snip of source diagram)
- DIF-compatible output (raw2root process-able)

Procedure		reg.	bit
ASIC reset	WC	1	2
Start acq.	W	2	0
(200 ms wait)			
Stop acq.	C	2	0
Start readout	WC	2	2
Wait readout	R	4	3
(wait till bit on)			
Obtain # bytes	R	13,14	
Obtain data	Rn	15	

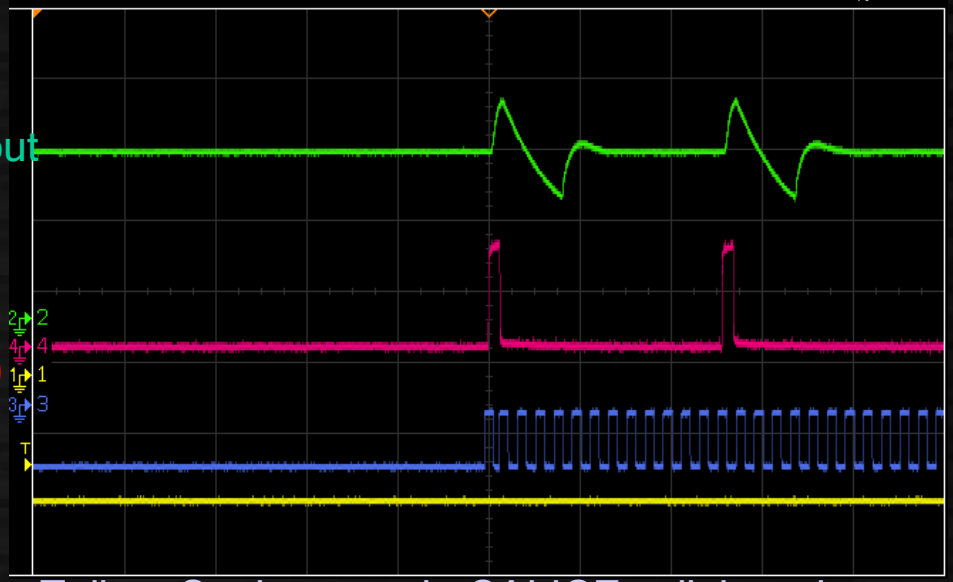
OMEGA labview software (ported to Linux)

- Initialization
- Slow control
- Analog probe

Power pulsing in testboard



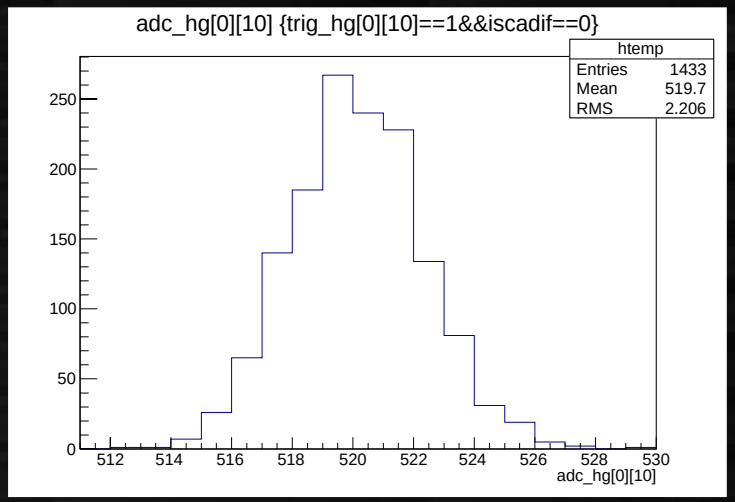
One of power lines can be controlled from outside (this time Analog is tested)

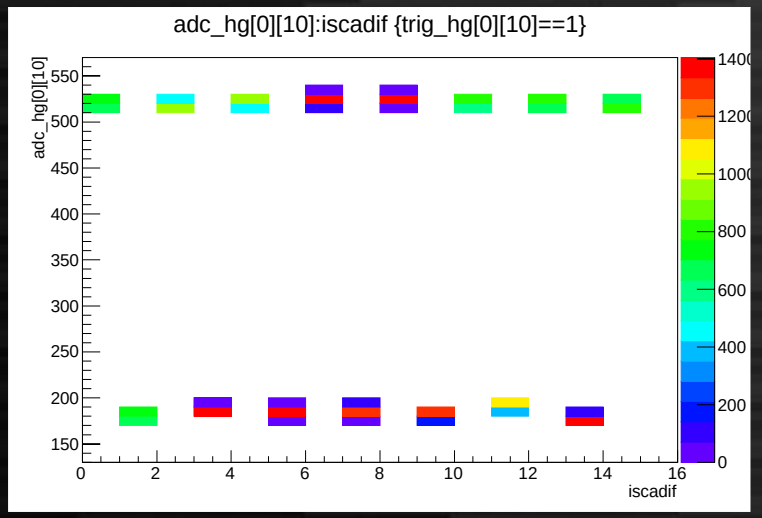


Slow clock is provided
Problem: readout also depends on the clock: slow down due to inactive 99.5% of time

Start of slow clock delayed several ms from power_on_a (Modification on testboard needed for quick recovery)

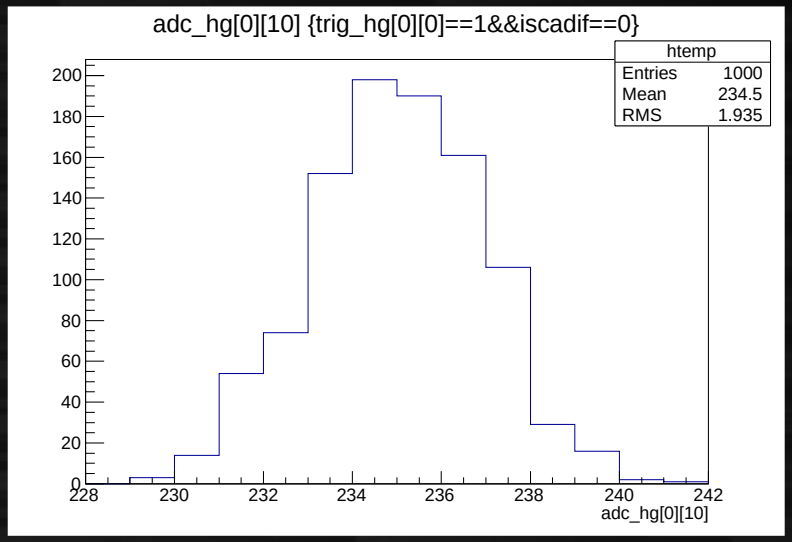
Data sample with 3 ms delay, 5 MIP

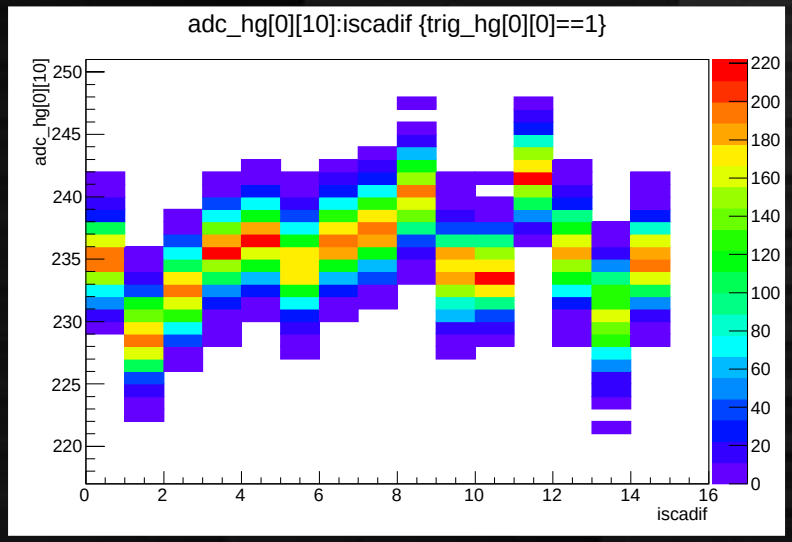




Signal with 5 MIP (memory = 0)

Signal vs memory





pedestal

Performance studies

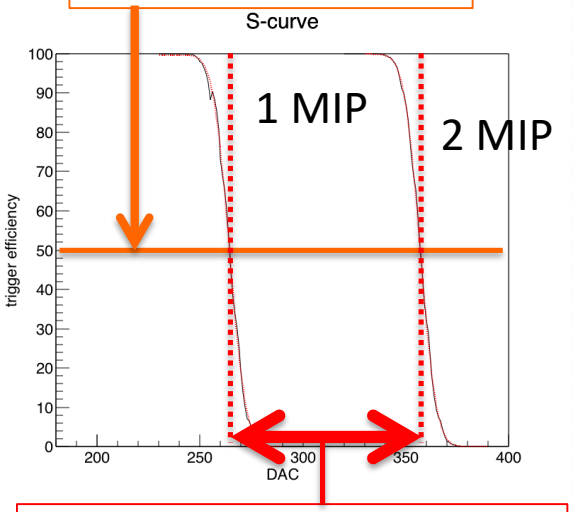
- Fast shaper (trigger S/N)
  - with various gain (feedback capacitance)
  - without power pulsing
- Slow shaper (ADC S/N)
  - Comparison with and without power pulsing
- TDC
  - First look of timing resolution

All studies are with test pulse, no detector connected

Fast shaper & triggering @SKIROC2,2A

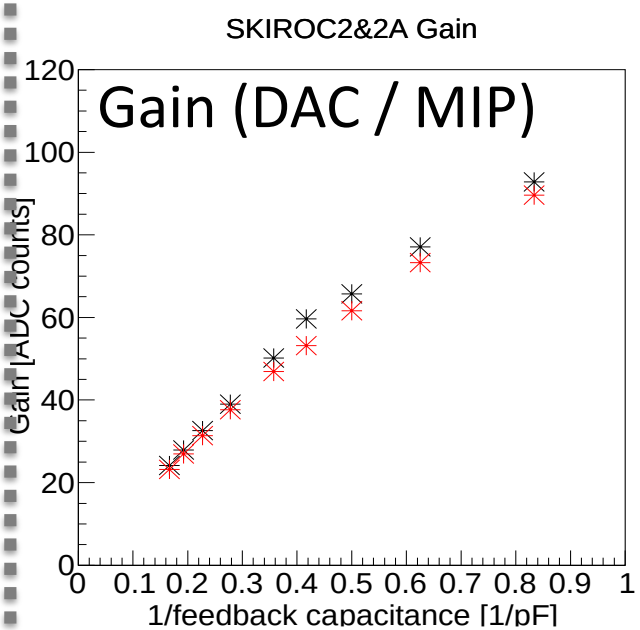
S-curve

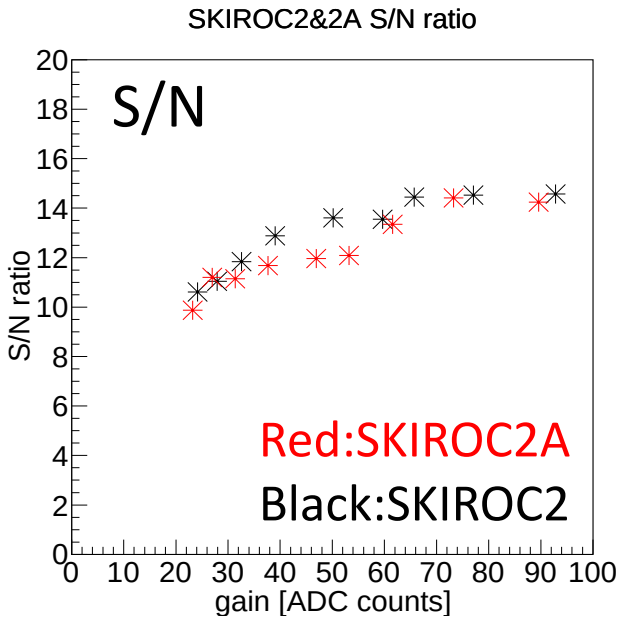
50 % efficiency



Gain : DAC count of 1-2 MIP (50% point)

- Test pulse in ch10
- Preamp of all ch active
- Trigger of all ch active
- Dependence on gain by feedback capacitance
- Socket version of testboard is used





S/N=13~14, no difference seen between SKIROC2/A

Fast shaper@SKIROC2,2A

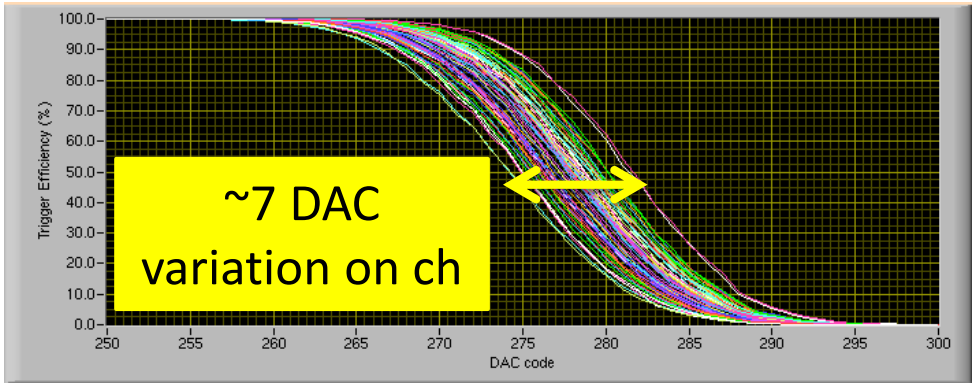
Soldered version (SKIROC2A)

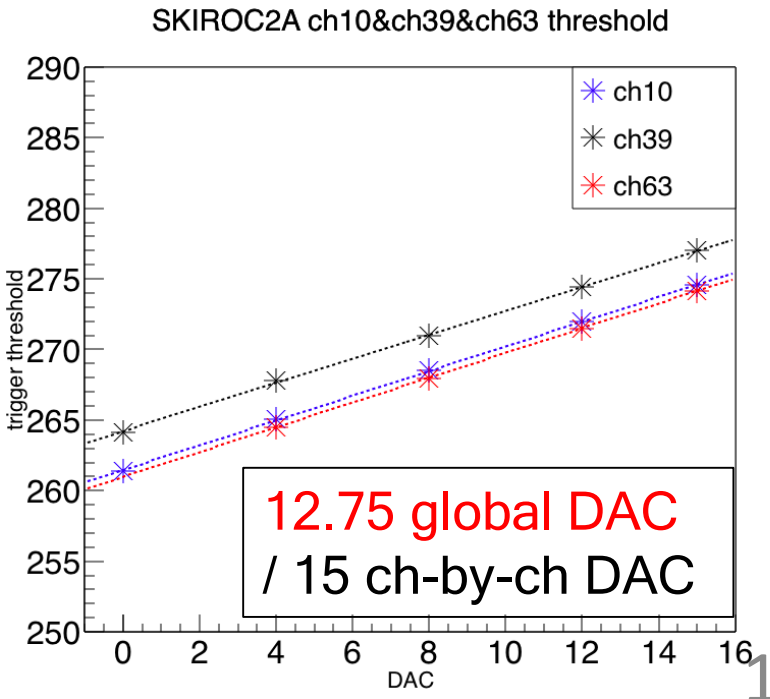
All 64ch s-curve @SKIROC2A

channel	Gain	width @ 1MIP	S/N
10	86.12	5.46	15.76
39	87.58	5.29	16.58
63	86.79	5.64	15.38

feedback capacitance: 1.2 pF
compensation capacitance: 6 pF

Slightly better than socket version
(result should be confirmed)





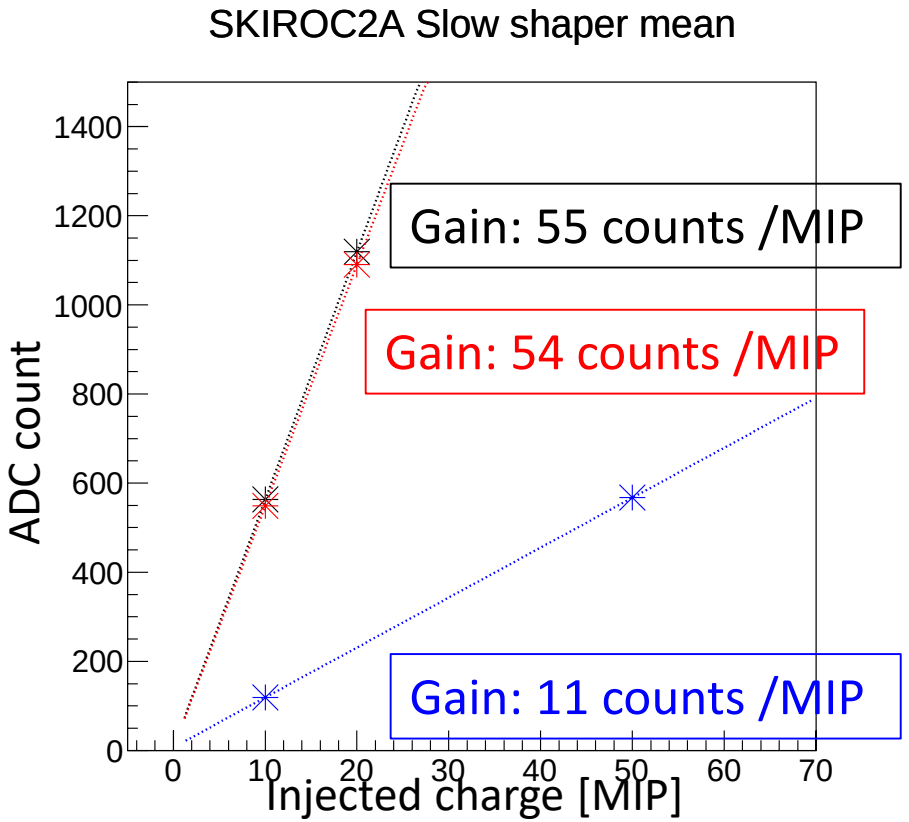
Individual trigger threshold
is checked: dynamic range of 13 DAC

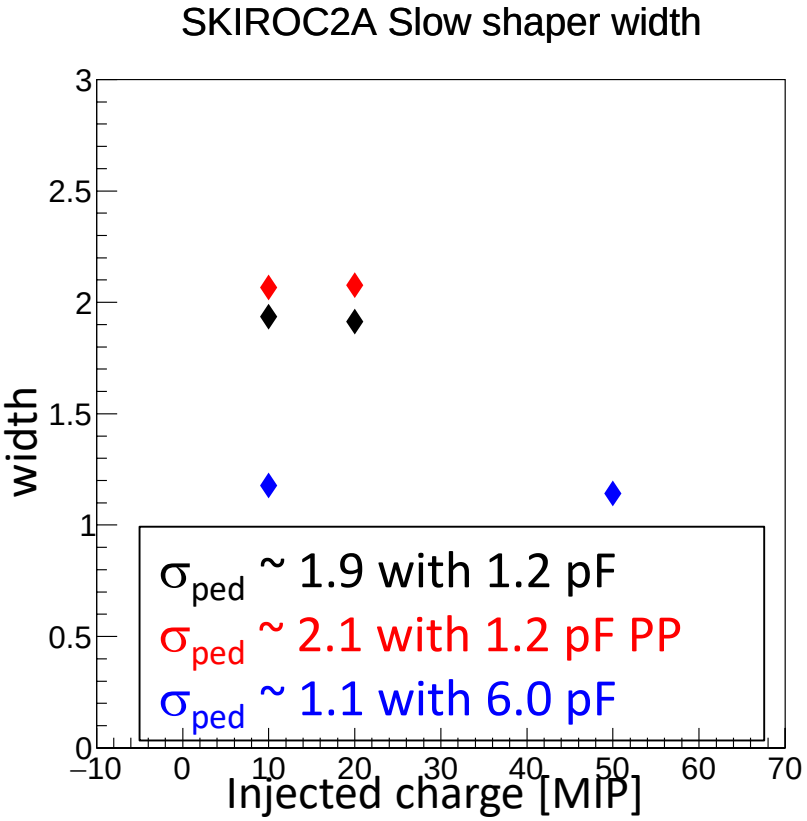
Slow shaper @ SKIROC2A

- Test pulse(100 kHz,1-100 MIP)
- power pulsing: 3 ms delay

Testboard 2

Black: 1.2 pF fb. cap.
Blue: 6.0 pF fb. cap.
Red: 1.2 pF fb. cap. with power pulsing

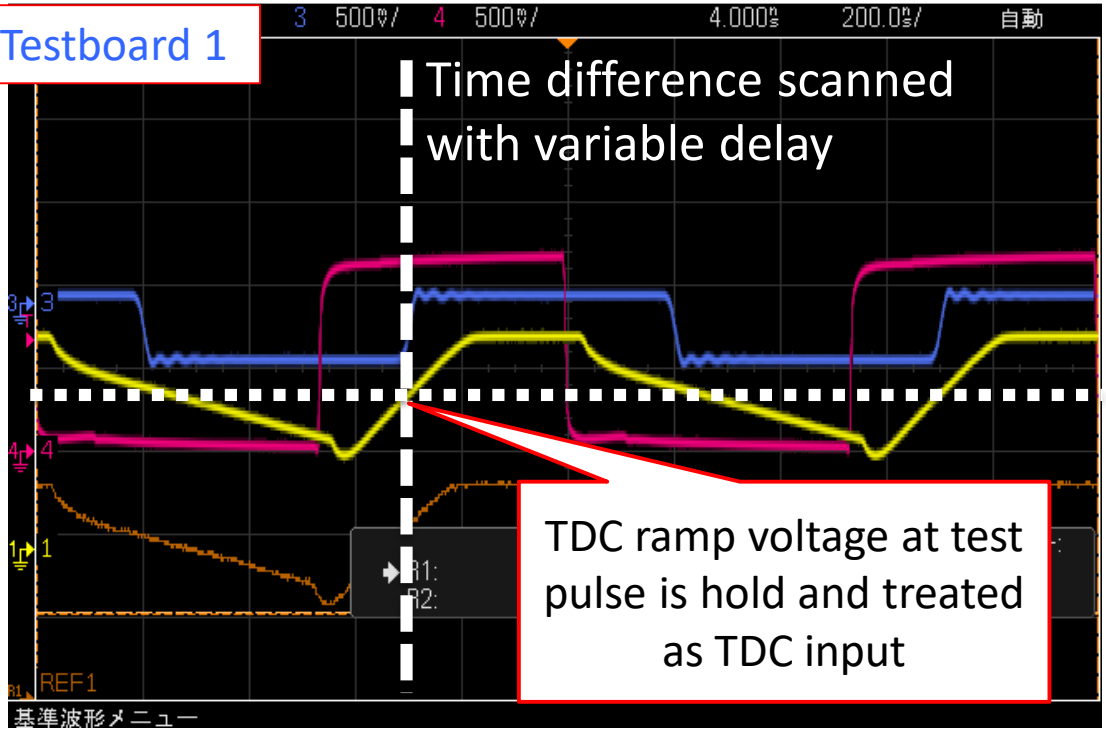




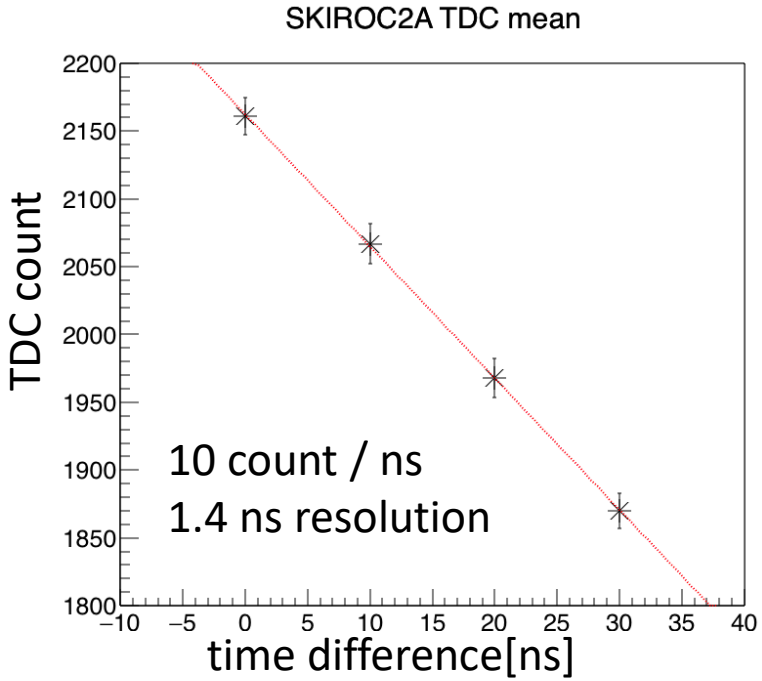
Gain ~ 55 counts / MIP, σ_{ped} ~ 1.9 , S/N ~ 29 with 1.2 pF
Gain ~ 54 counts / MIP, σ_{ped} ~ 2.1 , S/N ~ 26 with 1.2 pF
Gain ~ 11 counts / MIP, σ_{ped} ~ 1.1 , S/N ~ 10 with 6.0 pF

Time measurement with TDC on SKIROC2A

Testboard 1



feedback capacitance: 1.2pF
Compensation capacitance: 6.0pF



Blue: Test pulse
(1MHz,10MIP)
Red: Clock for TDC
(1MHz,1.0V)
Yellow: TDC ramp voltage

- 2.5MHz clock
- fast trigger: 30 ns shaping time

10 count / ns TDC slope
1.4 ns resolution @SKIROC2A

To do (short term)

- Power pulsing
  - Remove decoupling capacitors for fast recovery (effect of capacitors can be checked)
- Testbeam/FEV issues
  - Try to reproduce issues found in the FEV studies
- Statistics on performance
  - We have 10 SKIROC2 and 10 SKIROC2A
- Detector capacitance
- External Trigger, more study on TDC, etc.

Plans (longer term)

- Input to the FEV production/validation
  - What causes the current issues?
- A platform for quality control
  - For bare chip probing
  - For checking sensor quality (crosstalk etc.)
  - For checking packaging ASIC (if needed)
- A platform for sensor study
  - Various type (pad, strip, PSD, avalanche, …)
  - S/N ratio with sensor connection is the issue