Preparation of next beam tests:

setting up
the test benches at LAL

SiW-ECAL meeting

A. Irles, Orsay 21st Mars 2017

Outline

- LAL testbenches
  - Prototype (with LLR electronics and power rack)
  - Small testbench, currently with FEV8_cob (see next talk)
- Software roadplan: data quality
- Hardware roadplan (with beam test on the scope)
- Preliminary results with the prototype
  - Scurves
  - BCID issues
- Beam test:
  - Preparation
  - Schedule and organization.

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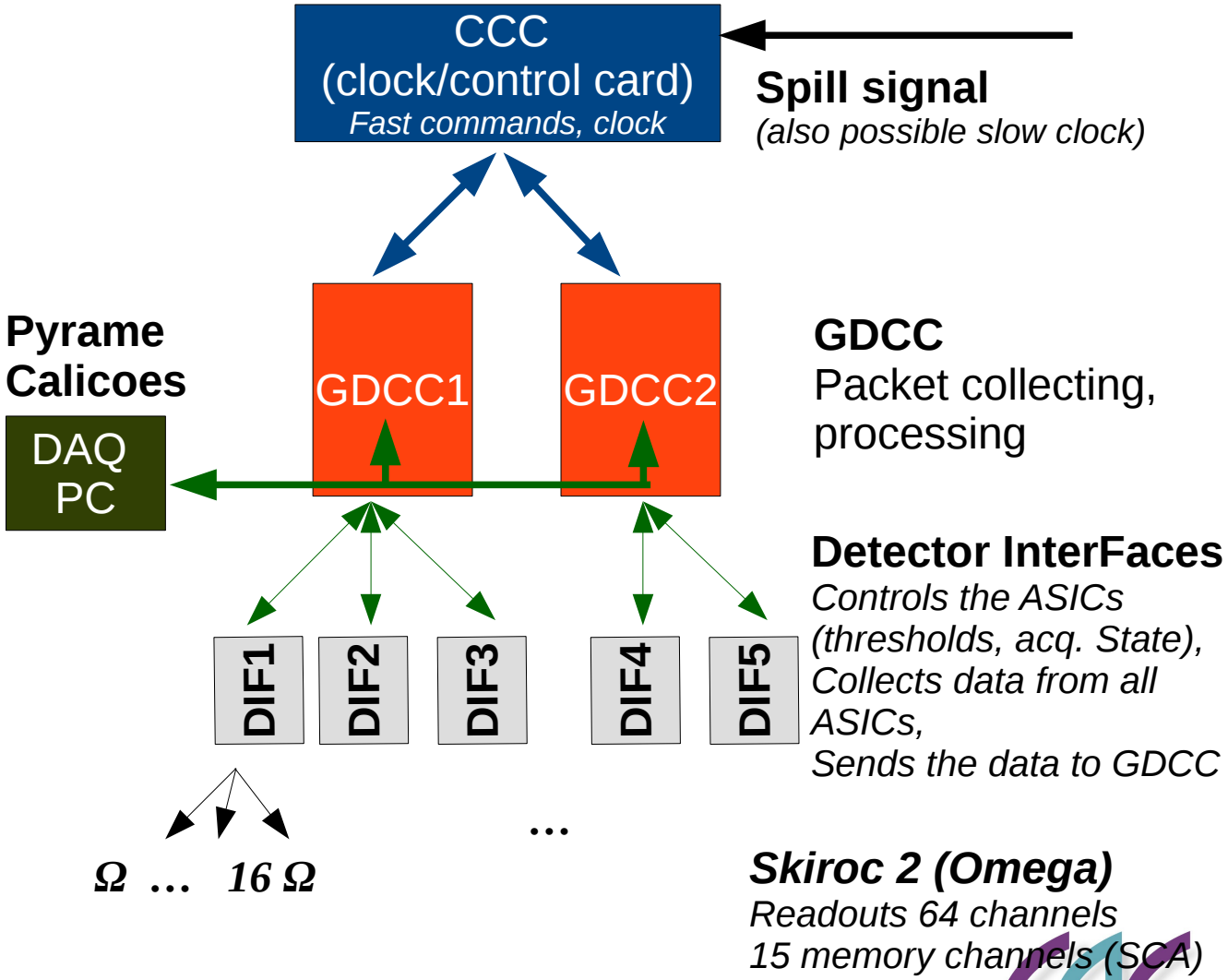
DAQ & electronic setup schematics



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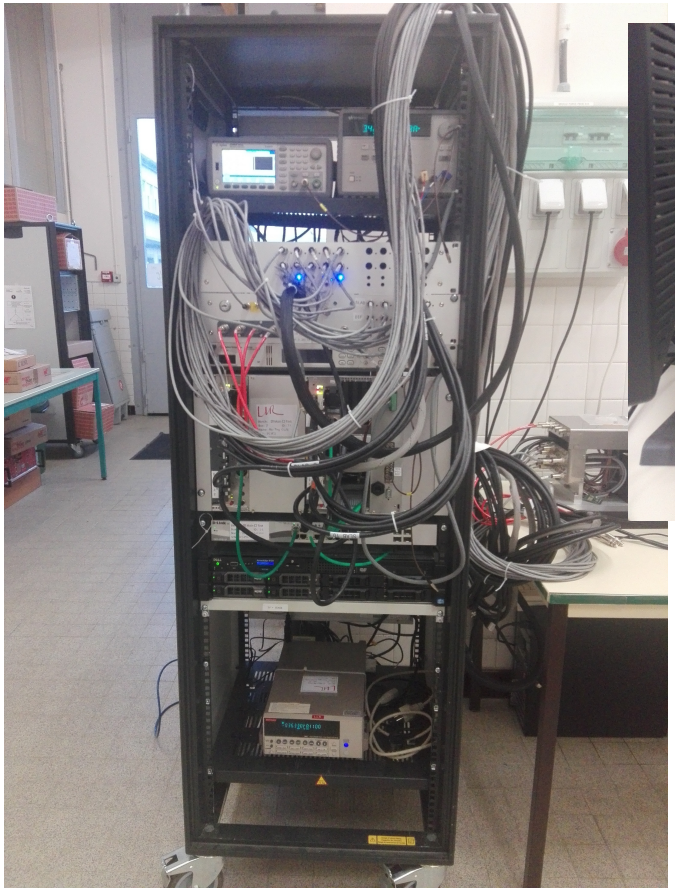
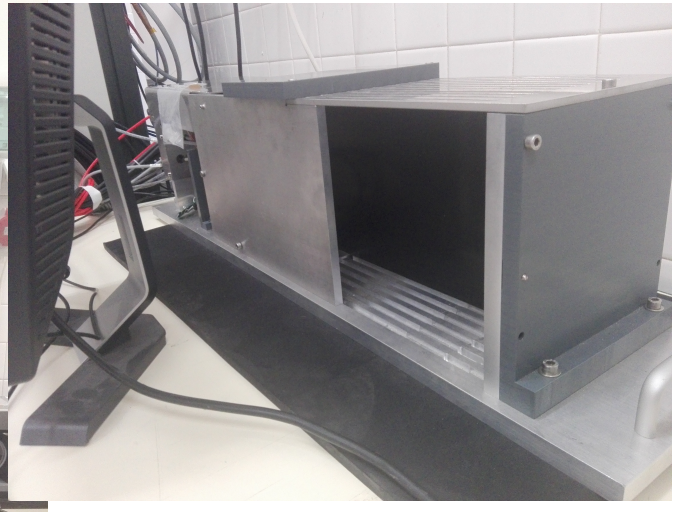
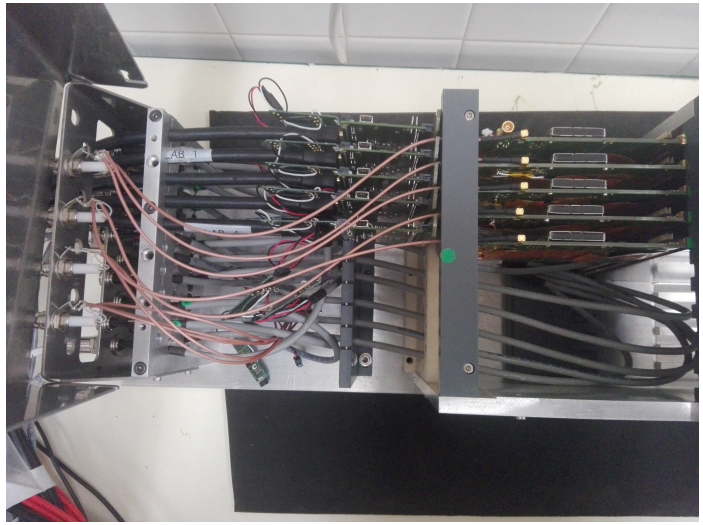
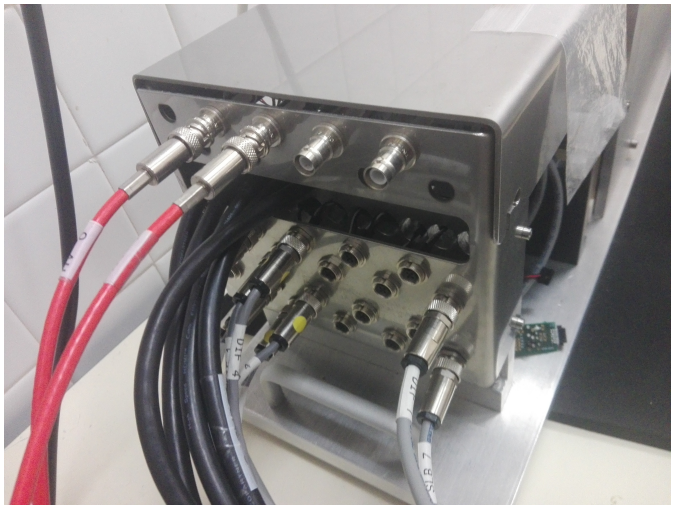
Testbench(es) 2017



LLR rack with all servers and electronics -->plug and play







Prototype equiped with **5 FEV10 modules** with 16 chips **(skiroc 2)**, 64 chn each = 5120 chn.

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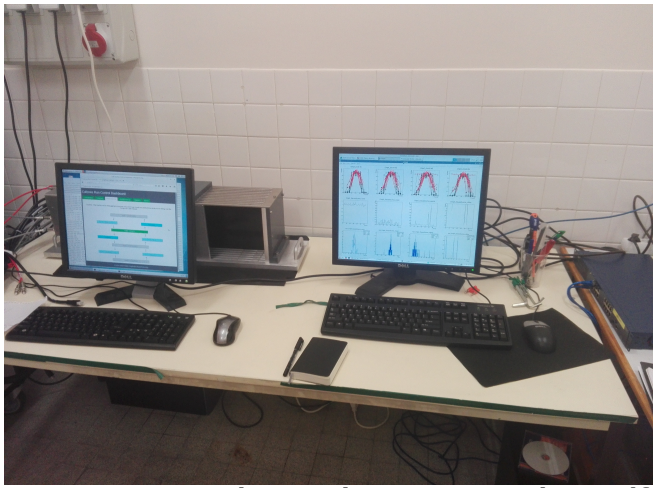
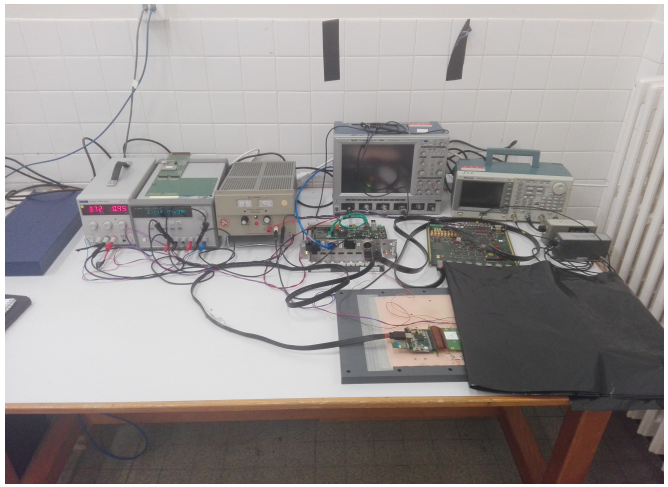
TestBench 2017





- Two testbenches together (from left to right)
  - Electronic rack for the prototype
  - Control PC of the proto
  - Prototype itself (5120 calorimeter cells behind a 15” screen)
  - Monitoring PC (used for both testbenches)
  - Testbench of single modules (FEV8)
- Weeks of work together with engineers from LAL, LLR and OMEGA

TestBench 2017 : next steps

- Set up the LAL rack
  - Power supplies, DAQ electronics, networking, etc
  - Didier Jehanno (Super KEKb) in close collaboration Remi Cornat
- Carefully test the new DAQ software and the prototype performance
  - First results already coming (we had already some very fruitful meetings at LAL and LLR)
  - **Workgroup created and progressing.**
- Hands on with Huisu Kim and Bokyeom Kim from Korea
  - See next talk.

Coming hardware changes/updates

- Sk2a replacing SK2 (see Artur's talk)
- New set of CCC from Mainz to replace the old ones.
- FEV12 and new wafers production/commisioning/integration

- All these items are ordered or under test/preparation → available after June testbeam
  - Not covered in this talk.

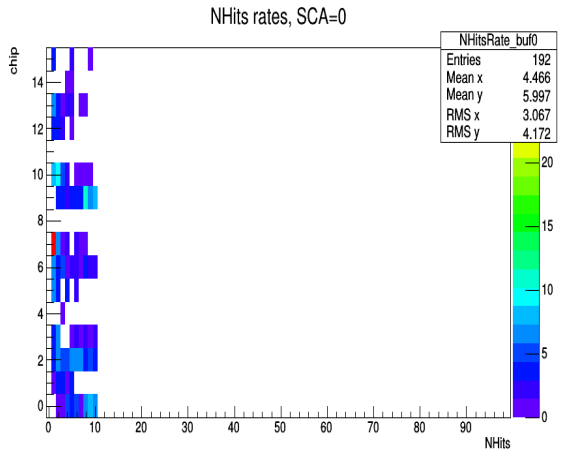
Data Quality: software

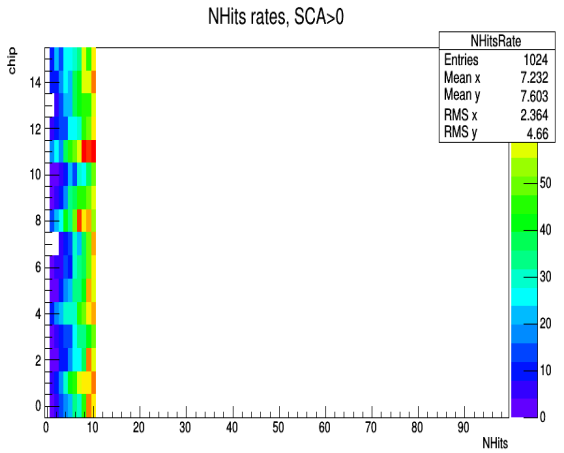
- I will work together with Frederic in the implementation of the online monitoring within CALICOES (DQM4HEP ?)
  - The facility is already there →work done during last test beam preparation.
  - Need small additions, testing and the development of the analysis methods.

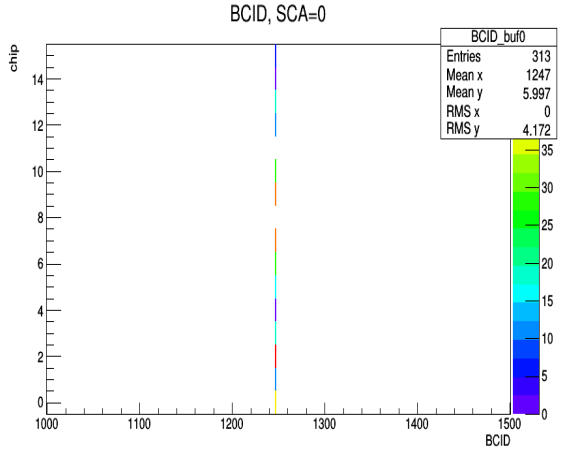
- For the moment we have a semionline Data Quality analysis framework that fulfills two functions:
  - Quick monitoring (chip and channel modules)
  - Quick analysis module manager: scurves, pedestal (ADC) extraction, MIP fit with pedestal subtraction, etc.
- It is under development: temporary repository https://github.com/airqui/tpecal/
- Uses root files as input. Nothing else is needed (calicoes, pyrame, etc).
  - Scriptable and exportable.
  - Feedback from V. Balagura (monitoring tool writen in R)

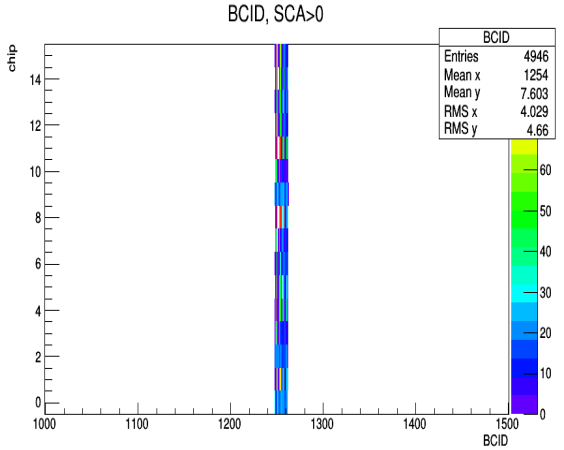
Preliminary results (I): Data Quality plots

- Data taken at LAL with the prototype.
  - Noise run, with low fast shaper threshold value (DAC = 190)
  - FEV10, SK2.
  - HV = on
- Plots for one ASIC
  - Nhits (SCA=0 and SCA>0)
  - BCID (SCA=0 and SCA>0). As the threshold is quite low, the BCIDs are ~ val_evt BCID.









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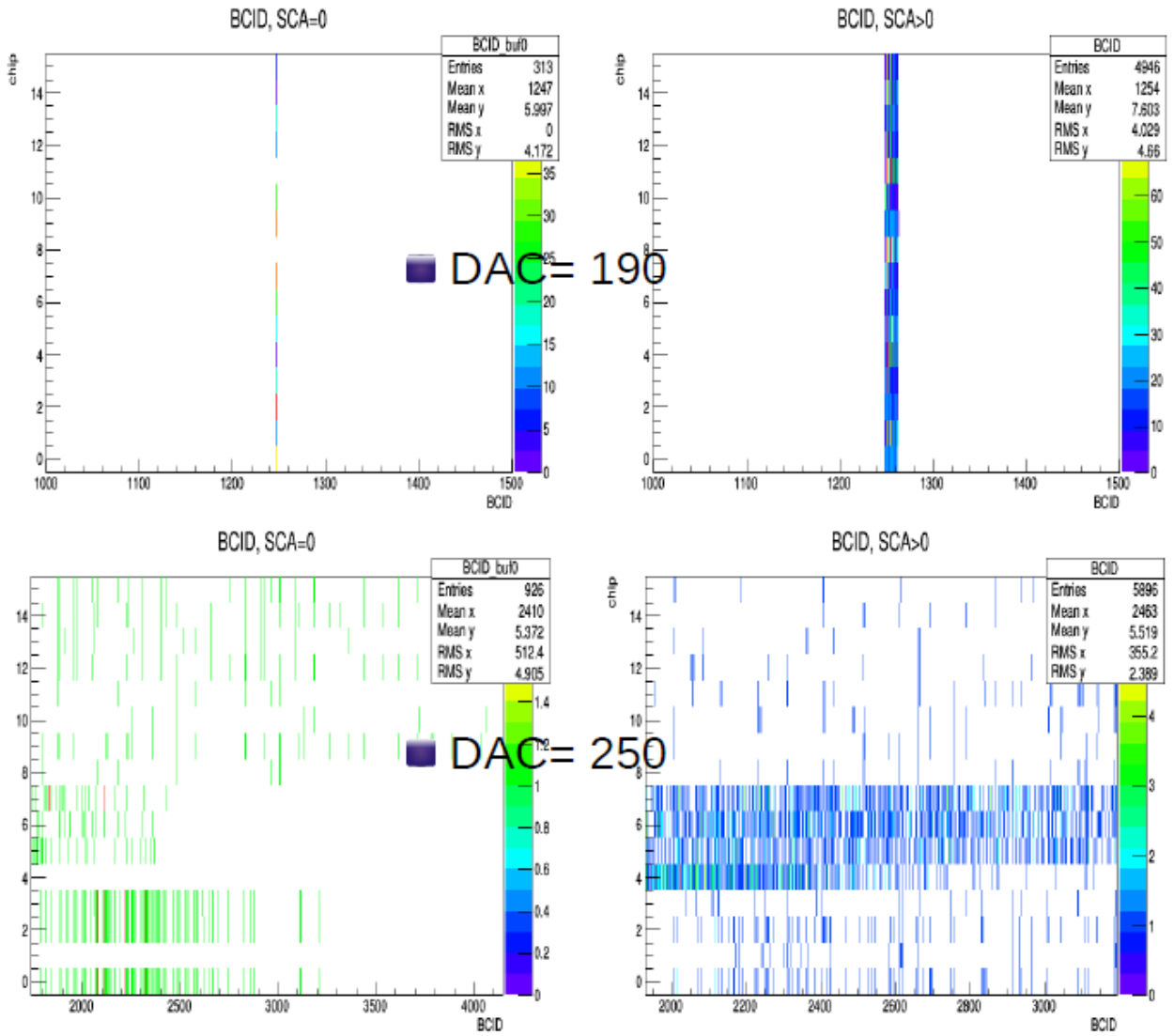
Preliminary results (I): Data Quality plots

- Comparison of same plots for low and high threshold values.
- Some features are observed in the BCID values:
  - Repetitive patterns for group of chips that trigger all at the same time.

    → First tests with HV off make the patterns dissapear.
  - BCID values larger that spill (in principle, maximum BCID should be 2500 in these runs) → **under investigation.**



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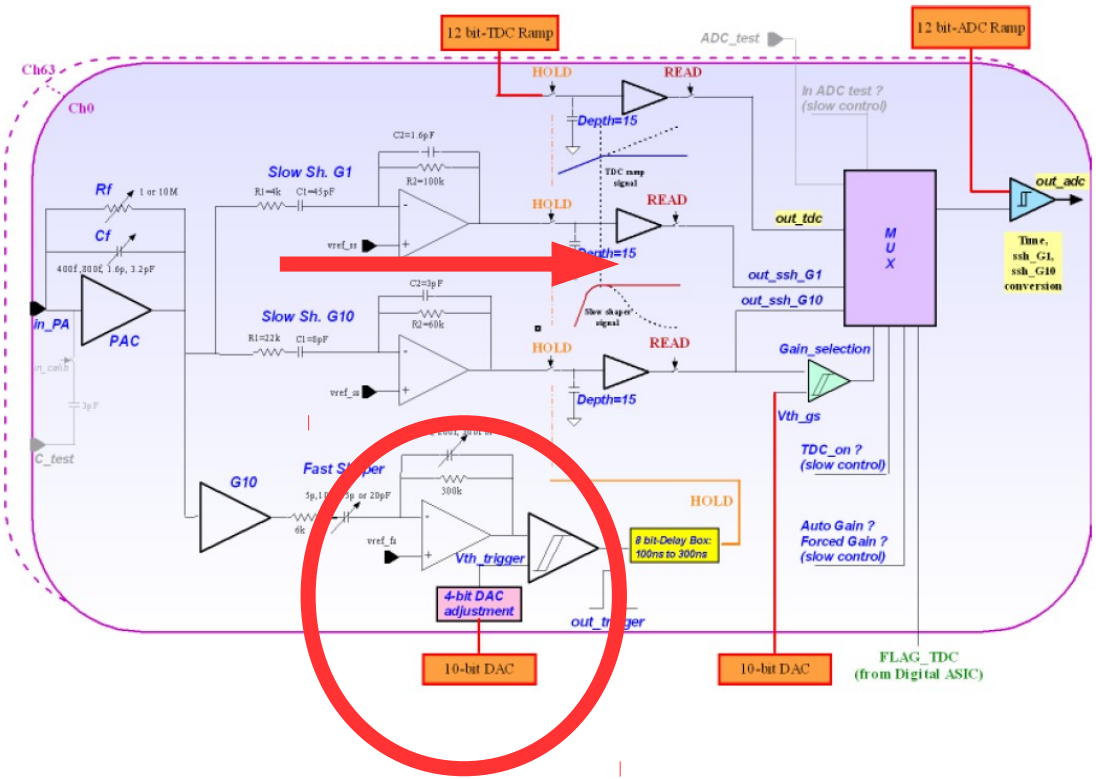
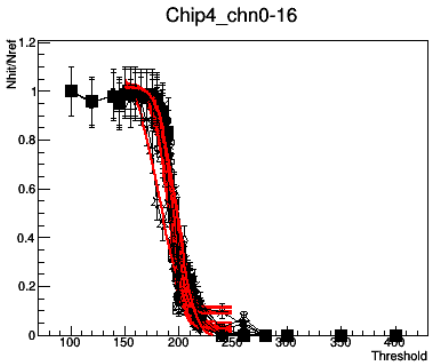
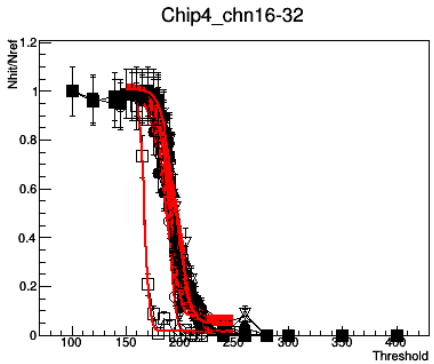
Preliminary results (II): noise threshold scans or scurves

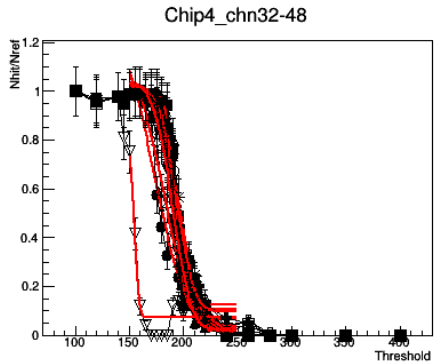


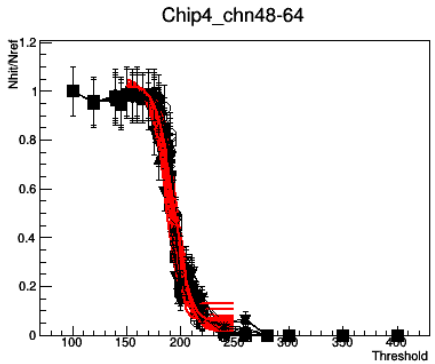
- Establish the pedestal of the fast shaper threshold (DAC)
- Scurves with DAQ
  - Make a scan varying the threshold values.
  - Count number of hits per channel (hit bit == 1)
  - Count SCA = 0 or all (two different approaches with similar results)
- Data taken for all 5 DIFs

Preliminary results (I): noise threshold scans or scurves

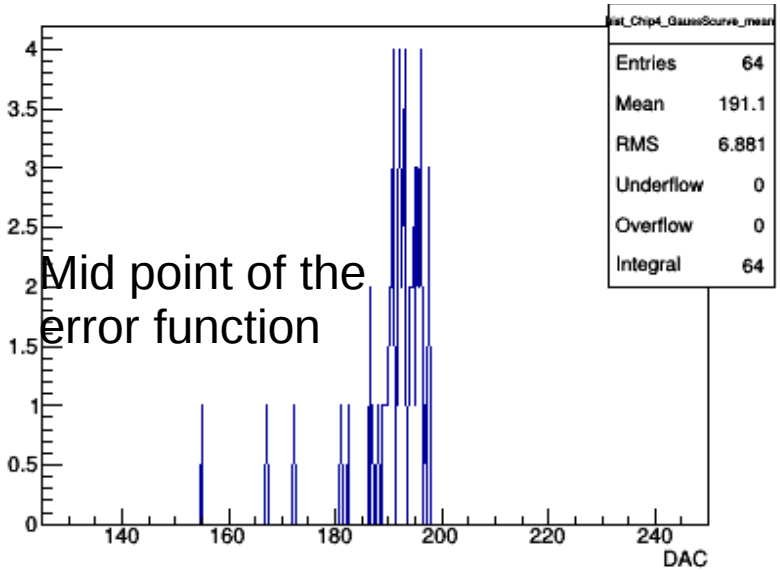


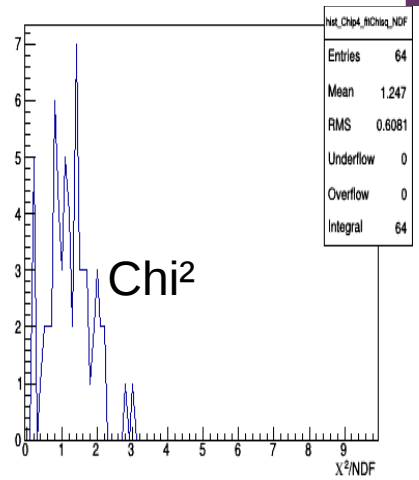






- DIF 1, chip 4 (representative result)
  - All channels enabled at the same time.
  - High gain preamp.
  - Threshold value (DAC) scan.
- Plot hits vs DAC for SCA = 0
- Fit 1-error_func to data
  - Threshold mean = 191.1±6.8 DAC





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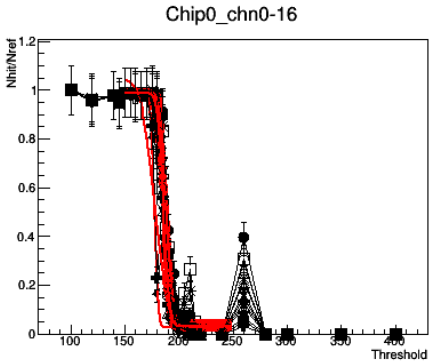
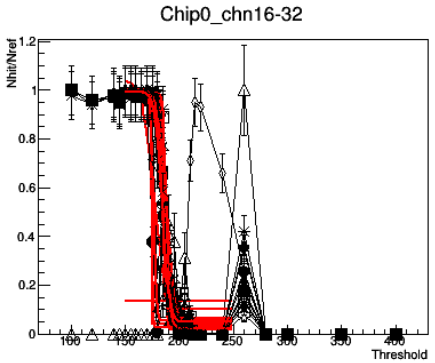
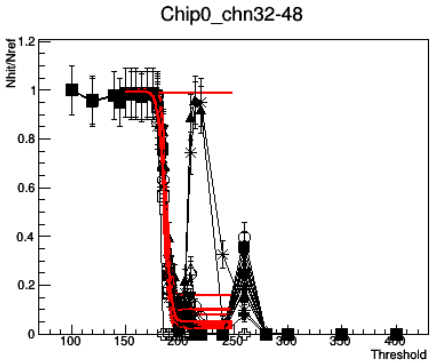
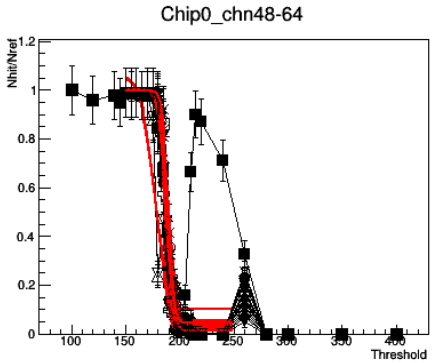
Preliminary results (I): noise threshold scans or scurves









- Chip 0, same DIF.
- Noise ?
- Observed in other chips → more detailed studies needed

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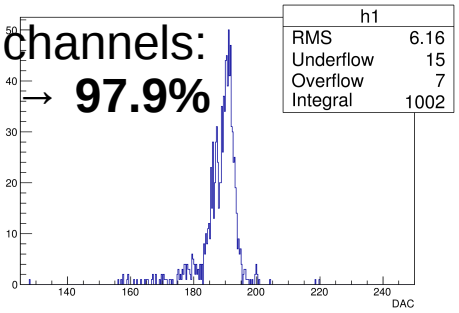
Preliminary results (II): noise threshold scans or scurves

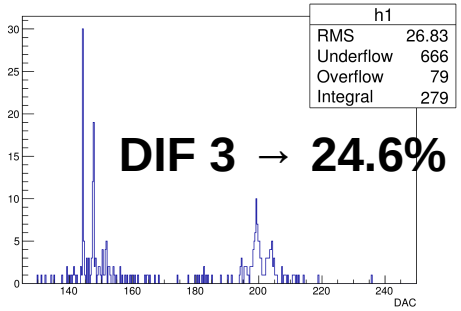
- Summary plots of optimal threshold fit for all DIFs

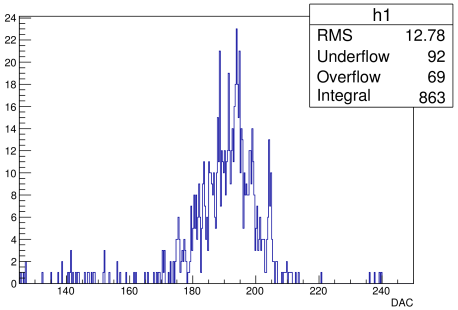
Fitted channels:

DIF 1 → 97.9%



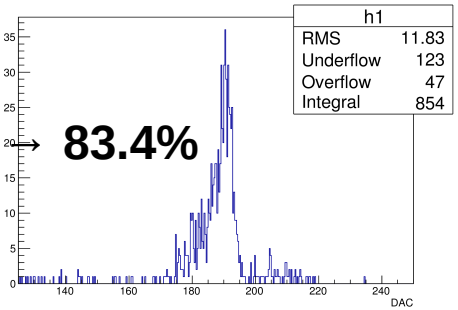
DIF 3 → 24.6%



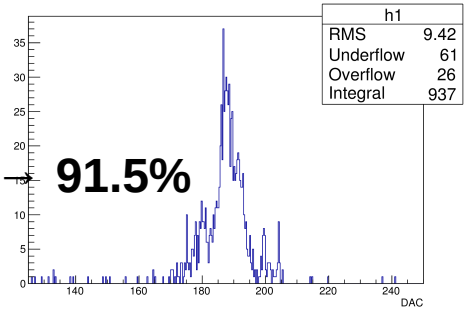


DIF5 → 84.3%

DIF 2 → 83.4%



DIF 4 → 91.5%



- Preliminary results not optimized analysis or results checked carefully but … **promising**.

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Towards test beam

- **Still preliminary and non conclusive results but...**
- **The tests and debugging has now really started at many fronts.**
  - I will focus on the prototype and DQM
  - Artur & Shriddha, sk2a and various testbenches at LLR.

- We have started a weekly meeting (“TB2017 task force”)
  - Frequency to be reduced eventually → we are creating the momentum!
  - Agenda Linear Collider (is this the right place for such kind of very technical meetings?)
  - https://agenda.linearcollider.org/category/155/

Towards test beam

- Roadplan:
  - Understanding of the BCID issue
  - S-Curves or FindNoisy to define a first set of trigger thresholds
  - Test and improve the setup with cosmics runs
  - Integration of the other 5 layers into the stack

Beam Test Schedule

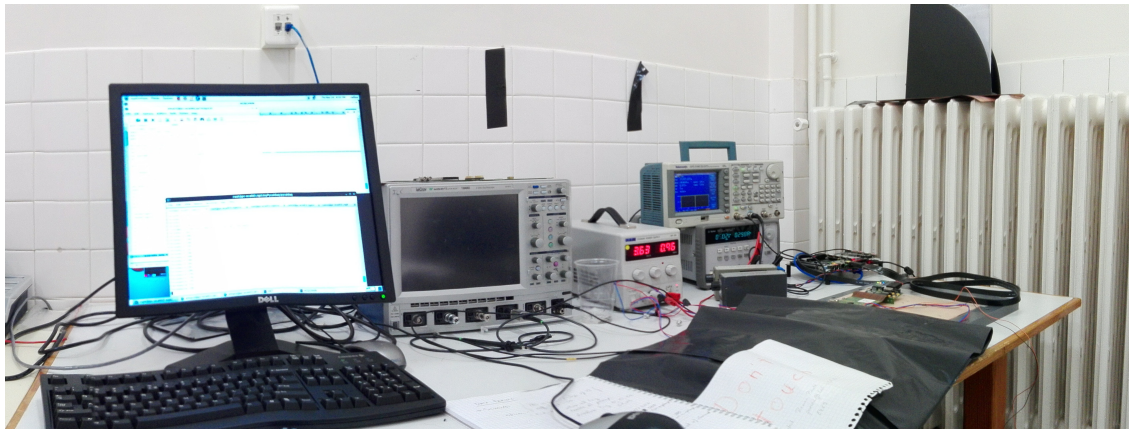
- We have booked two weeks at DESY, TB24/1
  - 12-25 June
  - http://particle-physics.desy.de/sites/site_particlephysics/content/e252106/e261123/infoboxContent275972/Testbeam_schedule2017v9_ger.pdf
- CERN beam test in September with SDHCAL ?
- Beam test readiness meeting by mid April ?
  - invite external reviewers as e.g. the Chair of the CALICE TB

Backup

Test bench, 2016

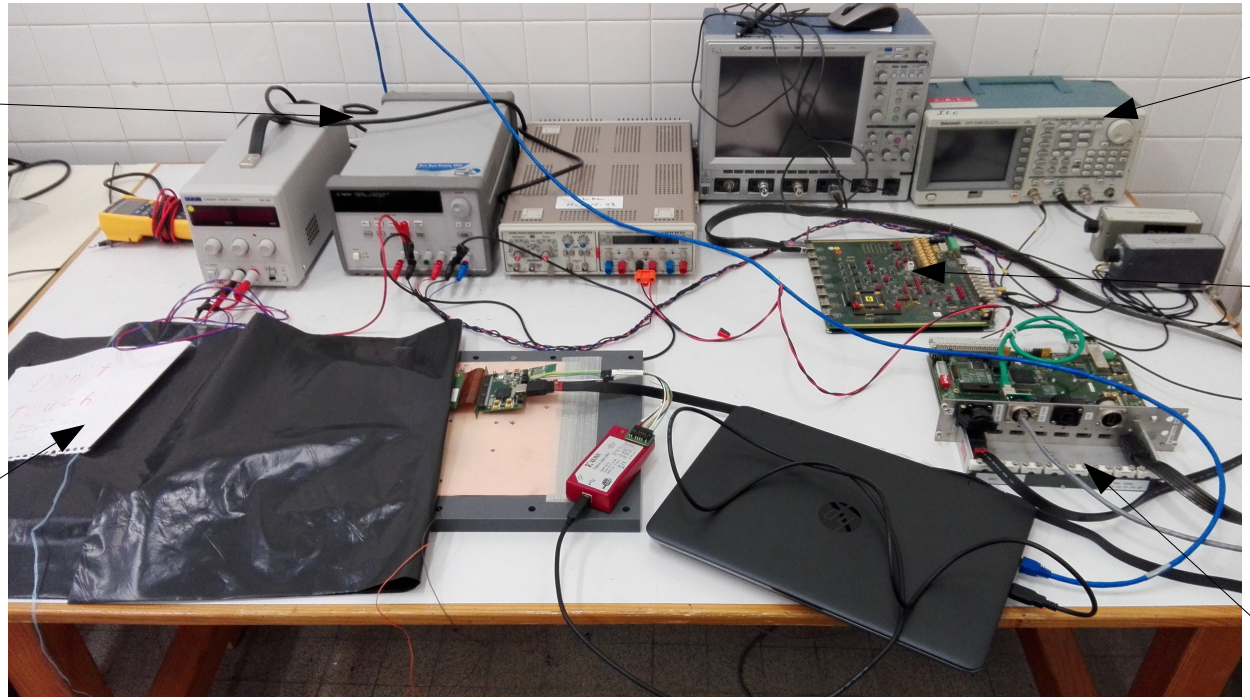
- FEV8_COB module (only one)
  - 8 chips
- DAQ:
  - “old” LDA (link data agregator)
  - Outdated DAQ software

    (calicoes 2.1-2)
- Main issues:
  - Intermitent usage → testbench not maintained



Test bench, 2016

Power supplies



Spill signal generator

CCC: Control clock card

Hardware under test

→ with high tech cover

GDCC → data concentrator

PC Connected To the GDCC

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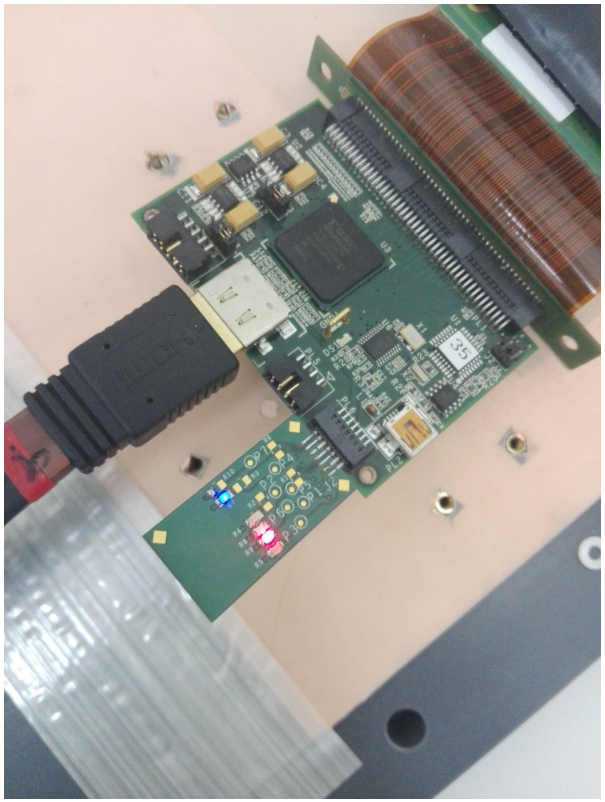
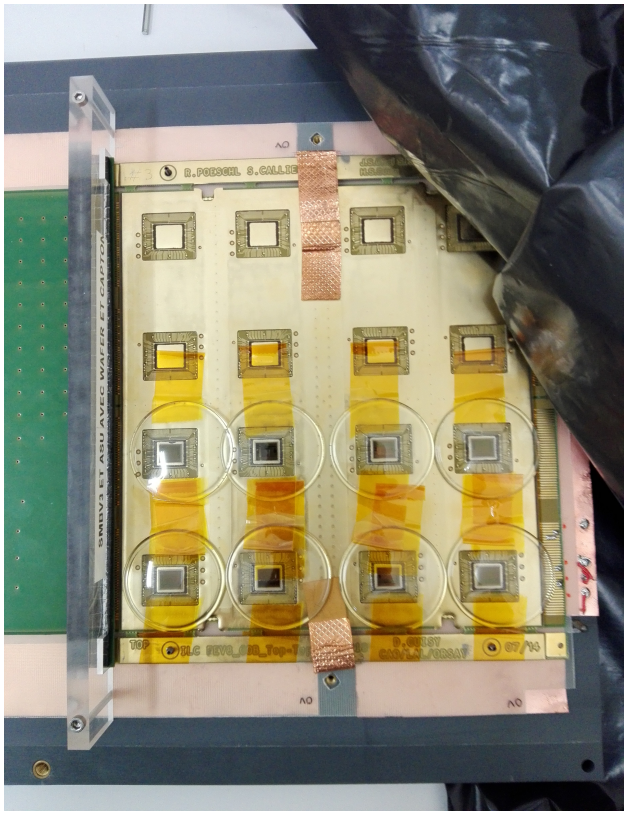
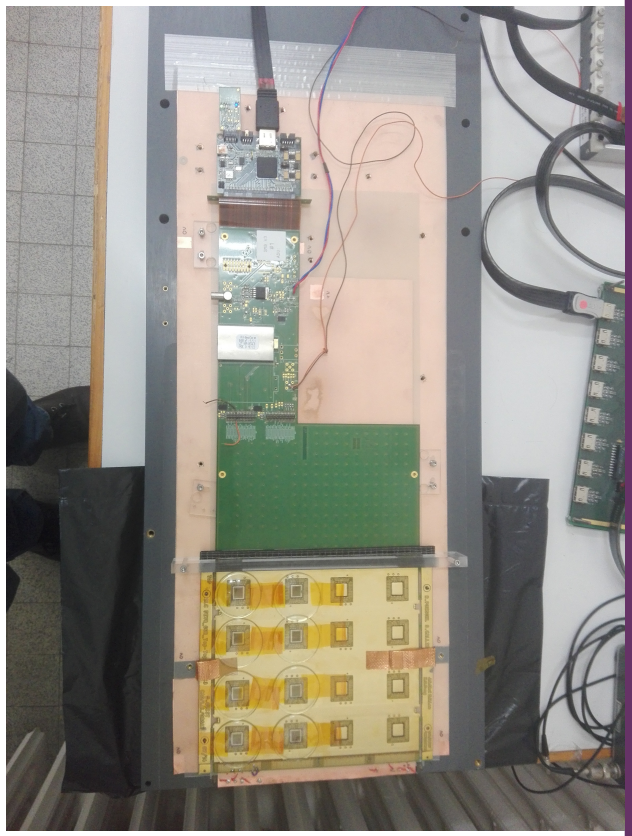
Test bench, 2016



DIF: Detector card interface.
Sends configuration and control commands to the chips and gets the data of the chips and send tehm to the data concentrator.



FEV8_COB
Module with the chips and (in general) Si wafers



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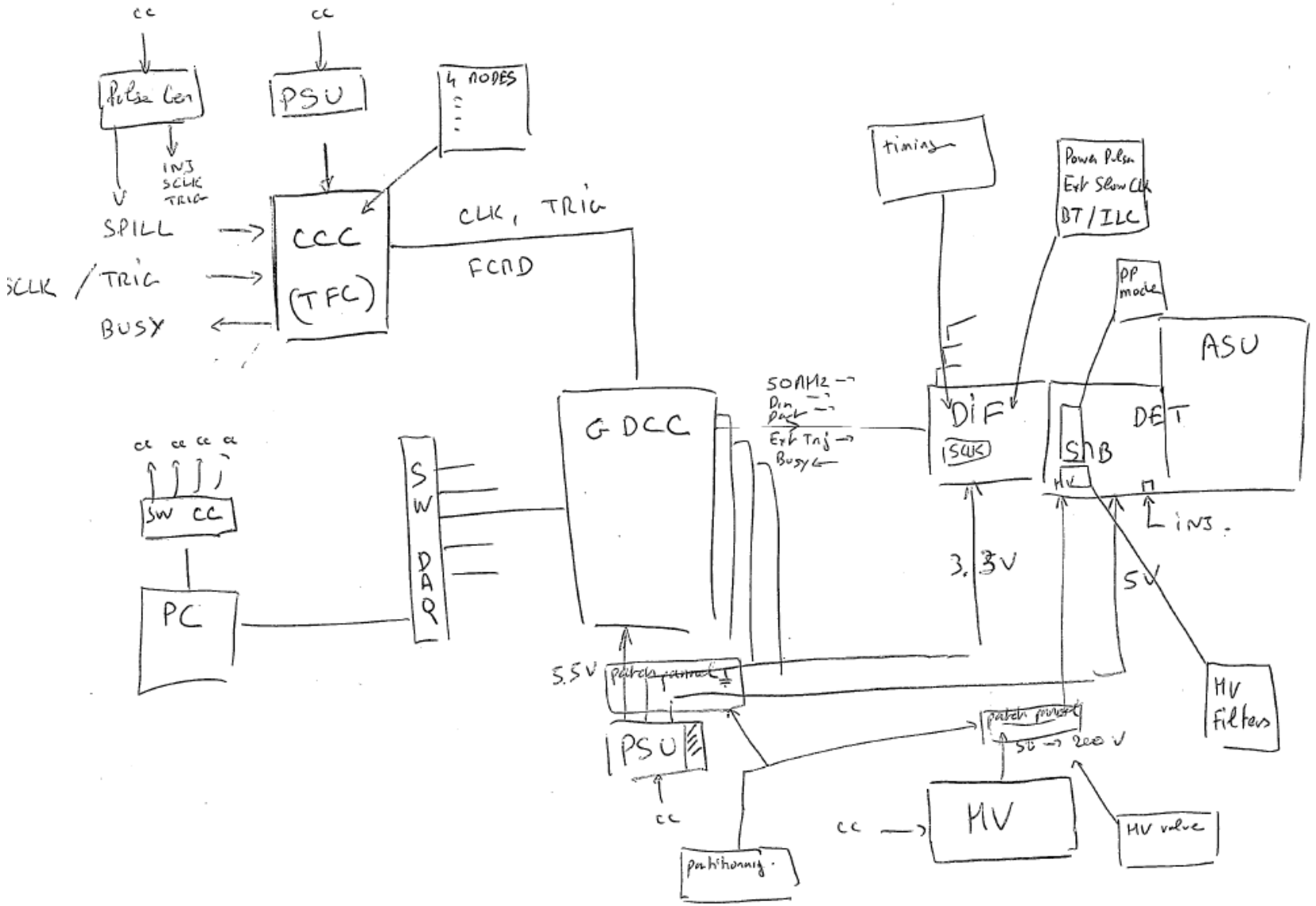

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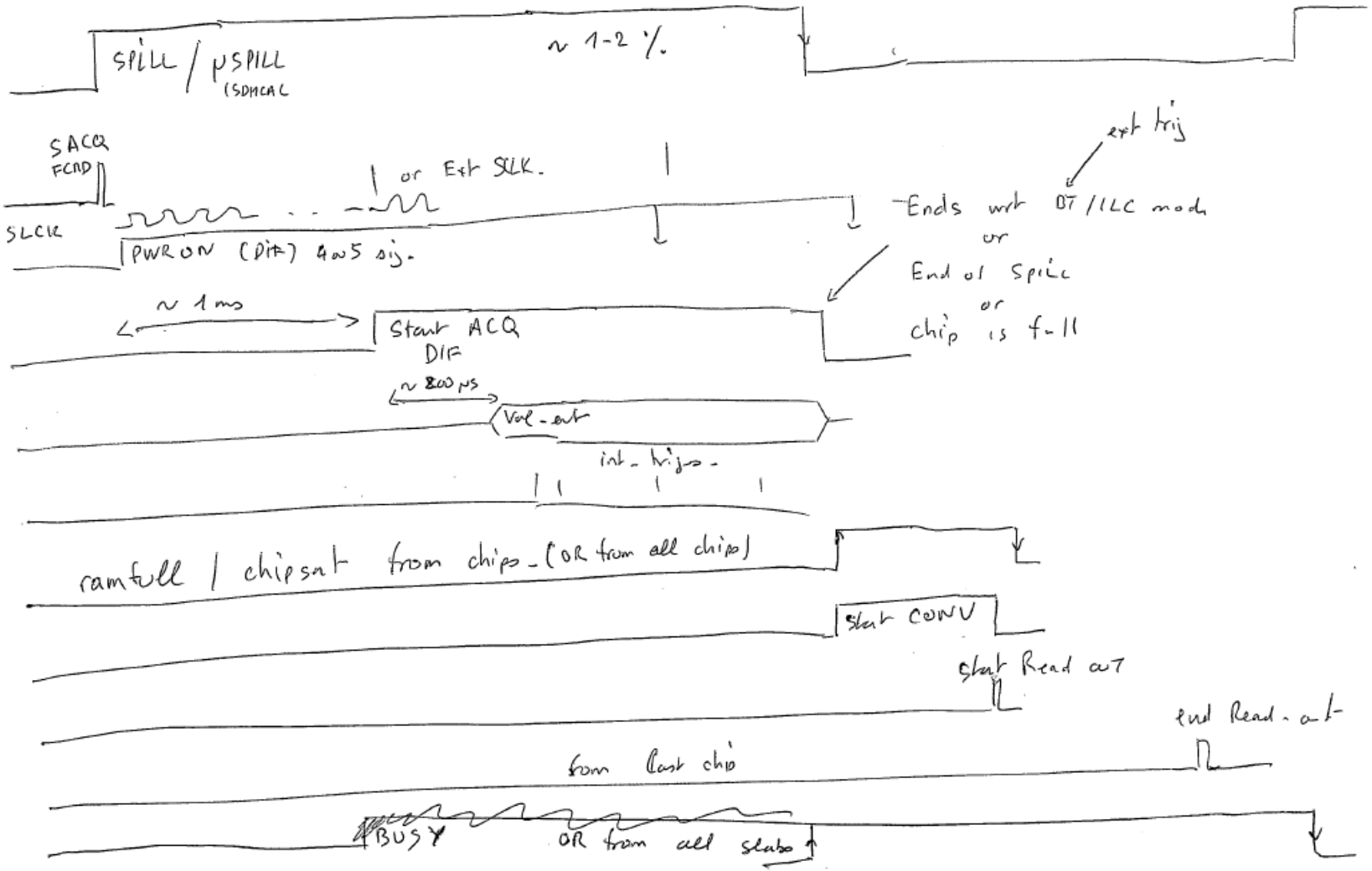

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