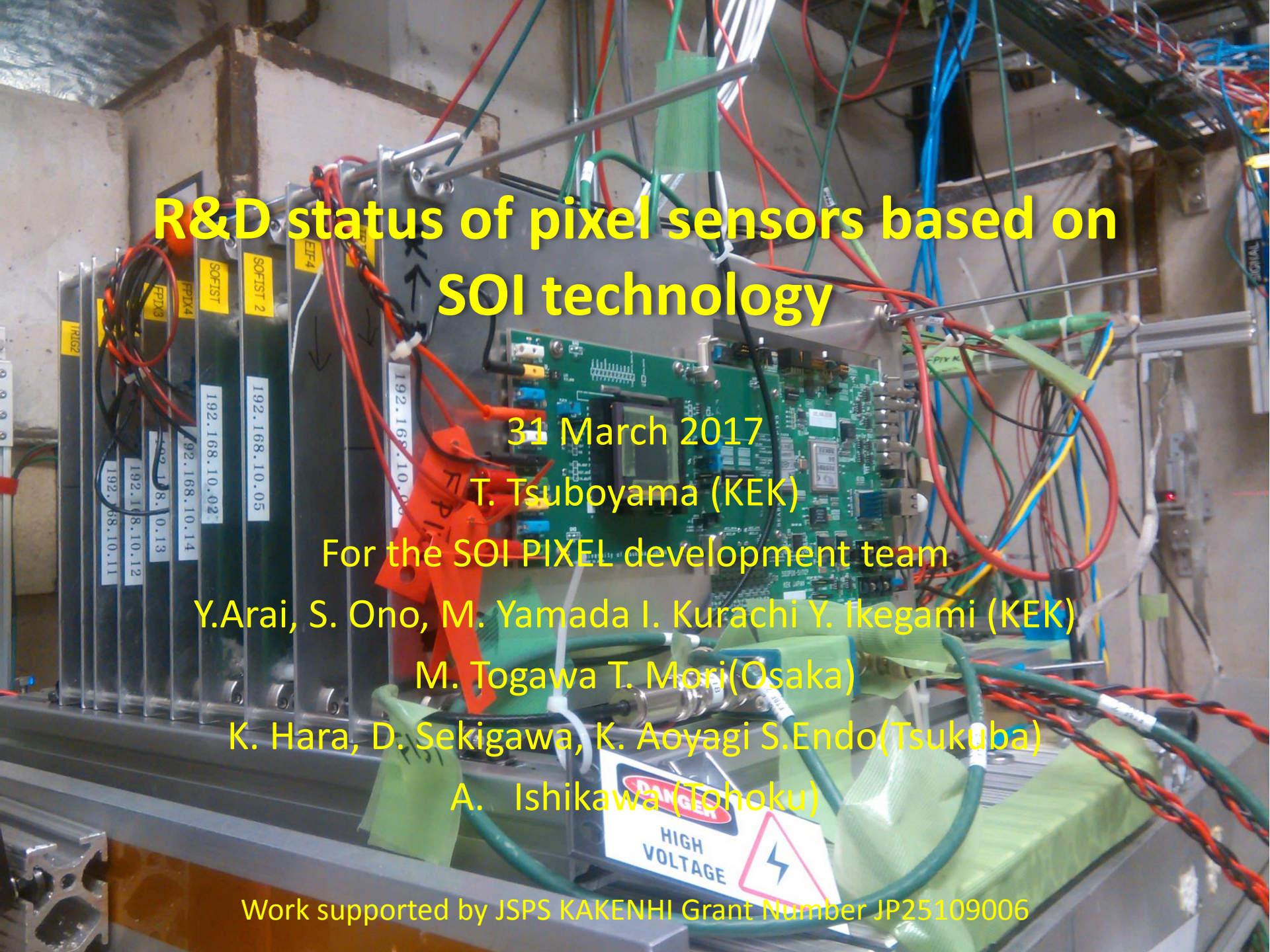

R&D status of pixel sensors based on SOI technology

31 March 2017

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For the SOI PIXEL development team

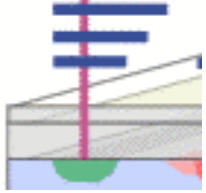
Y.Arai, S. Ono, M. Yamada I. Kurachi Y. Ikegami (KEK)

M. Togawa T. Mori(Osaka)

K. Hara, D. Sekigawa, K. Aoyagi S.Endo(Tsukuba)

A. Ishikawa (Tohoku)

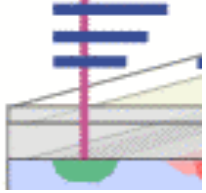
Work supported by JSPS KAKENHI Grant Number JP25109006



R&D status of pixel sensors based on SOI technology

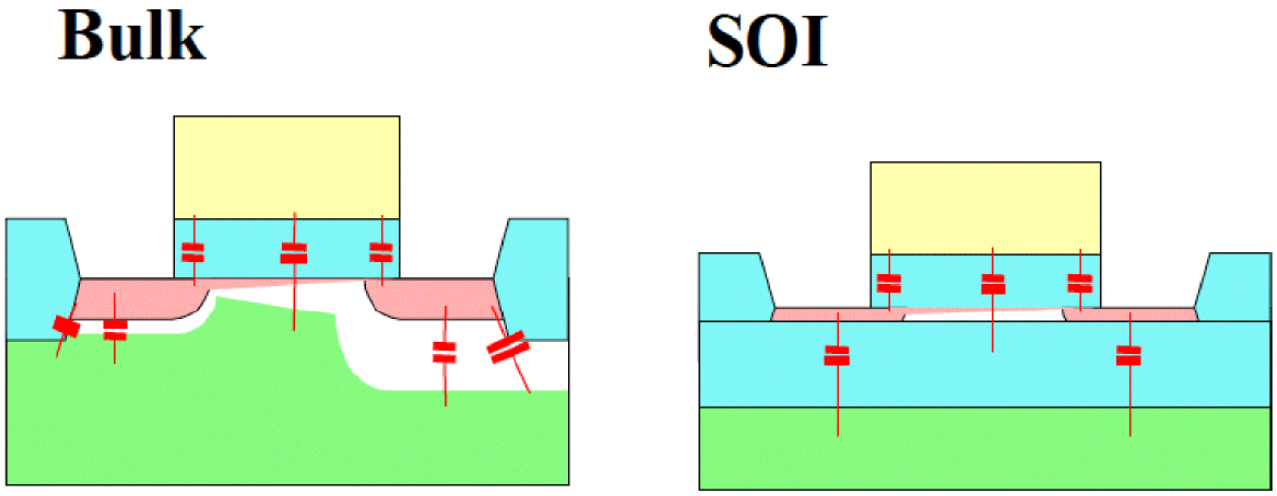
- Introduction
- R&D for the pixel sensor for the particle tracking
- 2017 Beam test result (tentative)
- Near future plans
- Summary

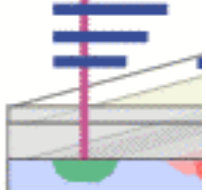
- Most information are from talks in 2017 Spring JSPS meeting: S. Ono M. Yamada, D. Sekigawa and K. Aoyagi.



SOI technology

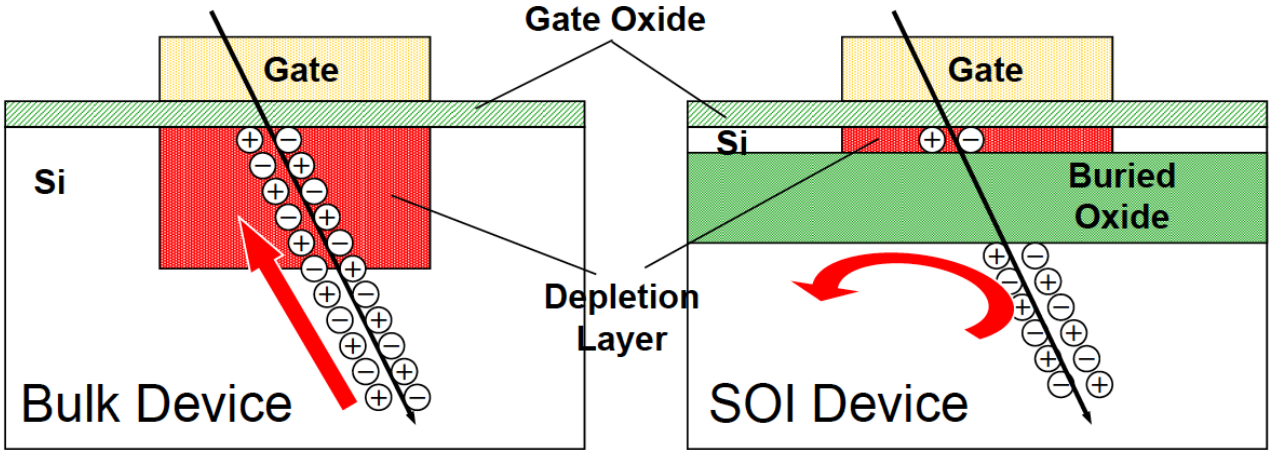
- SOI was originally developed for a low power/high frequency CMOS circuit:
- MOS transistors are isolated each other.
  - Lower stray capacitance enables a lower power operation at same clock, or, higher clock operation within given power consumption.

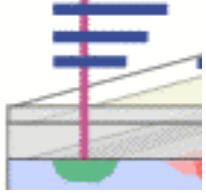




SOI technology

- Suitable for operation in harsh radiation condition
  - Insensitive to Single-event effects because transistors are isolated from the wafer (bulk) silicon.
  - Latch-up free circuit: No parasitic thyristors.
  - High-temperature operation: Leak current from wafer is avoided.
- By processing the charge induced in the bulk, SOI can be used as a radiation sensor.





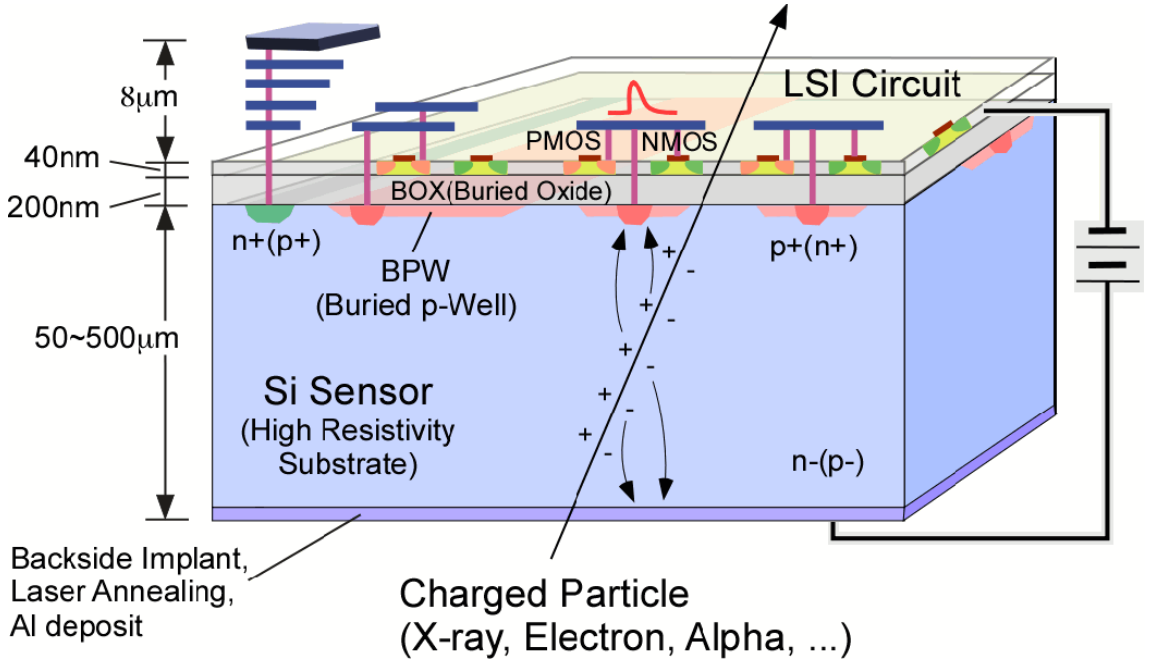
Lapis Semiconductor

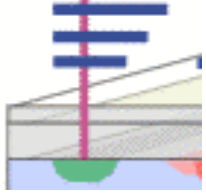
- We are working with Lapis Semiconductor, Japan.
- We can use standard CMOS designing/verification tools.
  - Not only the CMOS circuit, but also sensor part can be designed with normal procedure. (Thanks to engineers in Lapis).
  - If you are familiar with ASIC designing tools, you can produce a pixel sensor easily.
- Chips are delivered about 4 months after submission.

Slide presented in LCWS2016 by Y. Arai

TID effects to SOI

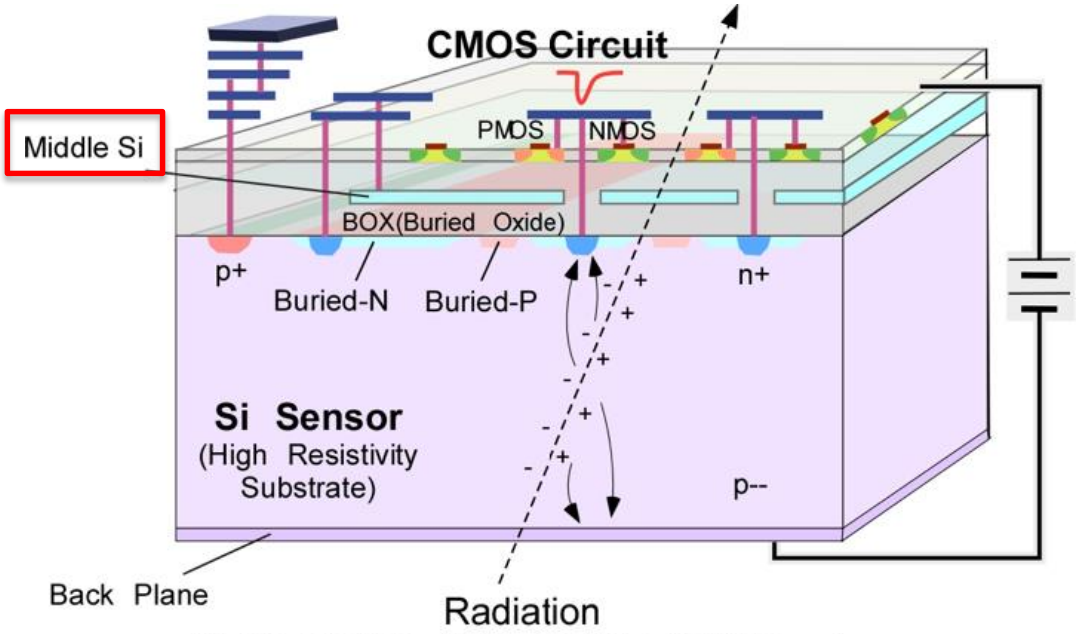
- The SOI has two shortcomings
  - The bias voltage applied to the sensor side changed the transistor parameters.
  - The charge accumulated in the BOX layer due to radiation changed the transistor parameters.

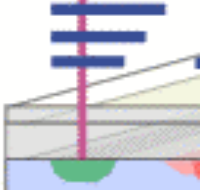




Double SOI technology

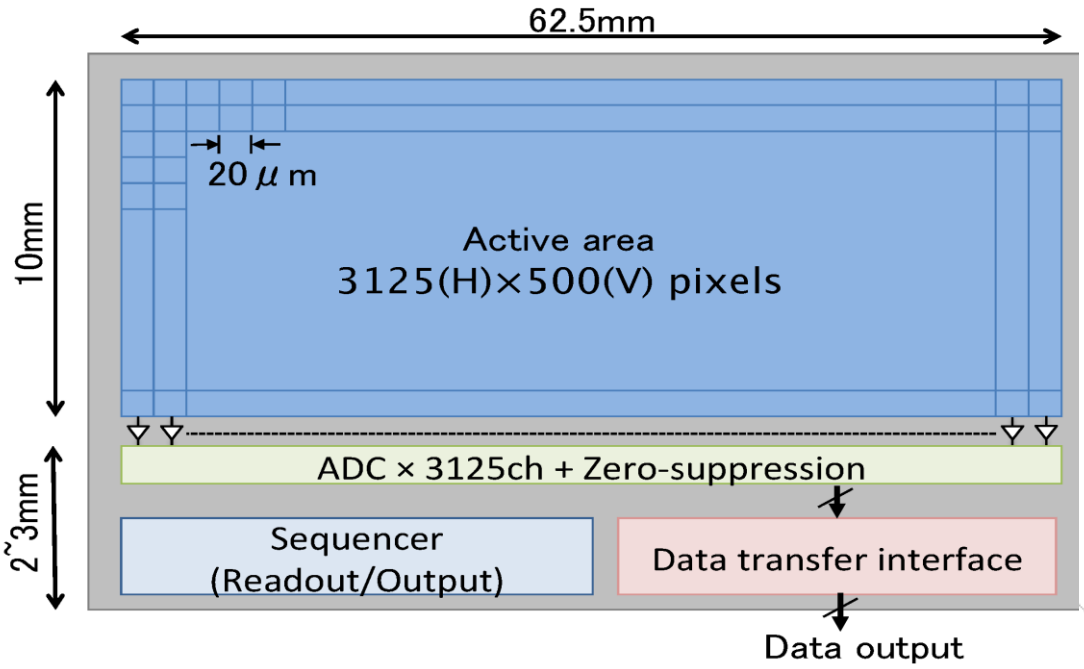
- The SOI development team proposed to add one SOI layer.
- "Double SOI structure (DSOI)"
  - The effects of back gate potential and TID can be cancelled by applying compensation voltage to the added silicon layer (middle silicon).
  - The EMI between circuits, especially among digital and analog circuit, is reduced significantly.

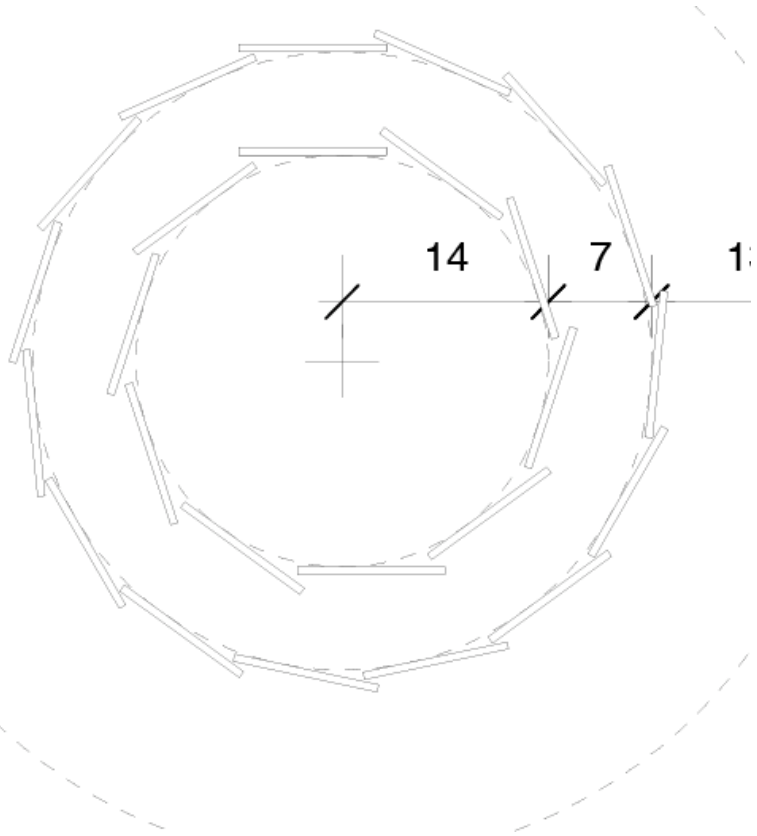




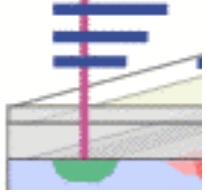
SOFIST

- Design goal:
  - monolithic pixel sensor that covers first 2 layers of the ILC vertex detector.





Base design was done by M. Togawa (Osaka) and S. Ono (KEK)



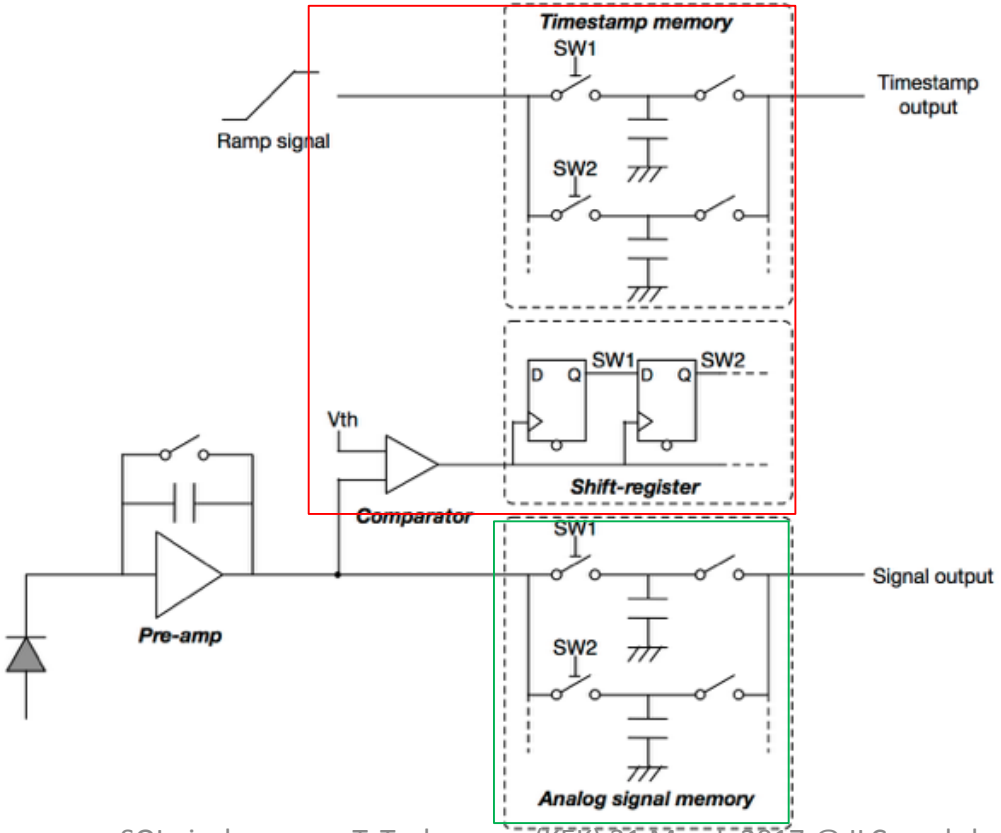
SOFIST

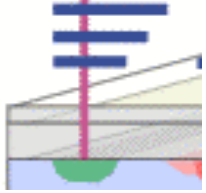
- The data for 1 bunch train is accumulated in each pixel.
- Analog and time stamp memories to accumulate multiple hits from different collision bunches.
- Data is readout in the 200 msec interval by using column ADC

Hit time recording (Sofist2)

Hit decision logic

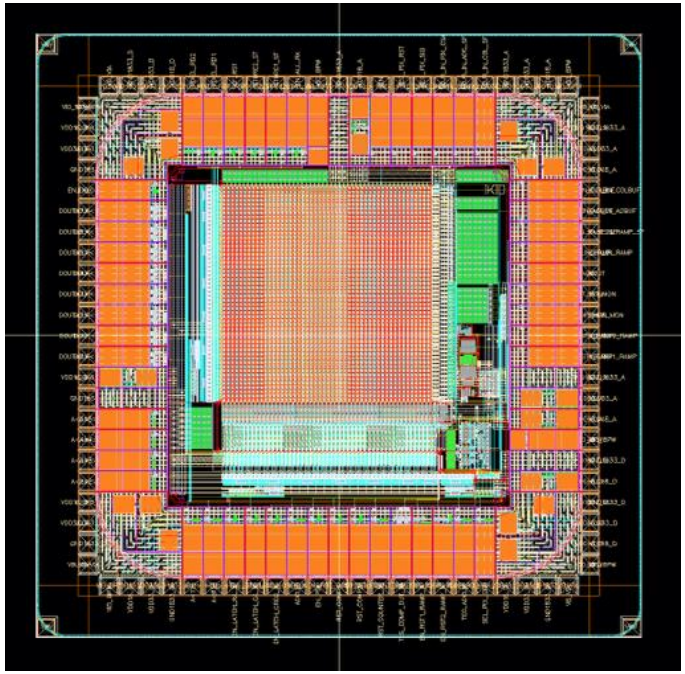
Hit charge recording (Sofist1)

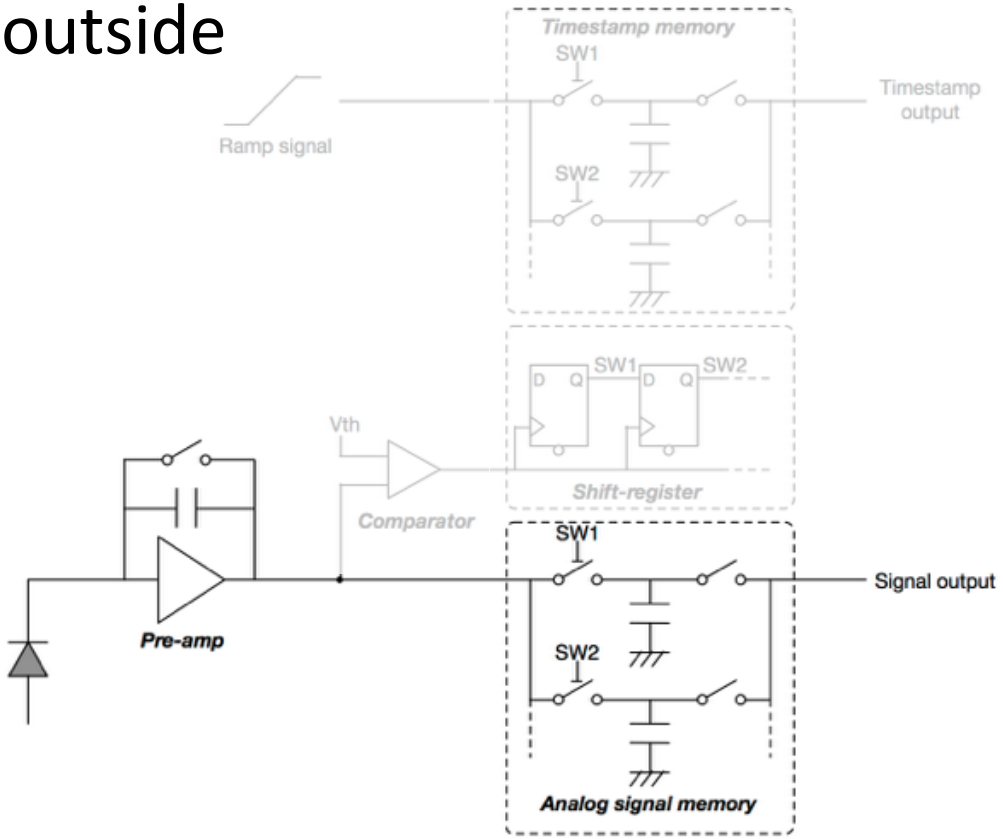


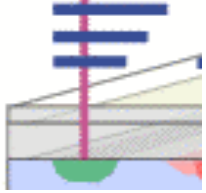


SOFIST 1

- Two charge memories
- Pixel size 20x20 µm2
- Chip size 2.9x2.9 mm2
- Trigger is supplied from outside
- Wafer SOI FZ n-type



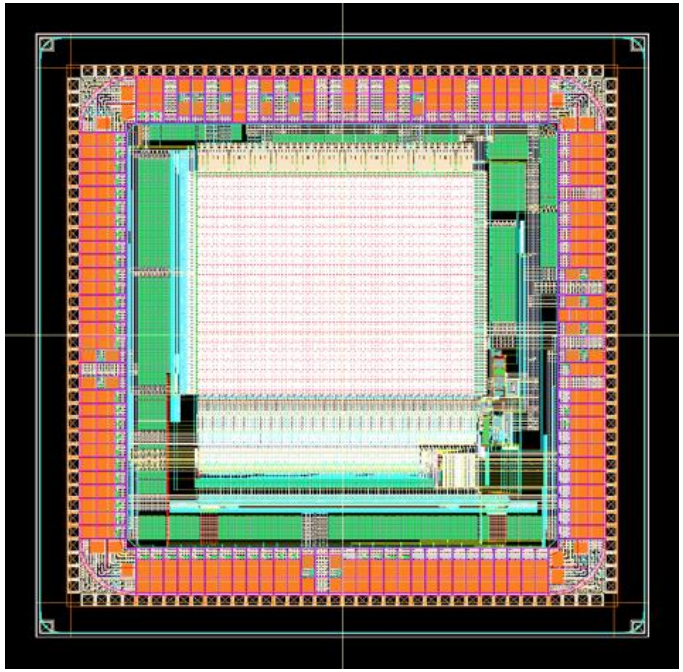


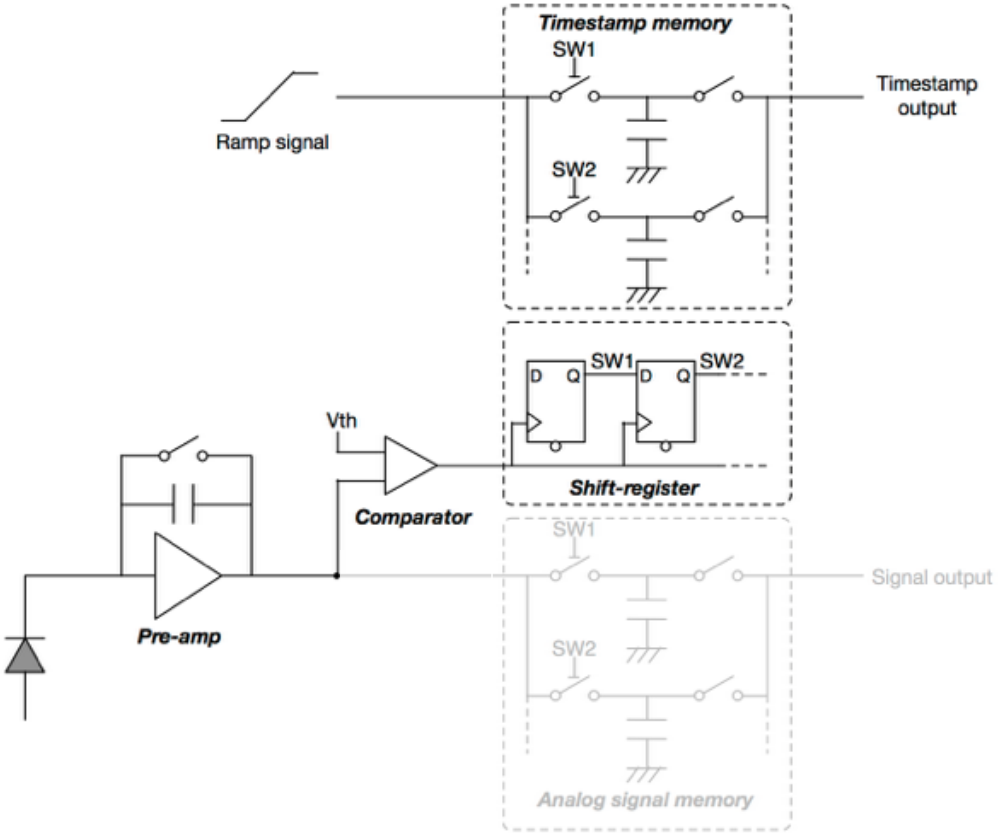


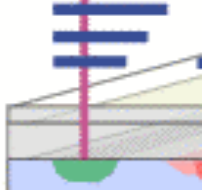
SOFIST2

- Chip size 4.5 x 4.5 mm^2
- Pixel size 25x25 μm^2
- 80x64 pixels
- Wafer: DSOI FZ p-type

Design started 2015 Autumn
Submitted 2016 May
Chip delivery End of 2016

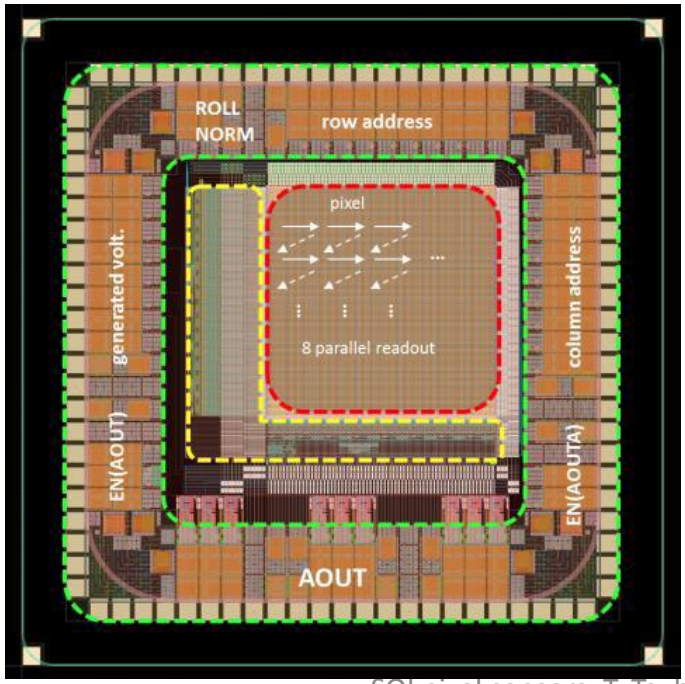


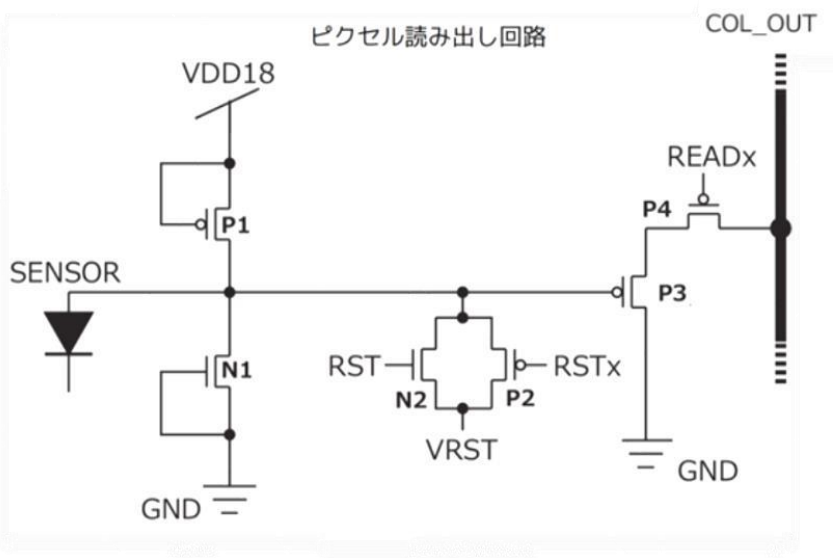


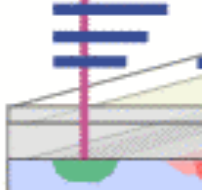


FPIX2

- Pixel size 8x8 μm^2
- Readout is in rolling shutter mode.
- chip size 2.9x2.9 mm^2 1mm x 1mm active area
- Pixel size 8x8 μm^2, 128x128 pixels
- Wafer: DSOI FZ n-type

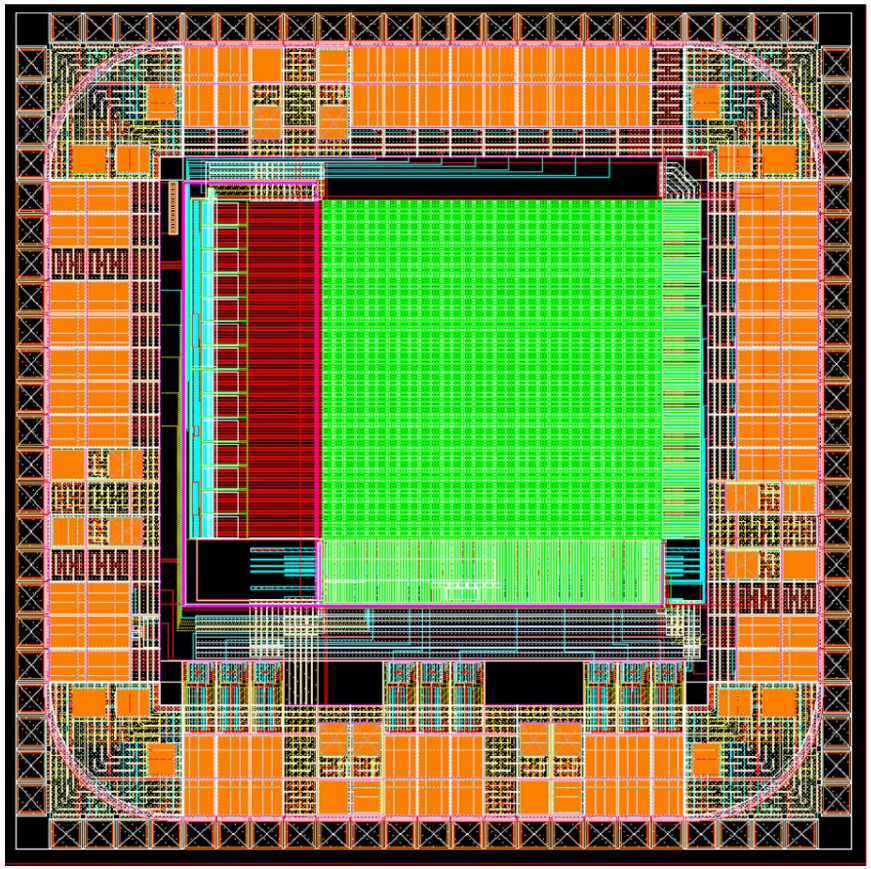






FPIX3

- Produced in2016



Pixel size 9 um × 9 um
Pixel array: 112pix × 112pix
Active region: 1 mm x 1 mm

6 compensation voltages for NMOS and PMOS in pixel, decoder and IO blocks.

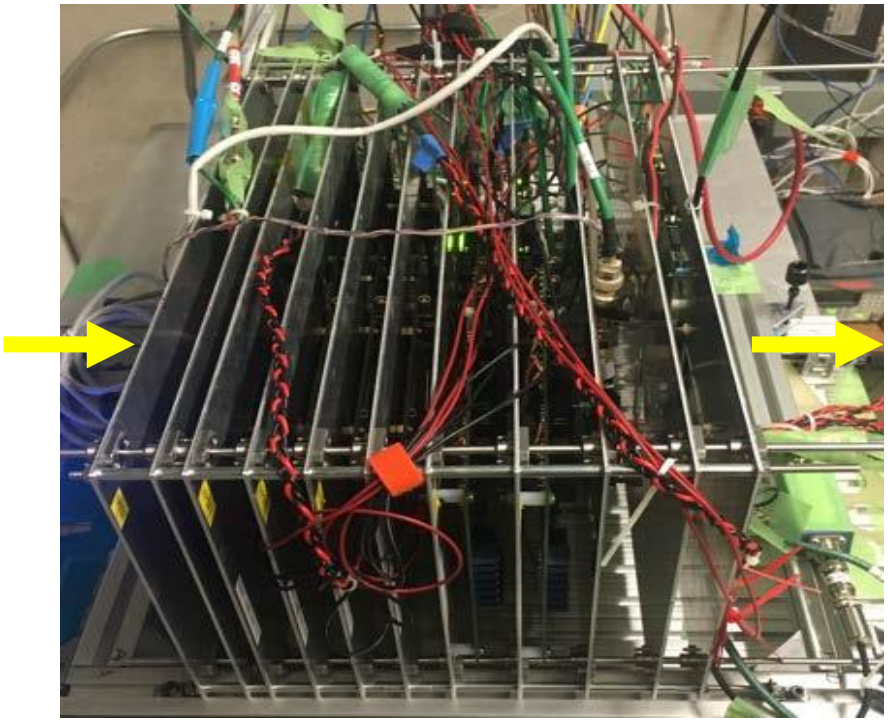
LDD doping level increased

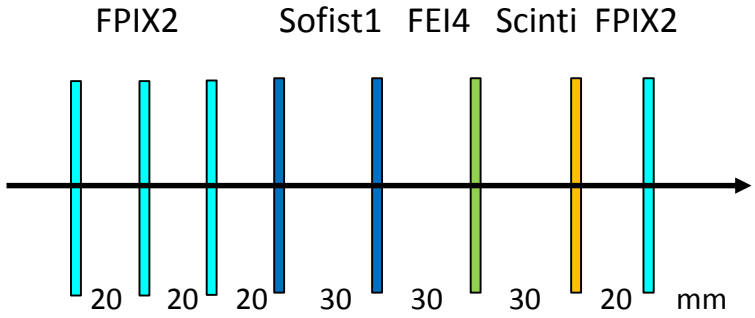
Result: FPIX3 responded to IR laser signal even after 1MGy (100 Mrad) TID accumulation.

SOI pixel technology is now one candidate of pixel detector for high luminosity hadron collider.

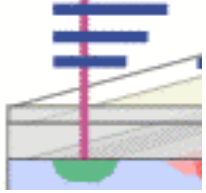
2016 Fermi Lab beam test

- Four FPIX2 and two SOFIST1 chips were tested with Fermi Lab 120 GeV proton beam from 24 Jan. to 9 Feb. 2017.
- Thickness of pixel wafer was 500 um.
- Data is taken varying the bias voltages in order to simulate thinned pixel sensors



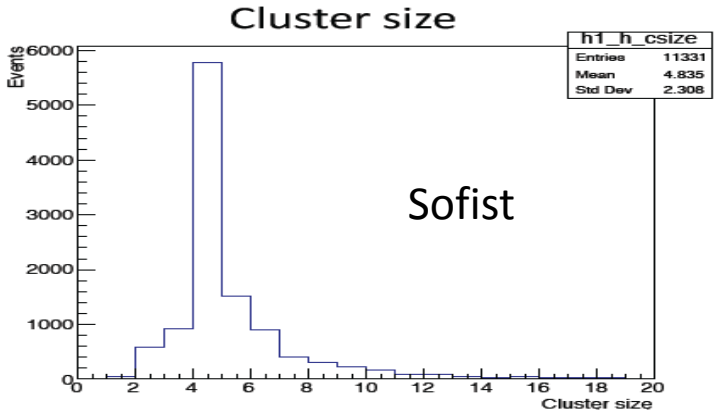


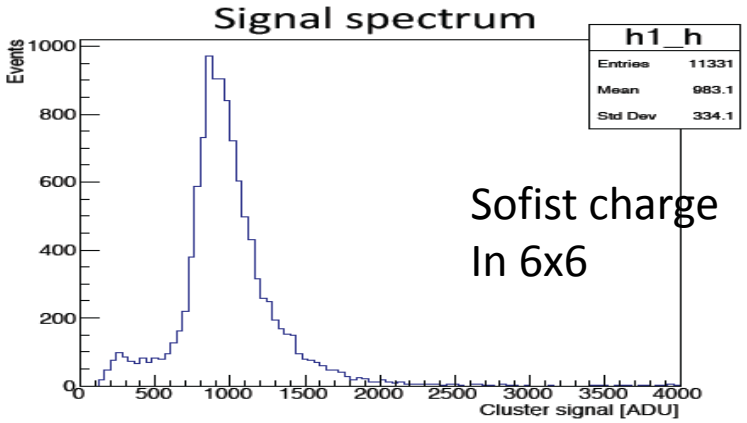
Beam test Setup

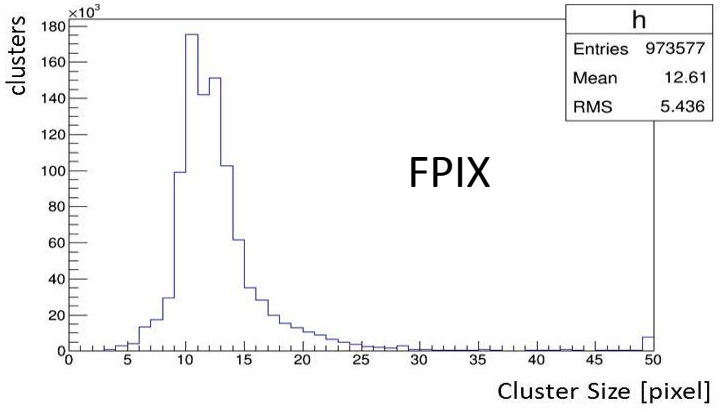


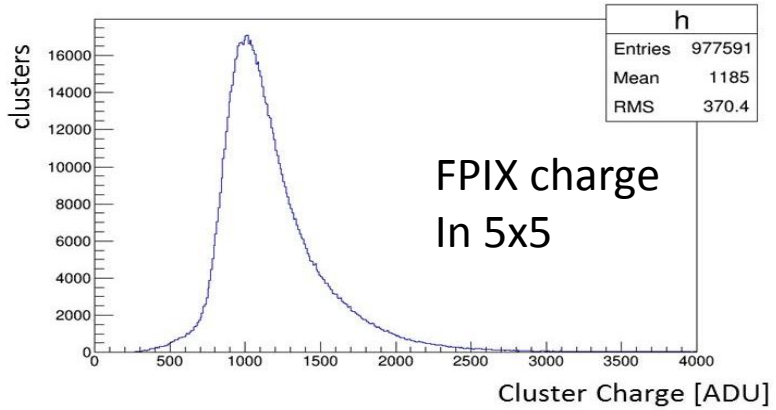
Preliminary result(1)

- Cluster size and cluster charge

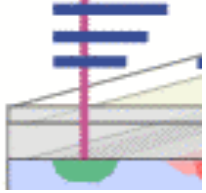








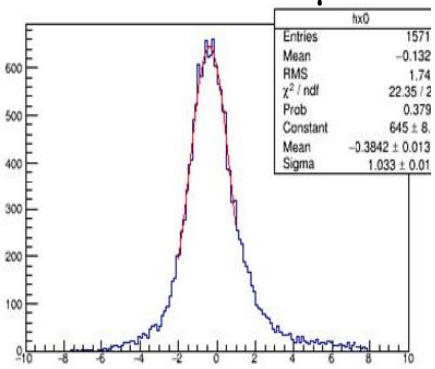
	Pixel size (μm^2)	Depletion width (mm)	Single pixel Noise (ADU)	Signal peak (ADU)	Ave. cluster size	S/N single
Sofist	20x20	0.5	2.2	800	4.8	360
Fpix	8x8	0.5	2.0	950	12.6	475



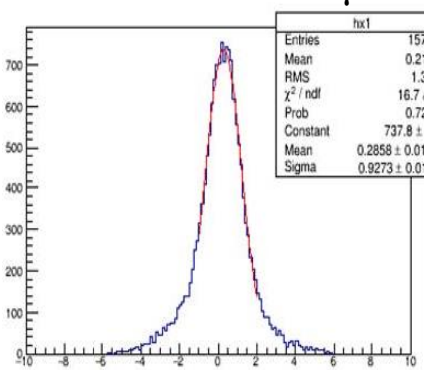
Preliminary result(2)

- Point resolution estimation
- Tracking excluding DUT → Calculate residue at DUT

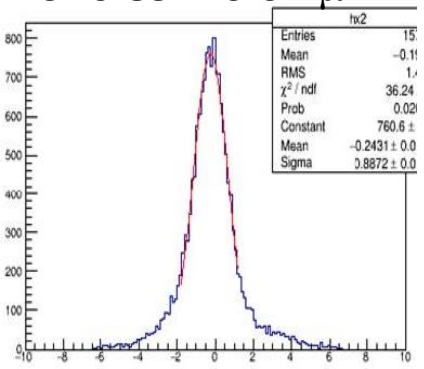
σ=1.03±0.02 μm



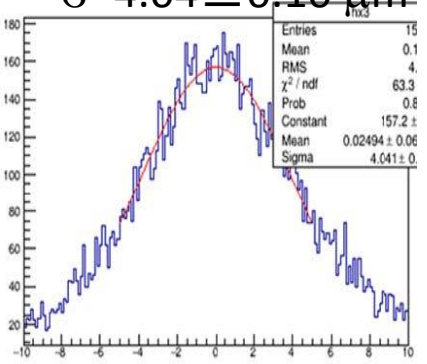
σ=0.93±0.01 μm

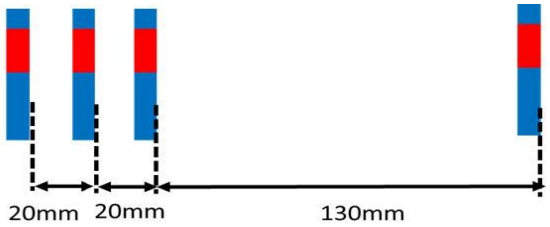


σ=0.89±0.01 μm

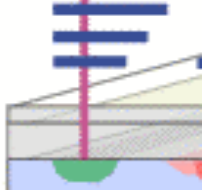


σ=4.04±0.10 μm





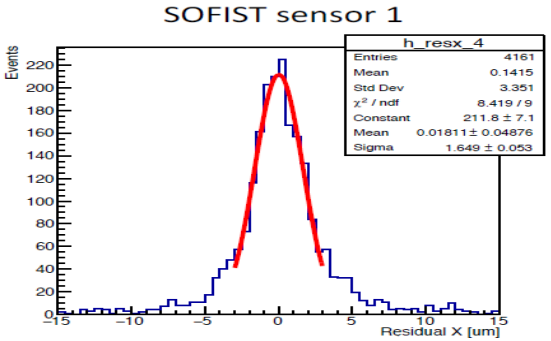
- Effects of multiple scattering and tracking error are not subtracted yet.
- We observed the special resolution 0.98 μm or less.



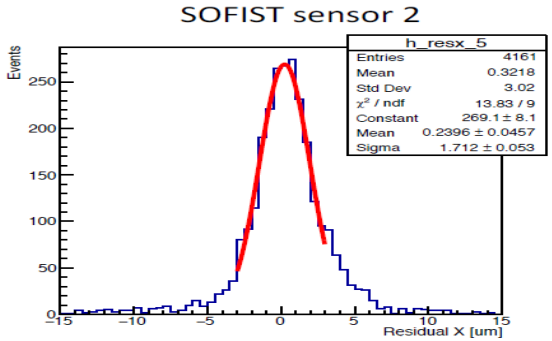
Preliminary result(2)

- Point resolution estimation
  - Tracking excluding DUT → Calculate residue at DUT

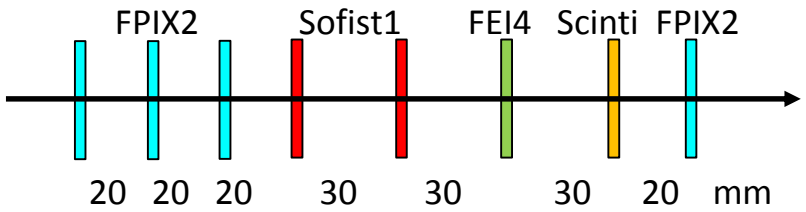
σ=1.65±0.05 μm



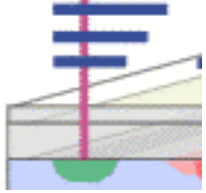
σ=1.71±0.05 μm



SOFIST Residual width: ~1.7 [um] (Preliminary)

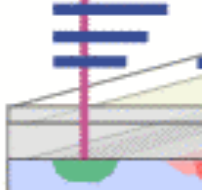


- Effects of multiple scattering and tracking error are not subtracted yet.
- We observed the special resolution 1.7 μm with 20μm□ pixel sensor

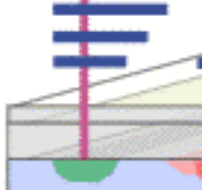


Tentative beam test summary

- With Sofist1 (20 μm□) and FPIX2(8 μm□) SOI pixel sensors, we observed 1.7 μm and 0.8 μm position resolution.
  - The tracking error and multiple-scattering effects are not subtracted yet.
- Reservations:
  - The results are from fully depletion(500 μm thick case).
    - We obtained data with lower bias voltage.
  - The thinned sensor (75 μm thick) were prepared in March 2017 and tests are starting.
  - We do not understand the cluster size distribution yet: Elaborate simulation (GEANT+TCAD) may be necessary to understand the distribution fully.

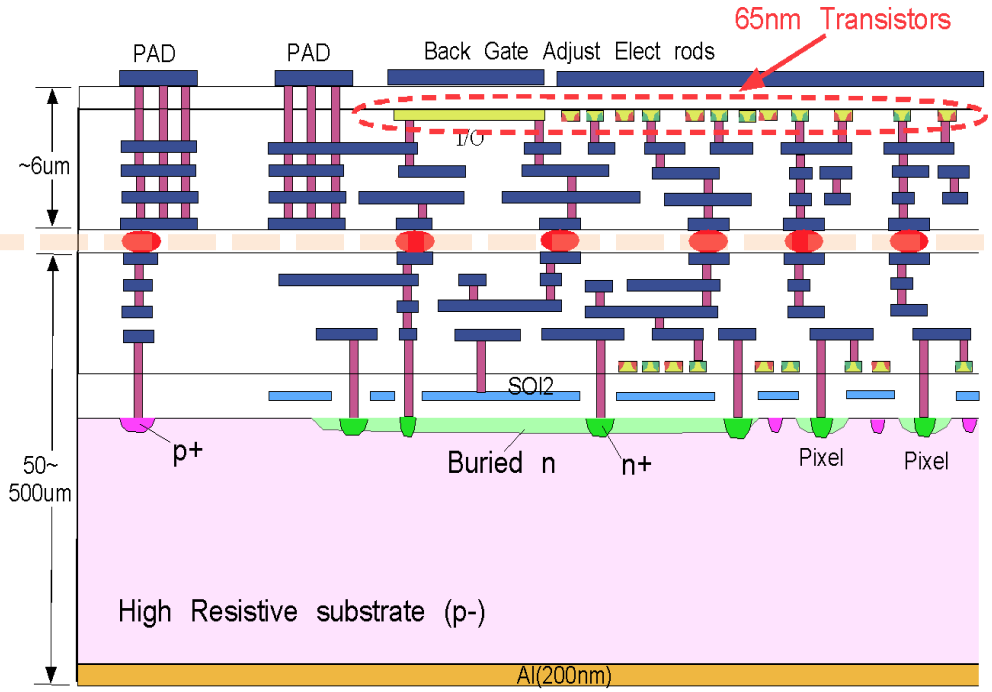


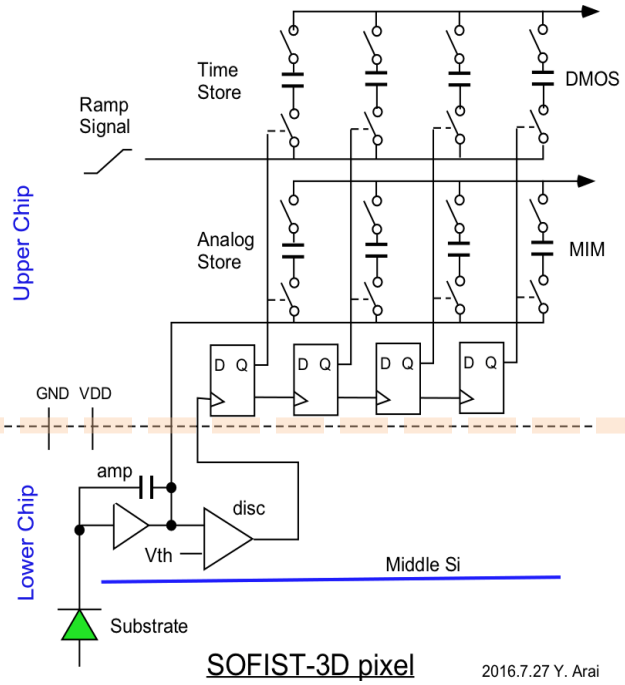
Current activities

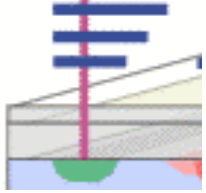


3D stacking

- 3D stacking
  - We concluded analog and time information can not be stored together in a 20 µm x 20 µm pixel.
  - Solution is 3D integration of additional circuit.
  - SOI is suitable for 3D stacking

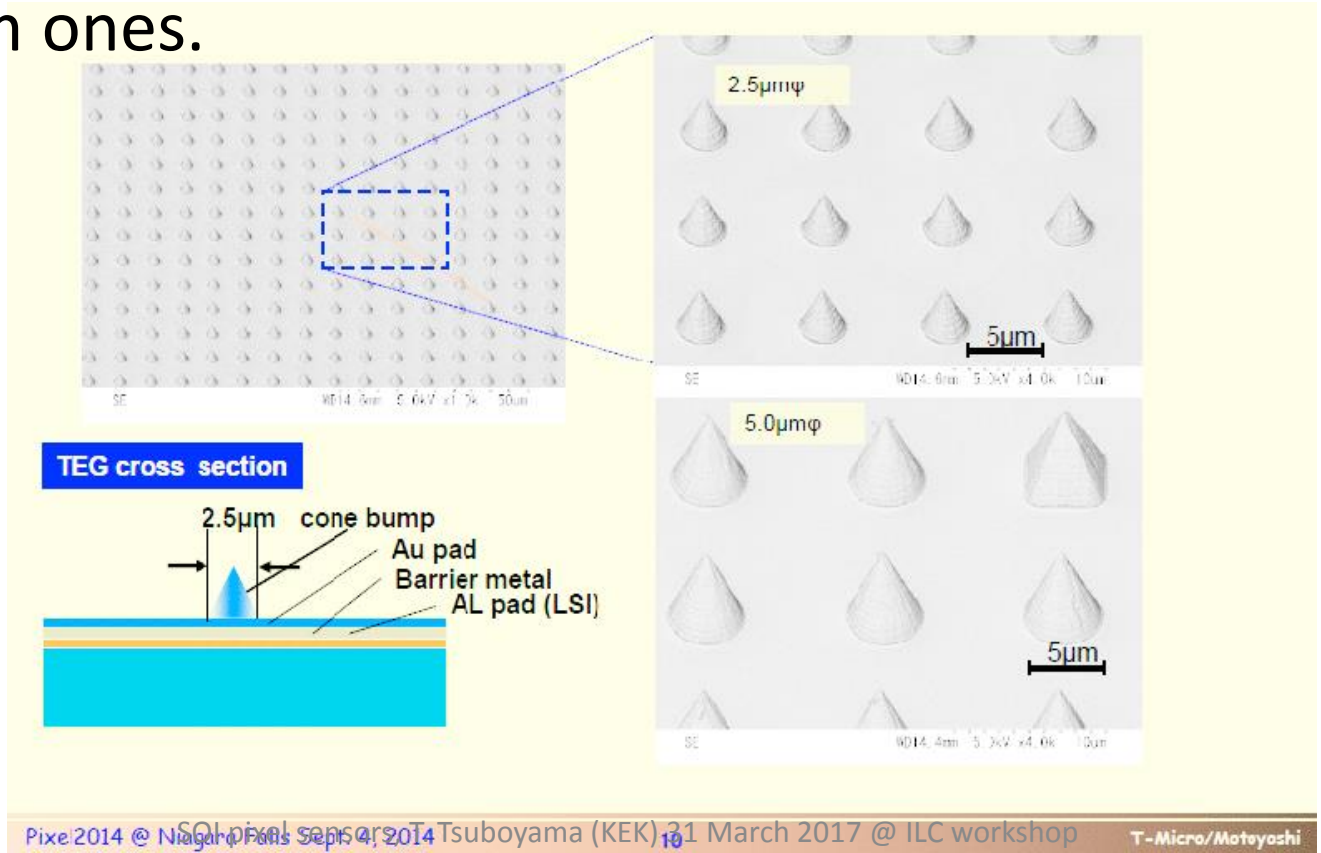


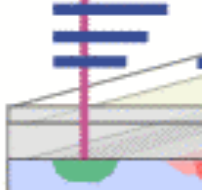




3D stacking

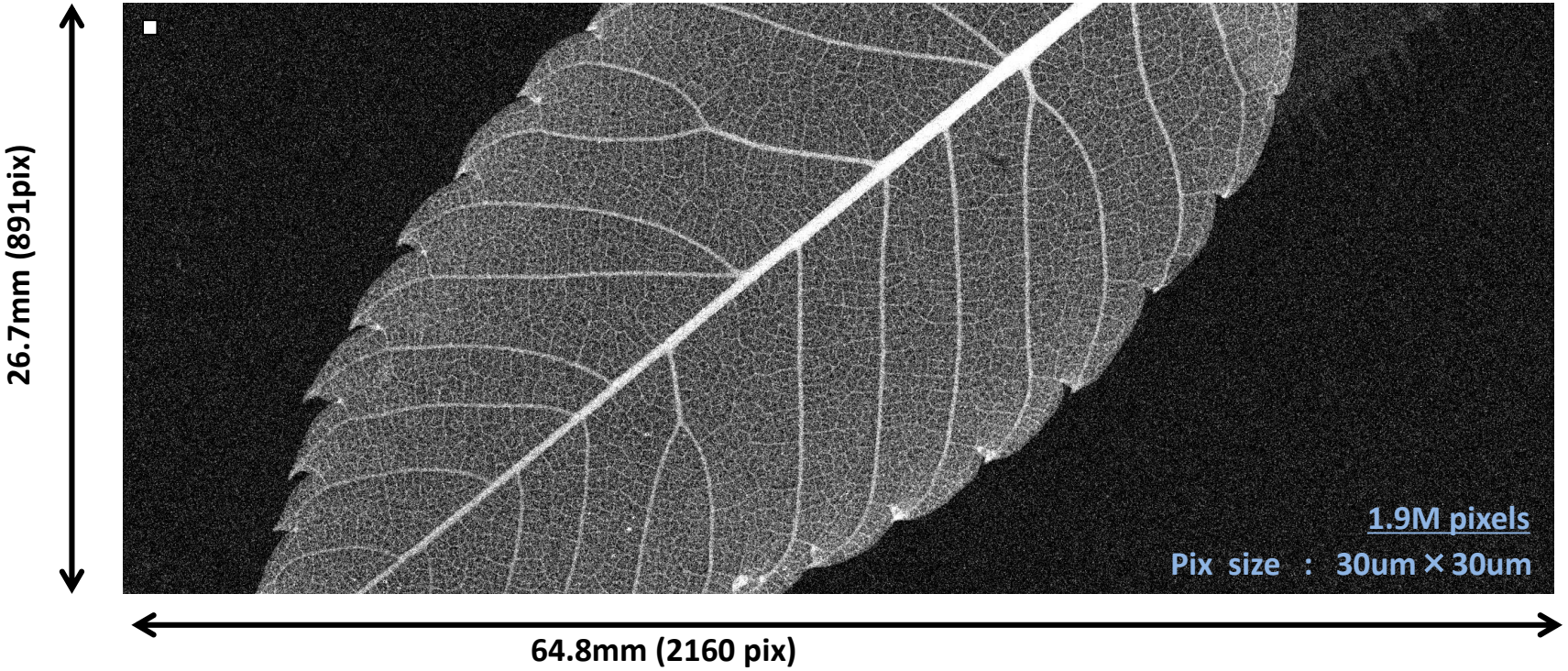
- Collaboration T-micro, a venture company doing 3D stacking, has started.
- They are establishing a new method to bond wafers with high yield by using "gold micro cone bump" instead of indium ones.





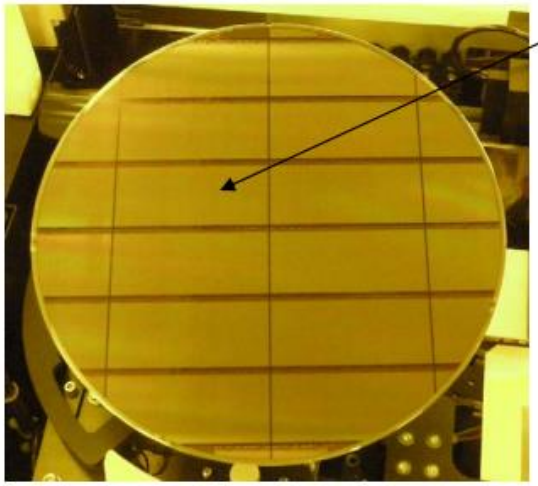
Chip size

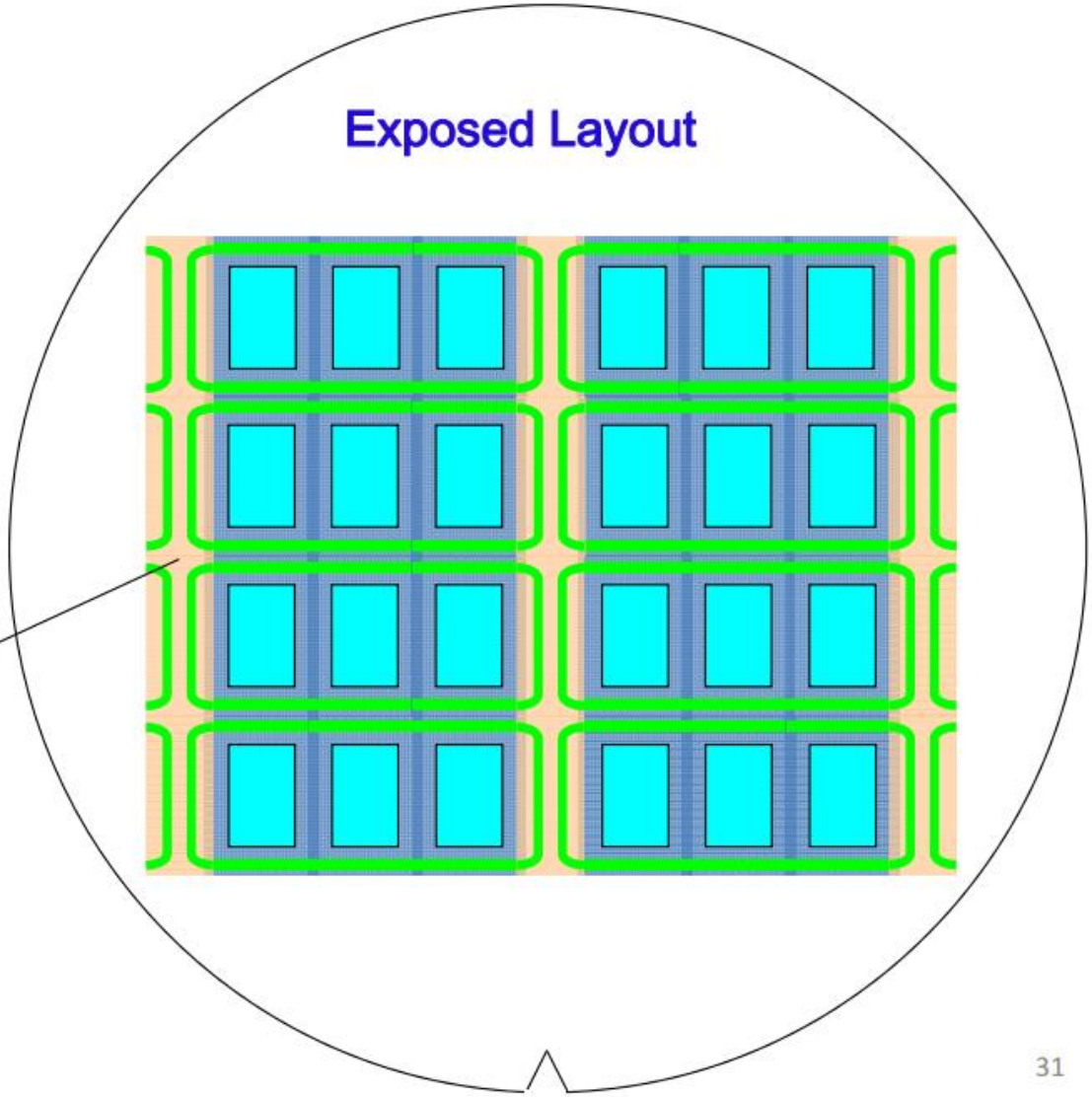
- The reticle size of Lapis SOI is 30 mm x 24 mm.
- You can purchase SOI pixel sensor as large as 27 mm x 65 mm, developed Spring-8 XFEL detector.

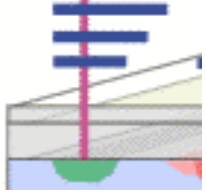


Sensor size

Stitching Exposure for Large Sensor

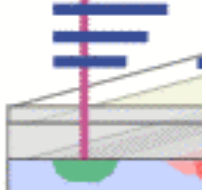






Summary

- R&D of SOI monolithic pixel sensor has been presented
- By using DSOI technology, low nose and high radiation tolerant pixel sensor are realized.
- The next challenge
  - 3D integration of Soifst chip.
  - FPIX sensor operative above 1 MGy irradiation.
- In order to start realistic sensor design, we need more information
  - Features of Physics and Background hit occupancy
  - Cluster size distribution by using test beam.

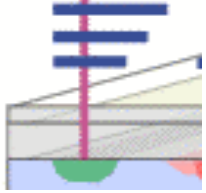


SOFIST and FPIX developments

- a

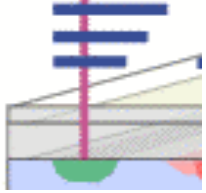
Sofist	wafer	Pixel size (μm^2)	Pixels	Chip size (mm^2)	Note
Sofist1(2015)	SOI	20x20	50x50	2.9x2.9	Charge x 2
Sofist2(2016)	DSOI	25x25	64x(64+16)	4.5x4.5	Time stamp x 2 (16 are charge readout)
Sofist3(2017)	DSOI	30x30	128x128	6x6	Charge and time stamp x 3
Sofist4(2017)	DSOI	20x20	128x128	4.5x4.5	3D stackin of Sofist3

Sofist		Pixel size (μm^2)	Pixels	Chip size (mm^2)	Note
FPIX2(2015)	DSOI	8x8	128x128	2.9x2.9	
FPIX3(2016)	DSOI	9x9	112x112	2.9x2.9	Individual compensation
FPIX4(2017)	DSOI	9x9		6x6 ?	Large



Materials

- Y. Arai
  - https://indico.cern.ch/event/452781/contributions/2297593/attachments/1345183/2028139/1609Vertex_arai_v2b.pdf
- K. Hara
  - https://kds.kek.jp/indico/event/21579/session/4/contribution/48/material/slides/0.pptx
- M. Yamada
  - https://kds.kek.jp/indico/event/22867/session/6/contribution/9/material/slides/0.pdf
- S. Ono
  - https://indico.cern.ch/event/452781/contributions/2194859/attachments/1344385/2026196/A_monolithic_pixel_sensor_with_fine_space-time_resolution_based_on_silicon-on-insulator_SOI_technology_for_the_ILC_vertex_detector_20160919.pdf



SOI pixel sensor development

- In 2006, KEK DTP started and SOI group was organized.
- Prof. Arai invited scientists from various fields in addition to particle physicists: Satellite / Material / Biology…
- In 2012, a 5-year glant-in-aid funding was approved and more intensive R&D became possible. This is the 4th year of the project.
- Multi-project-wafer run: 1.5 submission per year.
- A group of "pixel sensor for particle physics (Osaka, Tsukuba, Tohoku, KEK)" was organized
  - Monolithic pixel sensor to be used in future collider experiments
  - On-chip High performance data processing
  - Improve radiation hardness
  - Small size pixel