Pixellated Option of SIT Derived from CPS Development for ALICE & CBM

M.Winter / IPHC, 30 June 2017

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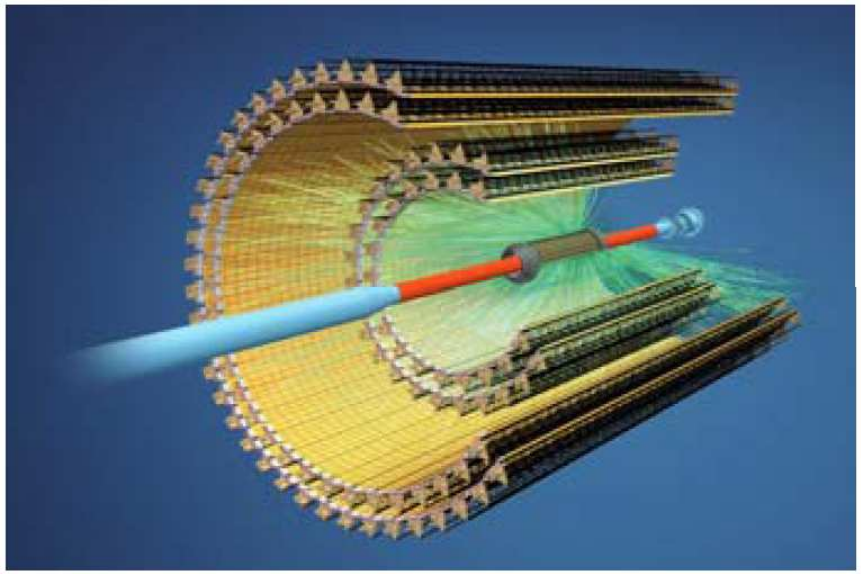
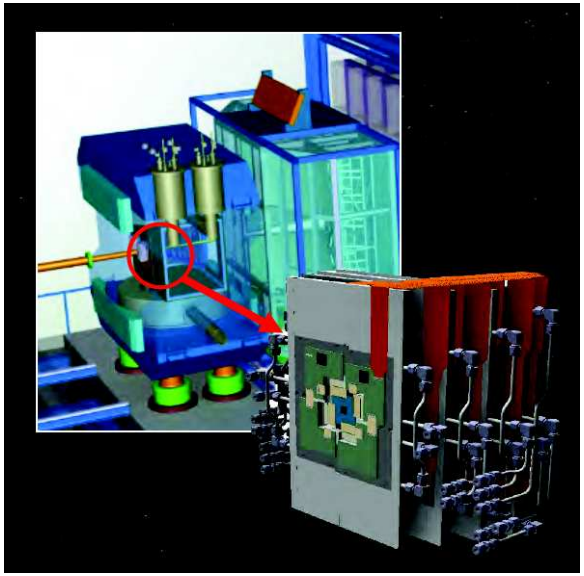
- **Current pixel sensor and ladder developments used to derive a pixellated SIT concept**
- **Expected performances**
- **Potential improvements**
- **Summary**

Starting point: CPS for the ALICE-ITS & CBM-MVD

ALICE-ITS



CBM-MVD

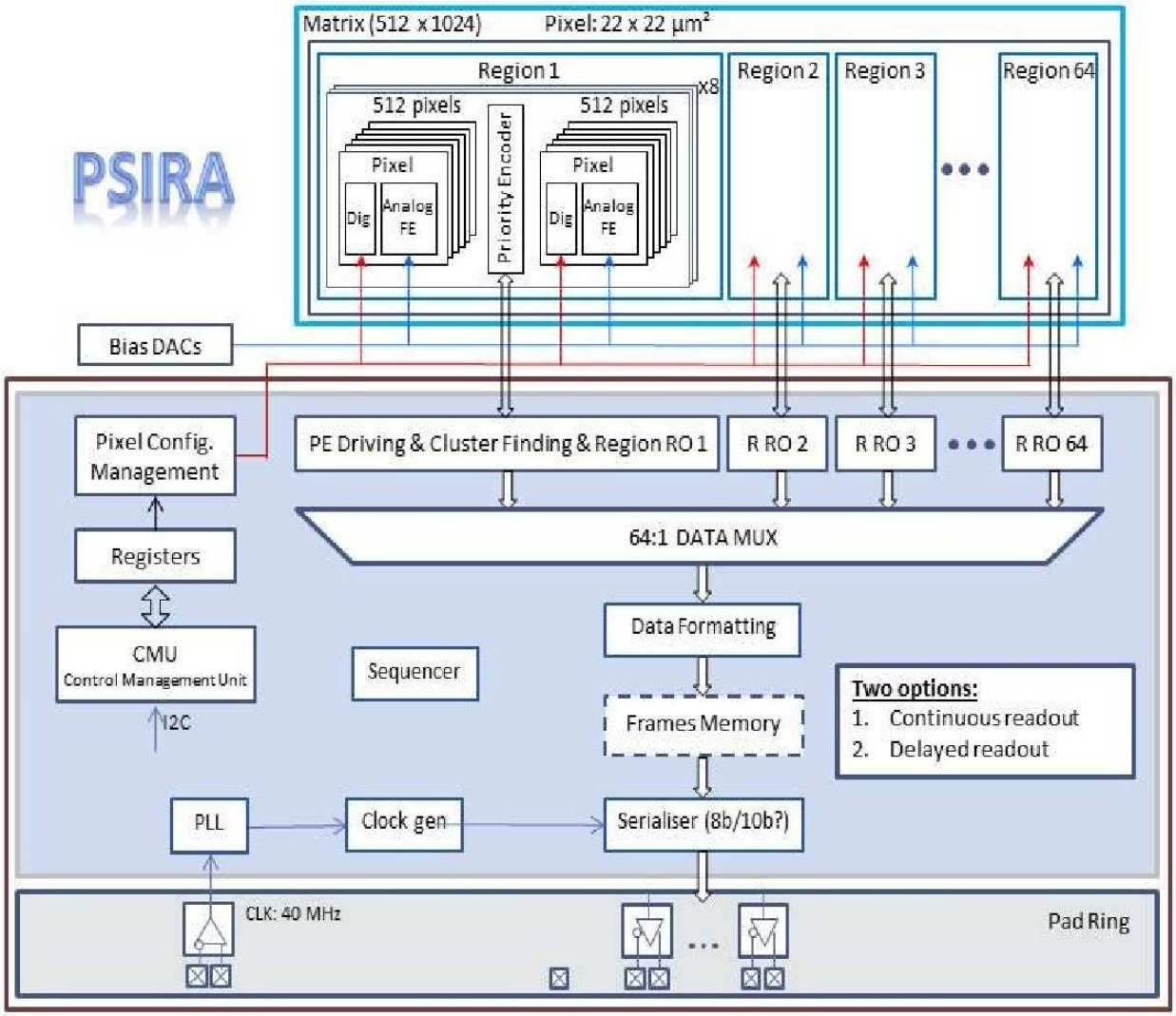


	ALICE-ITS	CBM-MVD
Pixel dimensions	26.9μm x 29.2μm	26.9μm x 30.2μm
Spatial resolution	$\sim$ **5** μm	$\sim$ **5** μm
Time resolution	**5–10** μs	$\sim$ **5**μs
Hit rate	$\sim$ 10^6/cm^2/s	$\sim$ 10^8/cm^2/s
Power consumption	$\lesssim$ 20-35 mW/cm^2	$<$ 200 mW/cm^2
Insensitive area	$\sim$ 1.2mm x 30mm	1.5mm x 31mm
Rad. tolerance	300 kRad & 2·10^{12} n_{eq}/cm^2	1-3 MRad & 1-3·10^{13} n_{eq}/cm^2

Improving the Time resolution

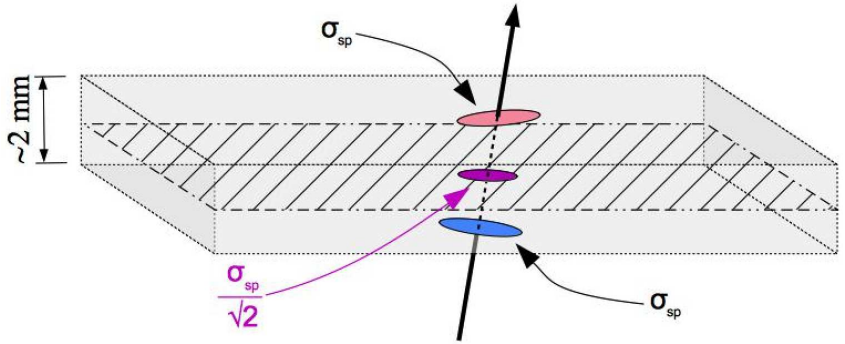
- **Elementary read-out region:**
  - 8 pairs of columns counting 512 pixels
  - pitch $\simeq$ 22–29 μm^2 $\Rrightarrow$ S(region) $\simeq$ 4–7 mm^2

- **Expected performances:**
  - signal peaking time $\lesssim$ 2 μs
  - single pixel address read-out
    takes 50 ns (20 MHz clock)
  - if clusters have 5 pixels (inclined e$^{\pm}$ tracks)
    $\Rrightarrow$ 250 ns / hit $\Rrightarrow$ 4 hits/region/μs
    $\Rrightarrow$ 100 hits/cm^2/μs
  - if clusters have 3 pixels
    (BS at "larger" radii or signal)
    $\Rrightarrow$ 150 ns / hit $\Rrightarrow$ 7 hits/region/μs
    $\Rrightarrow$ $\lesssim$ 200 hits/cm^2/μs

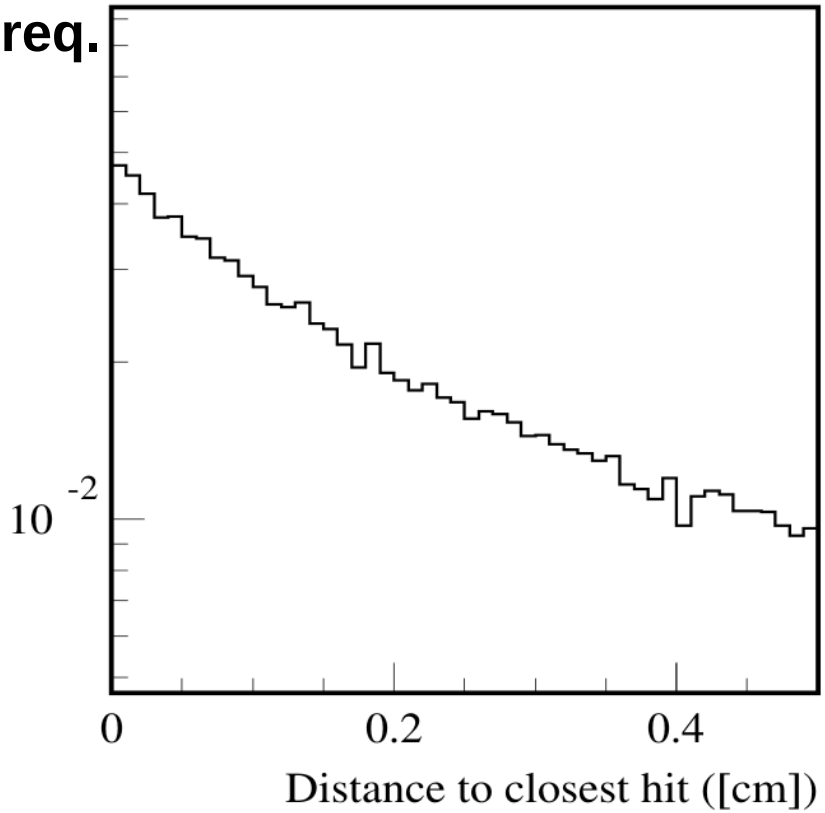


Application to ILD Silicon Inner Tracker (SIT)

- **Concept :**
  - 2 double-sided layers ⇛ 2 mini-vectors per track
    ⇛ improved spatial resolution & track seeding
  - Baseline sensor performances:
    - $\sigma_{R\Phi,Z}$ = 5 μm
    - Δt = 1 μs (assumes compressed peaking time)



- **Expected occupancies :**
  - Beamstrahlung: 10^{-2} hits/cm^2/μs
    ⇛ negligible impact on read-out time
    and size of data sample
  - Physics: may be $>$ 4–5 hits/region/μs
    ⇛ governs read-out time ⇛ **MC values required**



- **Read-out time :**
  - Assume 3 pixels/hit (signal)
  - 4–5 hits/region/μs ⇛ 12/15 pixels hit
    ⇛ 600/750 ns read-out time needed

Potential improvements of the Time resolution

- **Potential improvements on the 2 parametres governing the read-out speed:**
  - pixel address encoding: 50 ns $\rightarrowtail$ 25 ns
  - signal shaping during pre-amplification: 2 μs $\rightarrowtail$ $\lesssim$ 500 ns
- **Pixel address encoding:**
  - revisit the hierarchy of the priority encoder
  - reduce the number of nodes/steps

  $\hookrightarrow$ accelerating the clock frequency to 40 MHz (minor impact on power consumption)
- **Signal shaping:**
  - increase the pixel current to shorten the time-over-threshold **but** $I_{pix} \sim 1/t_{shaping}$

    Ex: going from 2 μs to $\sim$ 300 ns requires $\gtrsim$ 5 times higher current in the pixel

    power density of pixel array raises from 8 mW/cm^2 to $\gtrsim$ 40 mW/cm^2)
- **Remark:**
  - the above applies to the TJsc 0.11/0.18 μm CMOS process

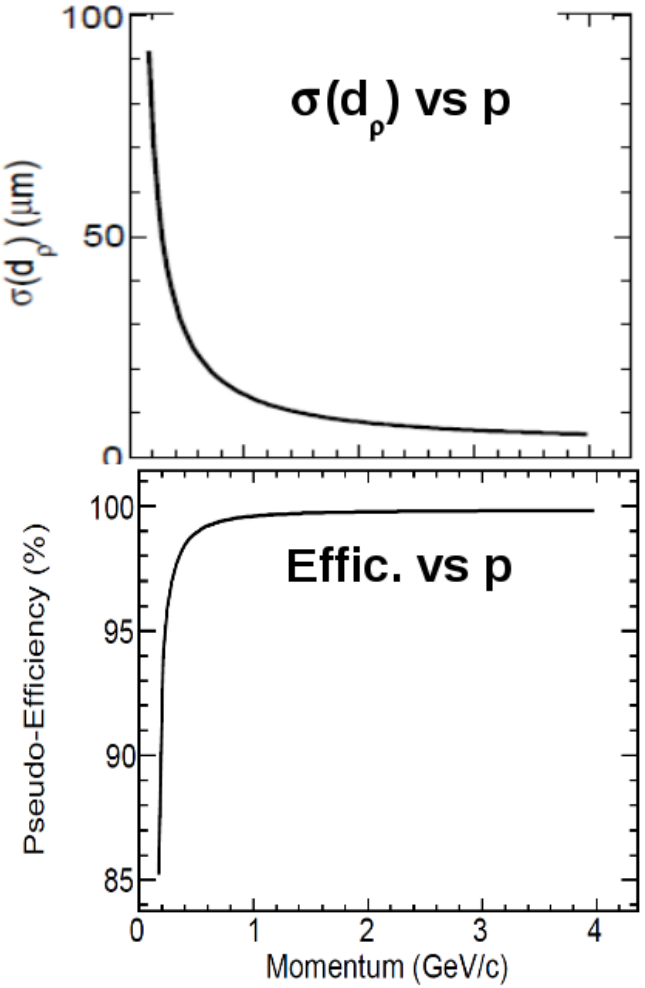
    $\Rrightarrow$ smaller feature size and larger N(Metal Layers) would allow further improvements
  - alternative sensor architectures are being explored, aiming at read-out times $\ll$ 1 μs

GUARIGUANCHI Tool [A. Pérez-Pérez]

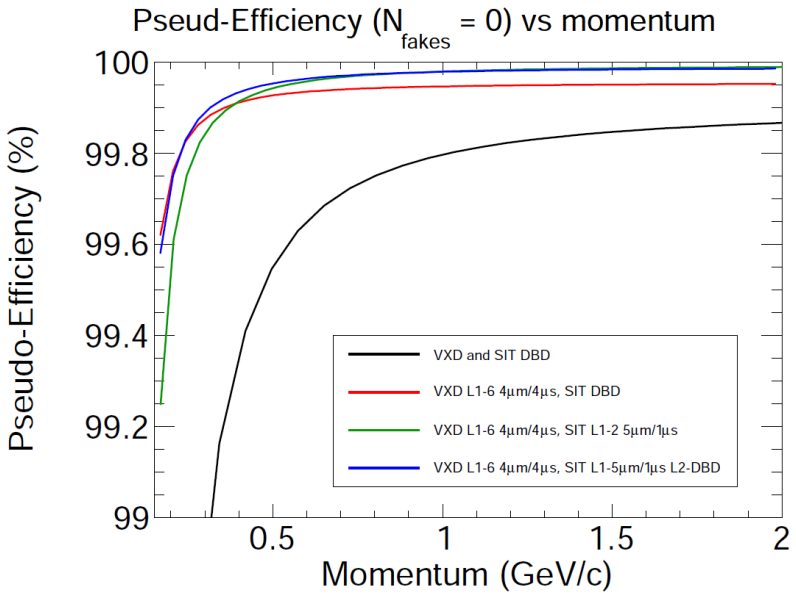
- **Track resolution and efficiency main aspects for tracker design. Mainly dependent on**
  - Geometry (material distri.), detector performances (σ_{sp}, $t_{R.O.}$, ε_{det}), and hit rate (environment)

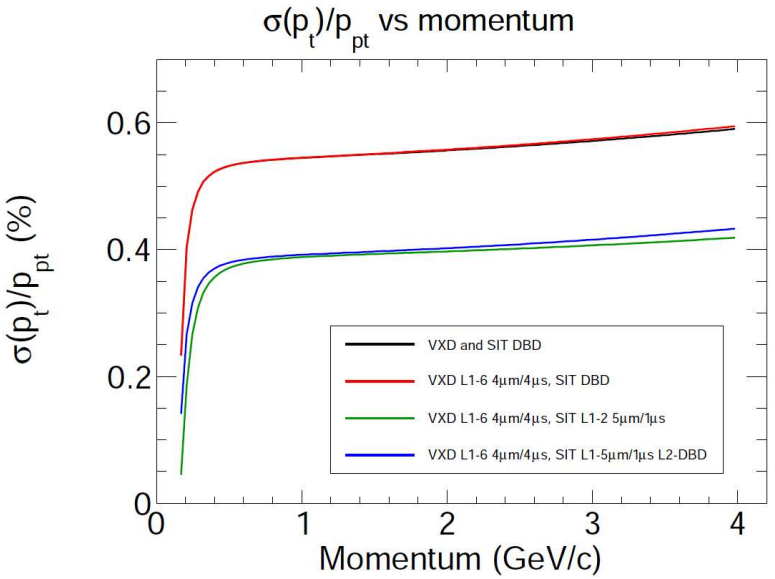
- **Guariguanchi Tool: analytical calculation of average track resolution and pseudo tracking efficiency**
  - Average track resolution calculated using nominal trajectory and covariance matrix (including multiple scattering) of measured points
  - Pseudo-efficiency calculated with simple model of probability for adding background hits to track

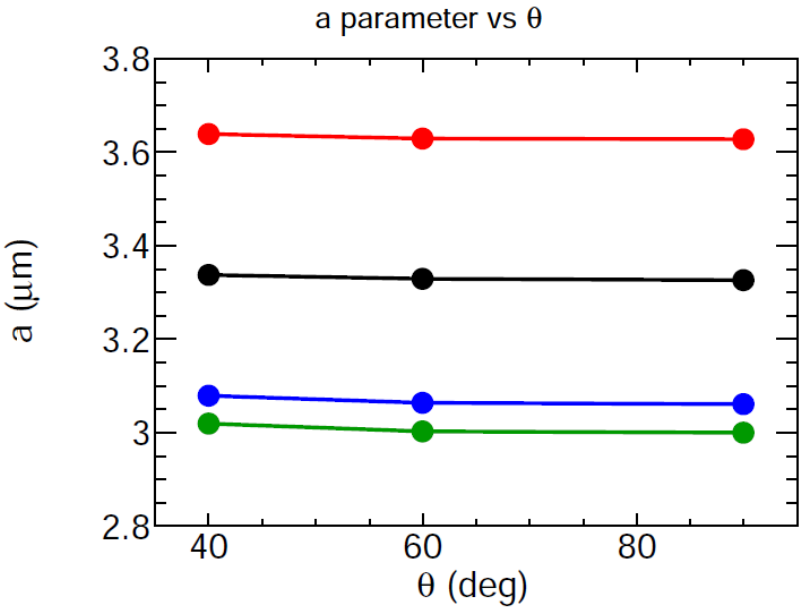
- **Calculation ignores effects only accounted for with full simulation, but it has some advantages**
  - Quick calculation of tracking performances for several geometries
  - Can be used to identify the crucial parameters in detector optimization process
  - Identify subset of detector geometries for full simulation

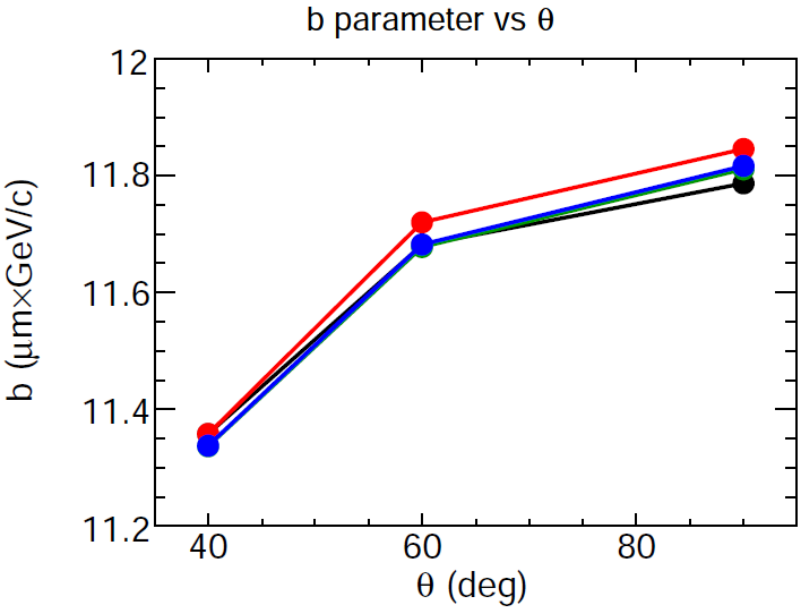


GUARIGUANCHI: Rec. Eff., Pt & DCA Resolution









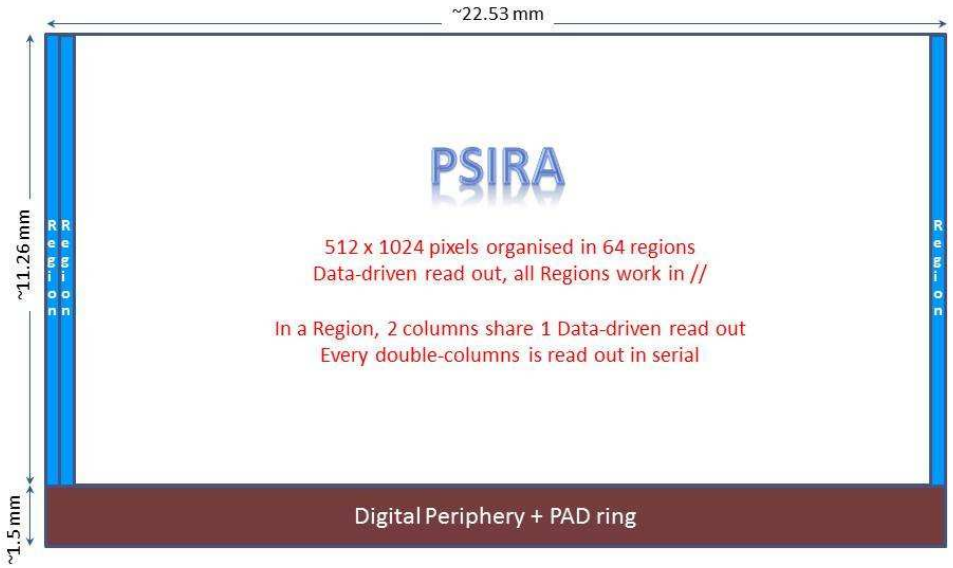
- **Ccl:** Pixellated SIT improves (moderately) tracking & vertexing wrt DBD (together with $4\mu m$, 4 μs VXD)

SUMMARY

- **Double-sided, pixellated SIT can be envisaged, based on present achievements of CPS (ALICE $\rightarrowtail$ CBM) and ultra-light double-sided ladders (PLUME)**

- **Expected performances for the ILD-SIT:**
  - CPS allow for double-sided layers $\Rrightarrow$ mini-vectors
  - $\sigma_{sp} \gtrsim 5\ \mu m$ in both directions
  - $\Delta t \sim 1\ \mu s$ **to be confirmed**

    by MC simulation of signal hit density



- **Remarks:**
  - Option under study: store data on chip during full train. followed by slow, low power, data transfer and to outer (& second ?) layer(s) of VXD
  - A faster read-out needs another step in R&D achievments (on-going)
  - R&D also addresses power saving together with **mild power cycling**