ECAL Silicon-Tungsten in ILD

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Collaboration between
IN2P3 laboratories (LLR – LAL – LPSC – LPNHE – Omega)
& Japan institutes (University of Kyushu, KEK)

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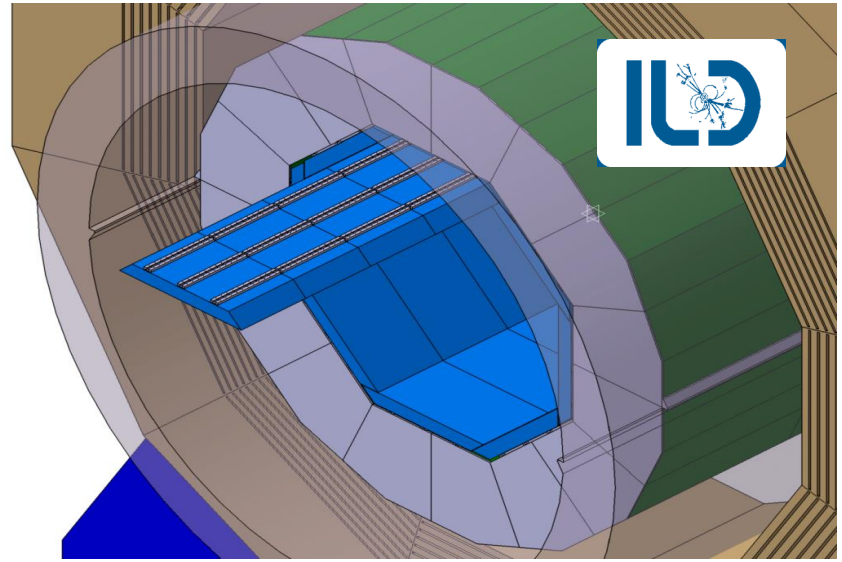
With contracts from IAF-France and EU

OUTLINE

- A small recall
- optimisation
- Test beam small prototype (Single PCB, multi Layers)
- R&D for the full scale device

Useful to recall the basic reasons for such an expensive device
(it is sometime forgotten, thinking we have no good reasons to propose it !!)



Tungsten radiator (X_0 = 3.5 mm, R_M = 9 mm, λ_I = 96 mm)

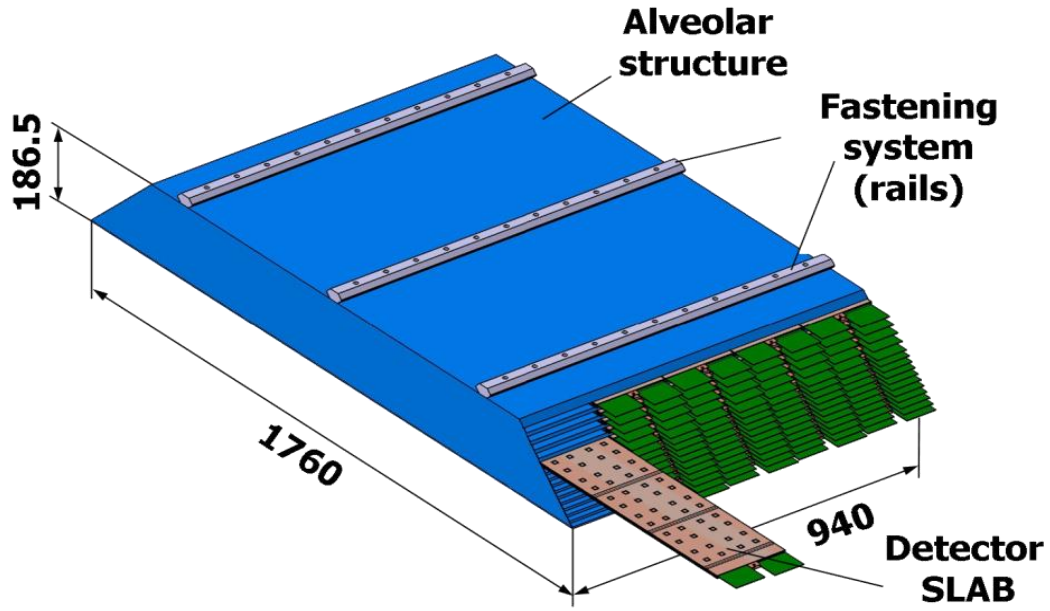
- Narrow showers
- Assures compact design (overall ECAL thickness)

Silicon as active material

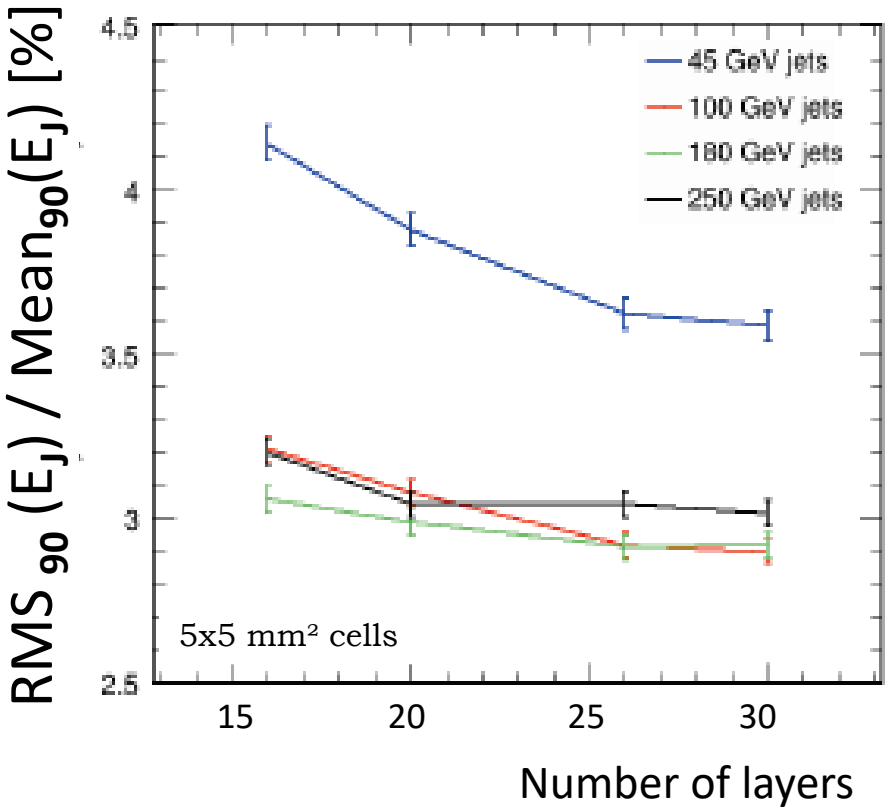
- Support compact design for a excellent S/N at MIP
- Allows for ~any pixelisation
- Robust technology
- Excellent signal/noise ratio: ≥10
- Intrisic stability (vs environment, aging)
- Timing capability
- Intrinsic linearity (number of mip)

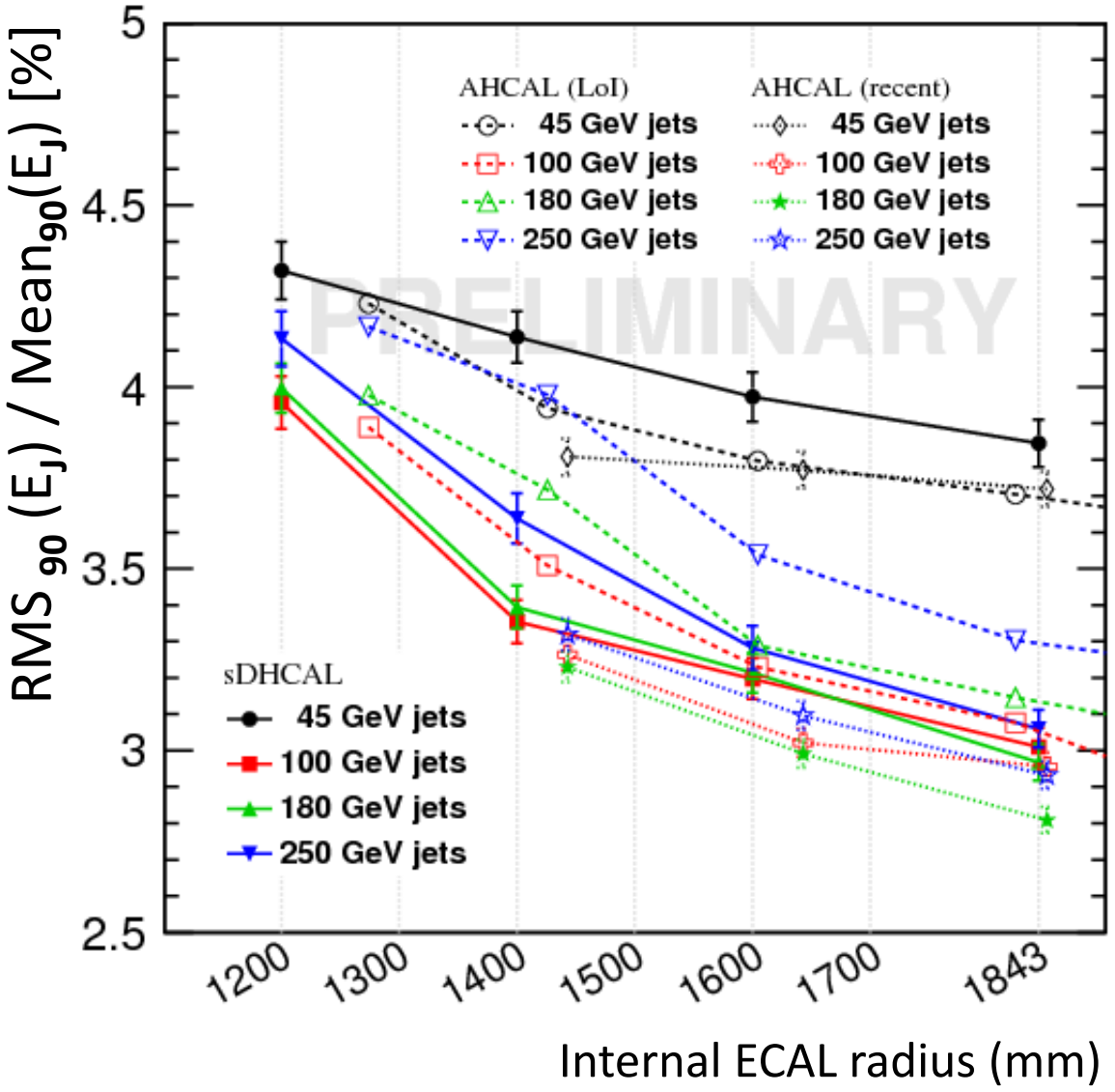
Tungsten–Carbon alveolar structure

- Minimal structural dead-spaces
- Scalability
- Easy assembling



Work on cost optimisation **before** the staging proposal





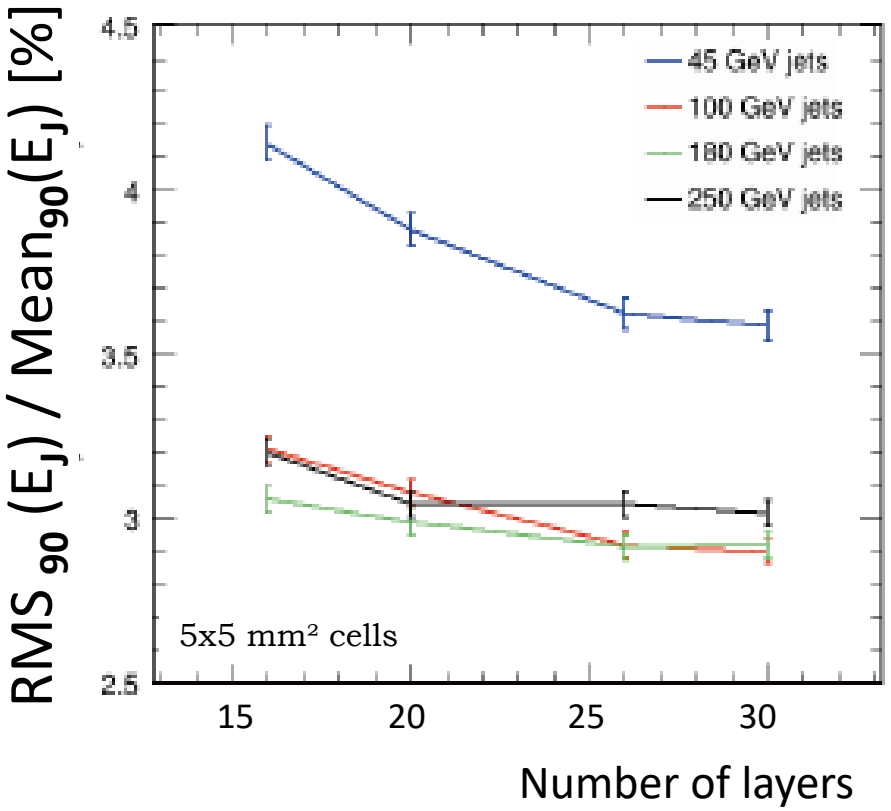
ILC Staging

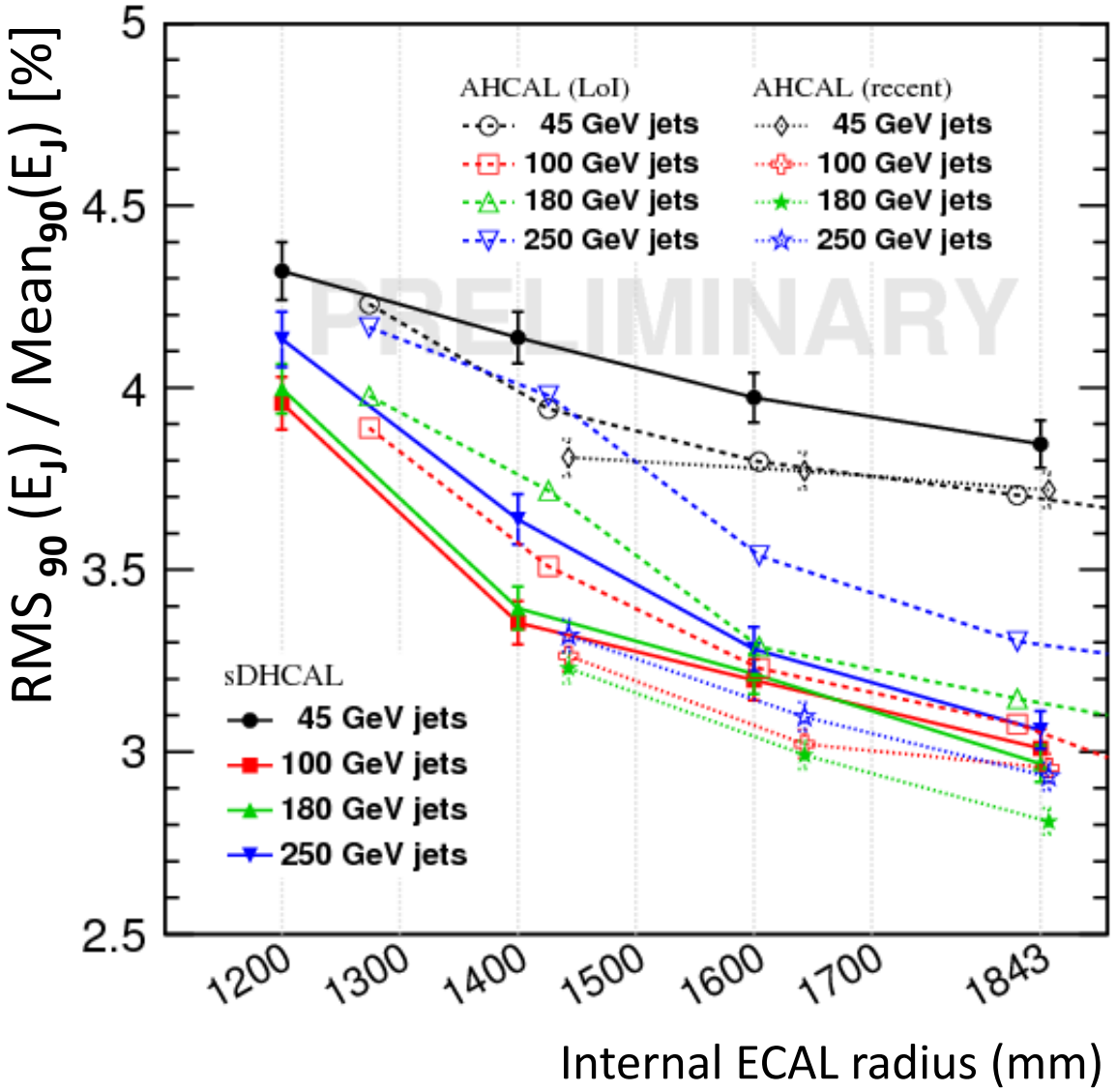
ILC running at 250 GeV , with 500 GeV possible !!

What does it change for ECAL .

- The need for boson separation with di-jet mass still true (but jet energy smaller) (WW, ZZ, ZH $\rightarrow$ 4 jets)
- The large number of channels still there to perform PFA (but $\Delta E/E$ more important & use of EFLOW mitigated …iteration)
- The shower/shower local separation still there (Molière radius and below)
- Optimization based on decreasing radius and reduce # layer ?? TO BE DONE

A new feeling , **AFTER** the staging proposal





Our conclusion :

ALL the good reasons choosing silicon are still valid

…..

Keep going with Silicon ECAL

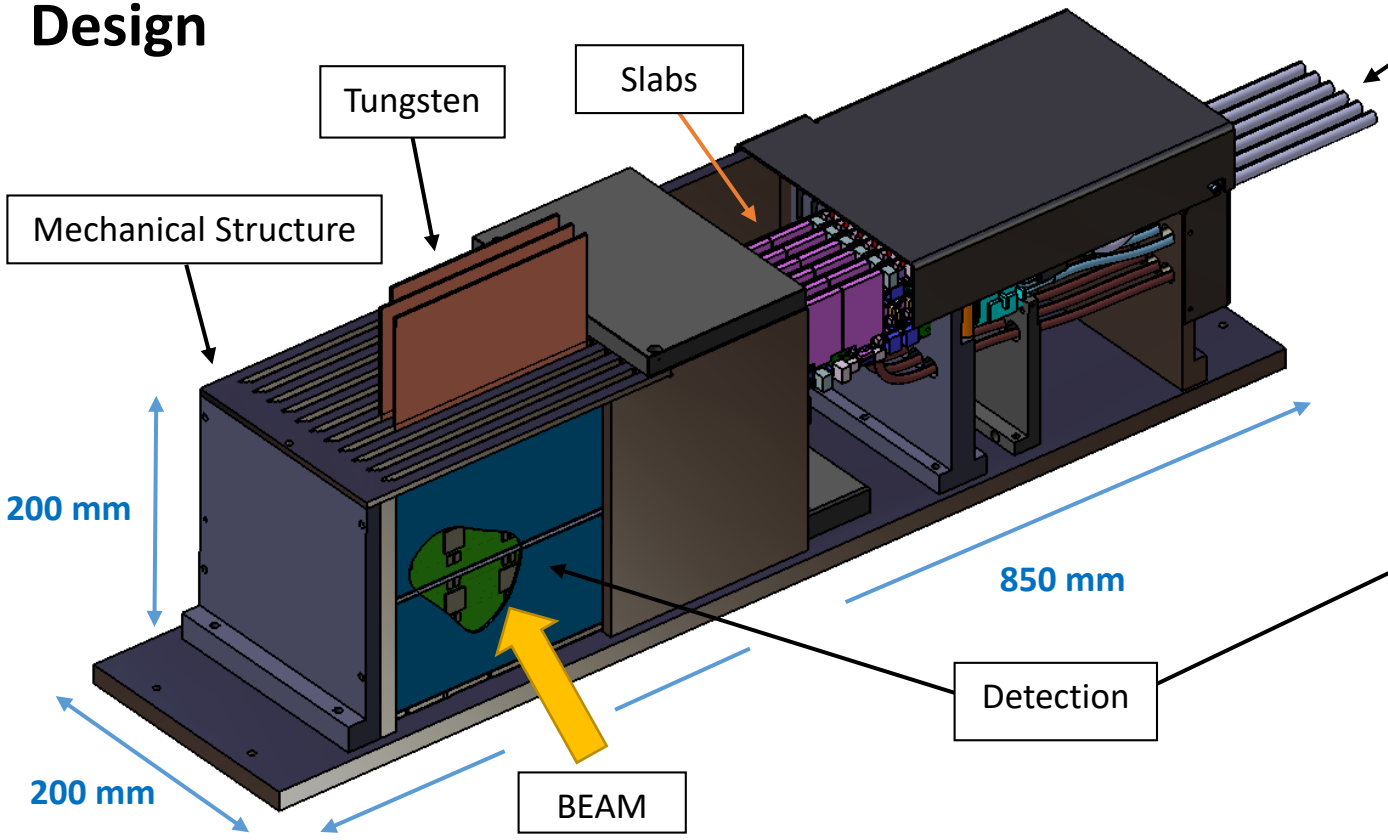
Initial Design for Beam Test Structure

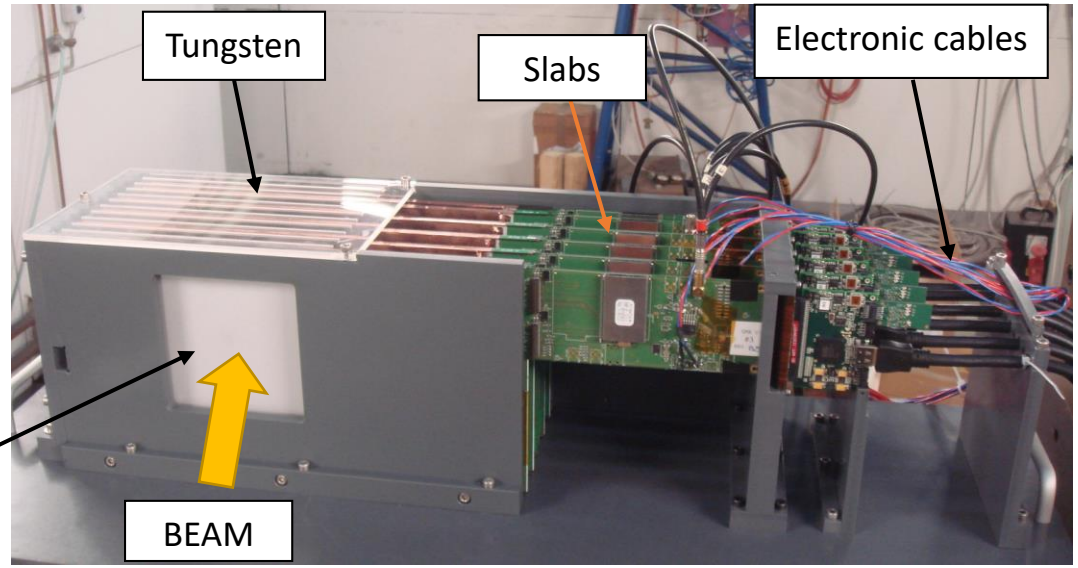
Specifications

- 10 slabs assembly
- Equal distance between slabs
- Possibility to insert 3 different thicknesses of tungsten between slabs

Constant gap between slabs : 8 mm
Constant gap between wafers : 15 mm

Design

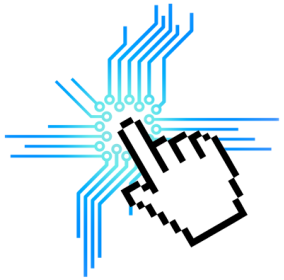




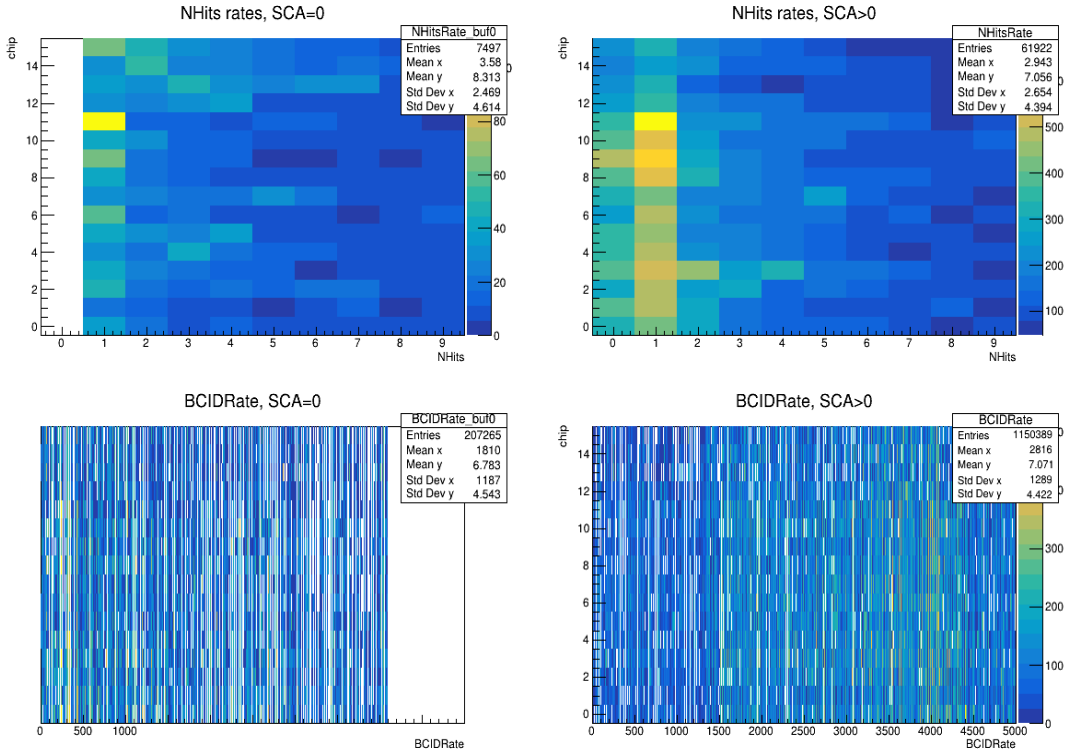
Desy beam test (2012)

New DAQ software

New Version Pyrame
flexible online monitoring system



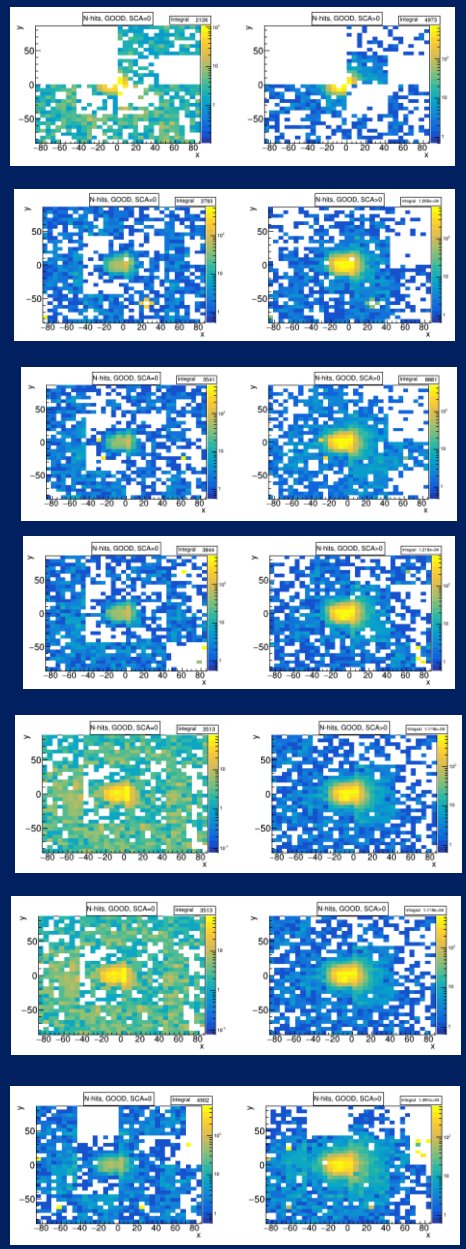
- Real-time data distribution between modules
- Chainable : treatment pipelines
- Data consistency checks
- 100MB/s by channel
- Automatic sub-sampling mechanism
- Available for C/C++
- Ease a lot the online monitor development



Si-W Ecal data integrity online monitor

Beam Test JUNE 2017 – DESY

Start with 7 layers

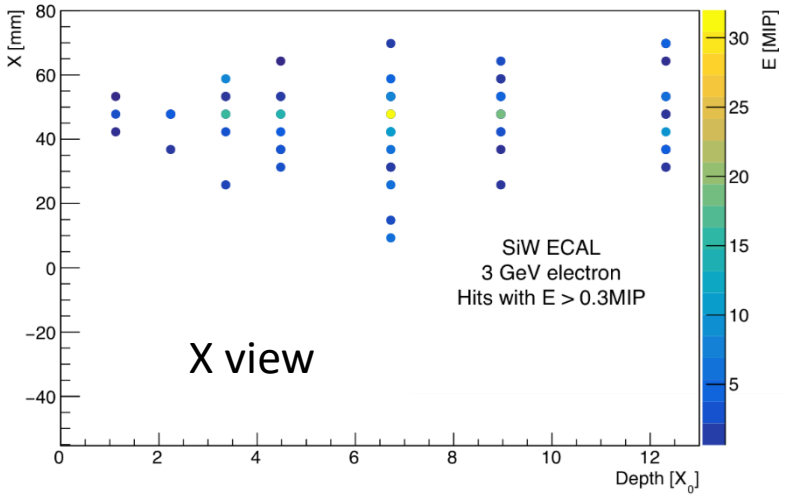


- DESY Test Beam , electron from 1 to 6 GeV
- DAQ use PYRAM 3 (100 MB/s)
- About 10 layers SCALABLE to ILD geometry
  (PCB+Si wafers has the size adapted to ILD geometry)
- Mimic ILC beam time structure
  (DAQ-on at 5Hz , for 2.5 ms spill (train-like))

← Results looks OK, 3 hours after installation, but need tuning (threshold, noise cut, etc..)

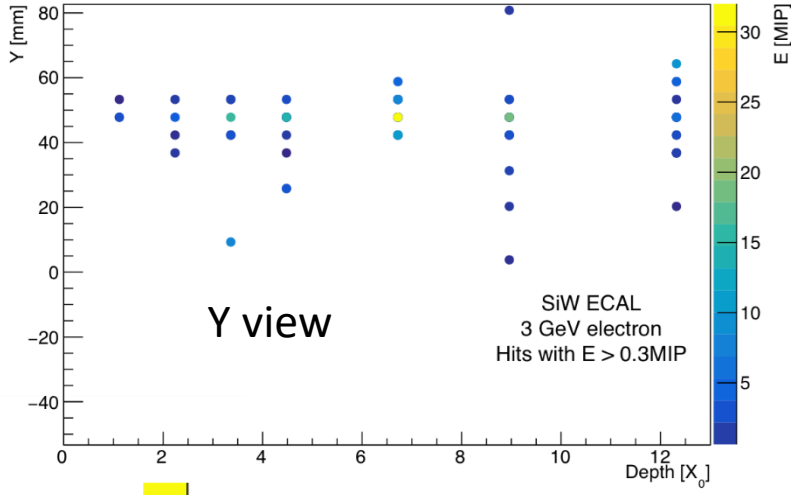
A lot to do to quantify the quality (S/N at mip, uniformity, fraction of dead channel, etc…) and to provide a guidance for final detector choices and assembling

Beam Test JUNE 2017 – DESY

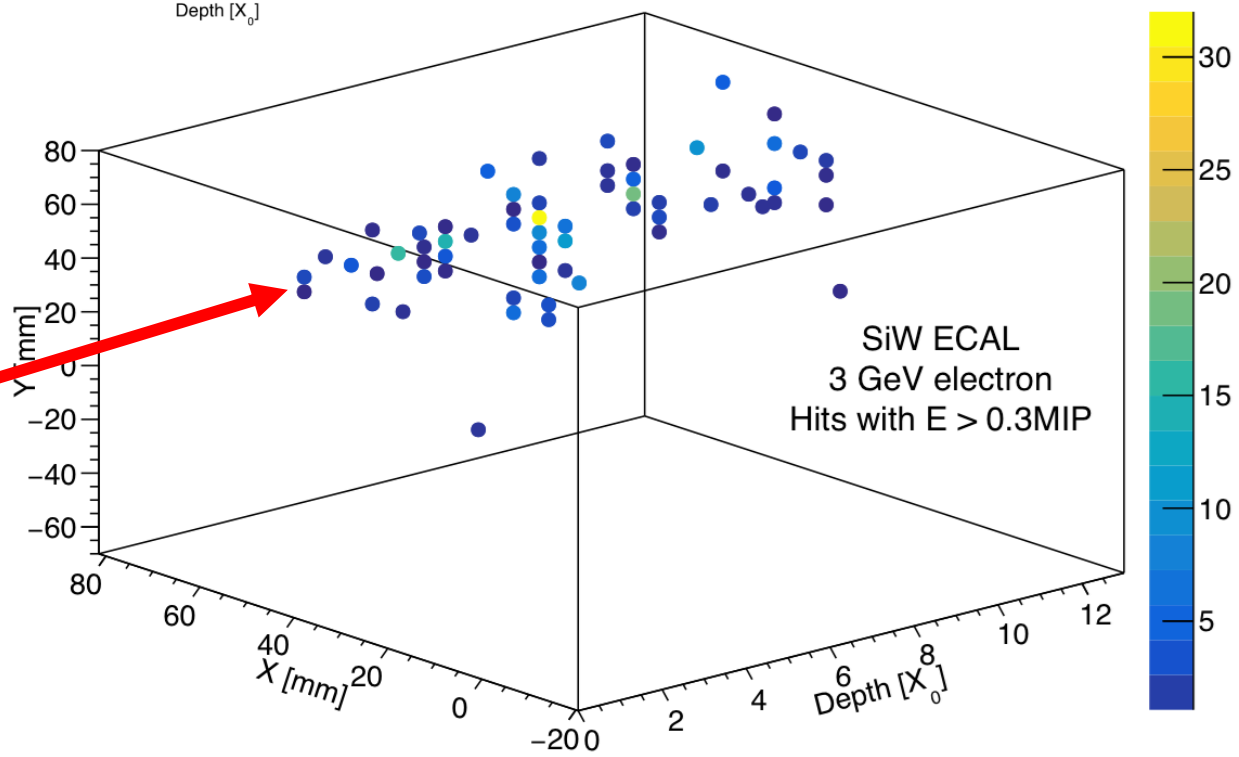


1024 channels/layer

Proto with > 7K channels



Electron beam



PLEASE !!
Note the small number of noisy channels (cut at 0.3 mip)

BESIDE test beam (single ASU, multi layers)

- Work on the full scale device
- New VFE SK2A
- Long slab studies
- Cooling and services

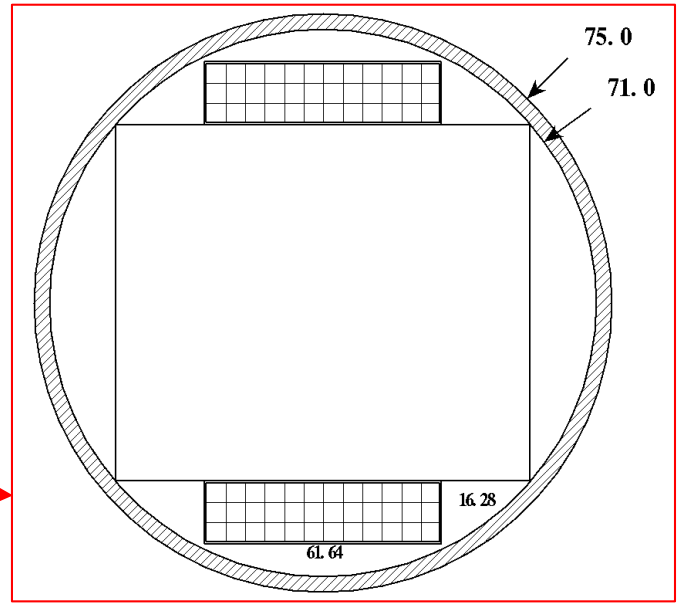
specific R&D for large scale device

- Services
  - power, mechanical support, plumbing, lineout etc… for ECAL
  - same for internal devices (tracker (TPC, SIT) and VDET)

- Large scale device
  - Long slab
  - large CFi-W structure
  - Relation with industry for production

- Assembling
  - off-site test
  - on-site assembling
  - inserting inside the ILD detector

- Production and cost
  - 8” wafers (new constraint from producers > constraint on geometry)
  - Use of small rectangles per wafers (where , level of cost reduction)
  - Reduction of internal radius .. Impact on mechanical model,



The options taken today in ILD are :

- Silicon square matrices (8” wafer a priori)
  > possible use small matrices in border of wafer – cost mitigation
  > square event !! Need to manage the Xtalk pixels-guardring

- Geometry “a la Videau”

- Carbon fiber – Tungsten structure

- Long slab inserted into the alveola (R&D on connexion, signal integrity, etc..)

- Passive cooling inside (all “plumbing” outside) …. Thanks to powerpulsing

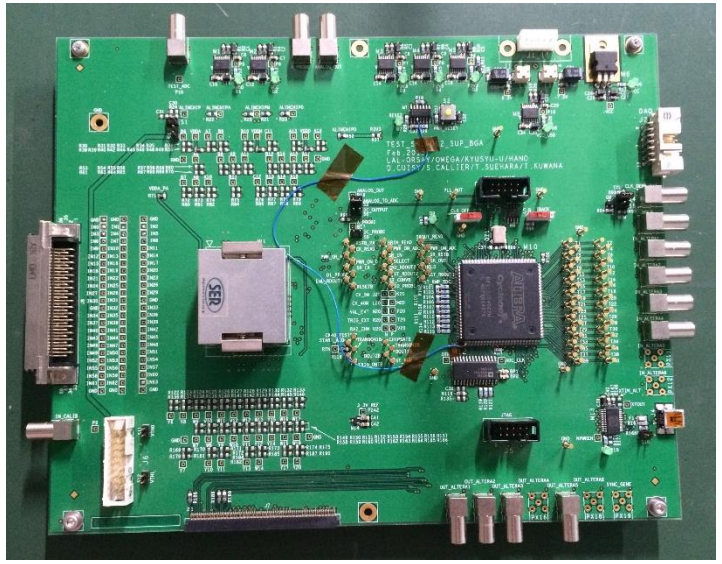
- VFE asic inside the detector (packaged allows industrial test, leading to chip burning).
  New version arrive this year (SK2A) - Tests look very promising

- INTERNAL RADIUS & number of Layers …. Still open

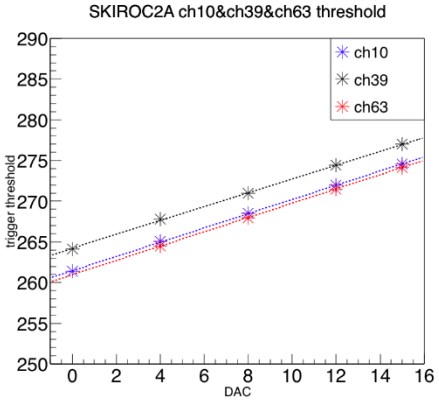
SKIROC2 → 2A improvements

Improvements at SKIROC2A

- Individual trigger threshold control
  (dynamic range too narrow in SKIROC2)
  → ~ 0.15 MIP dynamic range obtained in SKIROC2A
- TDC ramp voltage profile is changed (less dead time)
- Improved Substrate and Input Shielding
- Noise with the external trigger improved
- Trigerless event reduced
- AutoGain selection (with TDC) fixed
- Test of the naked dies (issue fixed)



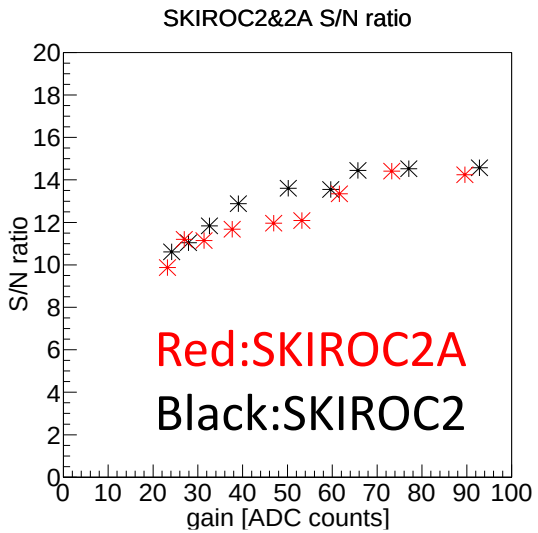
Measurement with testboard with a BGA socket for SKIROC2/A (Kyushu Univ.)



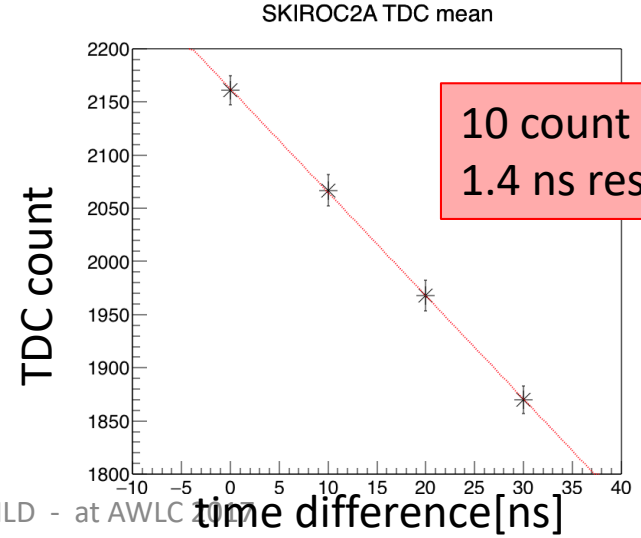
Individual threshold control at SKIROC2A

<SKIROC2 & SKIROC2A S/N ratio>

No significant difference, S/N=13-14



< SKIROC2A TDC>



10 count / ns
1.4 ns resolution

ECAL Services & Cables (Baseline)

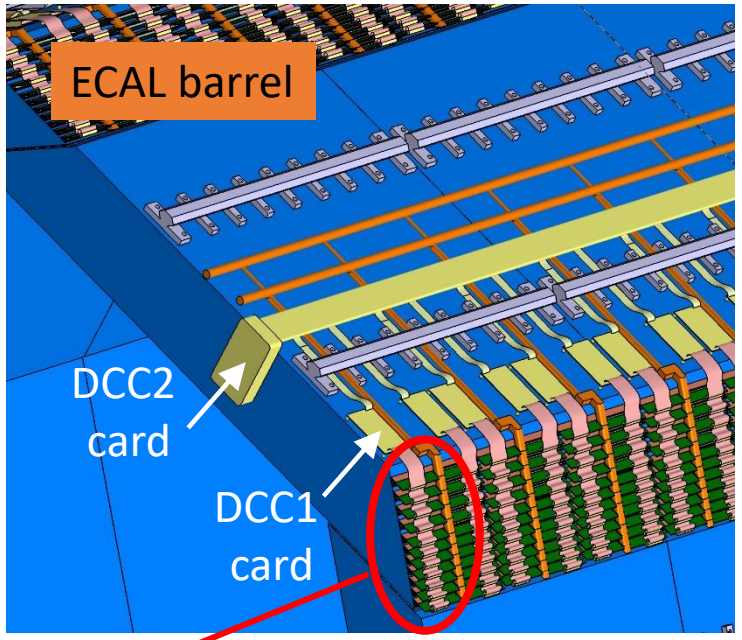
Power, cables and cooling would run between HCAL and ECAL on the back of ECAL (the way it is shown in the picture which exhibits the principle rather than any real design)

The paths of cables and cooling interfere strongly (cross).
As a working assumption the cables would run to one end of the staves and the cooling to the other end.

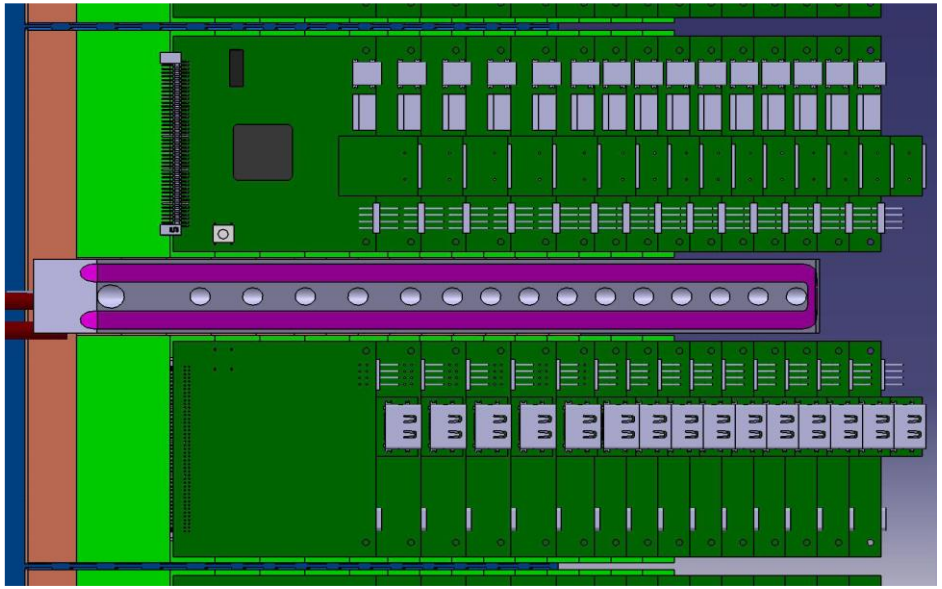
- DCC1 figures a concentration/distribution at the alveoli level
- DCC2 (or Hub2) a concentration/distribution at the stave level.

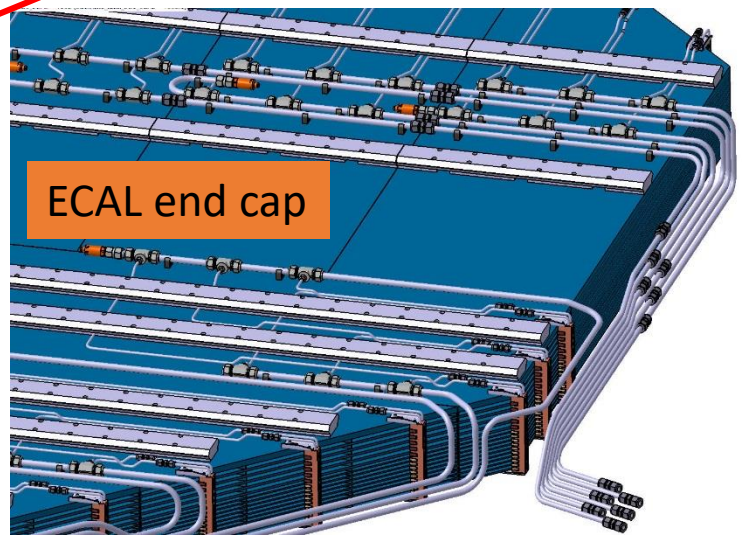
From then cables or fibres run along each sub-detectors to the outside

Same principle will apply for End cap cooling and cables



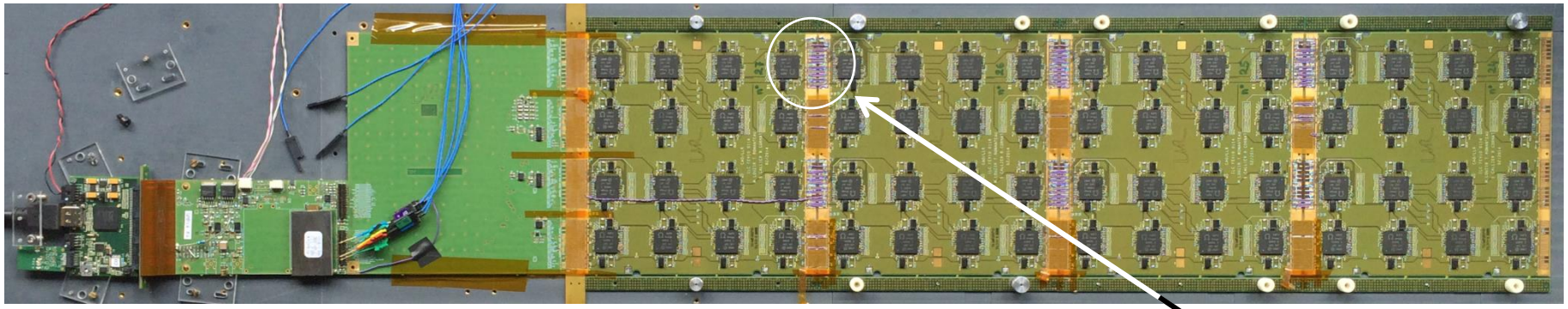
Pipes of cooling system





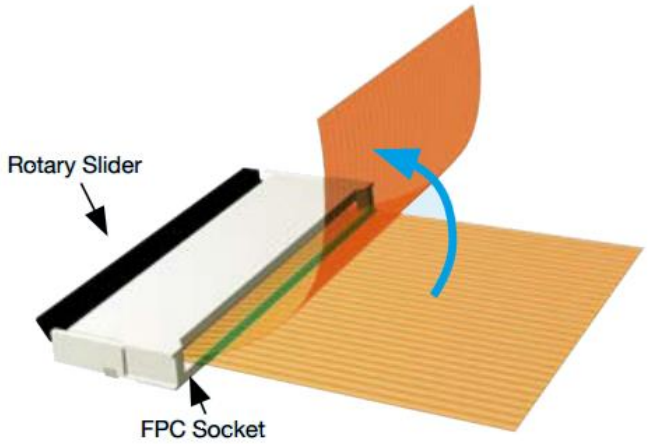
How to make 2m long device* in 4T ?
(different problems from AHCAL)

Preliminary long SLAB studies
ASU connections / first steps



ASU connections / first steps

- Many short circuits detected: kapton replaced by small wires (new process to connect ASU: in run)
- SlowControl on 4 ASU ✓
- Acquisition (trigger level) on 3 ASU
  (no acquisition on 4 ASU, short circuits probably always presents: to debug)
- Power loss along the slab



* Long slab barrel is ~R_{intern} and for endcap ~R_{intern} + (25+10) cm

Preliminary long SLAB studies

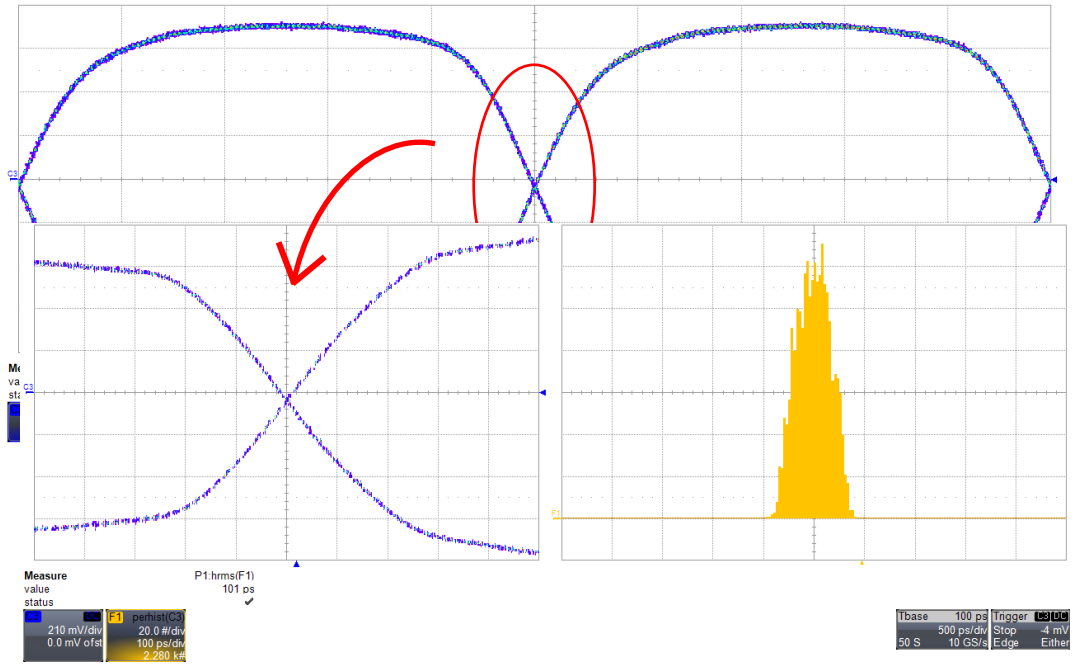
Clocks eyes diagram

Long SLAB contains 8/10 ASU cards, so we must checks clocks on the last card.

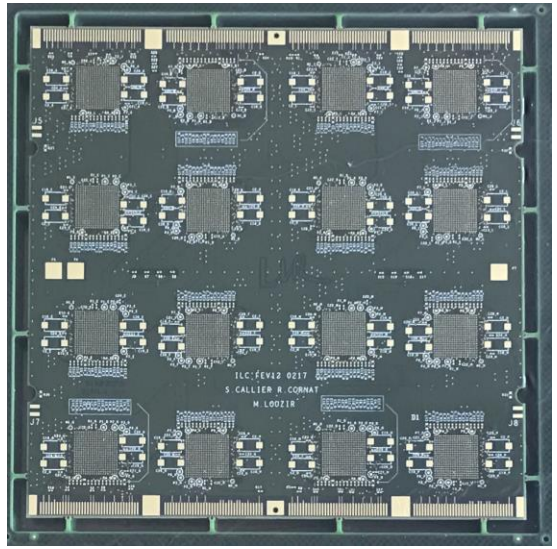
2 clocks :

- fast clock 40MHz:
  - Jitter = 100ps ✓

- slow clock 5MHz:
  - Jitter = 120 ps ✓



Long slab – R&D to do



- Make a NEW long SLAB with NEW FEV12 and with SKIROC2 then use SK2A
- Make comissioning of new board with SKIROC 2
- Connect 2 new ASU with kapton/connectors
  - Mesure of clock integrity
  - Configure the 2 ASU (analysis of JTAG clock)
  - Take data (analysis of power supply)
  - Glue baby wafer (design a board to inject current on channels (to emulate the leakage current of wafer))
- Make comissioning of 2 ASU then 4, 6 and 8

- Maybe think about a power tree if our solution failed
- Take care of memory inside the DIF (to avoid to much busy or full memory) ➔ find the frequency/amount data limitation
- Modify the mechanical plate to receive ASU + baby wafer and possibility to rotate electronics (to glue baby wafer)

CONCLUSION

In PROGESS

- Test beam with 7 layers-single PCB ,
  VFE inside, good understanding of overall system – analysis will start soon

- R&D for full scale detector
  - Long slab
  - Cooling and mechanics
  - Cost reduction (Rint. , Number of layers, use of wafers edge…)

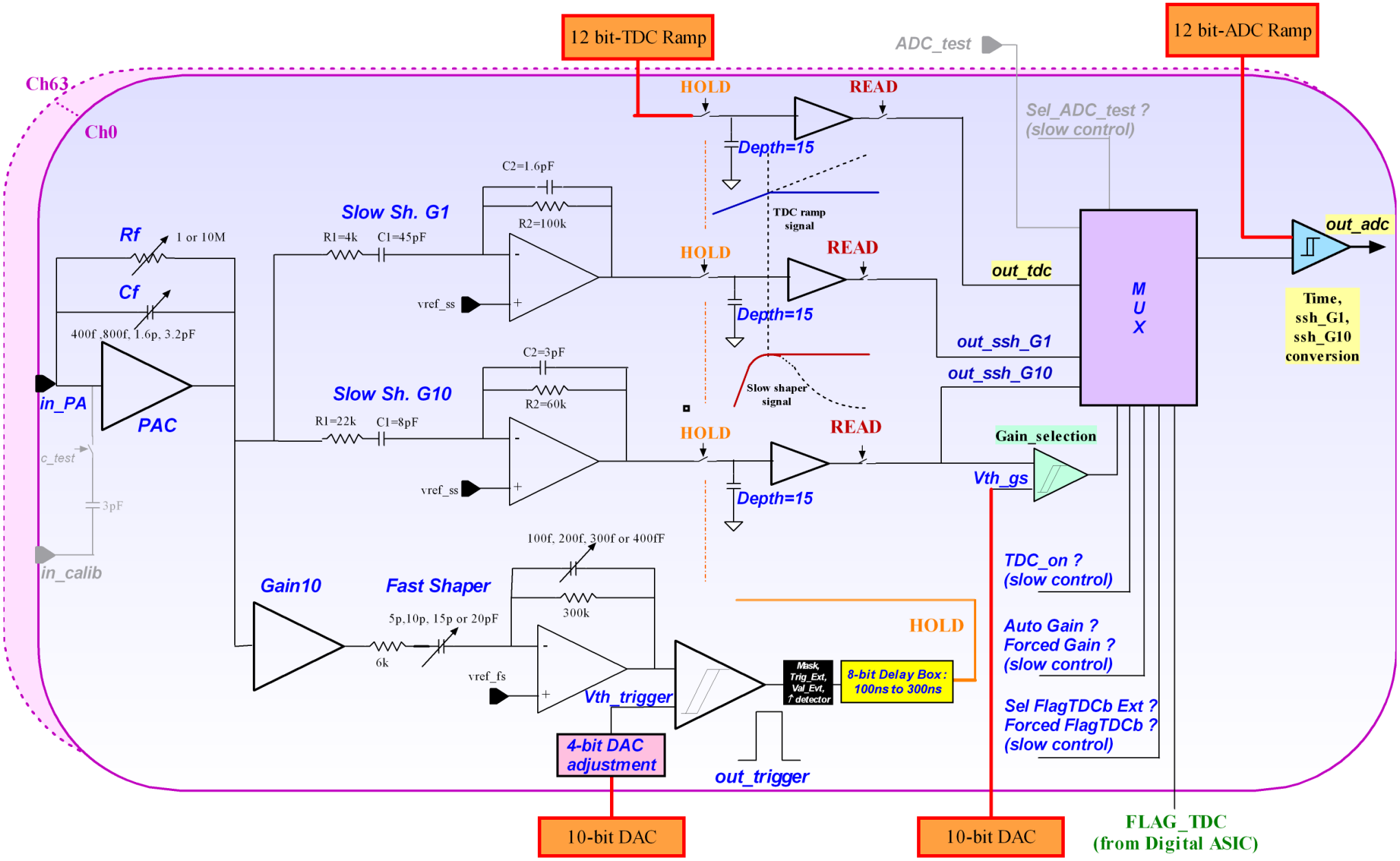
TO DO

- Finalize the R&D for a realistic ECAL proposal in 3 years

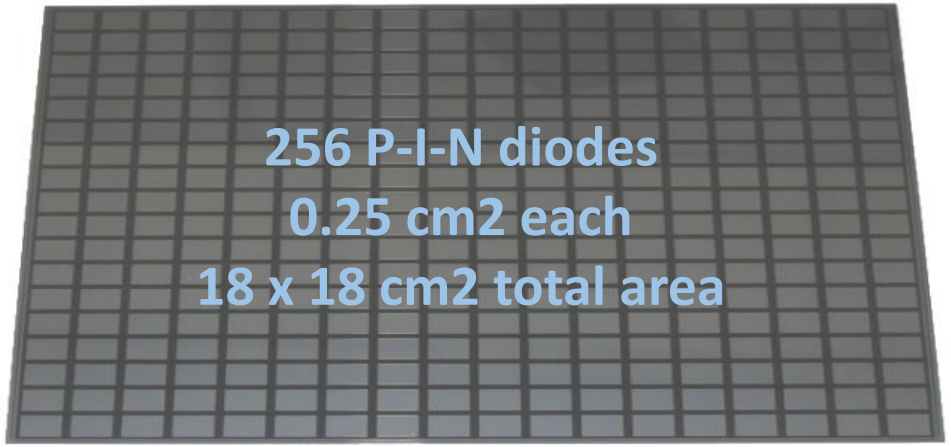
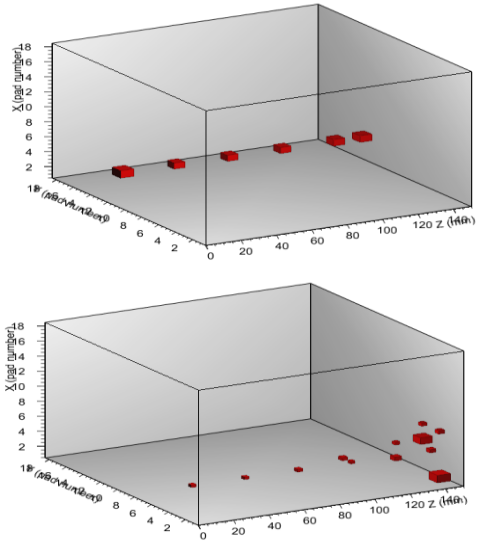
- Simulation to optimize for Ecms=250 Gev , upgradable to 500 GeV

BACK UP

SKIROC2 / 2A Analogue core



SKIROC2A Modifications

- BUG CORRECTIONS
  - Some « Zero events » during digitization **: OK** (added delays, cf. SP2C)
  - Substrate Shielding, Inputs Shielding **: IMPROVED** (added connections)
  - Test mode for naked dies (voltage drop off & missing pads) : CORRECTED (but not tested, N/A in BGA package)
  - Trig Ext path no more thru delay cells to store the analog data **: OK**

- IMPROVEMENTS
  - 4-bit DAC for trigger level adjustment **: OPTIMIZED to 1 DAC unit**
  - Bandgap **: CHANGED** (from chip HR3)
  - Delay Cell : Slightly IMPROVED
  - AutoGain Selection **: CHANGED : OK** (from SP2C)