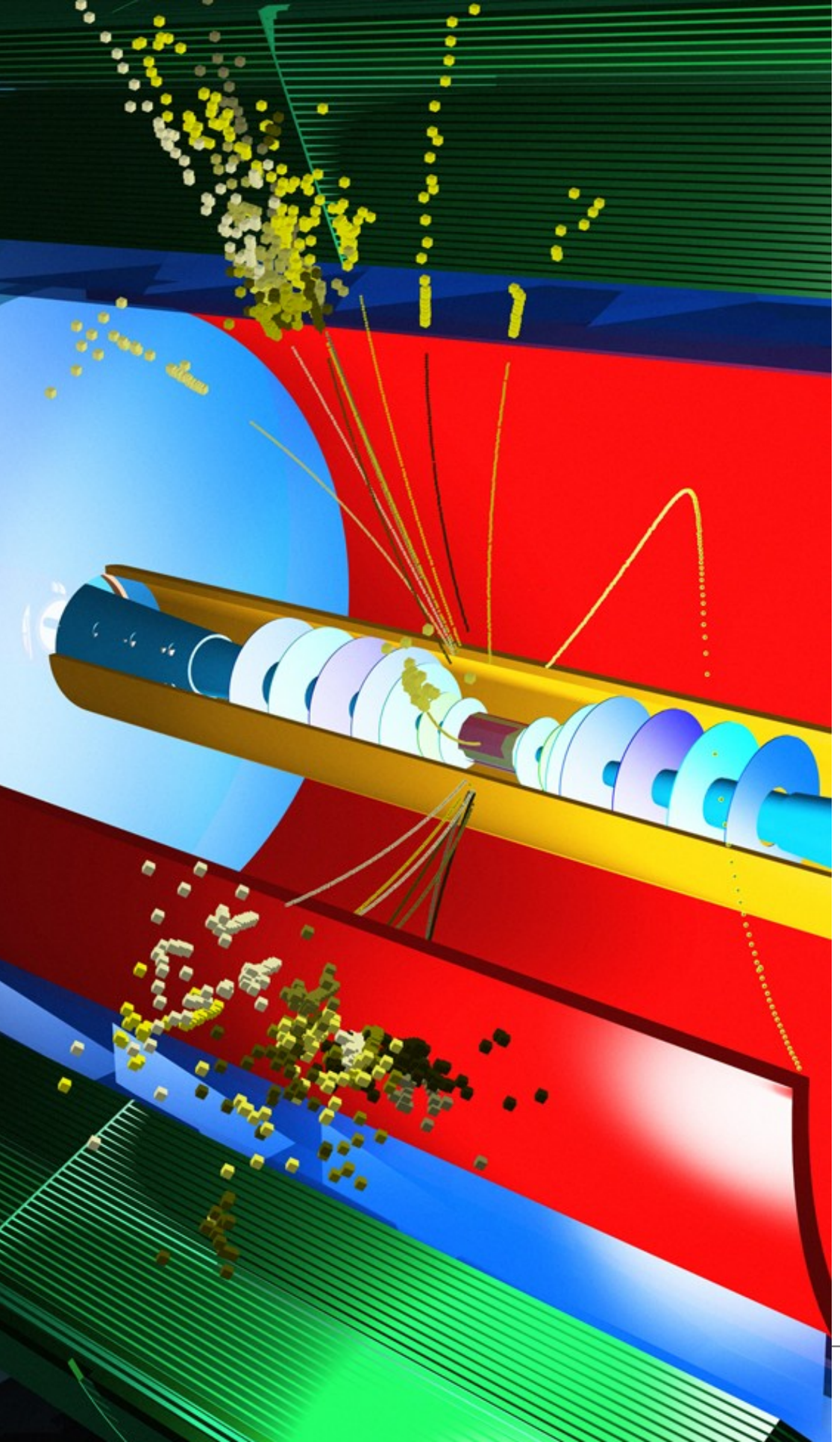


Vertex detector and forward tracking disks

+ other silicon (SIT, SET)

ILD technical meeting
Lyon, April 2017

Marcel Vos IFIC (U. Valencia/CSIC), Spain
With inputs from Auguste Besson, Akimasa Ishikawa, David Moya, Alejandro Perez, Miguel Angel Villarejo, Ivan Vila

Marcel.Vos@ific.uv.es

DEPFET Active Pixel Detector

ILD vertex detector

	a (μm)	b (μm GeV)
LEP	25	70
SLD	8	33
LHC	12	70
ILC	5	10

Vertex detector

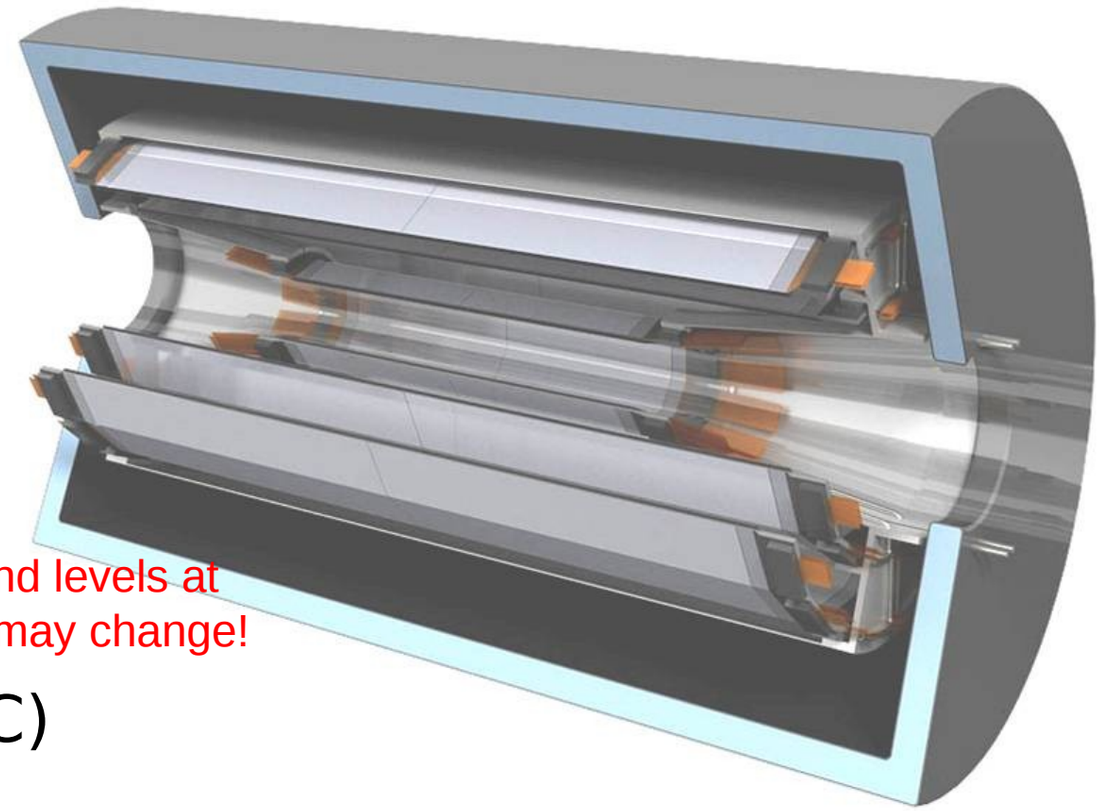
Reconstruct primary and secondary vertices,

flavour tagging, bottom/charm separation

Large polar angle coverage

Unprecedented performance:

$\sigma\ (d_0) < 5 \oplus 10/(p\ \sin^{3/2}\ \theta)$



Stringent requirements

Resolution: 3 x 3 μm^2

Read-out speed: < 25/100 μs

(down to 500 ns or even 0.5 ns at CLIC)

Material: 0.1...% / layer

Background levels at
250 GeV may change!

Strongly reduce the multiple Coulomb scattering term
(0.1 % X_0 / layer ~ 100 μm Si)

DEPFET Active Pixel Detector

Where are all those Silicon people?

Main urgency of the vertex detector R&D collaborations with mature technologies (MAPs/PLUME, DEPFET) is no longer the ILC

Progress requires more funding than is achieved for ILC-targeted R&D

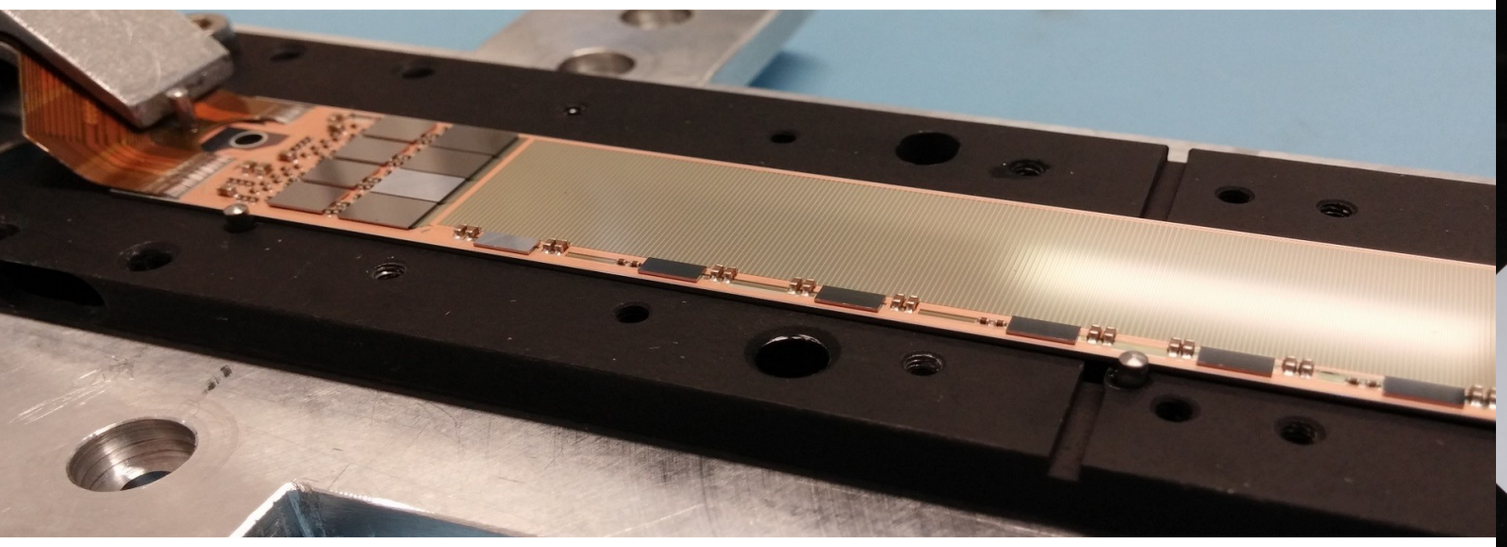
If a technology is mature it has to use its window of opportunity

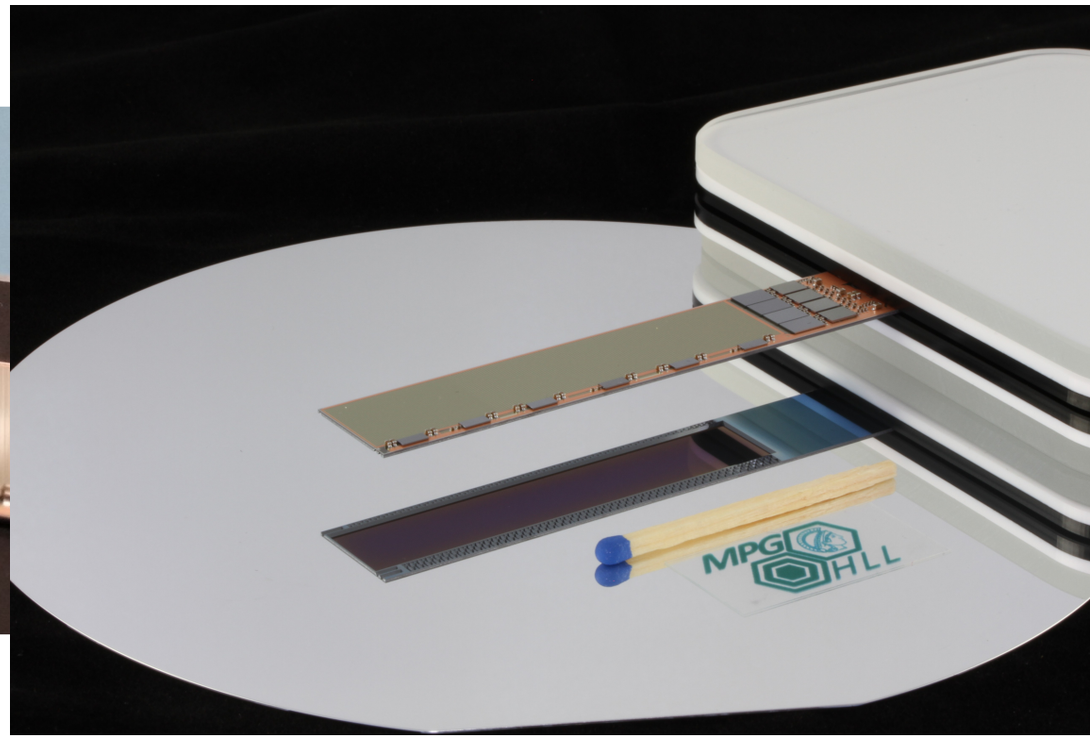
FPCCD are making steady progress. SOIPIX is new player.

The next-to-next generation of technologies (HVCMOS + 3D integrated detectors) are being pursued, with some intensity, but this effort is only very loosely connected to ILC effort.

Vertex detector R&D - DEPFET

Example: of DEPFET's O(100) members approximately 95 are entirely focused on Belle II (detector recently “rolled in”, VTX to be installed before physics run in 2018)





Fully functional ladders.... major milestone for the DEPFET project!

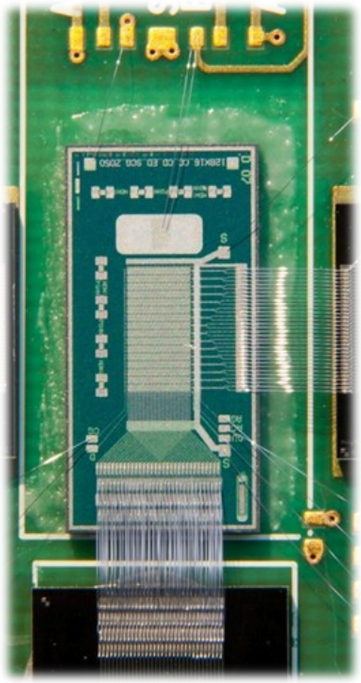
Belle II funding has been key to continue and accelerate the development of the sensors, to enable several iterations of the ASIC design, and to force the collaboration to come up with a complete solution for the off-detector system (from cables to cooling to DAQ)

Marcel.Vos@ific.uv.es

DEPFET
Active Pixel Detector

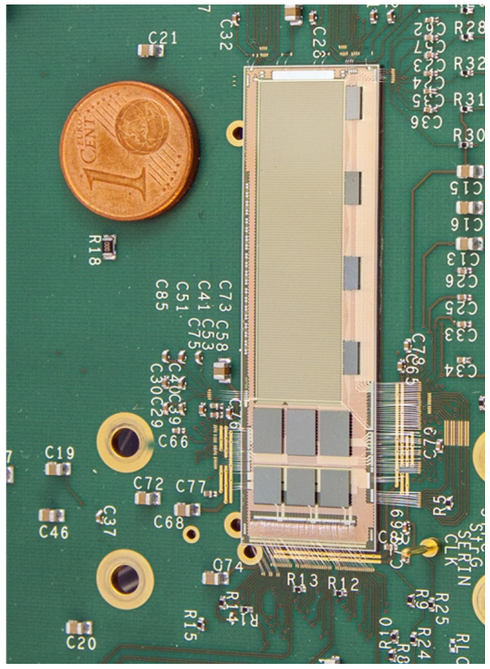
DEPFET time-line

"Early days"



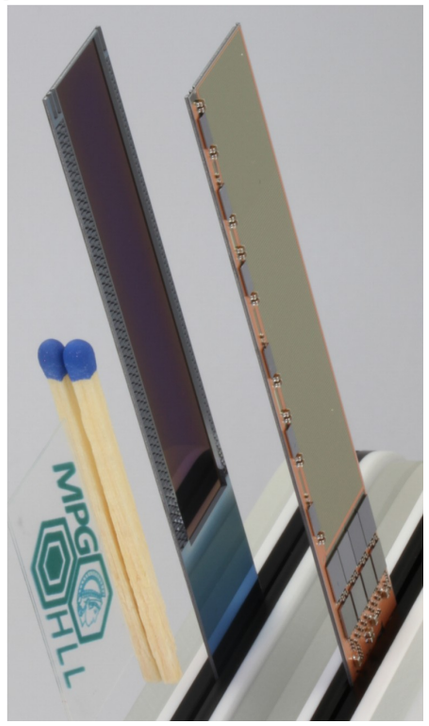
2007-2011 prototypes with O(10^3-10^4) pixels

"The most complex piece of silicon in the world", ECFA review



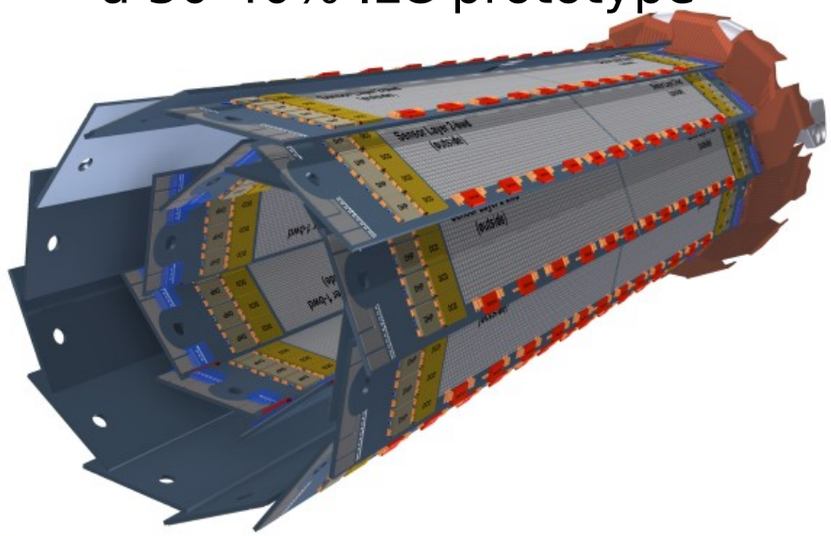
January 2014, first large-scale, multi-ASIC ladder at DESY TB

"The real thing!"



October 2015, first complete & operational Belle II ladder

The Belle II VXD
"a 30-40% ILC prototype"



Assembly Belle II VXD

DEPFET

Belle II upgrade

Proof-of-principle | Complete demonstrator | A real detector | Physics

2002.... 2007.... 2013 2014 2015 2016 2018

LC-specific detector

a vertex detector for TESLA

Small-pixel prototype with 1.5 µm resolution

DEPFET for ILC, IEEE TNS 60, 2, 2

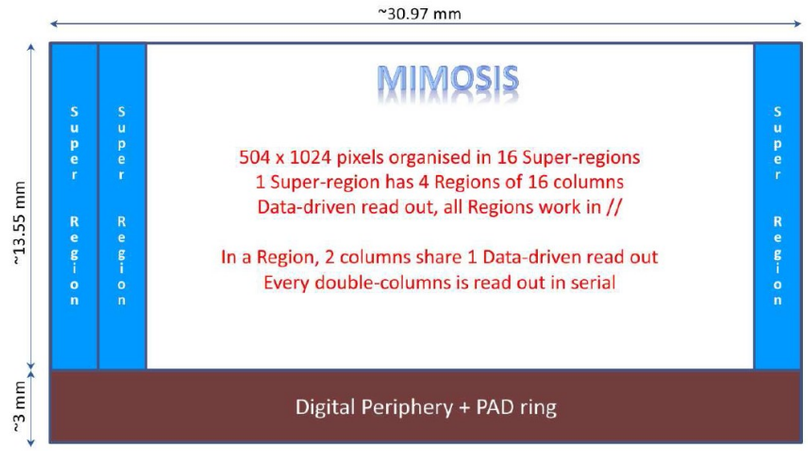
ECFA review: http://ific.uv.es/~vos/ECFA_DEPFET.pdf

DEPFET

ILC candidacy benefits from developments for Belle-II and X-rays

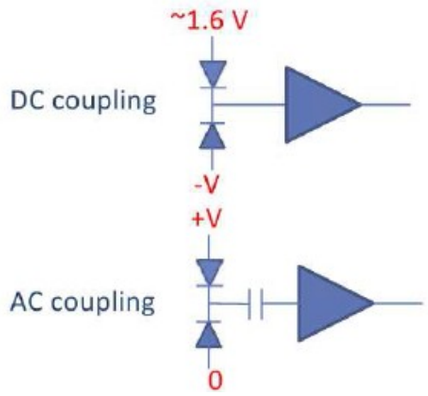
CMOS R&D (PICSEL-Strasbourg): CBM-MVD

- Asynchronous (fast) read-out architecture
  - MIMOSIS = based on ALPIDE pixel readout (ALICE-ITS upgrade)
- Specifications:
  - σ_{sp} ~ 5 µm
  - r.o. time ~ 5 µs
  - Enhanced data flux: ~1.6 Gbits/cm^2/s (peak) ➔ x 60 ITS rate
    - ➢ Revisited digital circuitry (data sparsification & transfer logic)
  - Enhanced radiation hardness: O(10 Mrad) & O(10^{14} $n_{eq(1MeV)}$)

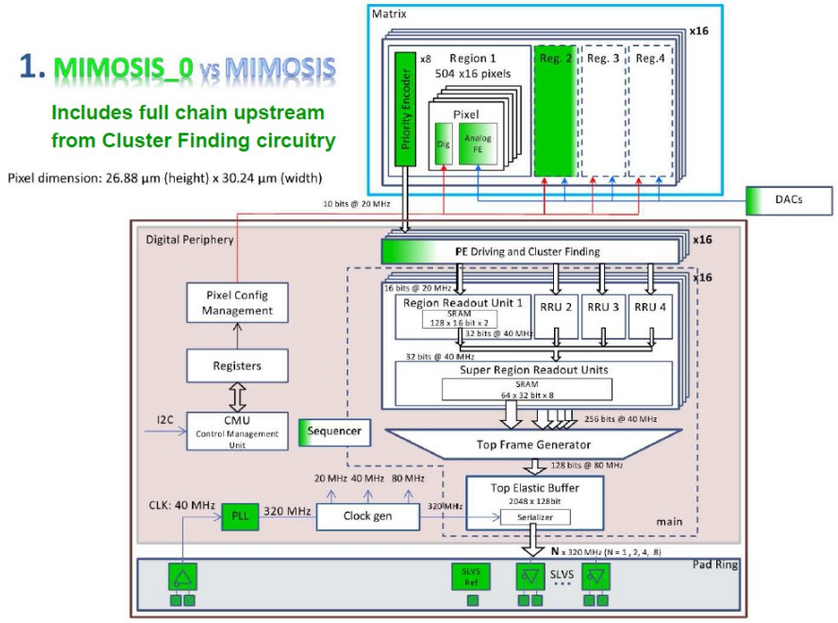


Pixel array & digital periphery developed in //

- MIMOSIS_0
  - ➢ Timing study of the data driven readout circuitry
  - ➢ DC & AC coupling foreseen to compare performances
  - ➢ Chip submitted in May 2017



- Digital Periphery
  - ➢ Design underway
    - ✓ Physical implementation of the different block
    - ✓ Timing vs Chip length
    - ✓ Data rate
    - ✓ Power estimation
  - ➢ 1st full scale prototype ~ 2018



Final preproduction sensor in early 2020

Other development: BEAST 2@ SuperKEK-B

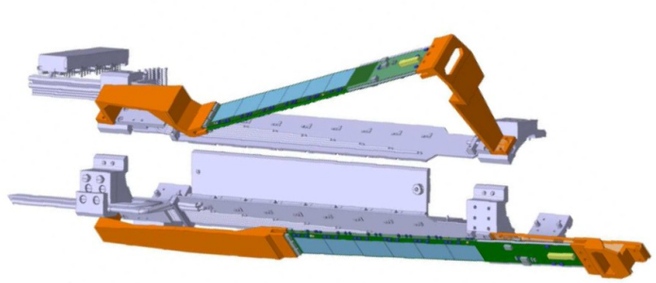
- Goal: beam background measurement For Belle II
  - Different detectors in inner volume

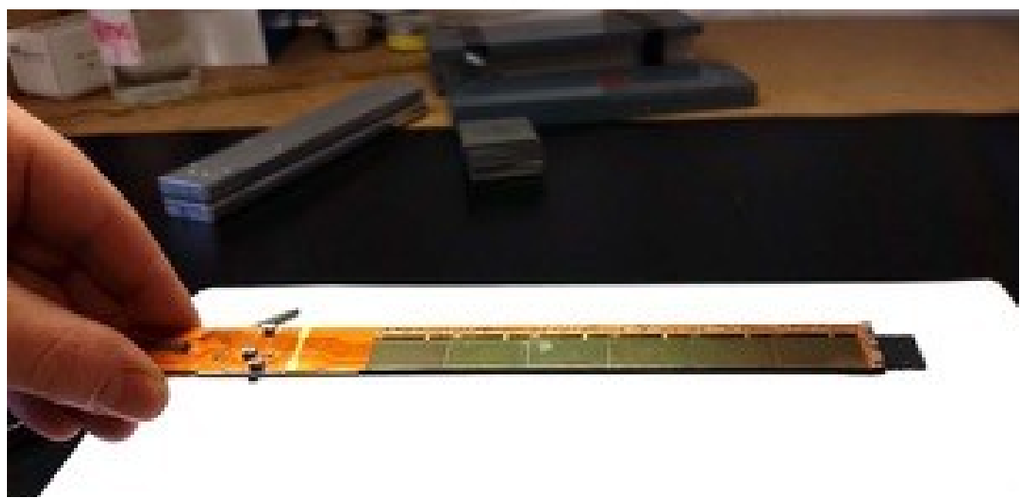
- Spin-off for ILC:
  - operation of PLUME ladders in real conditions
  - Exploiting the minivectors produced to help reconstructing soft electron trajectories

- Plume 02 prototype → Reduced mat. Budget
  - Cu flex cable (0.42 % X_0)
  - 2 ladders functional, 2 more for spares by June

- Timeline:
  - Q4 2017: Installation & comissioning
  - Q1 2018: Start of data taking

- Next steps:
  - finalize Al flex cable (0.35 % X_0)
  - Beam test @ DESY in 2017-18





FPCCD, Radiation Damage at the ILC500

- Radiation in the ILC ($1312\text{bunch},\ 0.5 \times 10^7 \text{sec/year}, \text{E}_{\text{CM}} = 500\text{GeV}$)
  - Pair background: 2.07 x 10^{11} e / cm^2 /year
  - Neutrons from beam dump: 9.25 x 10^8 n_{eq} / cm^2 / year

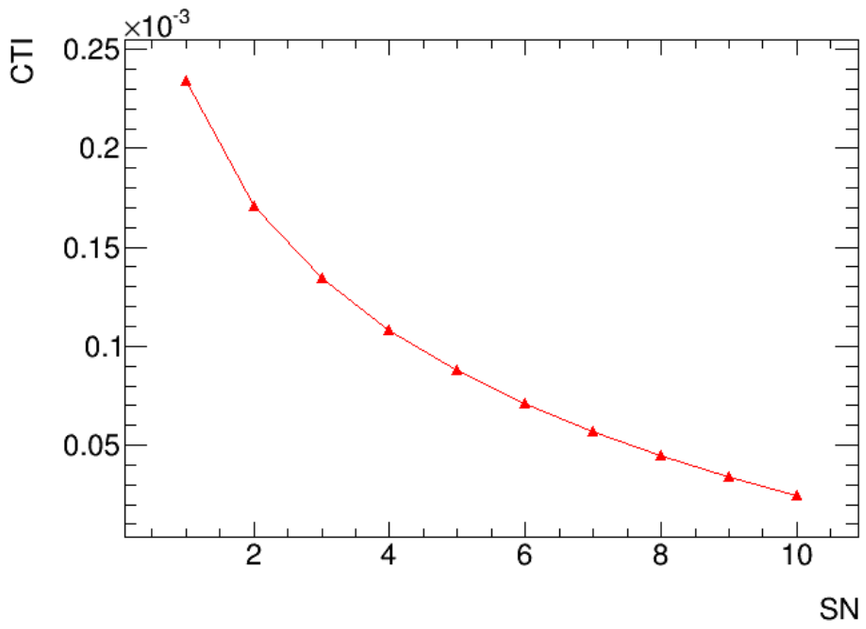
We need to simulate radiation at ILC250

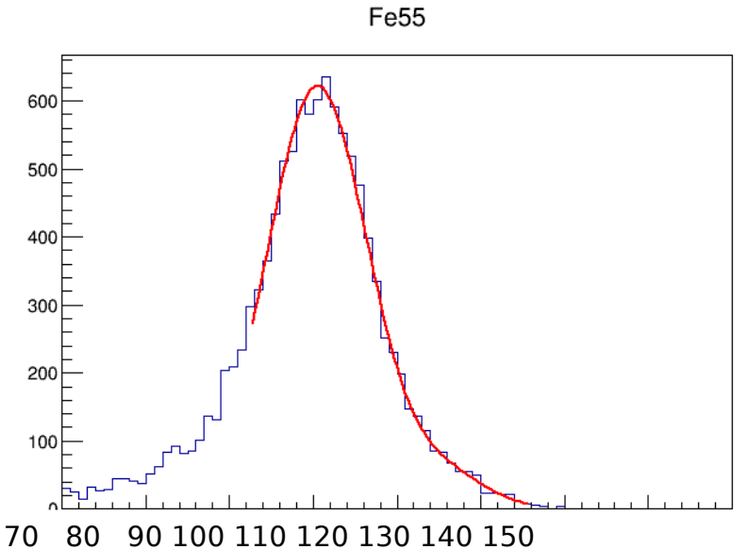
- NIEL hypothesis
  - Assumption that bulk damage is proportional to NIEL
  - Damage of 30MeV electrons is 16 times smaller than 1MeV neutron
    - 2.07 x 10^{11} e / cm^2 /year → 1.29 x 10^{10} n_{eq} / cm^2 / year
- Irradiation Test Performed
  - 65MeV Neutron beam
  - Fluence: $1.78 \times 10^{10}\ n_{eq}/cm^2$
    - Corresponding to 1.4 year running.

Charge Transfer Inefficiency measurement

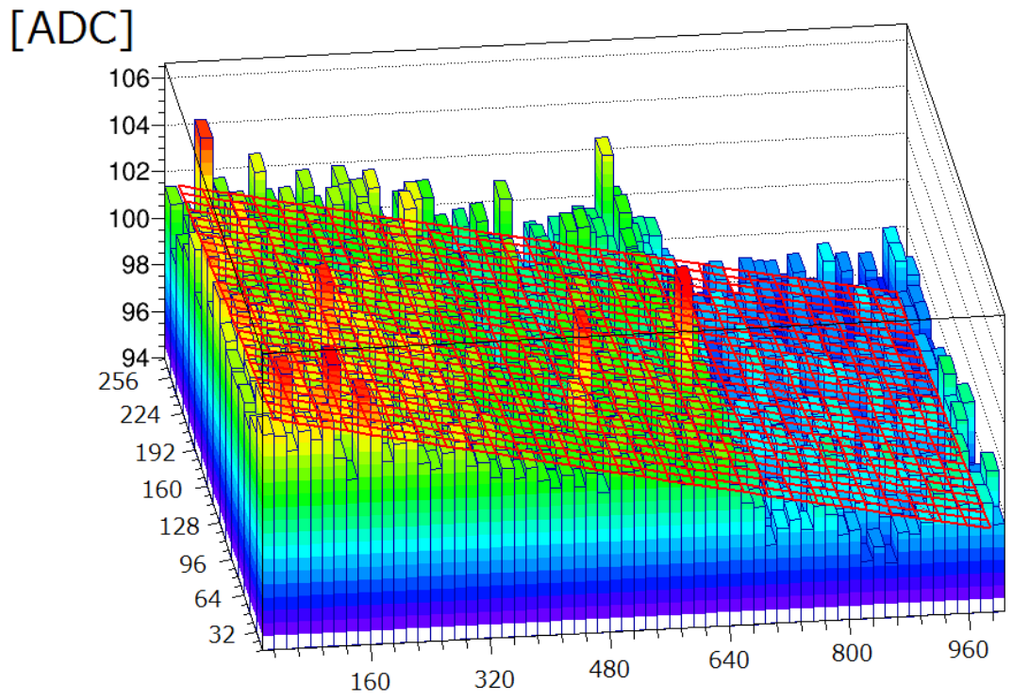
- Requirement of CTI VS S/N
  - If we take S/N=10, CTI < 2.5×10^{-5} is required
- Result closer to 6×10^{-5}

- About two times worse than requirement even th
  radiation corresponding to 1.4 year running





Fe55 peak



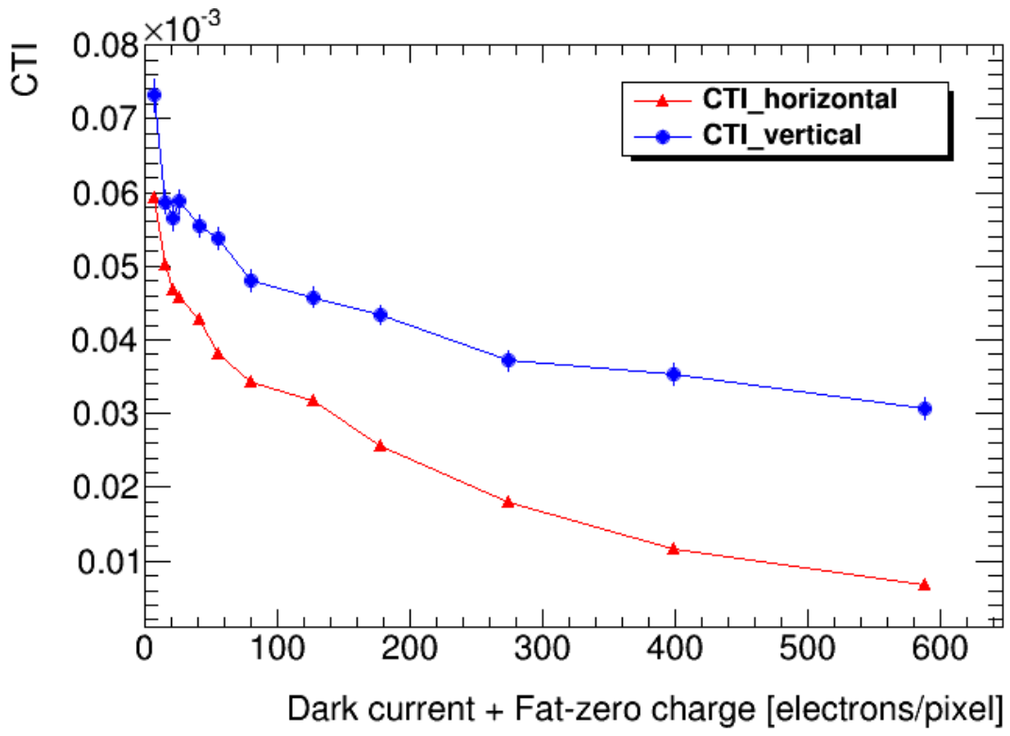
X-ray Signal distribution
after irradiation

Fat-zero charge injection

Fill lattice defect by background current. In this study, LED was used.

	No fat-zero charge		**600e/pixel injrcted**	
CTI_h		No fat-zero charge	600e/pixel injrcted	
	CTI_h	$(5.93 \pm 0.05) \times 10^{-5}$	$(0.68 \pm 0.04) \times 10^{-5}$	CTI_h $(5.93 \pm 0.05) \times 10^{-5}$ $(0.68 \pm 0.04) \times 10^{-5}$
	CTI_v	$(7.32 \pm 0.22) \times 10^{-5}$	$(3.07 \pm 0.15) \times 10^{-5}$	CTI_v $(7.32 \pm 0.22) \times 10^{-5}$ $(3.07 \pm 0.15) \times 10^{-5}$
CTI_v		No fat-zero charge	600e/pixel injrcted	
	CTI_h	$(5.93 \pm 0.05) \times 10^{-5}$	$(0.68 \pm 0.04) \times 10^{-5}$	CTI_h $(5.93 \pm 0.05) \times 10^{-5}$ $(0.68 \pm 0.04) \times 10^{-5}$
	CTI_v	$(7.32 \pm 0.22) \times 10^{-5}$	$(3.07 \pm 0.15) \times 10^{-5}$	CTI_v $(7.32 \pm 0.22) \times 10^{-5}$ $(3.07 \pm 0.15) \times 10^{-5}$

- Factor 9 improvement for CTI_h
  - CITv is less important since the number of transfer is smaller
- Need another factor 2 improvement
  - Reduce horizontal register size (smaller gap)
  - Notch channel
  - Annealing
  - Noise reduction.



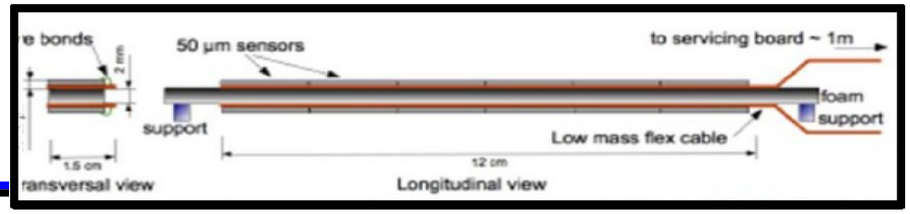
Low-mass mechanics

ECFA review of DEPFET and CMOS MAPs:

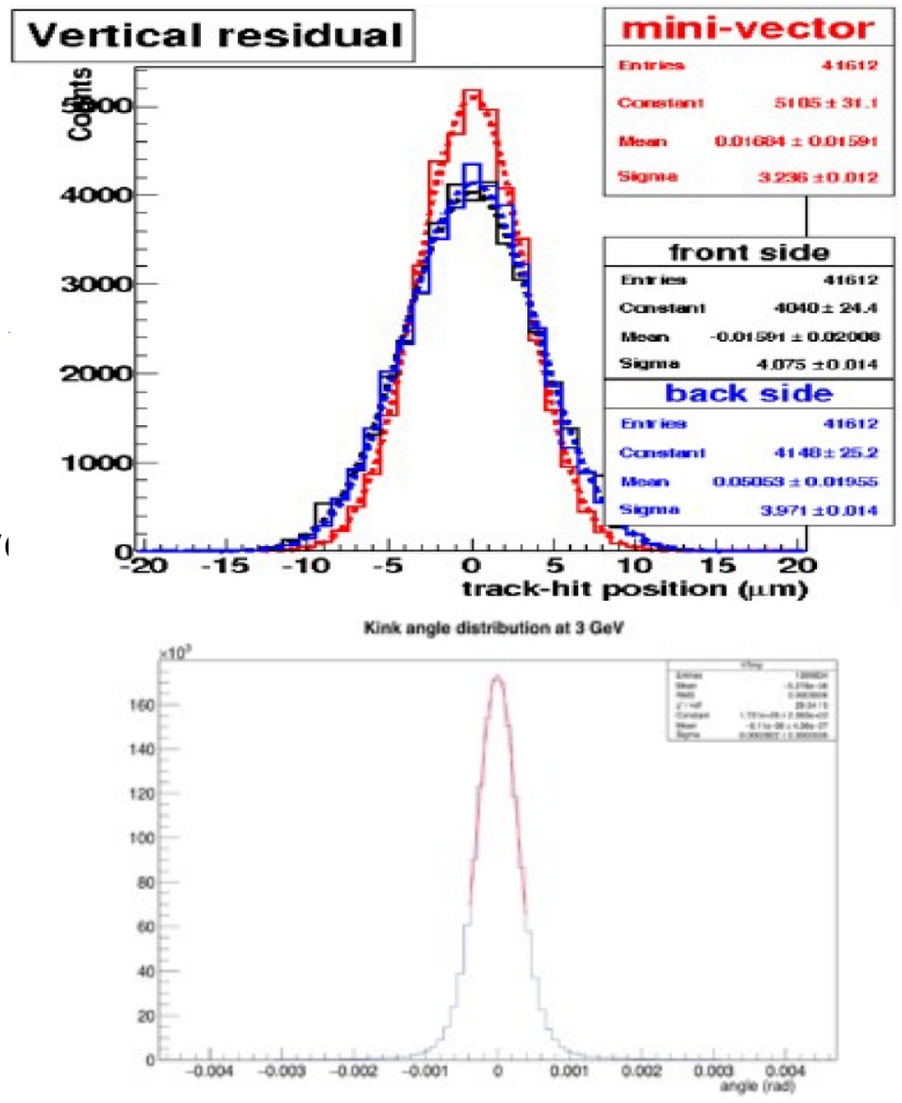
“... can profit from collaboration with other groups doing the same development.”

AIDA2020 collects efforts on micro-channel cooling (NA62, LHCb, ALICE, DEPFET-LC) and low-mass mechanics (ATLAS-Oxford, PLUME, DEPFET)

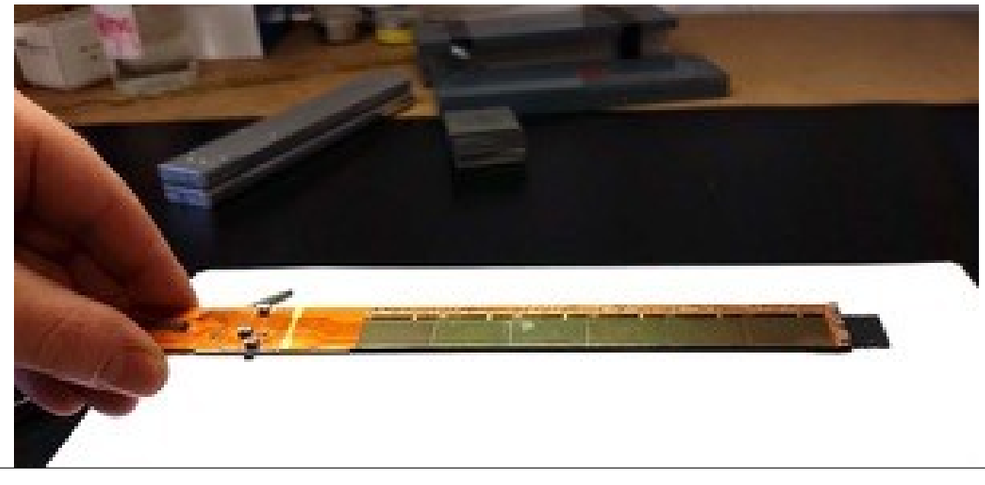
Integration: PLUME collaboration



- Plume collaboration (Bristol, DESY, IPHC)
  - Double sided ladders with minimized material budget
- Plume 01 prototype (fab. 2012)
  - 2x6 Mimosa-26 on 2 mm foam SiC
    - <mat.budget> ~ 0.6 % X_0 + Air cooling
  - Successfully validated in test beam
    - Mat. budget checked in test beam with kink angle in sensitive area: 0.47±0.02 % X_0 (0.45 expected) (B.Boitrelle PhD)
- Plume 02 prototype → Reduced mat. Budget
  - Cu flex cable (0.42 % X_0)
    - 2 modules functional, 2 more expected
  - Al flex cable (0.35 % X_0)
    - 4 modules. Connectors issue fix in 2017
  - 6 ladders expected (2 fabricated)
    - Modules functional. Tests ongoing in 2016
-



Kink angle distribution at 3 GeV



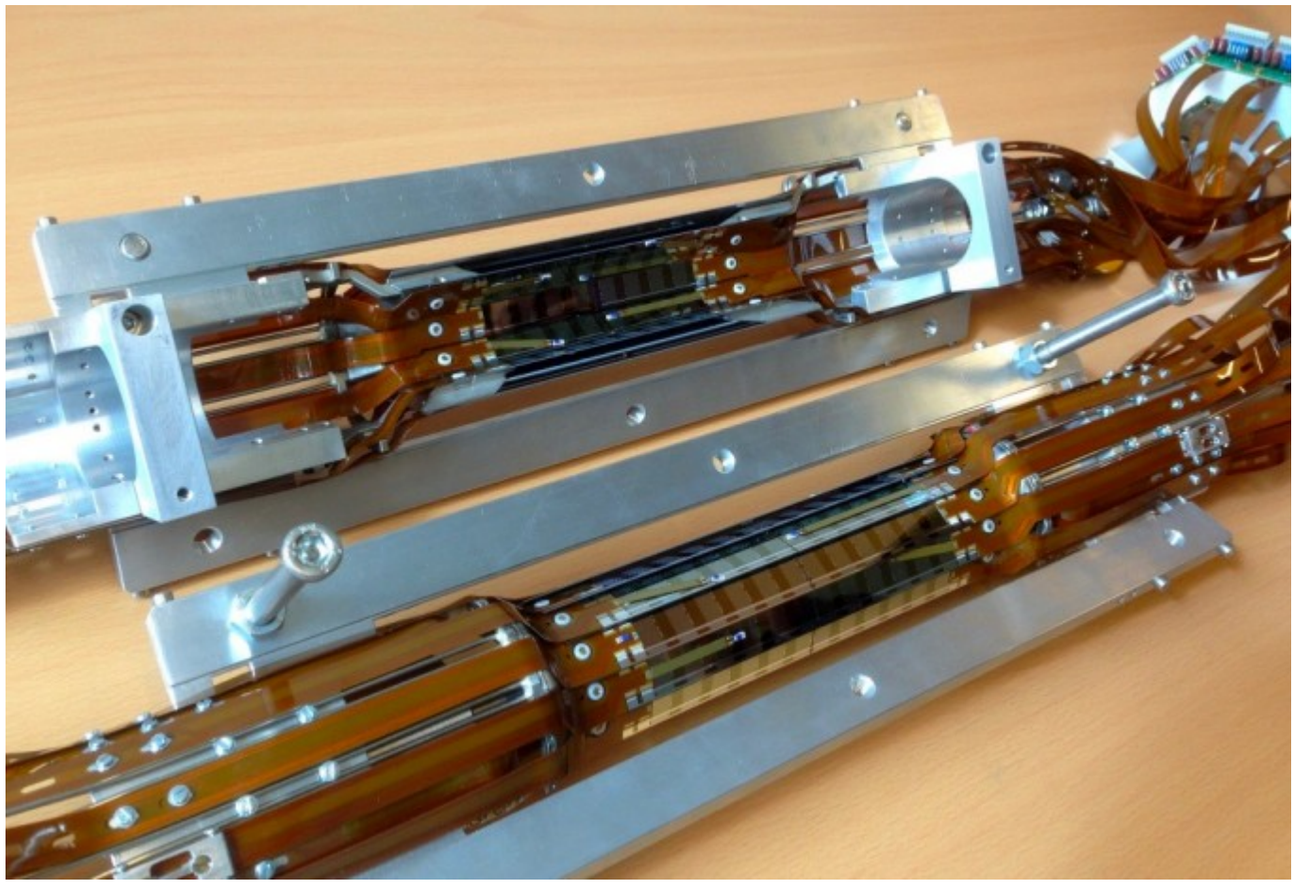
Ladders close to ILC mat.budget specifications

Air cooling

Blowing a gas flow over a 50 micron thick silicon layer that must be stable to better than 3 μm requires thorough validation.

CF space frames, CMOS sensors, kapton sealing (STAR/ALICE)

All-silicon ladders → Belle II vertex detector
arXiv:1607.00663 [physics.ins-det]



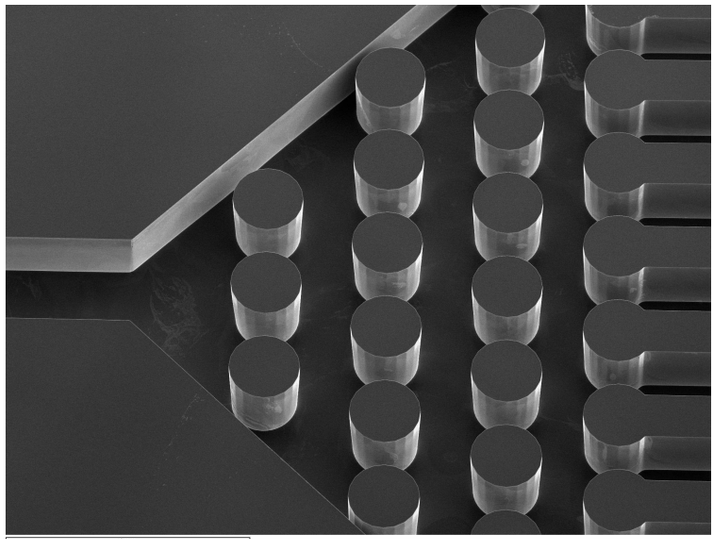
AIDA 2020

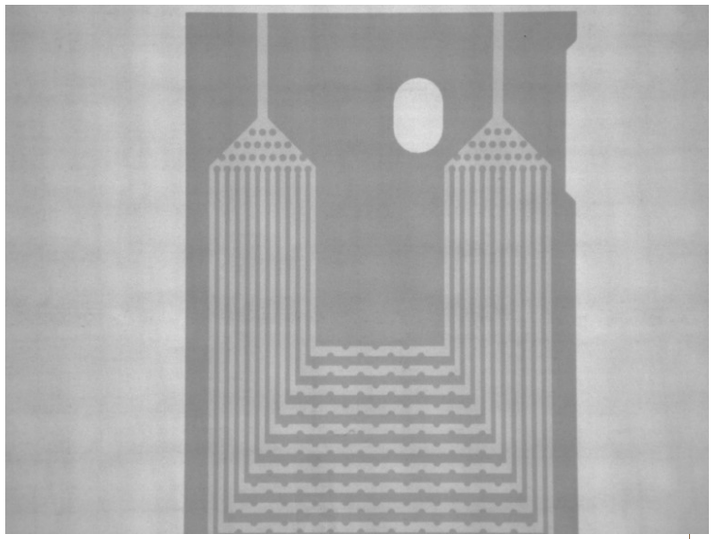
Oxford University to perform thermo-mechanical characterization of samples produced by PLUME and IFIC-HLL-Bonn

In realistic conditions!!

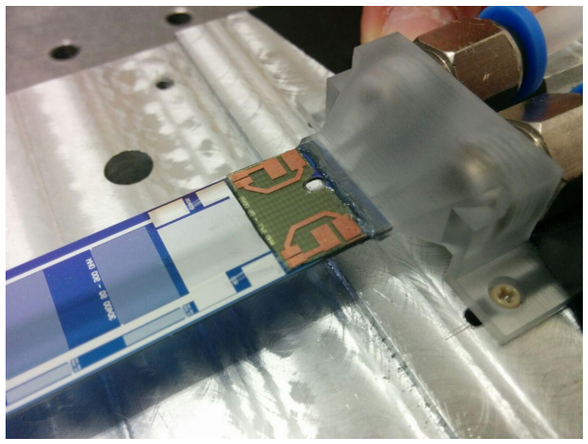
DEPFET Active Pixel Detector

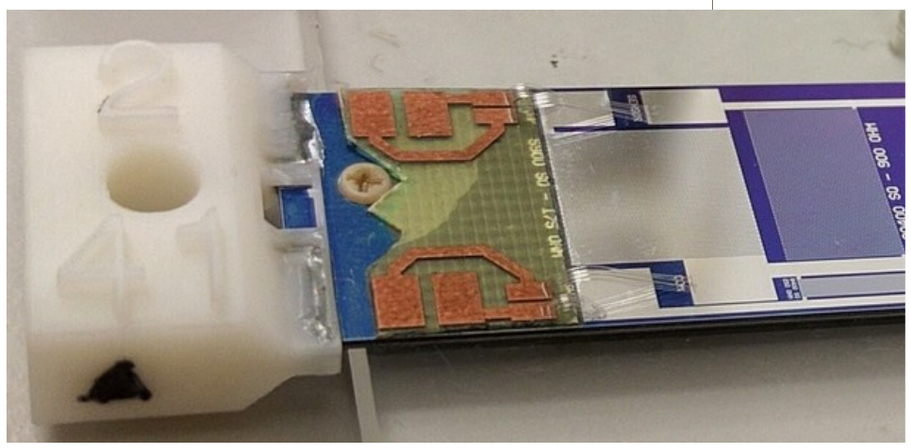
Micro-channel cooling

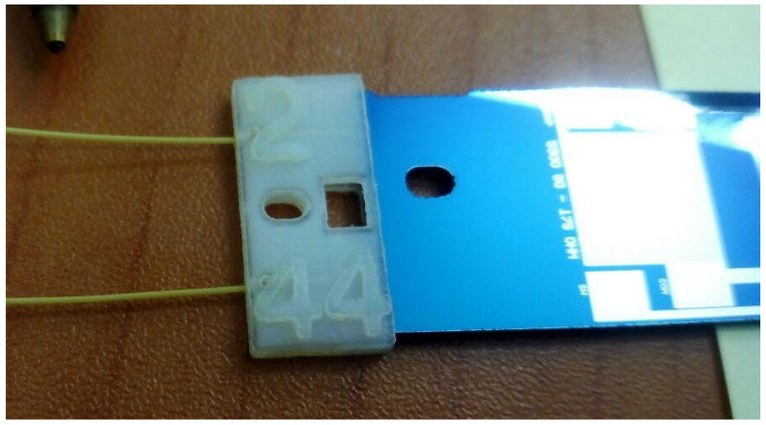




Micro-manifold before (photograph) and After wafer bonding (X-ray image) Samples produced at HLL.





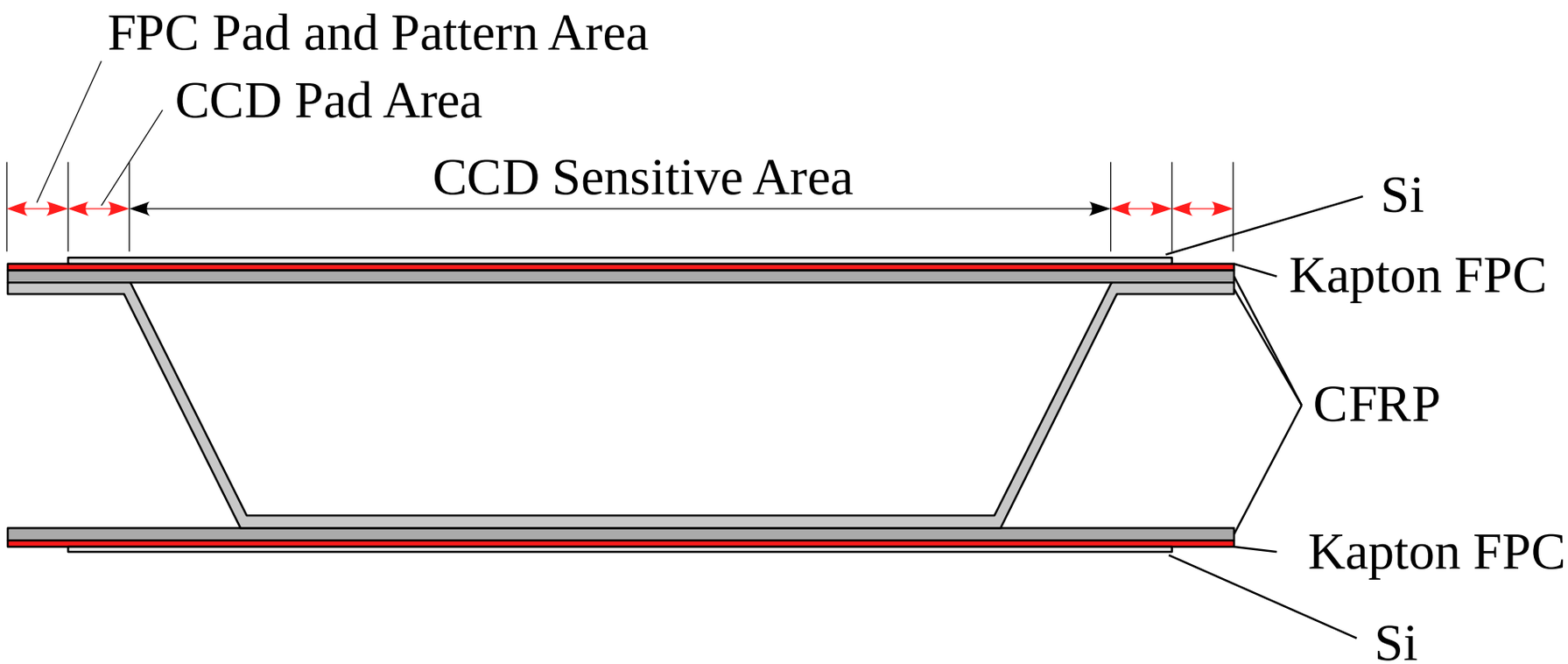


High-tech plumbing: custom, 3D-printed interfaces to commercial piping

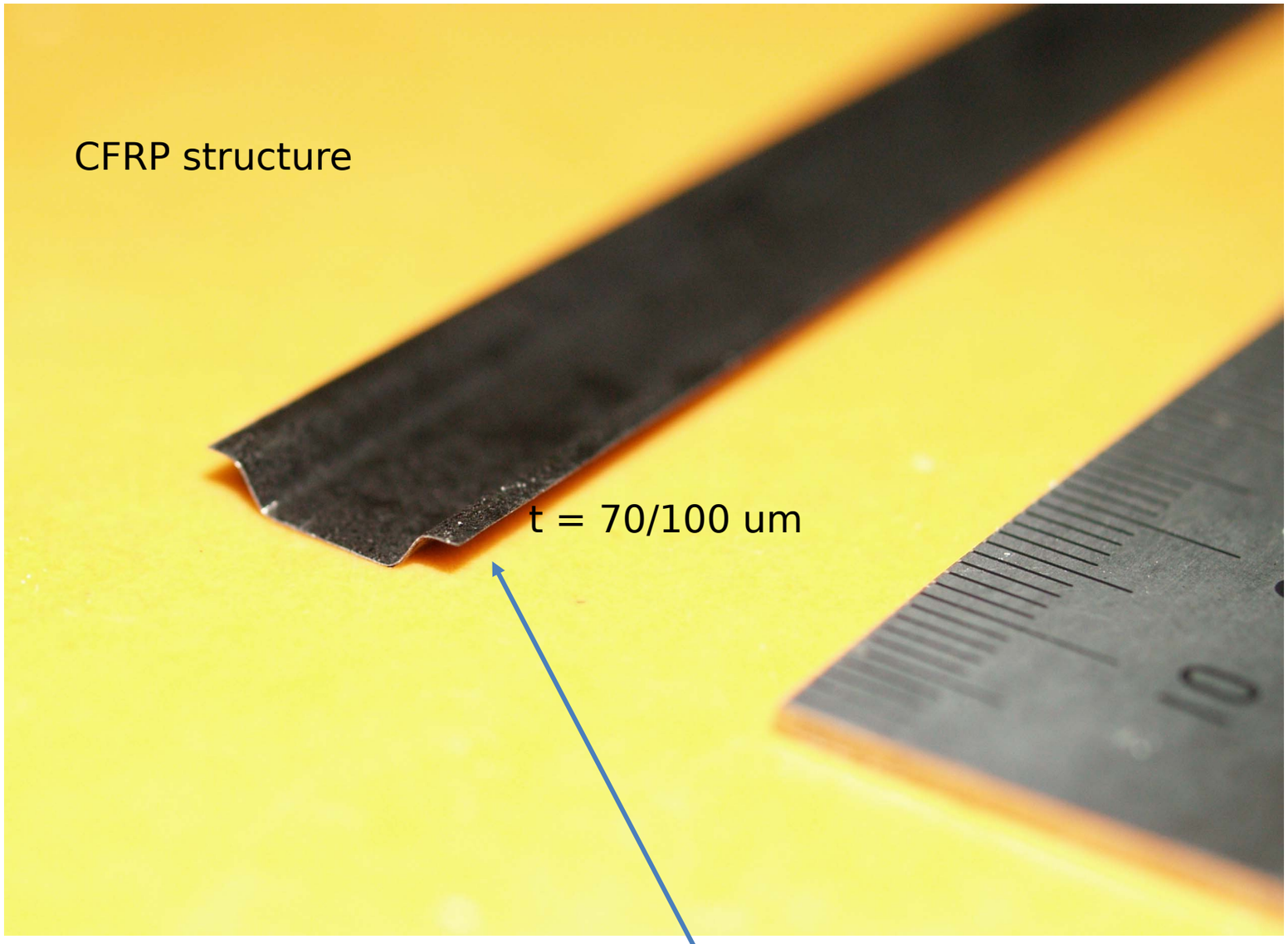
First encouraging results: “cool 40 W with 3 l/h and ΔT = 10 K”
Published in JINST (arXiv:1604.0877)

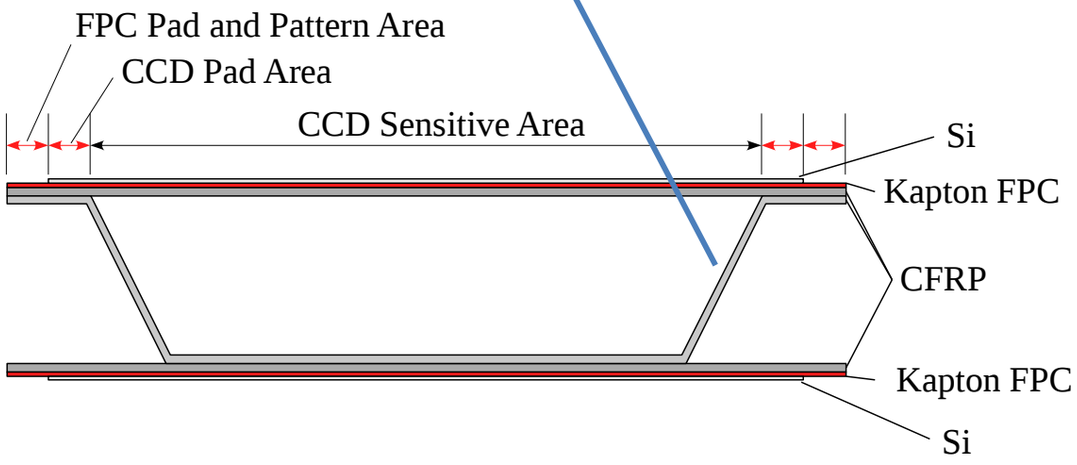
FPCCD Ladder R&D

- Ladder R&D started
  - Prototype flexible printed circuit (FPC) and CFRP support are made for l adder R&D
    - Study of gluing
    - Study of FPC cable impedance
    - Study of rigidity and thermal conductivity of CFRP
  - 3-dimensional CFRP structure
    - This could be also used for other options adopted doublet structure (CMOS)

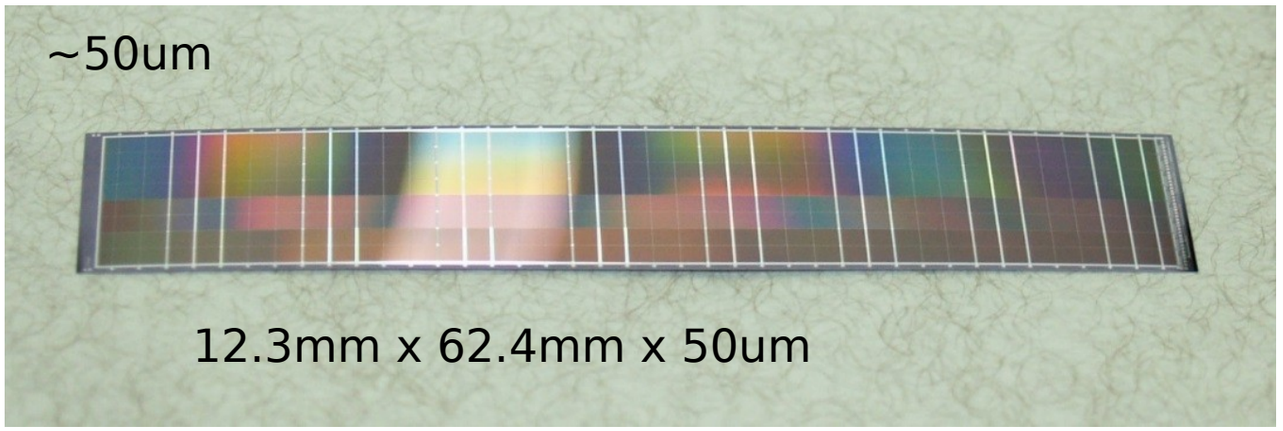


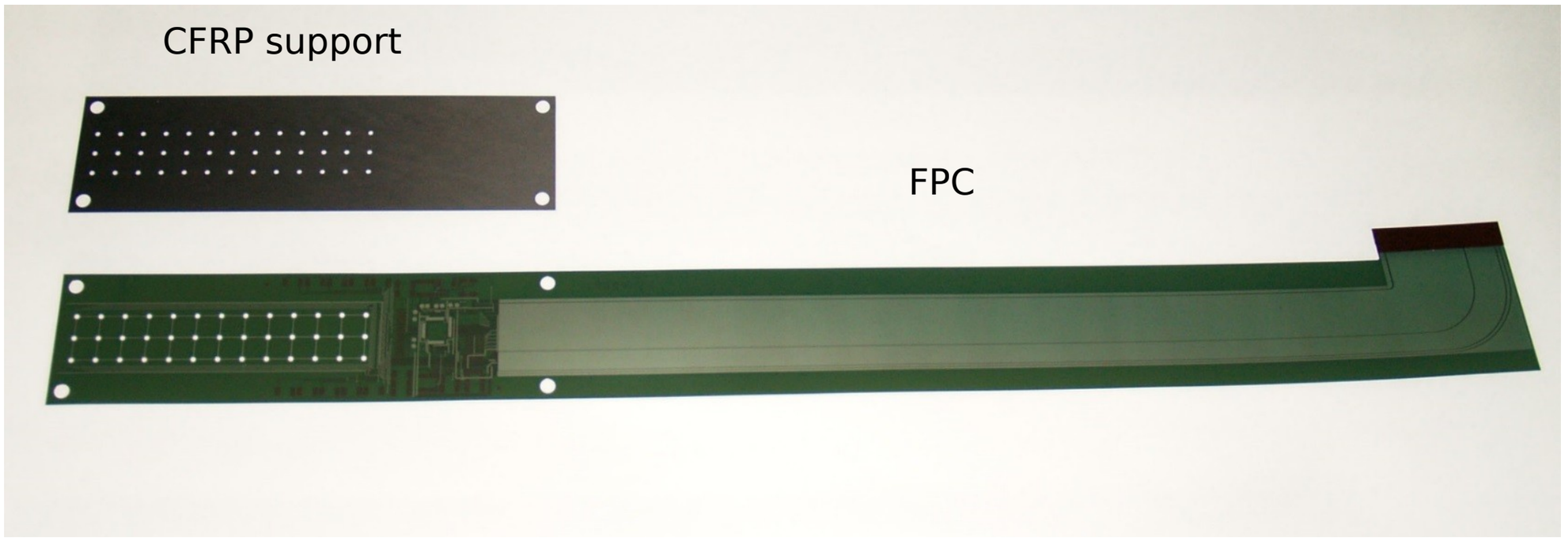
CFRP


CFRP structure
t = 70/100 um

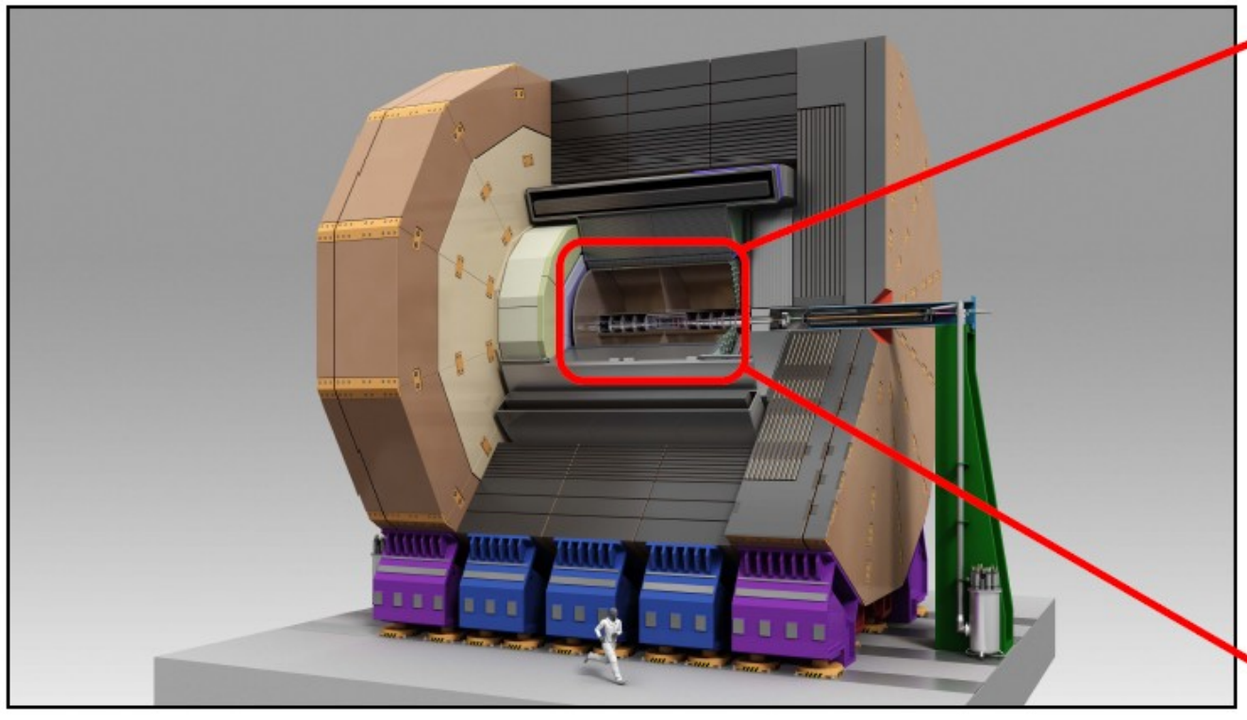

FPC Pad and Pattern Area
CCD Pad Area
CCD Sensitive Area
Si
Kapton FPC
CFRP
Kapton FPC
Si

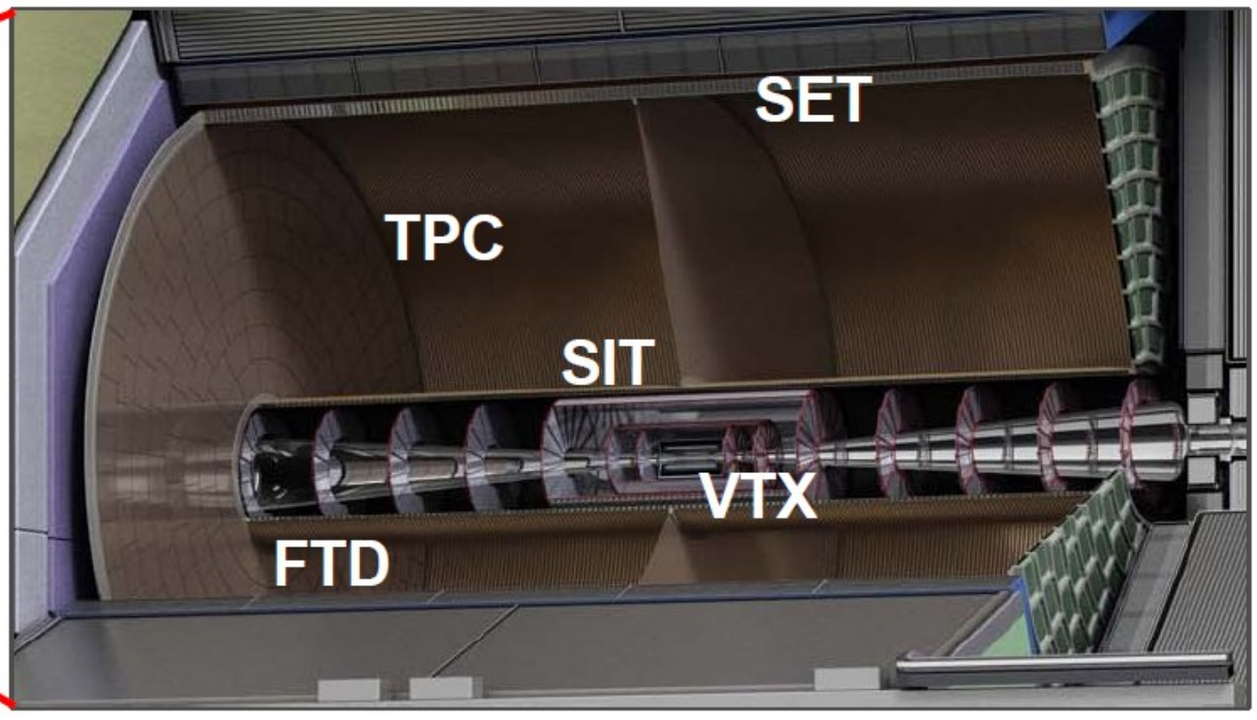
FPCCD and FPC Cable





ILD inner tracker





µ-strip tracker

Connect VXD and TPC (SIT, FTD)

Provide forward coverage (FTD)

Add precise point at large lever arm (SET)

Expected performance

Resolution: 7 µm

Read-out speed: ~1 µs

Material: <<1% X_0 / layer

Where are all these silicon people?

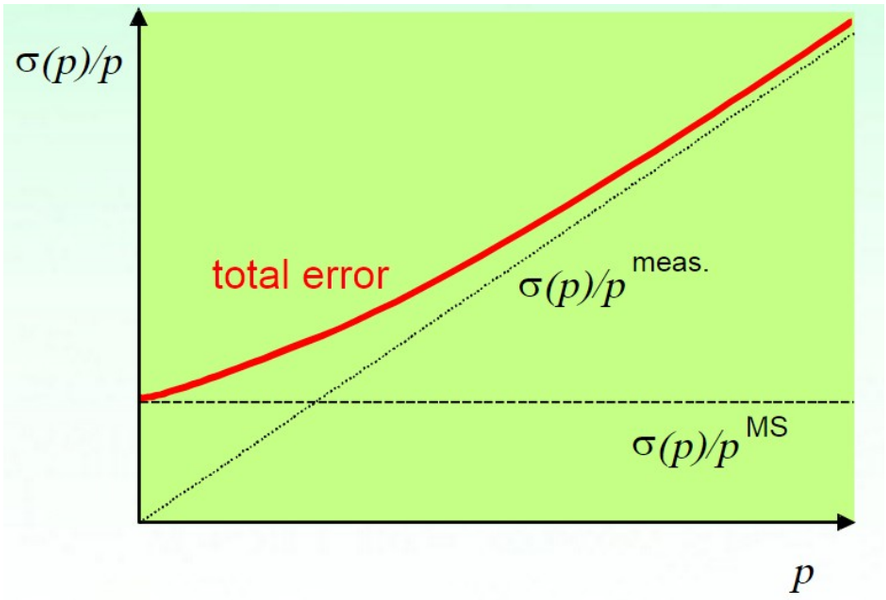
The silicon tracker is a different story. A large number of institutes works on micro-strips. The annual “tracker mechanics forum” attracts over 100 participants. Most are involved in the development of radiation-hard sensors (RD50) and the construction of the ATLAS, CMS and LHCb silicon micro-strip tracker upgrades (~200 m^2). Even that effort is suffering because too many groups move into pixel detector R&D.

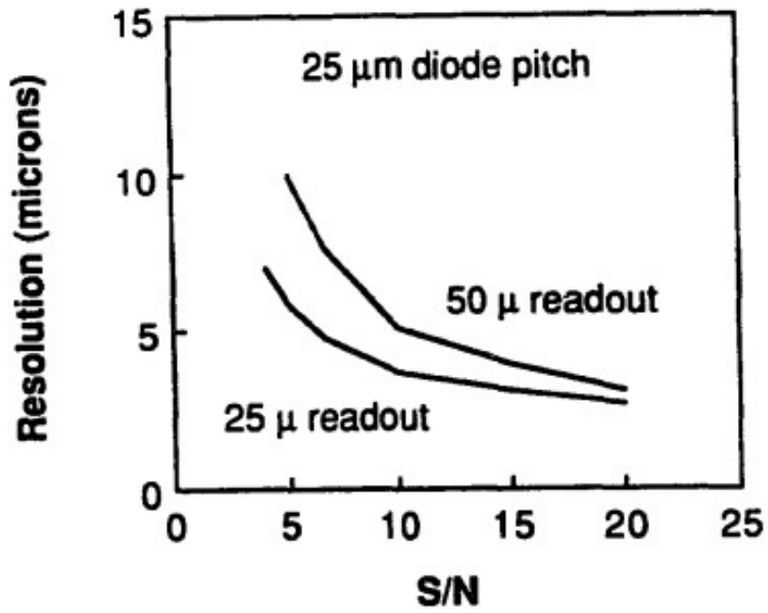
Attempts to build a European-centered micro-strip tracking R&D collaboration for the linear collider, back in 2007-2011, have failed. SiD initially (naturally) attracted a larger crowd, but has since lost much of its manpower.

The micro-strip effort in ILD is clearly insufficient. ILC-connected R&D efforts are ongoing at HEPHY Vienna (also CMS and Belle II) and IFCA in Santander + a number of associated technological institutes (providing coverage for the FTD). No name is assigned to SIT or SET.

Motivation for a strip detector with integrated signal gain

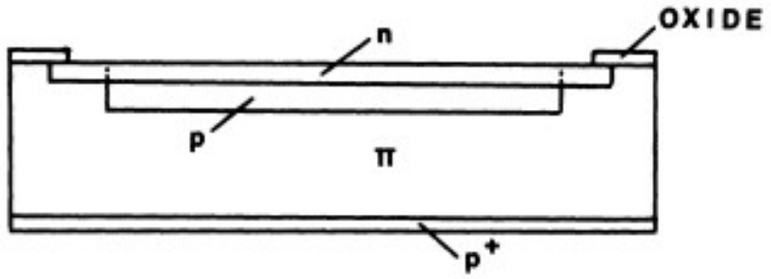
- Integrated signal amplification increases the Signal-to-Noise ratio increasing the tracking resolution:
  - Thinner detectors (reduction of the **multiple scattering**)
  - Improved **intrinsic hit resolution**.





Low Gain Avalanche Detectors 101

– Signal amplification implemented as reach-trough Avalanche Diode structure [Web74].



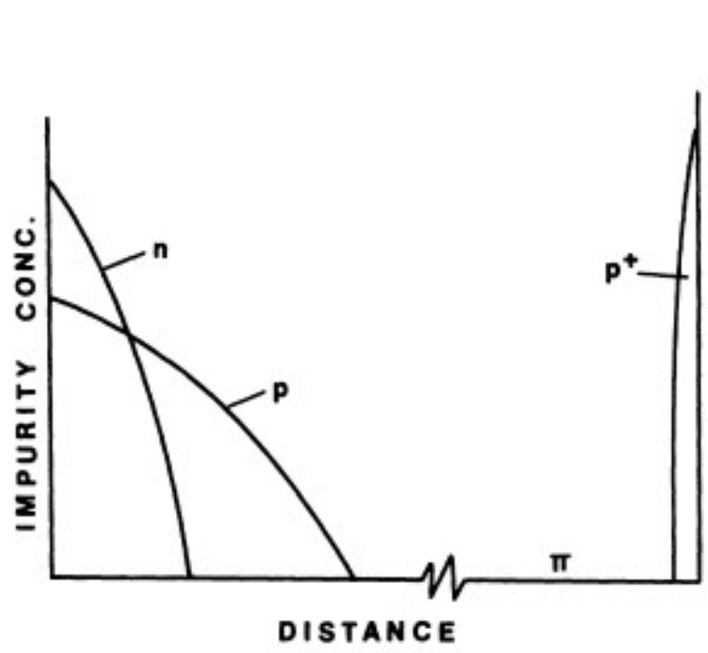


Fig. 1 - Reach-through avalanche diode structure and impurity concentration profile. The starting material is p-type silicon of about 5000 ohm-cm, resistivity. The p and n diffusions are, respectively, boron and phosphorus.

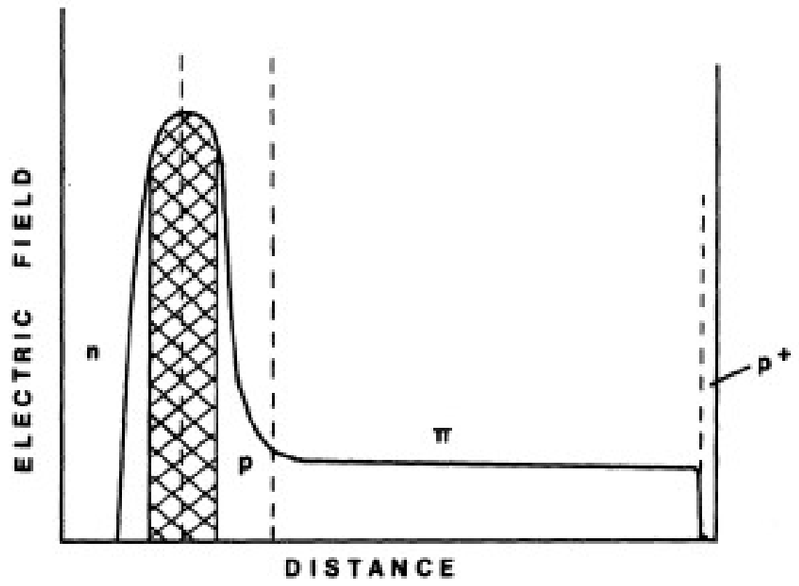
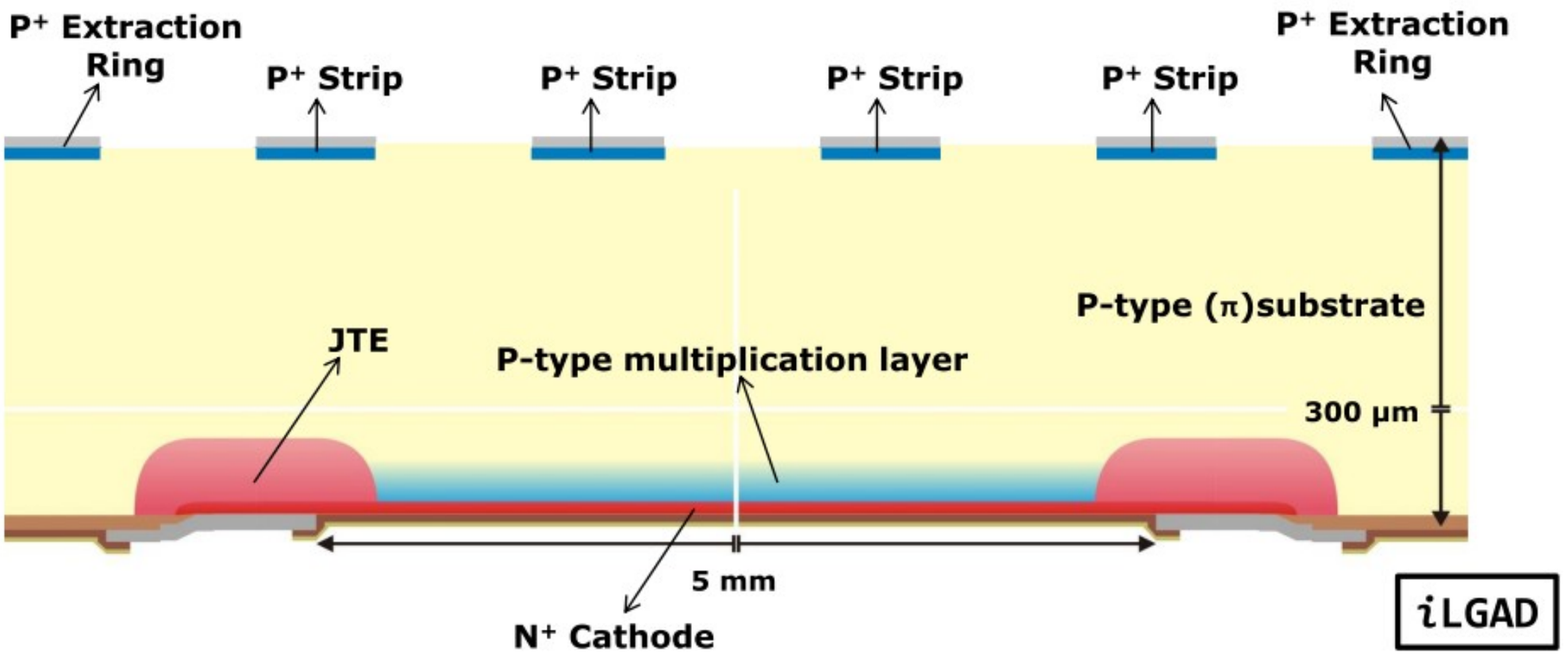


Fig. 2 - Electric field profile for a reach-through avalanche diode.

High electric field to trigger the production of secondary carriers by impact ionization.

Inverse- LGAD

- P-in-P LGAD with hole readout (ohmic contact segmented)
- Avoids issues with gain non-uniformity

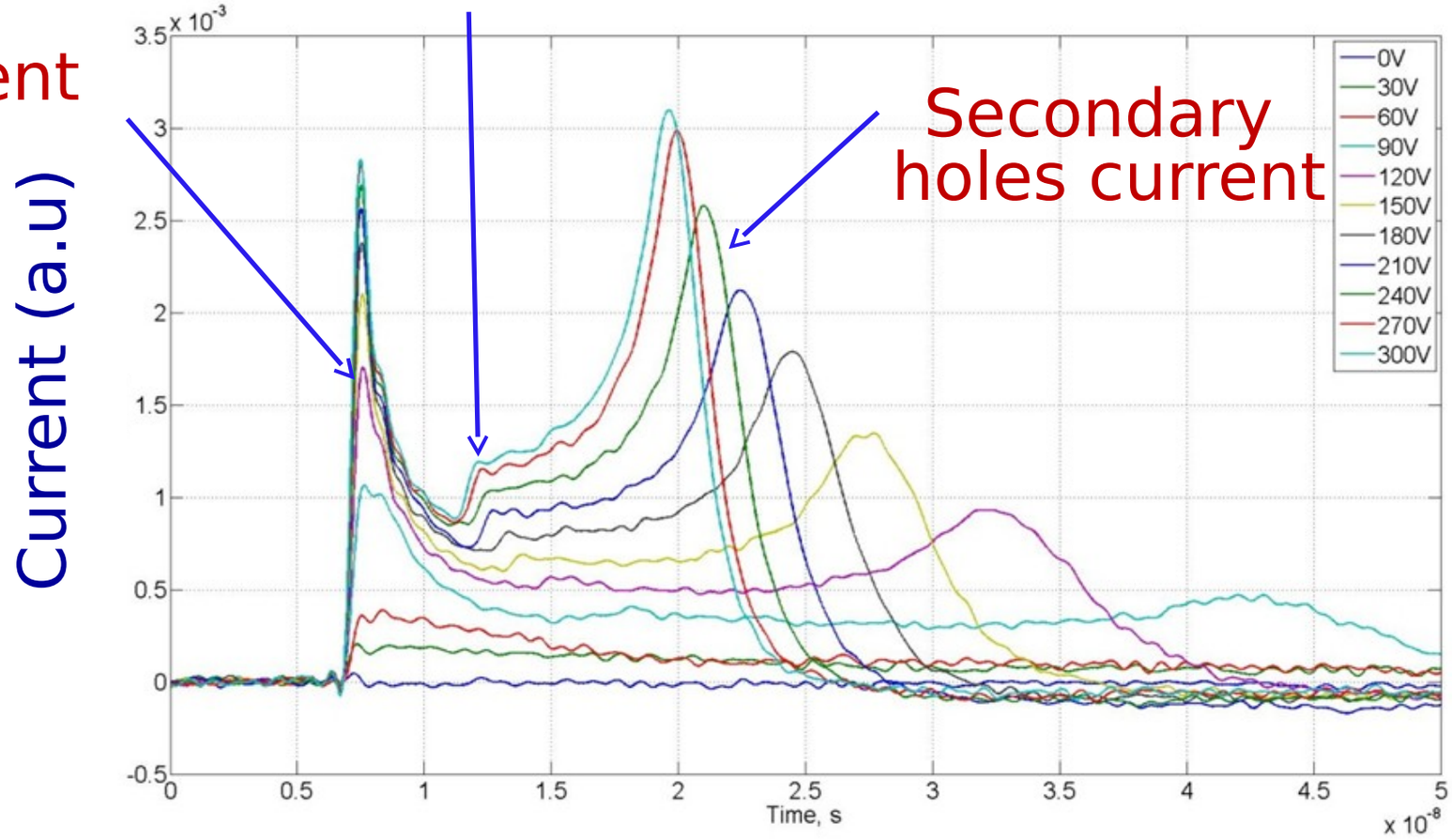


Inverse-LGAD TCT: Electron injection

First observation of signal amplification (June 2016)

Multiplication onset

Primary electron current



Secondary holes current

Current (a.u)

Time (ns)

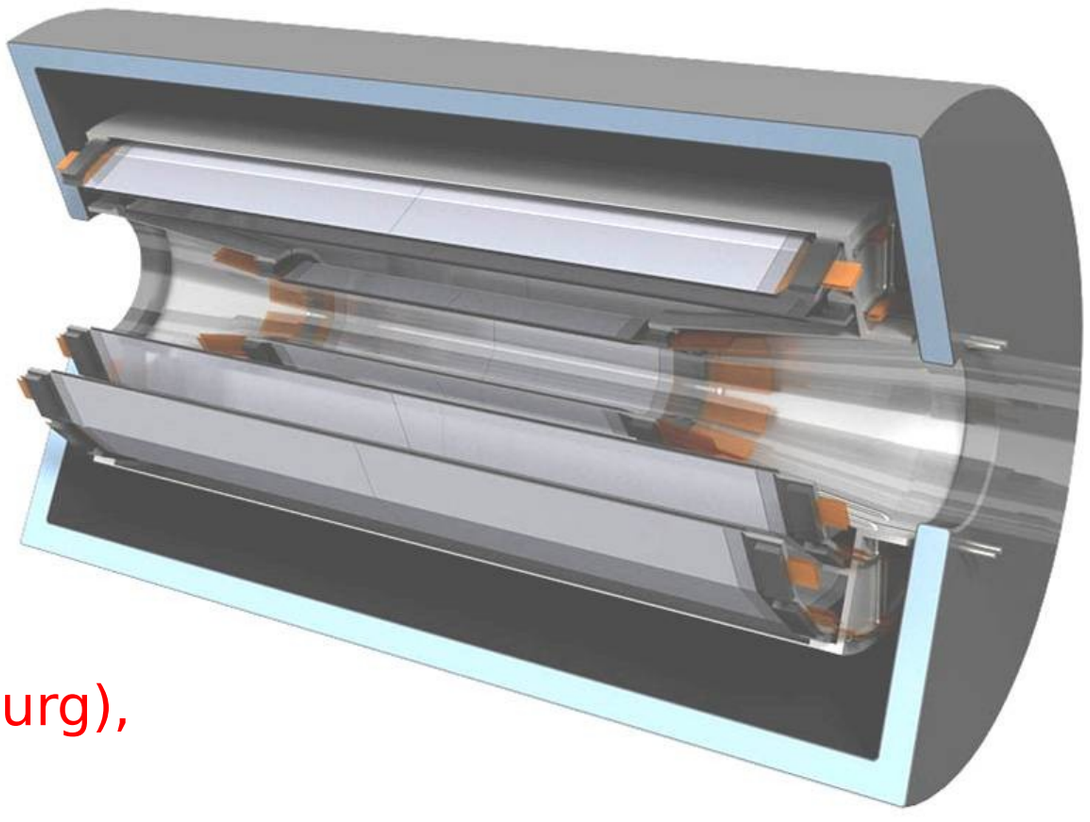
Gain of ~3 (wrt reference sensor) confirmed in test beam

Detailed, realistic design, VXD

Vertex detector design in MC still very “generic”

Estimate technology-dependent performance

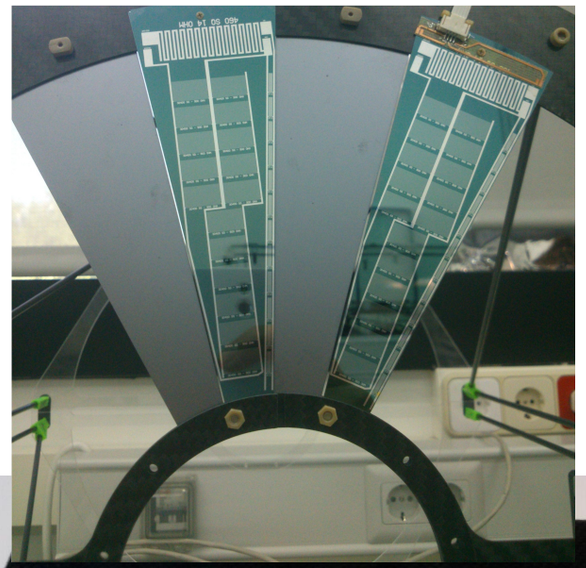
- detailed DEPFET/FPCCD/MAPs digitizers
  - Software exists, needs some effort
- realistic support structures
  - Double vs. Single layer
  - Refine as mock-ups evolve
- realistic end-of-ladder material for CLIC
  - M.A. Villarejo (now IFIC)
- realistic routing of services

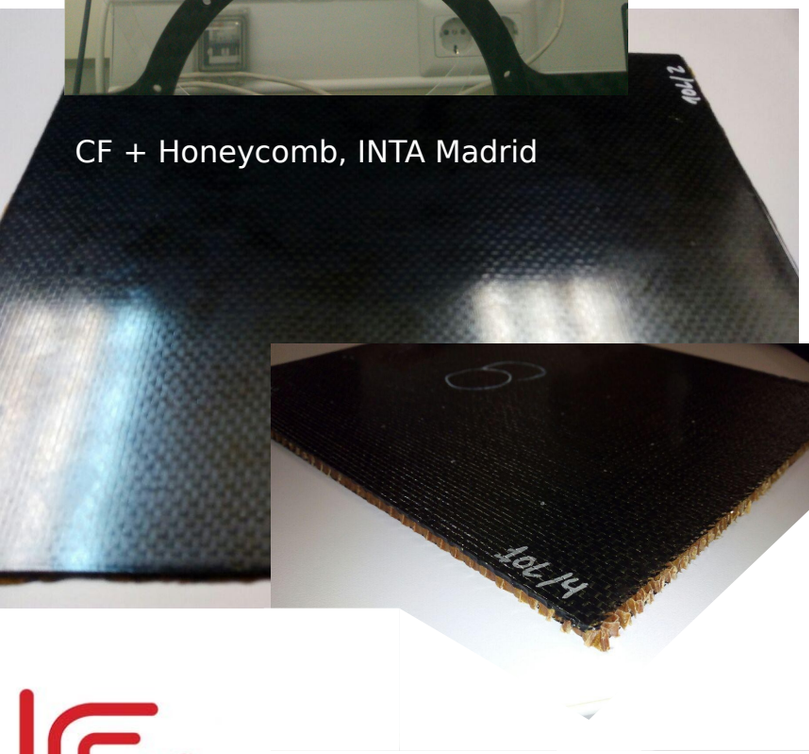


Person-power: Alejandro Perez (Strasbourg), see his talk this afternoon

Disk design and mock-up

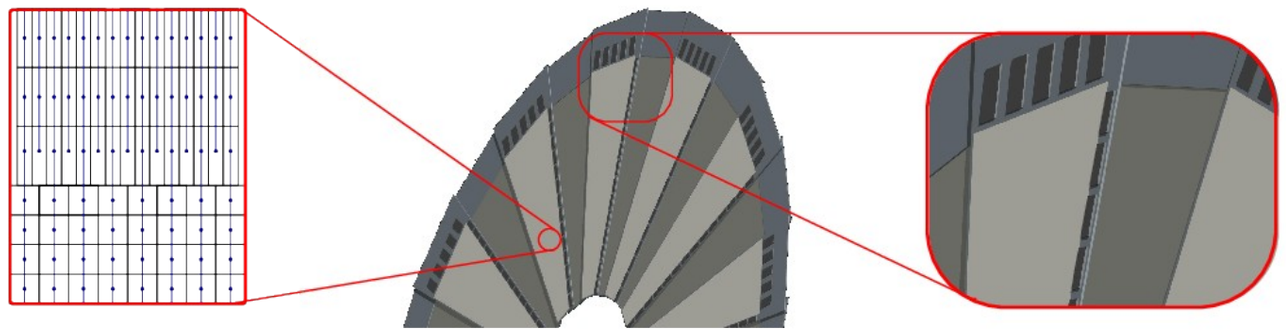
ECFA review panel: “For the ILC the main challenge is to engineer the forward tracking disk region. We recommend that the work on forward petal continues to demonstrate that petals that meet ILC requirements can be made... that more effort is made on the transition and forward regions to find a credible engineering solution , cooling and services.”





ILC detectors extend coverage to 6 degrees

- need end-cap for vertex detector



Subject thin DEPFET petals to ILC environment:

- ILD/FTD geometry
- low-mass CF support structure
- pulsed power in heater circuits
- forced air flow for cooling (no liquid!)

And monitor thermo-mechanical properties:

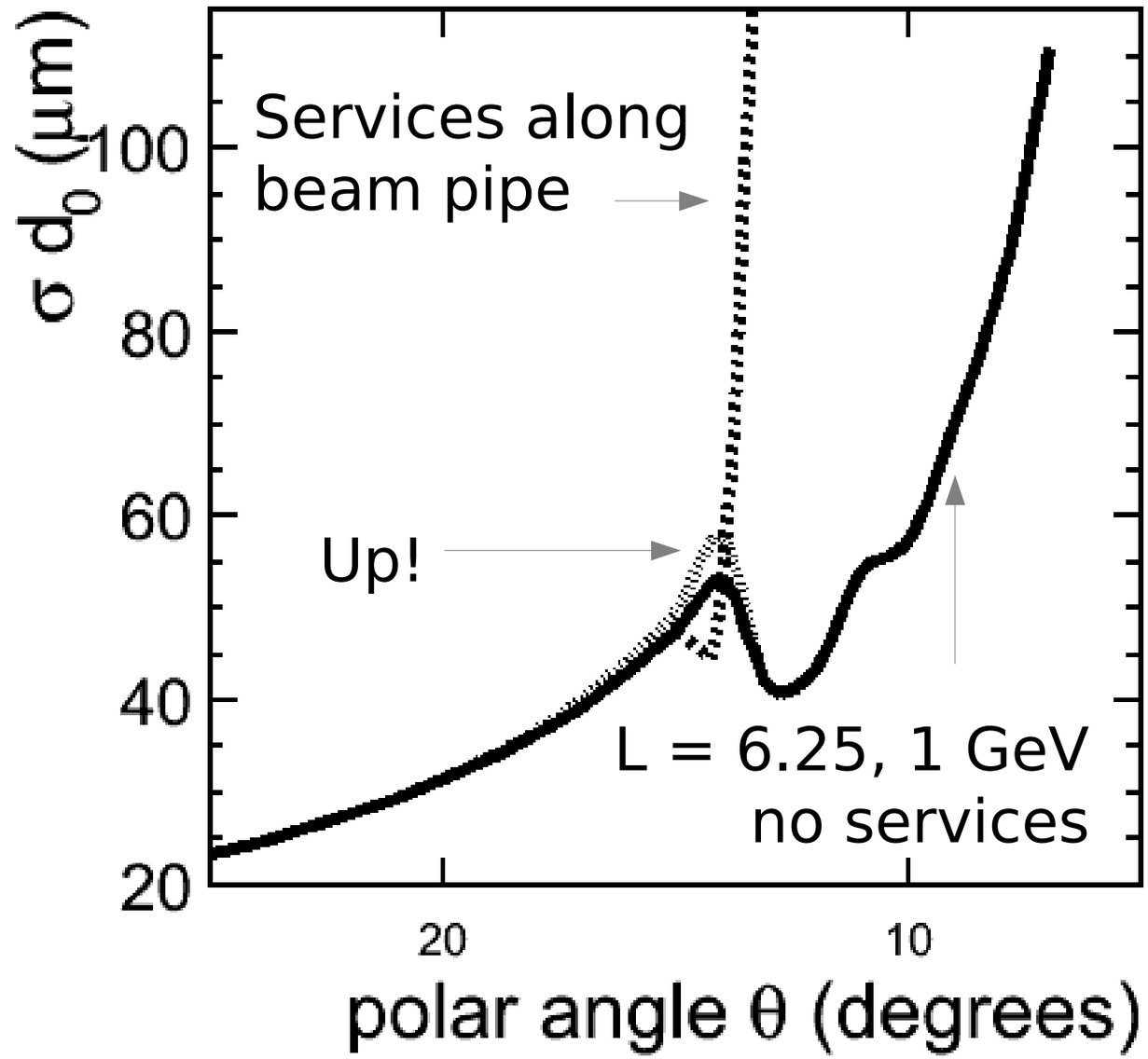
- power pulsing + air flow yield adequate cooling
- deformations and vibrations under control

Up! or along beam pipe?

Use S. Bilokin's study of e+e- → bb as a benchmark?

The forward region clearly does NOT like the services routed along the beam pipe

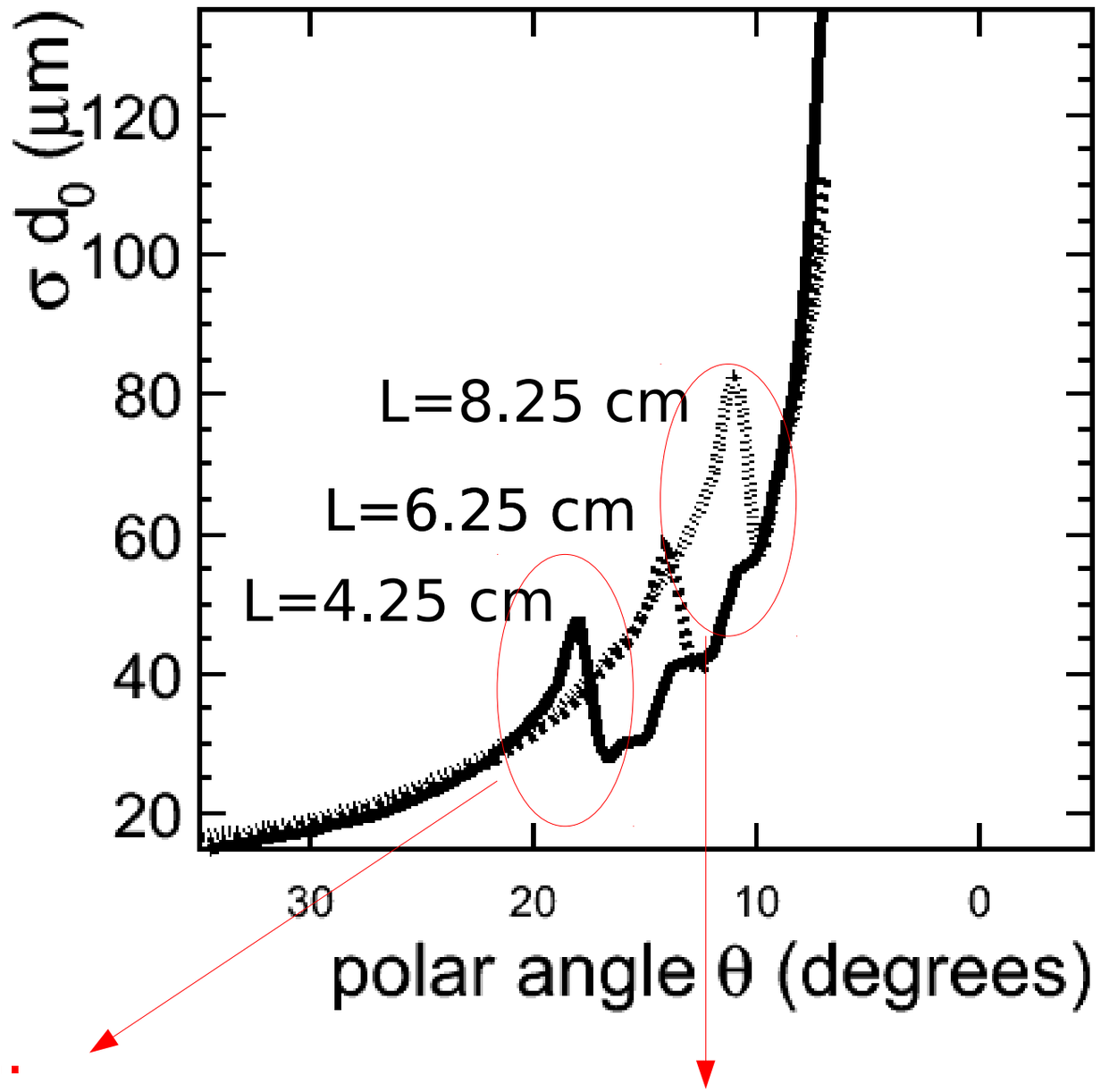
If anything close to a few radiation lengths comes in the way between endcap and interaction point we can forget about forward vertexing



Comparison L_{barrel}

A longer barrel removes the “material bump” from the central region...

Of course, the material comes back - with a vengeance – at smaller angle



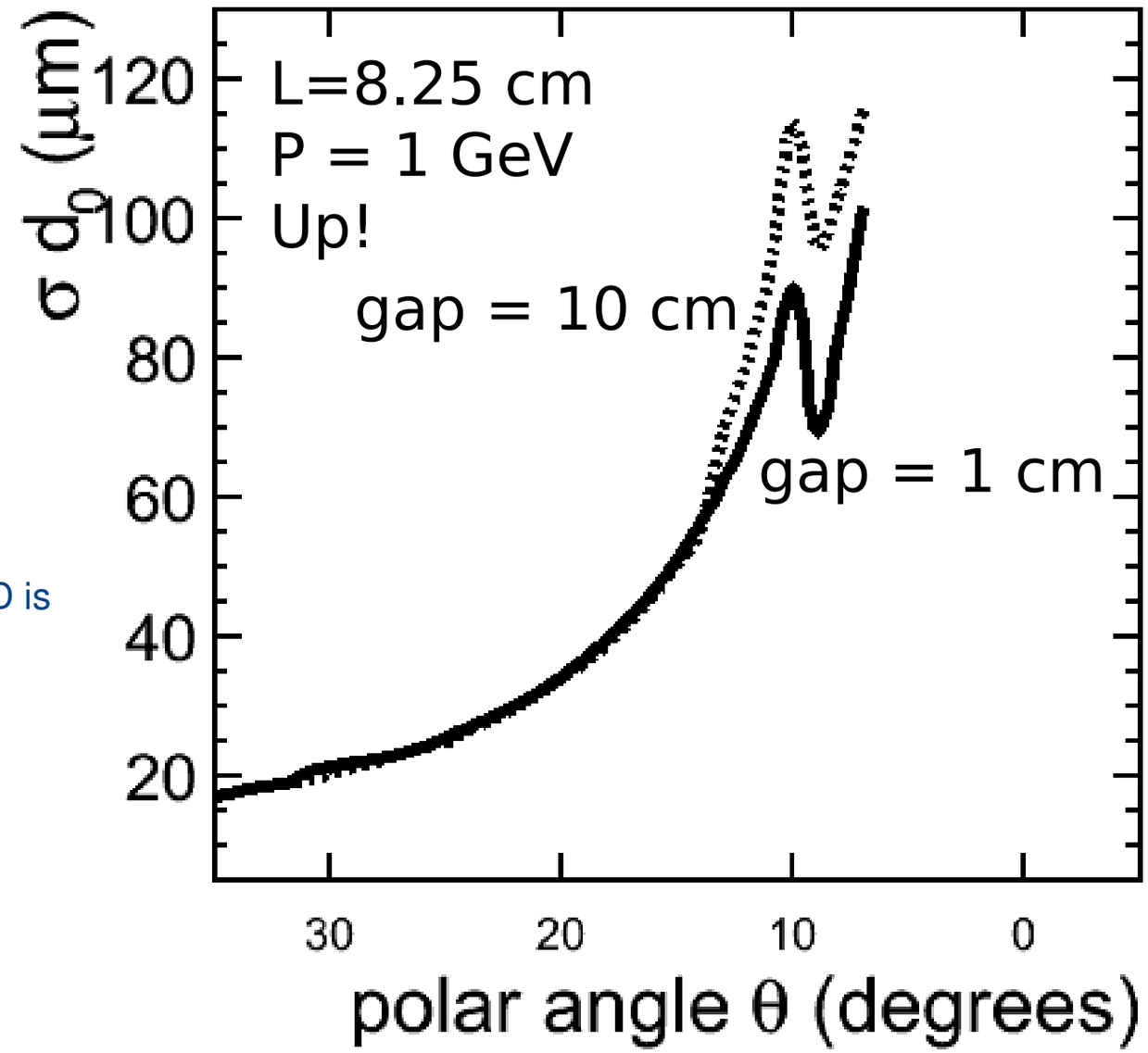
Save a little here....

Large distance, shallow angle

Comparison z_{gap}

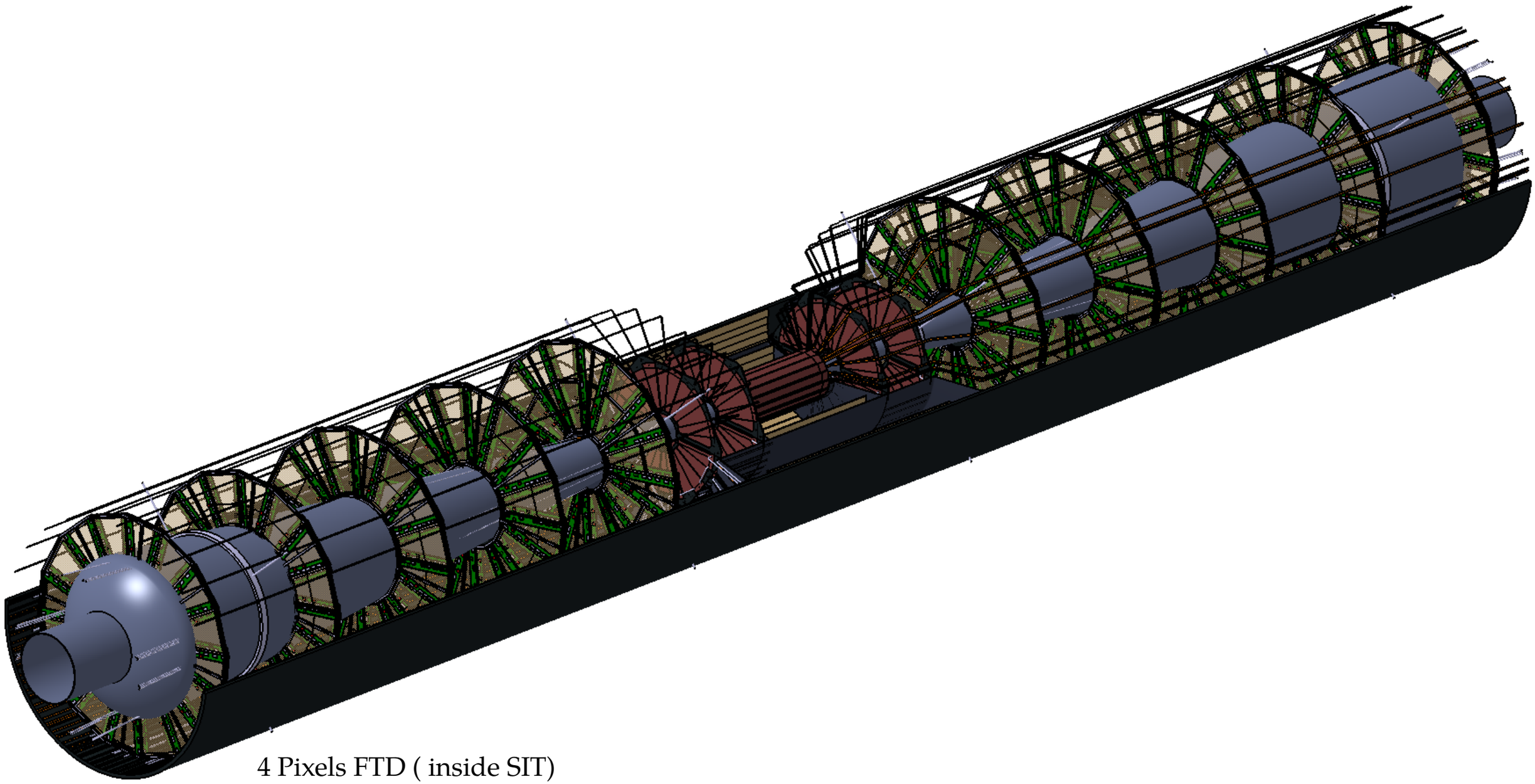
Minimize the gap! *

But: if we route the services along the beam pipe, the forward vertexing performance is terrible and essentially insensitive to z_{gap}



* In ILD the distance between VXD and innermost FTD is close to 10 cm. This clearance is motivated by the possibility to fit in a VXD cryostat. If a “cold” VXD technology is chosen, a short gap implies one has to install the innermost disks inside the cryostat.

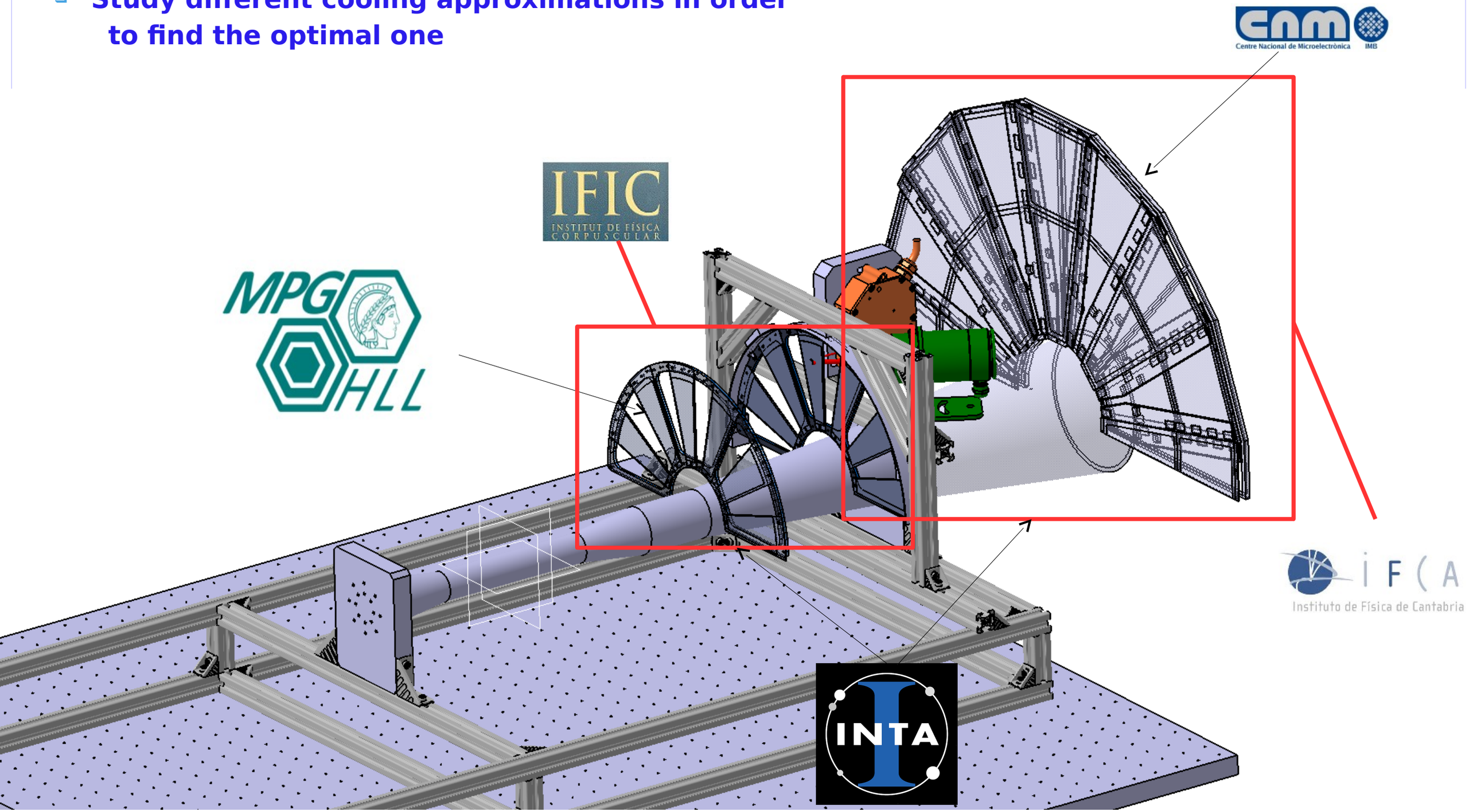
Realistic design FTD



4 Pixels FTD (inside SIT)
(Problem, not SIT design in order to make a proper FTD support design)
10 µstrip Disks supported by Inner support cylinder

FTD Mock-up

- The aim: Produce a realistic thermal and mechanical mock-up in order to test:
  - **Mechanical stability**
  - **Sensors, support, services Integration and mounting procedure**
  - **Study different cooling approximations in order to find the optimal one**



ILD FTD Collaboration

IFIC INSTITUT DE FÍSICA CORPUSCULAR

Pixels FTD disk activity coordinator
Support structures design

INTA

Carbon fiber support structure manufacture and design support

IFCA Instituto de Física de Cantabria

µstrips FTD disk activity coordinator
Support structures design

MPG HLL

Depfet Pixels Sensors Design , Manufacture and development

ITAINNOVA INSTITUTO TECNOLÓGICO DE ARAGÓN

Power supply design and support.

cnm Centre Nacional de Microelectrònica IMB

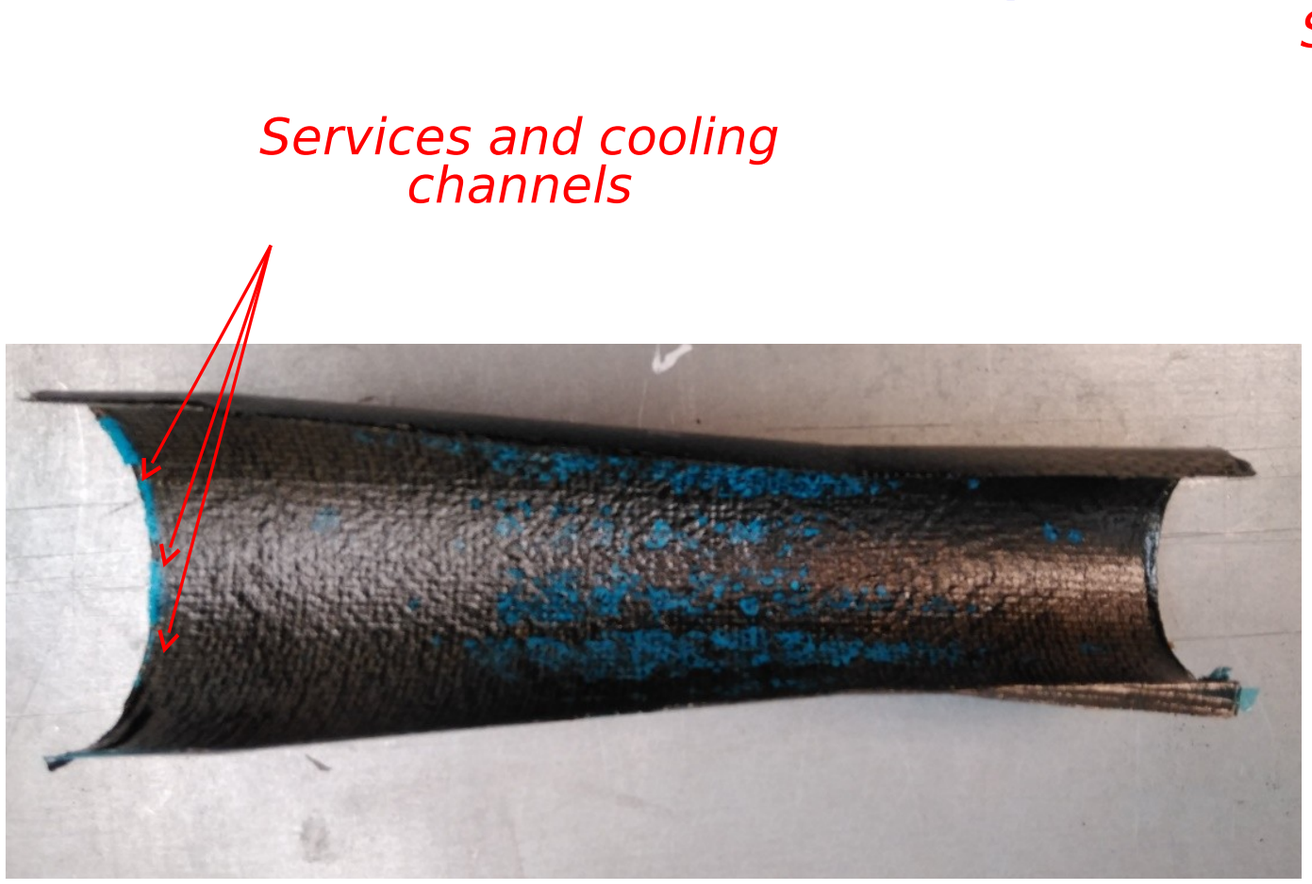
µstrips Sensors Design manufacture and development

Universitat de Barcelona

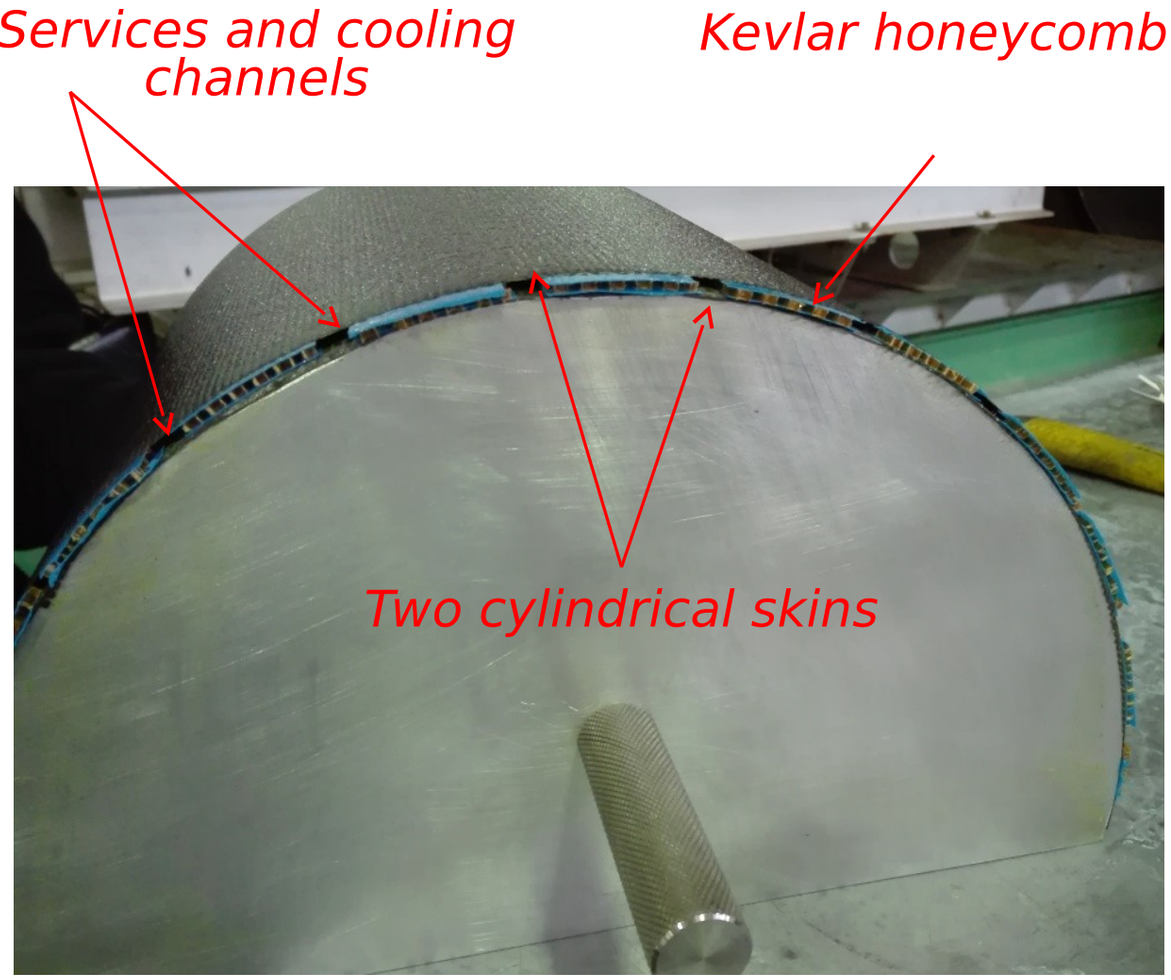
Asics design.

FTD actual status

- The manufacture of Pixel FTD support and service half cylinders and Cones ongoing:
  - **Manufactured with two M55J/CEM100 curved skins and Kevlar sandwich. Some free channels left for services and cooling.**
  - **Problems with the Cylinder: One of the half's broken (quite fragile in the area of the service channels.)**



Inner Half cone



Outer Half cylinder

FTD validation

The FTD micro-strip disks have an adequate level of detail
(J. Duarte, F. Gaede, several years ago)

Make sure the DD4HEP model follows the description in the LOI
(the DBD has inconsistent SIT inner radius and FTD outer radius)
Look for bugs introduced in porting to DD4HEP

No person identified...

SIT / FTD integration problem

cos θ doesn´t agree with dimensions

TDR SIT and FTD 1-3 Layout

SIT (baseline = false double-sided Si microstrips)			
	Geometry		
R [mm]	Z [mm]	cos θ	Resolu
153	368	0.910	R: σ=
300	644	0.902	z: σ=

FTD (baseline: pixels for two inner d		
	Geometry	
R [mm]	Z [mm]	cos θ
39-164	220	0.985-0.802
49.6-164	371.3	0.991-0.914
70.1-308	644.9	0.994-0.902

Dimensions does not match (SIT inside FTD 1,2,3 LOI volume)

LOI SIT and FTD Layout

SIT characteristics (current ba		
Geometry		
R[mm]	Z[mm]	cosθ
165	371	0.910
309	645	0.902

FTD characteristics (current baseline =		
Geometry		
R[mm]	Z[mm]	cosθ
39-164	220	0.985-0.802
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SIT? & SET????

SIT is clearly required to connect VXD and TPC

→ micro-strips seems reasonable option, but pixel technology may ultimately prevail

→ keep simple description until a group is found to take charge

SET is desirable for a number of reasons

(high-lever-arm precision point, TPC calibration)

→ micro-strips can provide required performance

→ tempting to consider SET the first active layer of the ECAL,

this has important consequences for mechanical stability requirements of the calorimeter

Conclusions

Silicon detector R&D is progressing mostly outside the LC, but with clear benefits for ILD

Important optimization studies and increased realism in simulation are not progressing as hoped

VXD workshop next week in Ringberg castle, with all major stakeholders

FTD marginally covered

SIT & SET will remain uncovered until the ILC is approved