SiW ECAL prototype: *"operation task force"*

- Results of the moving of the electronic/DAQ rack from LLR to LAL
- Determination of the pedestal of the fast shaper threshold
  - Small testbenches at LLR (fev11, fev11 with sk2a)
  - Prototype.
- Some Data Quality tools
- Issues to be addressed for the running of the prototype
- Future meetings?

A. Irles,

Orsay 8th Mars 2017

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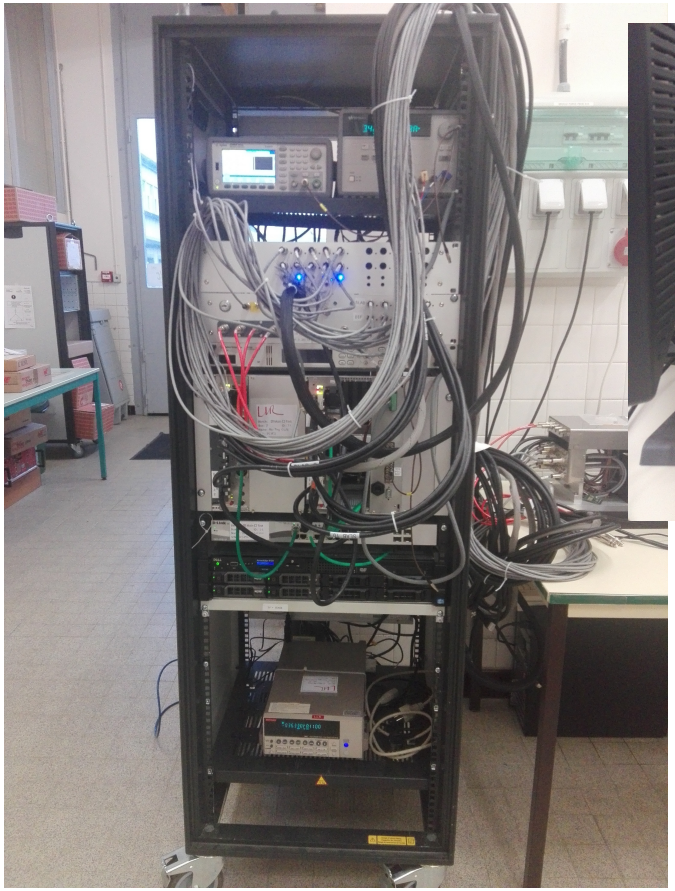
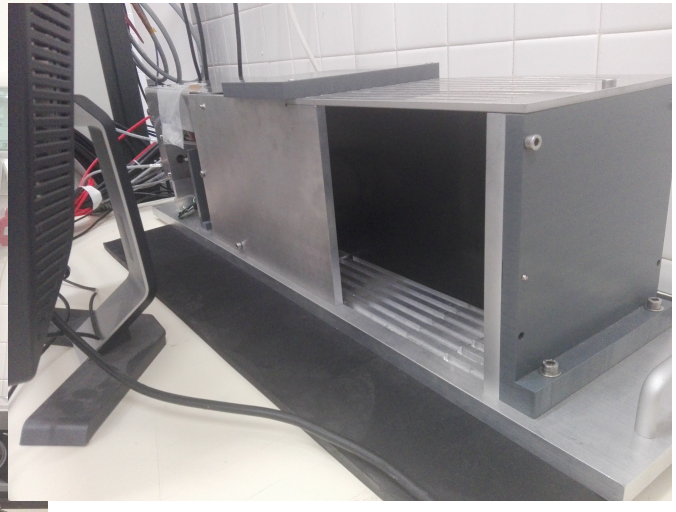
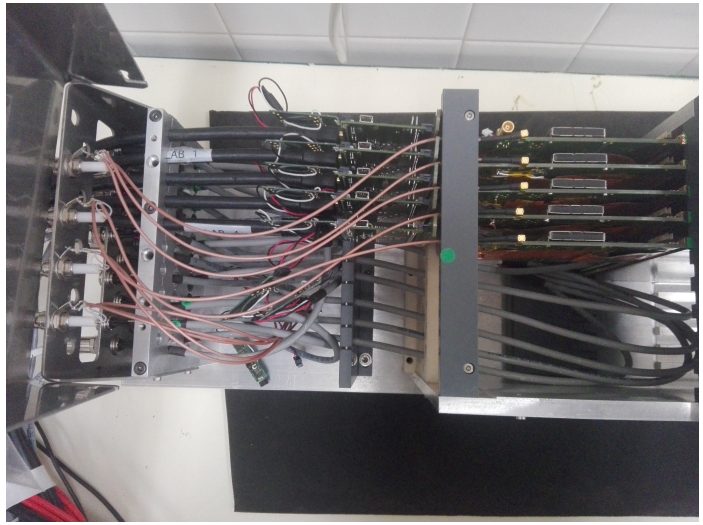
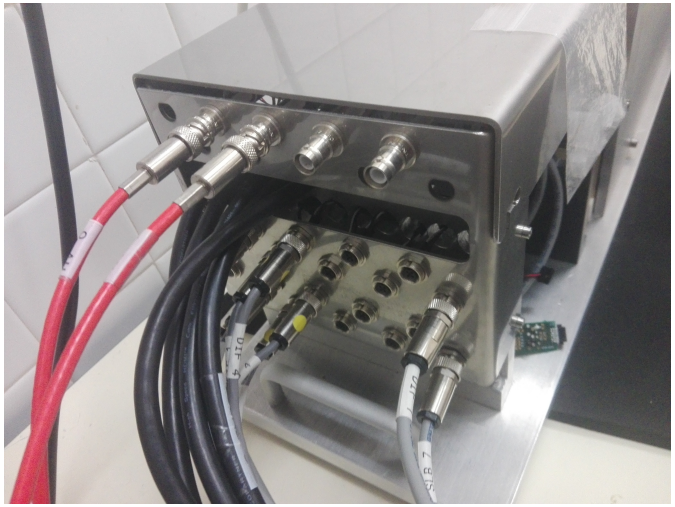
CALICE Calorimeter for ILC

Testbench(es) 2017









Prototype equiped with 5 FEV10 modules with 16 chips, 64 chn each = 5120 chn.

LLR rack with all servers and electronics -->plug and play !!

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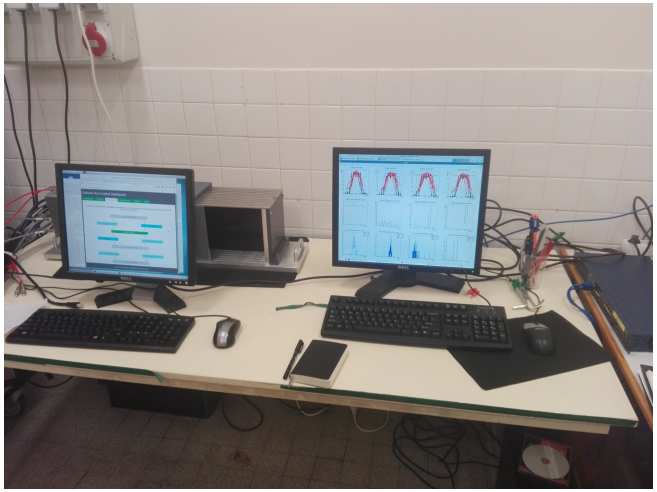
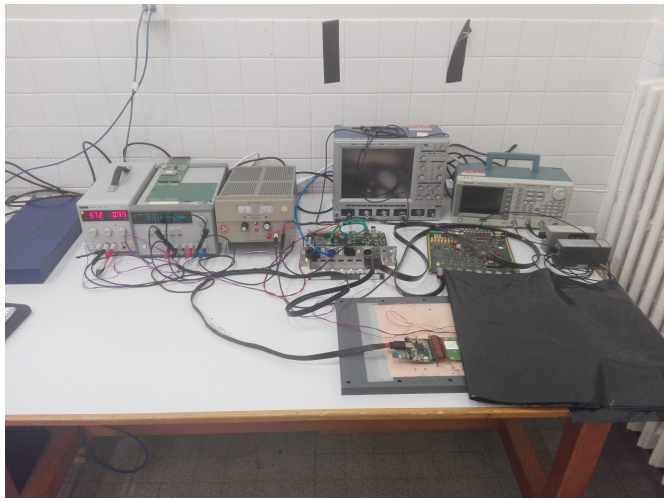
TestBench 2017





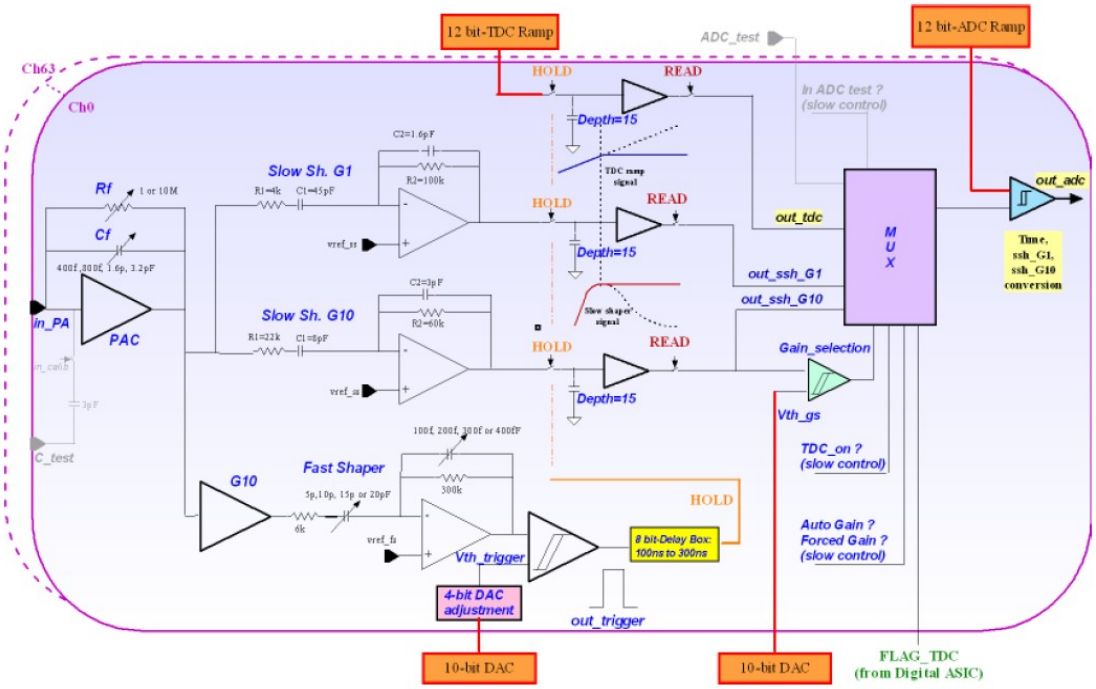
- Two testbenches together (from left to right)
  - Electronic rack for the prototype
  - Control PC of the proto and the proto itself (behind)
  - Monitoring PC (for both testbenches)
  - Testbench of single modules (FEV8)
- Weeks of work together with engineers from LAL, LLR and OMEGA

TestBench 2017 : next steps

- Set up the LAL rack
  - Power supplies, DAQ electronics, networking, etc
- Carefully test the new DAQ software and the prototype performance → noise studies
- Hands on with our colleagues from Korea
  - Still some issues observe during chip configuration but we get data that make sense (?)... → being investigated
- Continue developing and testing the Data Quality framework.

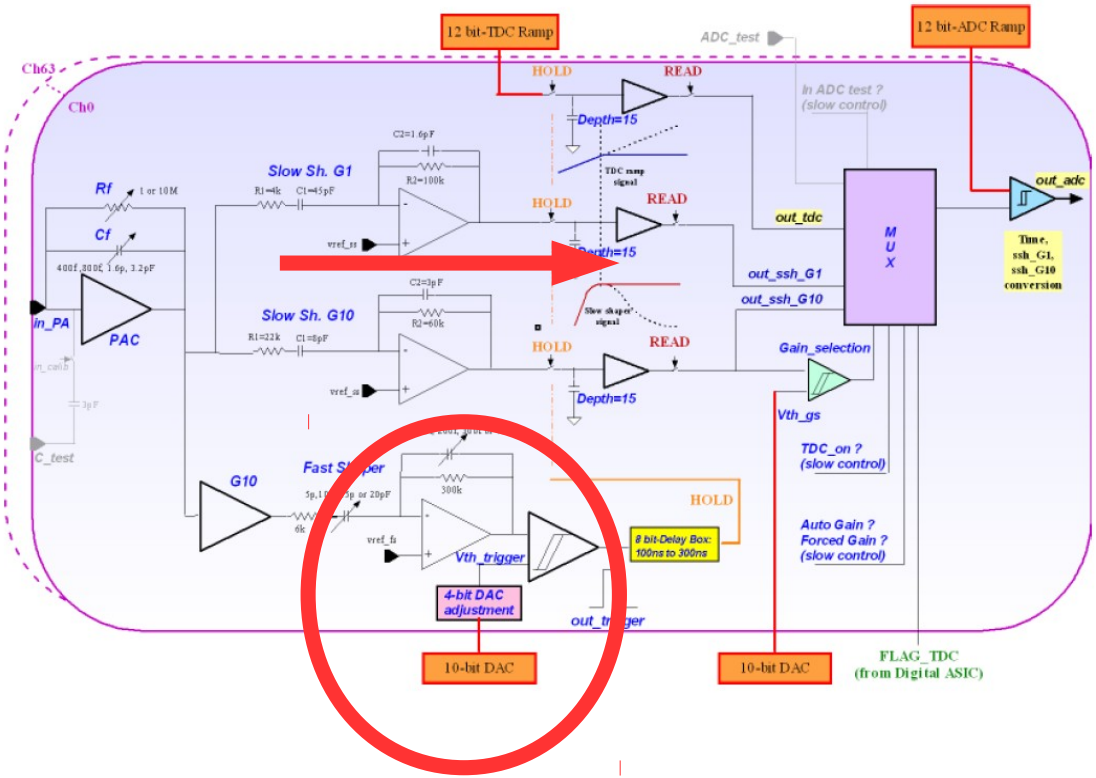
- Getting used to the full set of tools and test/debug methods → in close contact with Stephane, Remi, Frederic, Miguel, Jêrome, et al

Determination of the pedestal of the fast shaper threshold → Scurves



LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Determination of the pedestal of the fast shaper threshold → Scurves



- Establish the pedestal of the fast shaper threshold (DAC)
  - What precision is needed?
  - What are the historical values used (test beam, cosmic runs, etc)
- Scurves with DAQ
  - Make a scan varying the threshold values.
  - Count number of hits per channel (hit bit == 1)
  - Count SCA = 0 or all

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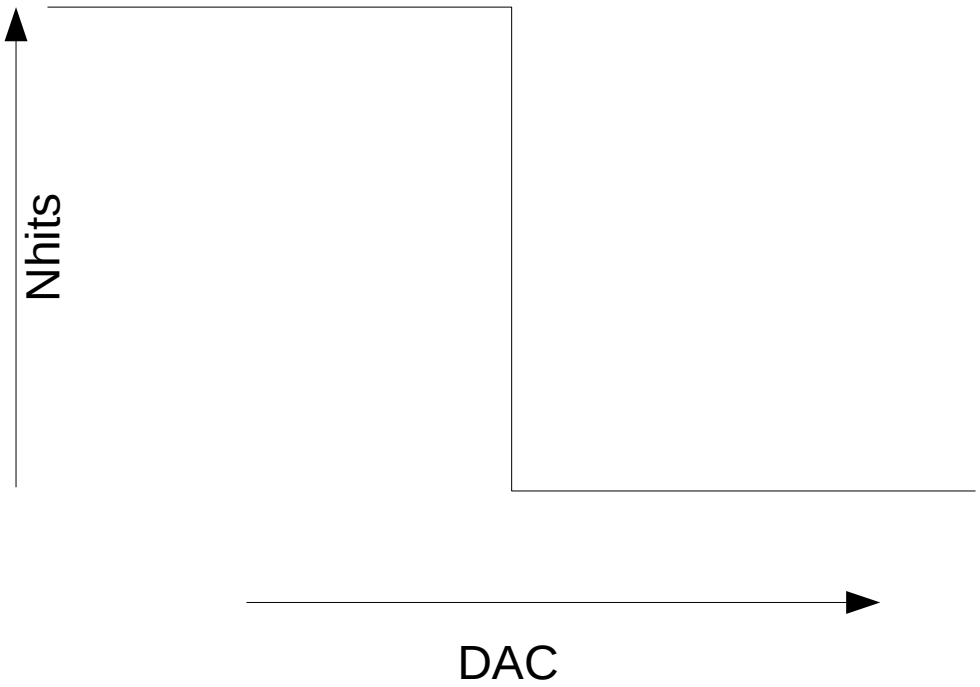
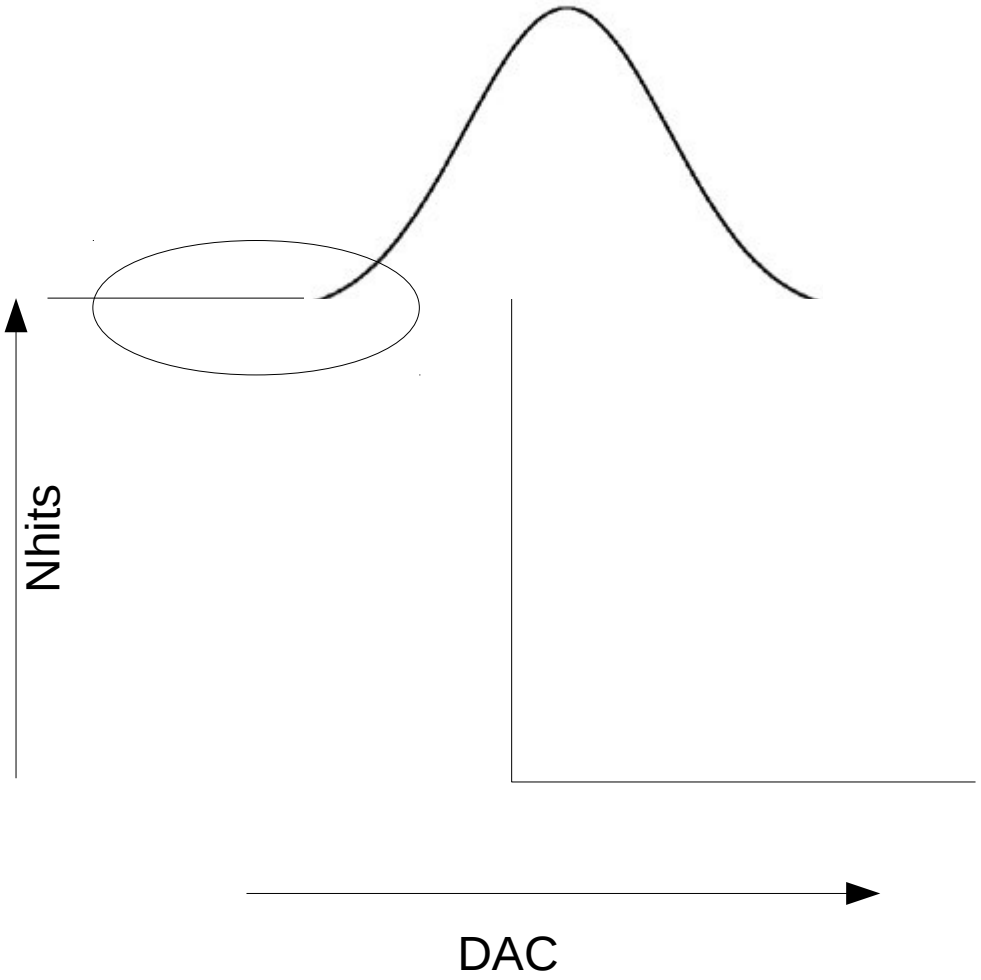
Determination of the pedestal of the fast shaper threshold → Scurves

- SCA = 0



LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Determination of the pedestal of the fast shaper threshold → Scurves



- SCA = 0
- SCA > 0
  - For low values of the threshold → “saturation”: in SKIROC/SPIROC, there is a Rising Edge detector... If a discriminator output is always set to 1, the detector doesn't see any rising edge, therefore the chip does not write anything.
  - Can be removed from the analysis by requiring
    BCID > val_evt_bcid + 15
    Needed?
  - Every SCA has different pedestal.

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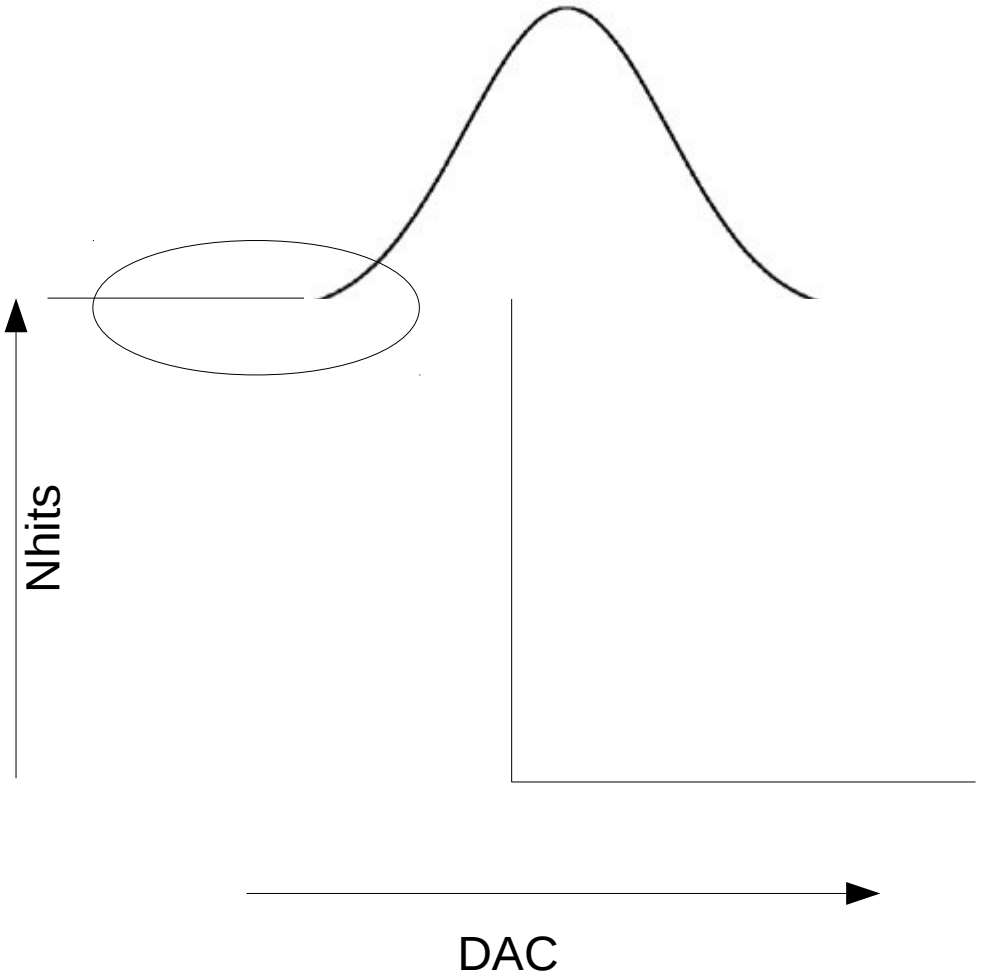
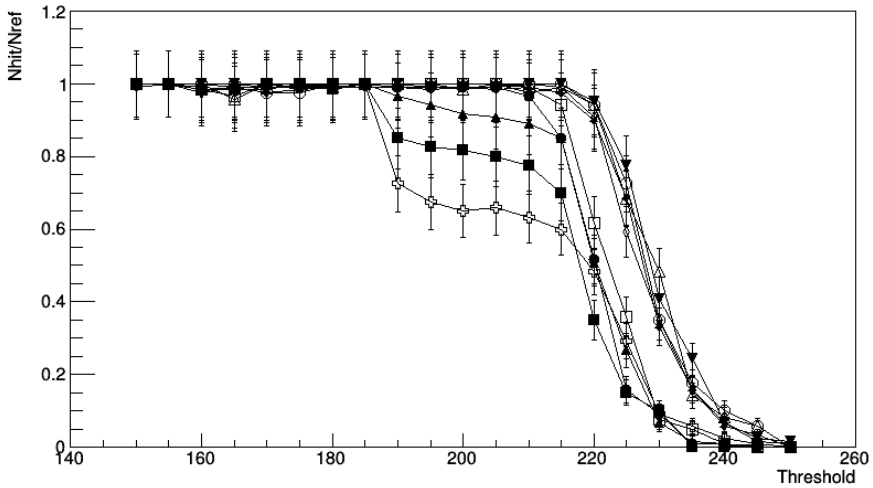
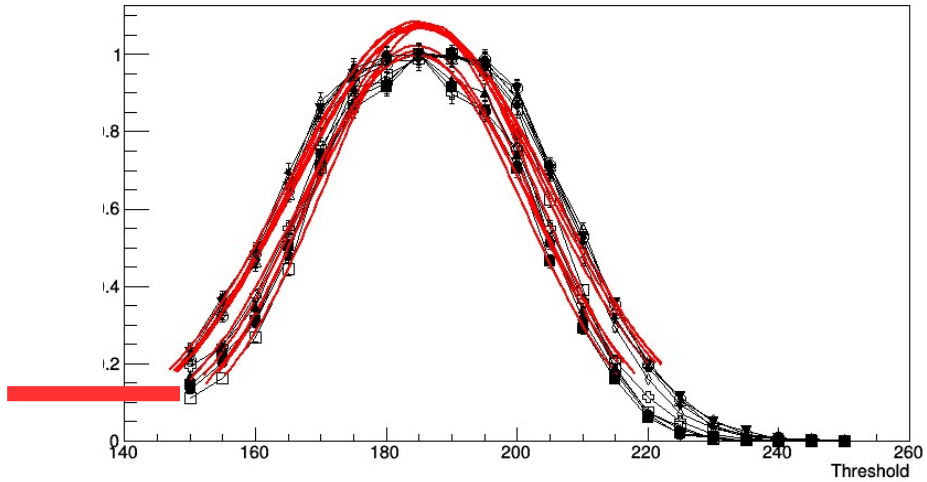
Determination of the pedestal of the fast shaper threshold → Scurves







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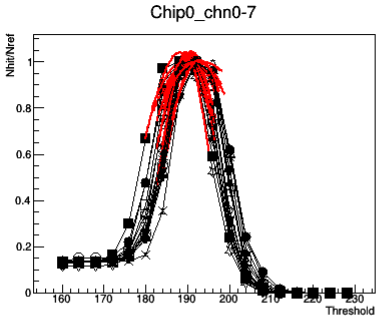
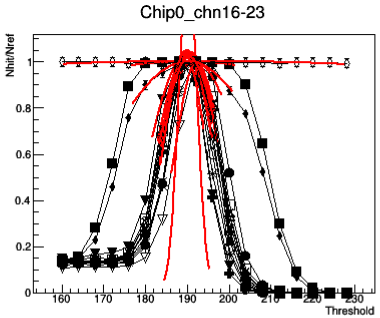
Some results from the “small” tesbenches at LLR

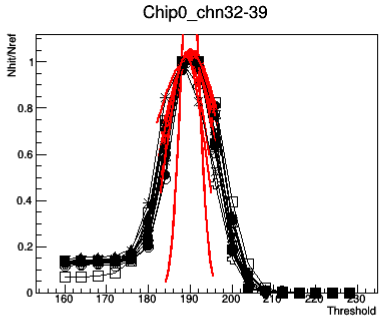
- Studies done after some discussions between Vincent, Artur, Shriddha and myself.
- Preliminary results → Artur has more data and he has look into it in more detail.
- Methodology → compare the scurves for the 15 SCA, taken with different conditions:
  - Enabling trigger for groups of 8 or only one channel
  - Long spill length (10-100 ms) vs short spill (few us) after the val event signal.

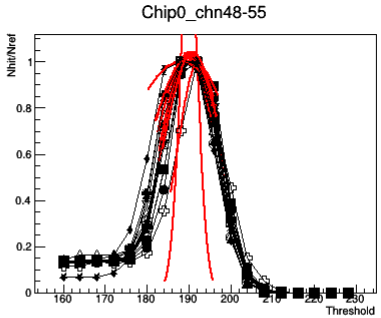
    val_evt_bcid == 1246
  - Fev11 with sk2 and fev11 with sk2a
- Fit of a gaussian to the scurves:
  - Iteration 1 → find the maximum
  - Iteration 2 → fit a gaussian around this maximum (all range), extract Mean1, sigma1
  - Iteration 3 → use Mean1, sigma1 as input and reduce the range to (M1-3s1,M1+3s1), extract M2,S2
  - Iteration 4 → use M2, s2 as input and reduce the range to (M2-s2,M2+s2), extract the final values.

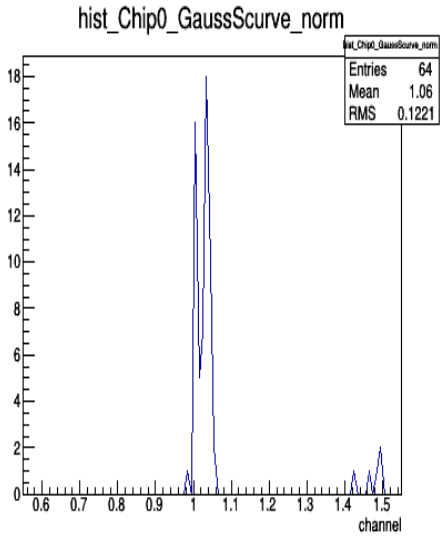
FEV11, SK2a: no cut in BCID

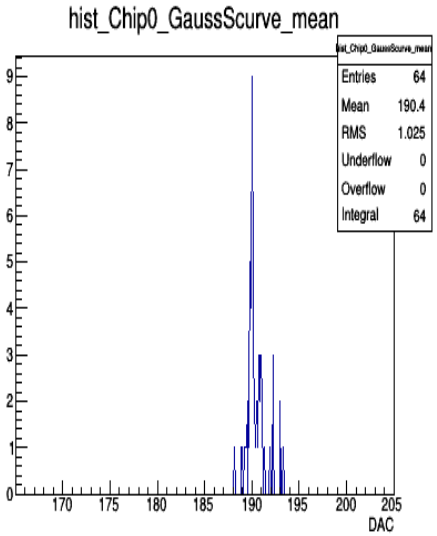


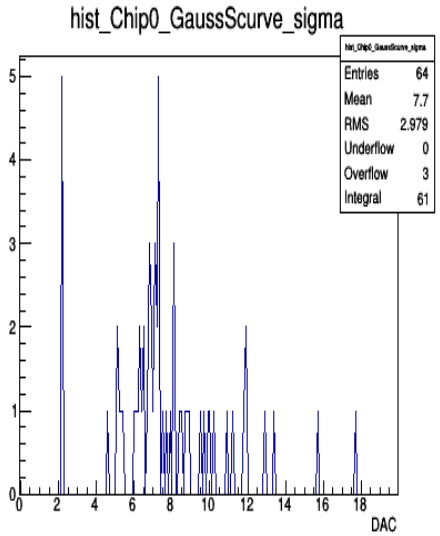


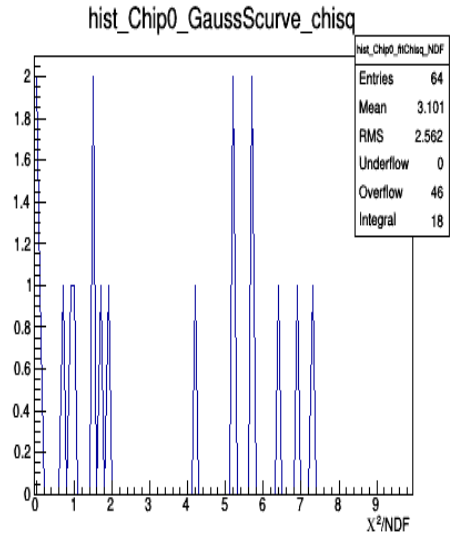












No BCID cut**, only one channel enabled**

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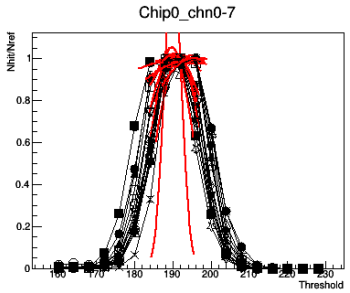
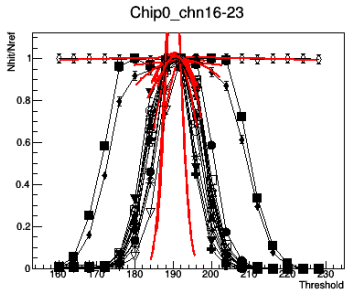
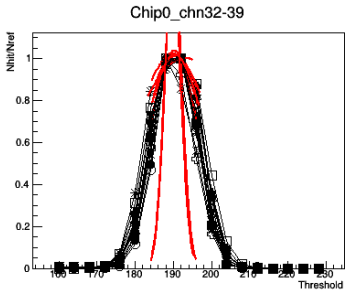
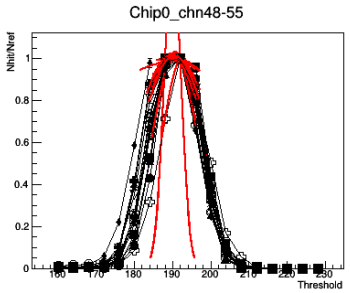
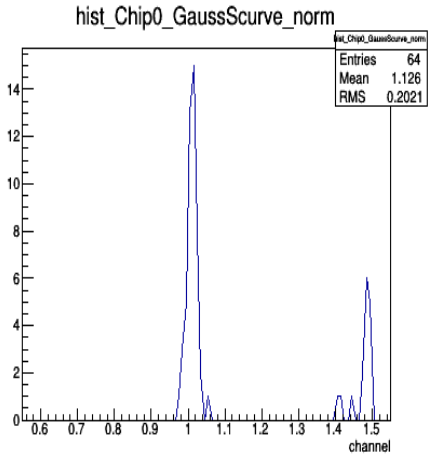
FEV11, SK2a: cut in BCID (remove val_evt bcids)

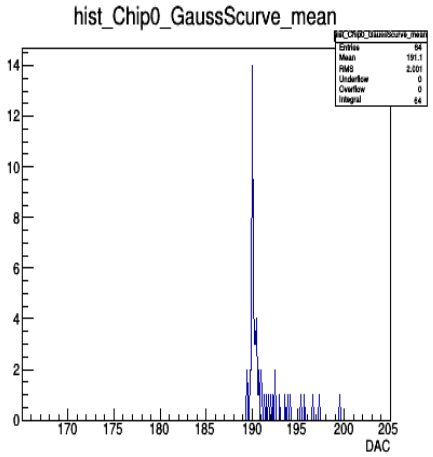


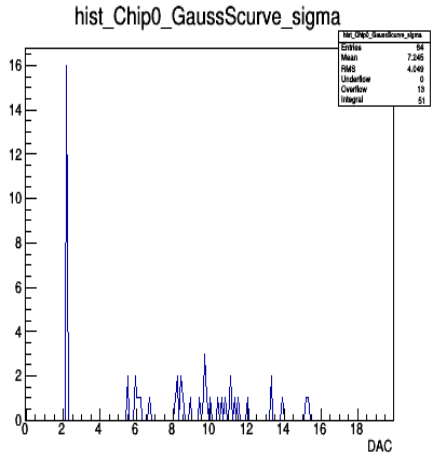


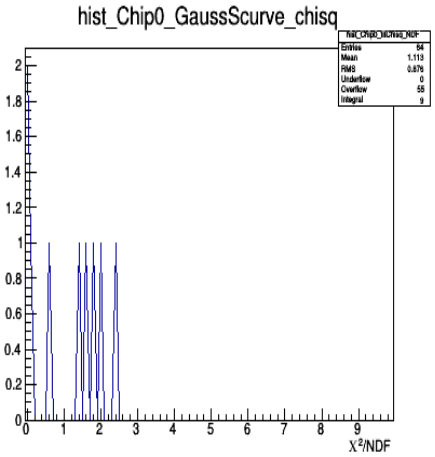












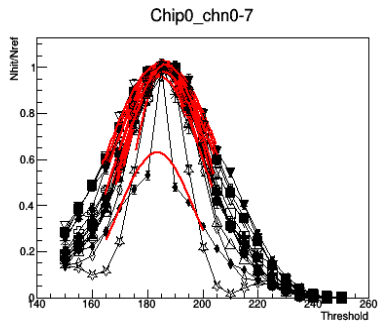
BCID > 1250**, only one channel enabled**

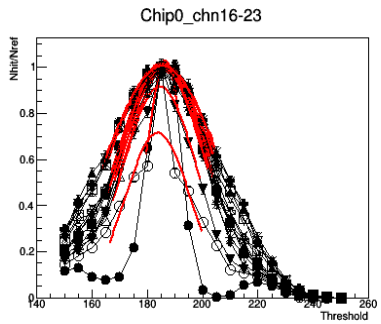
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

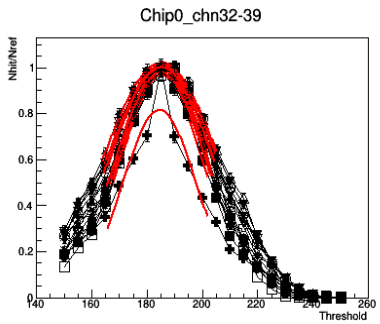
FEV11, SK2a: with val_evt vs without val_evt bcids

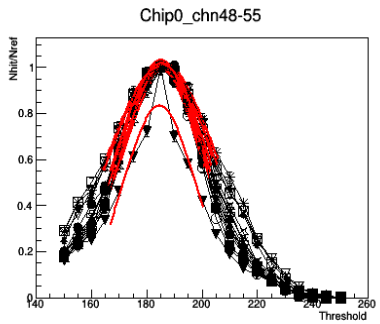
- Higher cuts in the BCID remove the “step”at low values of threshold
- The mean / var do not change substantially
  - But the quality of the fits seems to decrease (the cut in BCID eats a lot of events! → need longer runs)

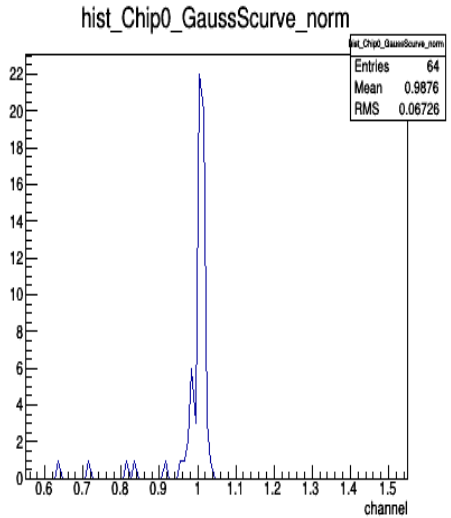
FEV11, SK2: short spill, no cut in BCID, 8 channels enabled

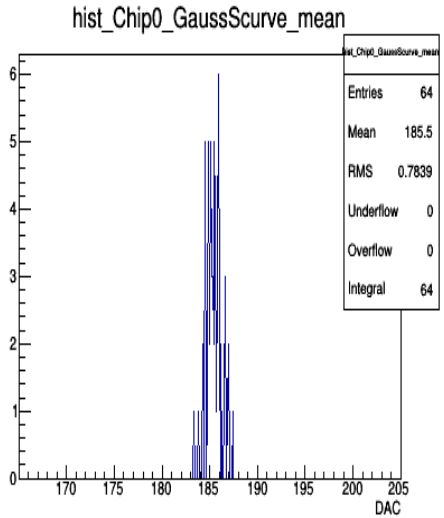


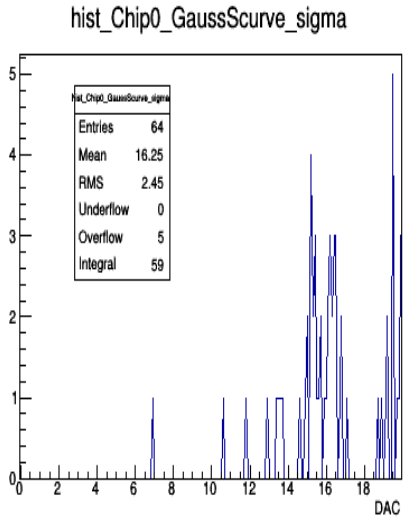


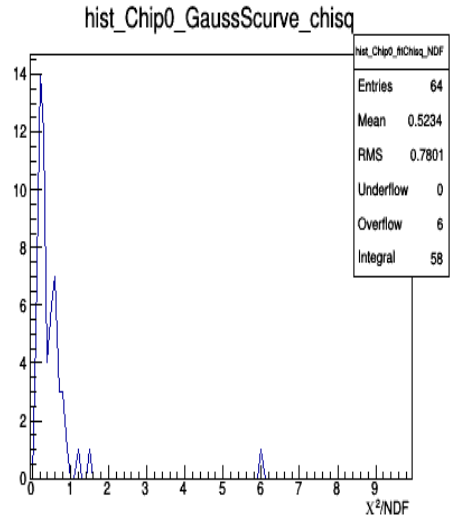












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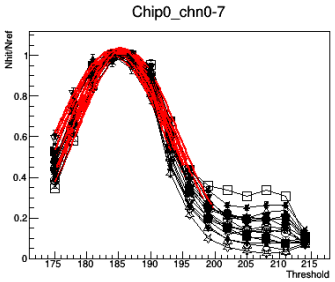
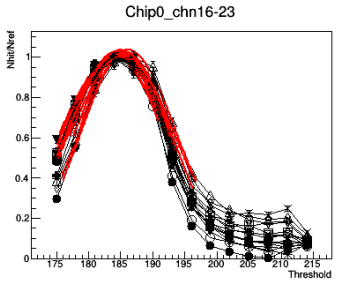
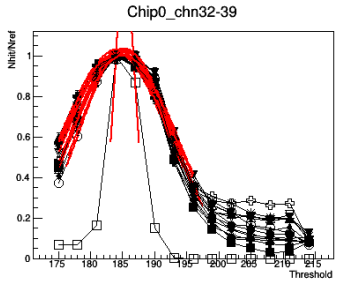
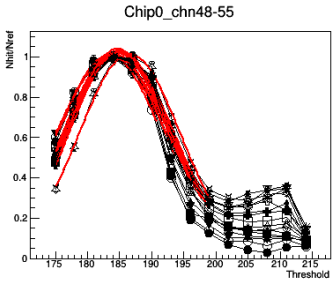
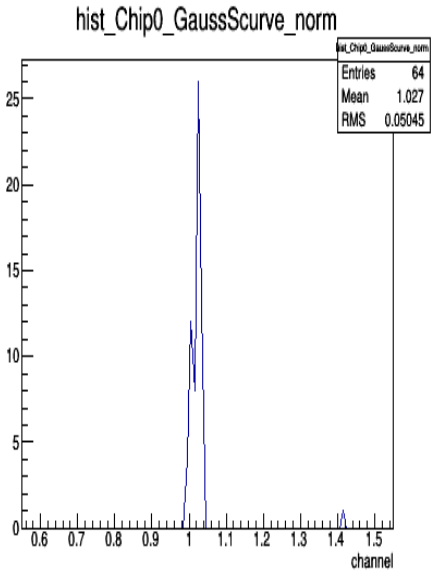
FEV11, SK2: long spill , no cut in BCID, , 8 channels enabled

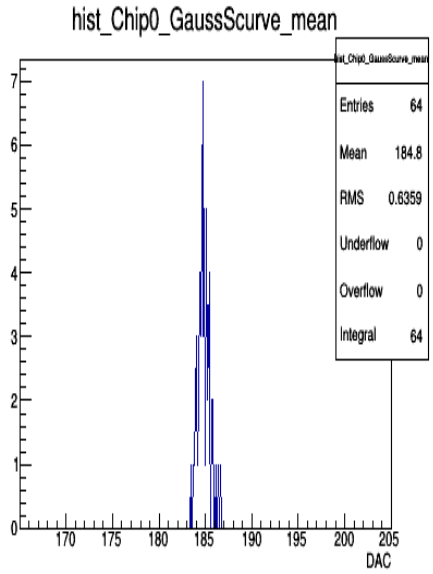


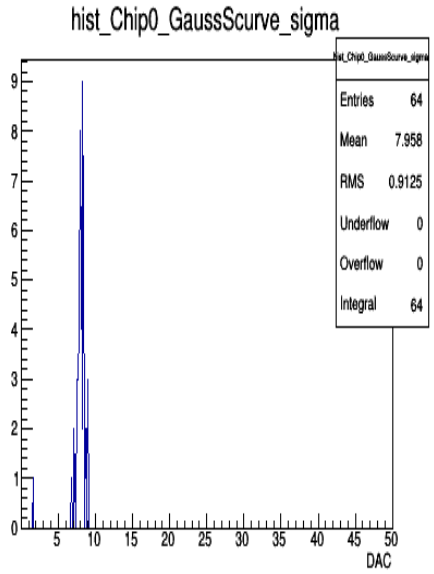


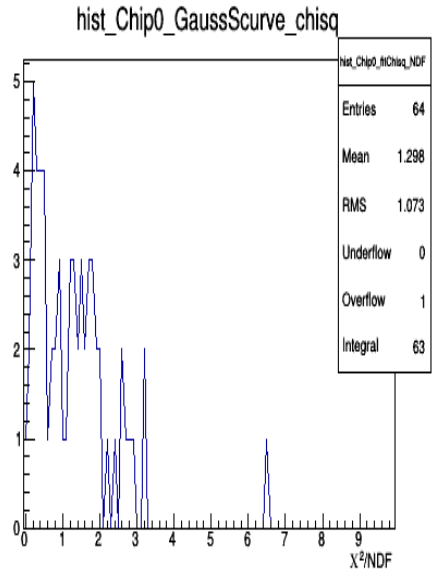












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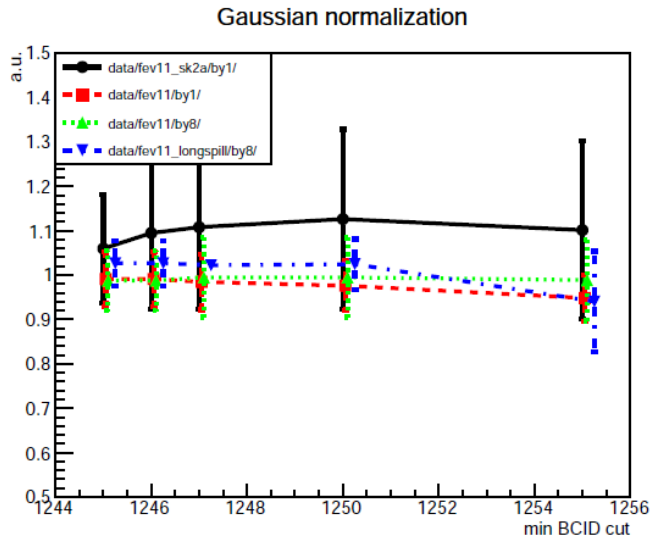
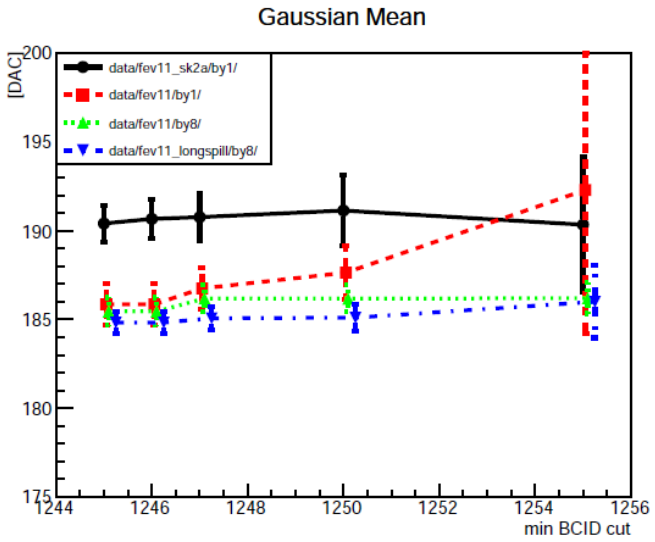
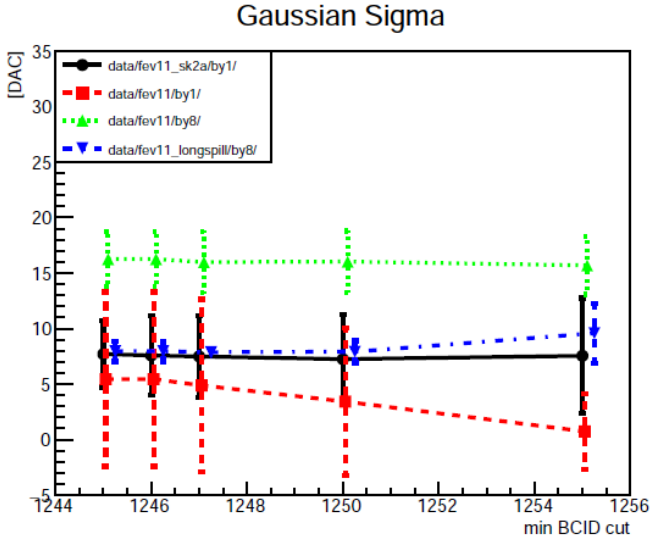
FEV11, SK2: long vs short spill

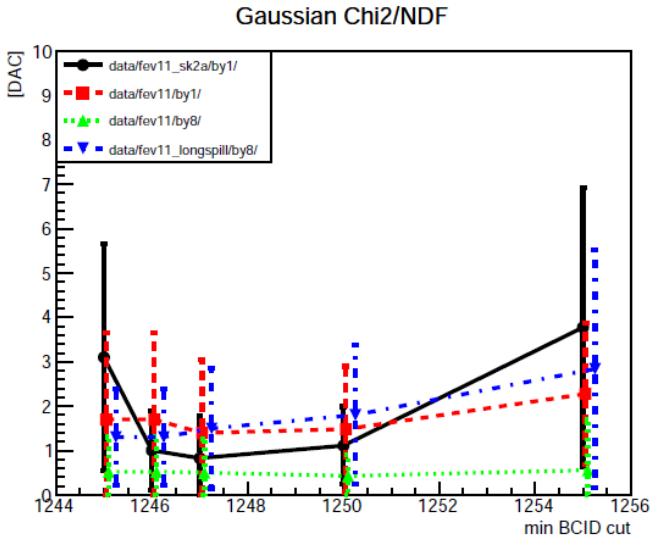
- The length of the spill affects to the shape of the scurve
  - The random BCID+1 issue?
- Mean value of the pedestal threshold are the same.
  - Short spill → mu=185.5(0.8) sigma=16,25(2.4) DAC
  - Long spill → mu=184.8(0.6) sigma=7,9(0,9) DAC

All comparisons: in general good agreement





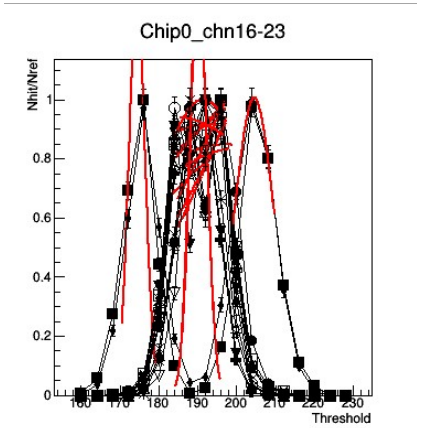




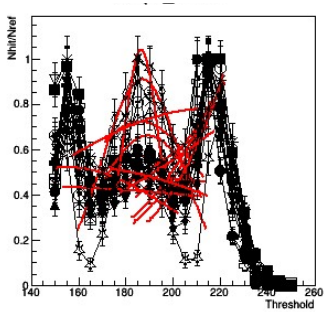
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

Issues observed:

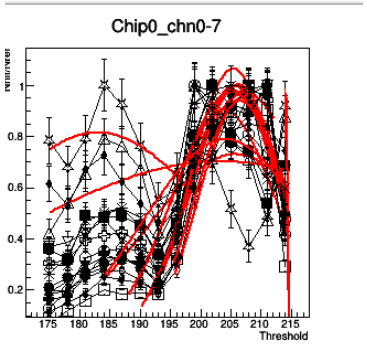
- Plane scurves → same number of hits for all threshold values (damaged channel? Missconfiguration?).
- Two-three peak structures when the cut in BCID is too high.



Sk2a, short spill



Sk2, short spill



Sk2, long spill

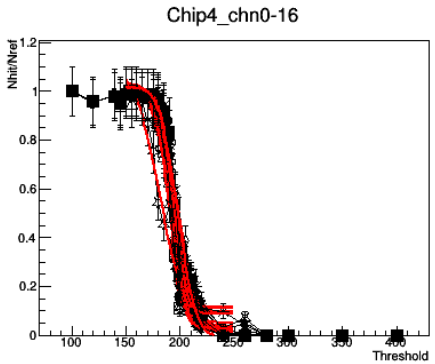
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

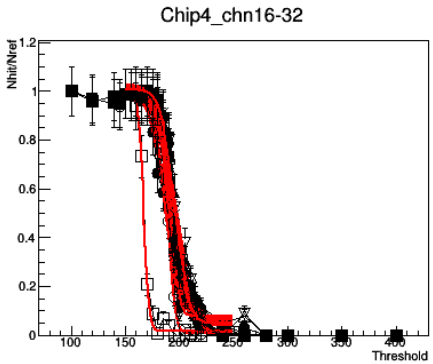
Some results from the SiWLC ECAL prototype: 5 slabs

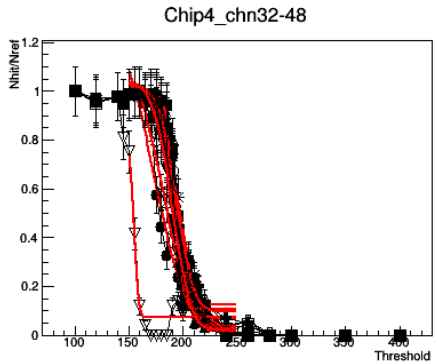
- Preliminary (fresh) results !!
- Methodology → compare the scurves with different conditions:
  - Groups of 8 channels or 64 with enabled trigger → **I only show plots today for 64 channels** enabled run but results look very consistent.
  - Only SCA=0 vs all SCA (short vs slow analysis)
- Done for 5 DIFs with 16 ASICs each
  - Only look at few chips.
- Fit to error/gaussian function also iteratively.
- No cuts in val_evt_bcid or short vs long spill comparisons → some issues observed during the data taking !! (see later)
- Only show results for DIF 1, chips 0 and 4 (more or less representative of all)

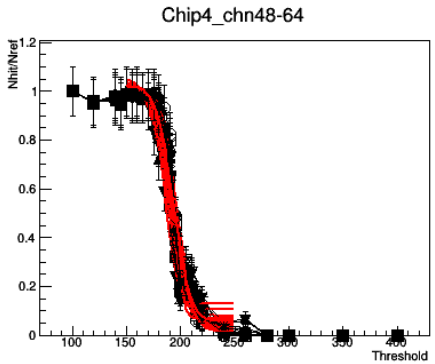
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

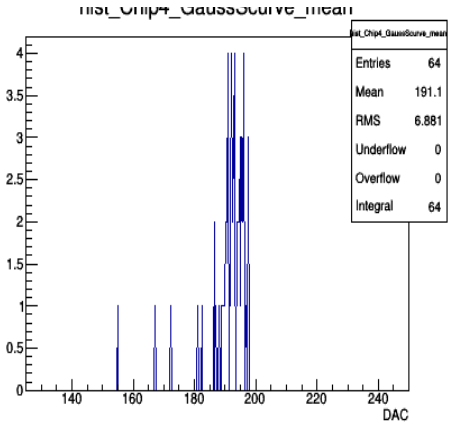
ASIC 4, 64 channels enabled, SCA=0



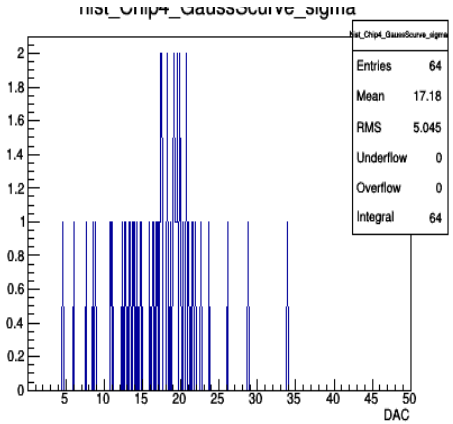




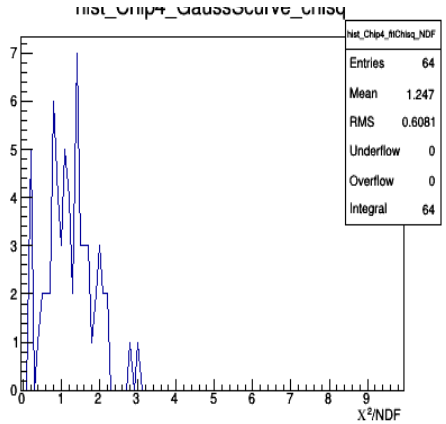




Mid point of the error function



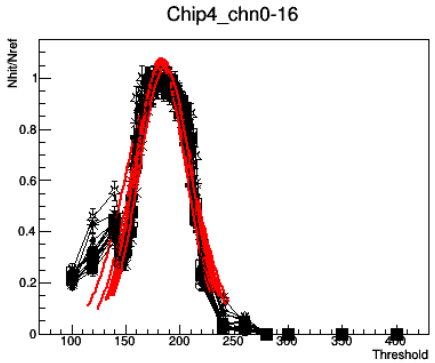
Width of the error

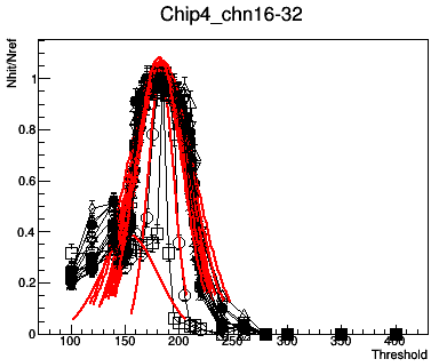


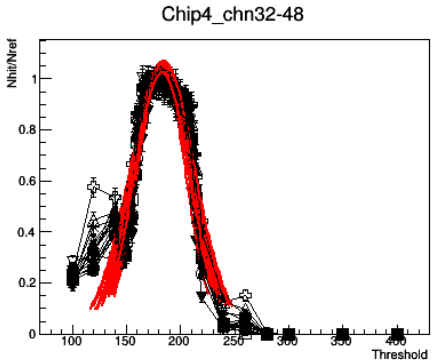
Chi²

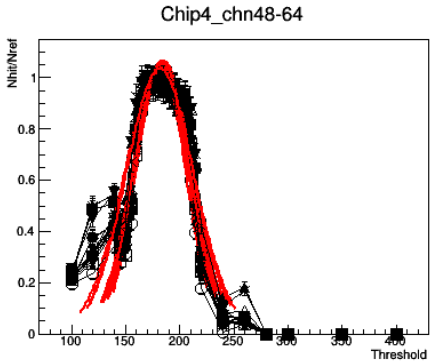
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

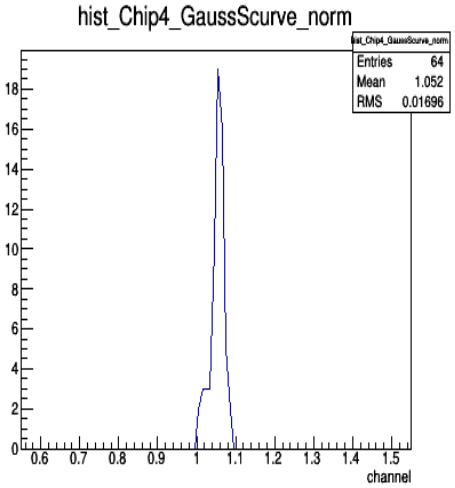
ASIC 4, 64 channels enabled, all SCA

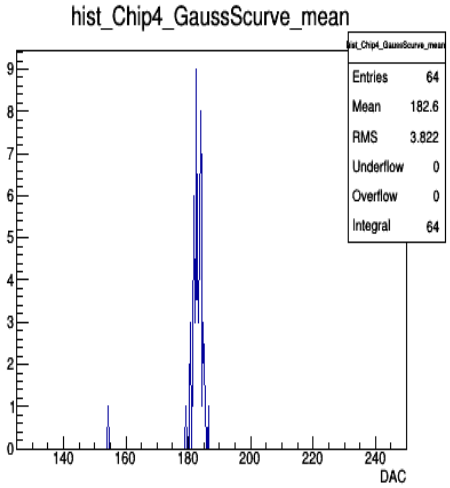


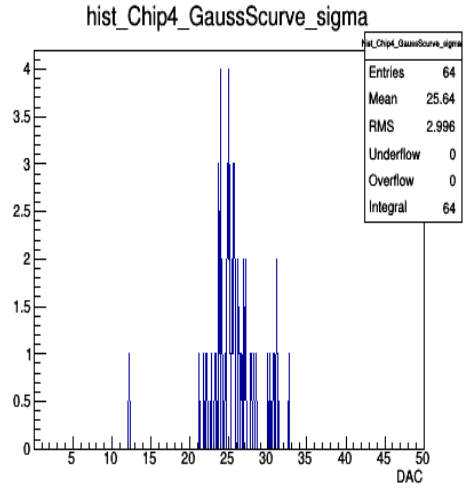


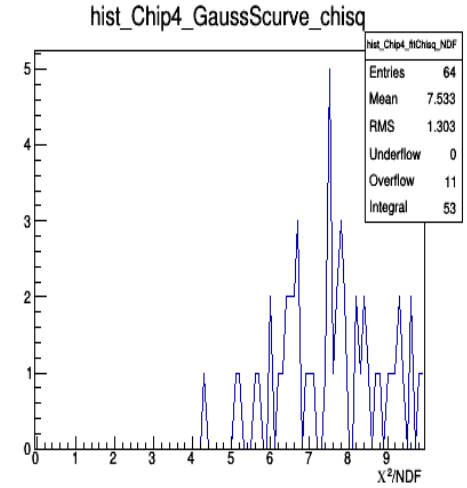










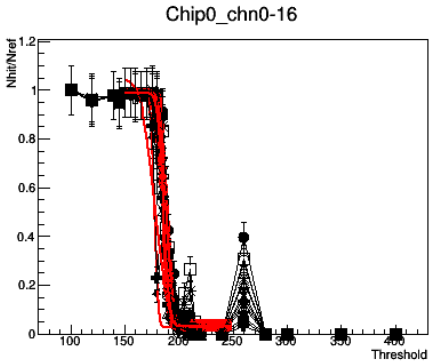


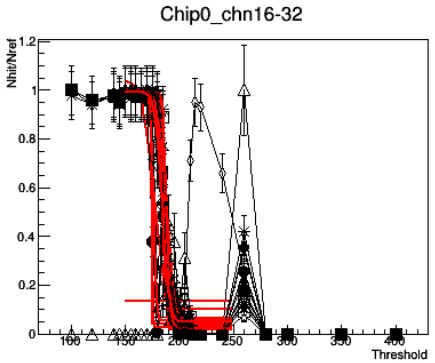
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

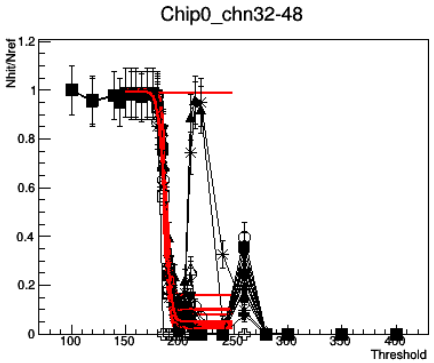
ASIC 4, 64 channels enabled, all SCA

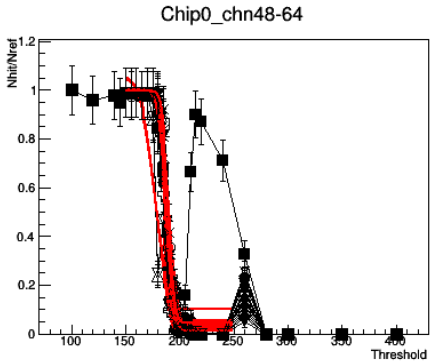
- Both methods allow to extract the value of the threshold to be far of.
  - The gaussians are a bit wide but the extracted values are consistent.

ASIC 0, 64 channels enabled, SCA=0





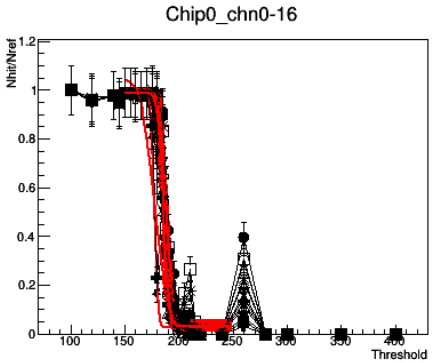


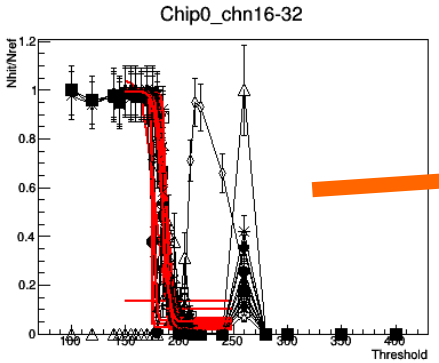


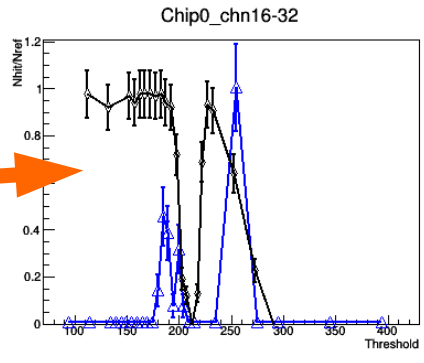
- Noise ?
- Observed in several chips → more detailed studies needed

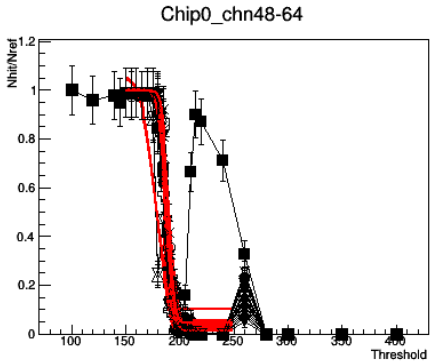
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

ASIC 0, 64 channels enabled, SCA=0





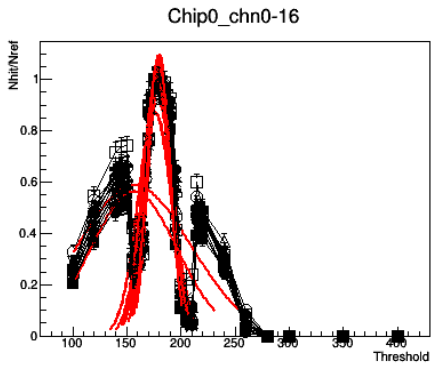


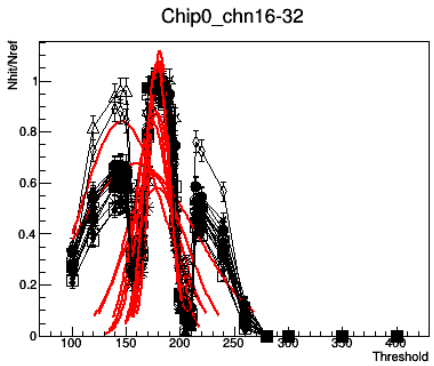


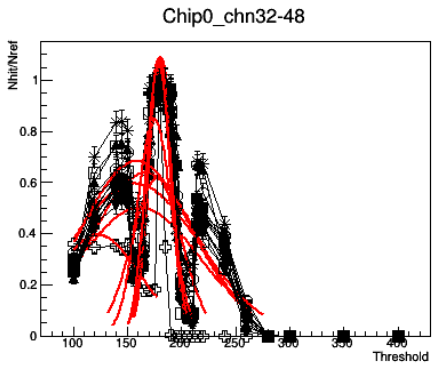
- Noise burst (?) consistent for several runs.
  - Stays if we enabled 64 or only 8 channels (what about 1?)

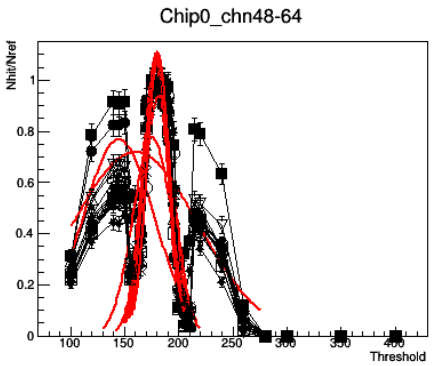
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

ASIC 0, 64 channels enabled, all SC









- ???
- Same chip and run than before.

LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

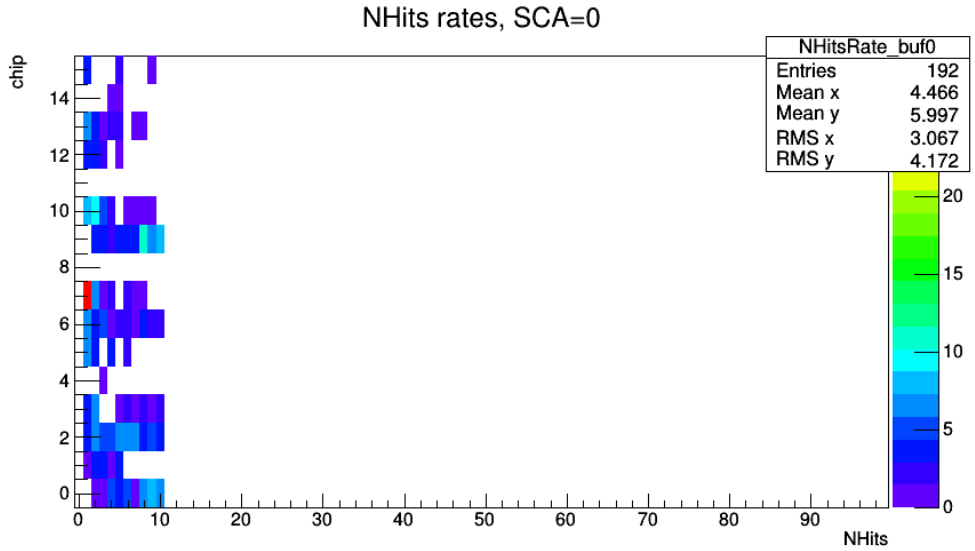
ASIC 1, 64 channels enabled, SCA>0

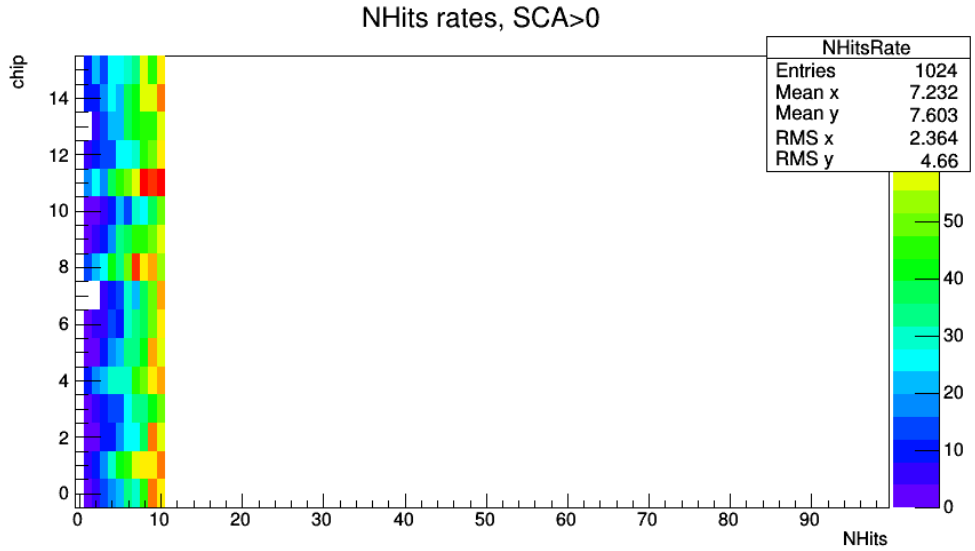
- Both methods allow to see how strange is the data
  - :-(
- Even if the analysis fails (fit to error function / gaussian), we can extract by eye a minimum value of the threshold to be set → larger than 250 DAC which already cuts in the MIP position :-(

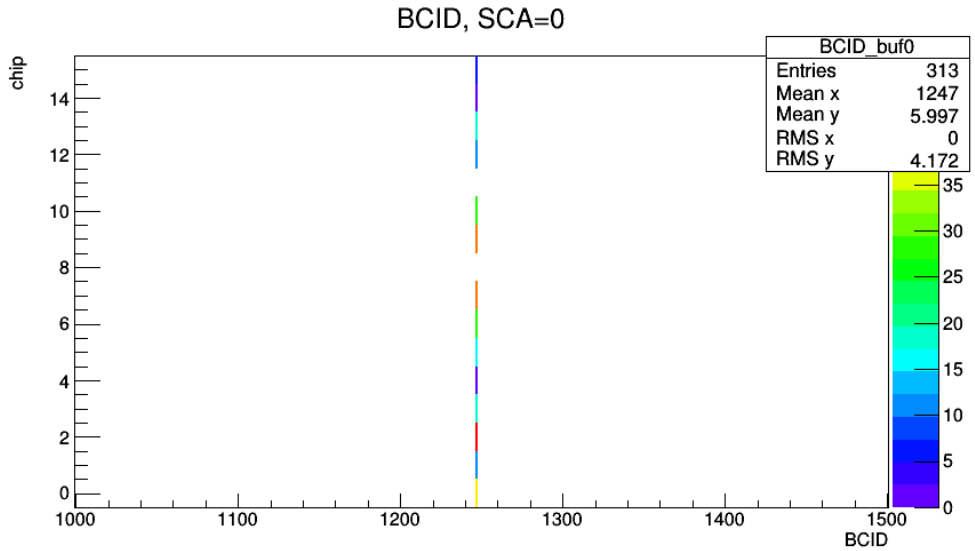
Data Quality

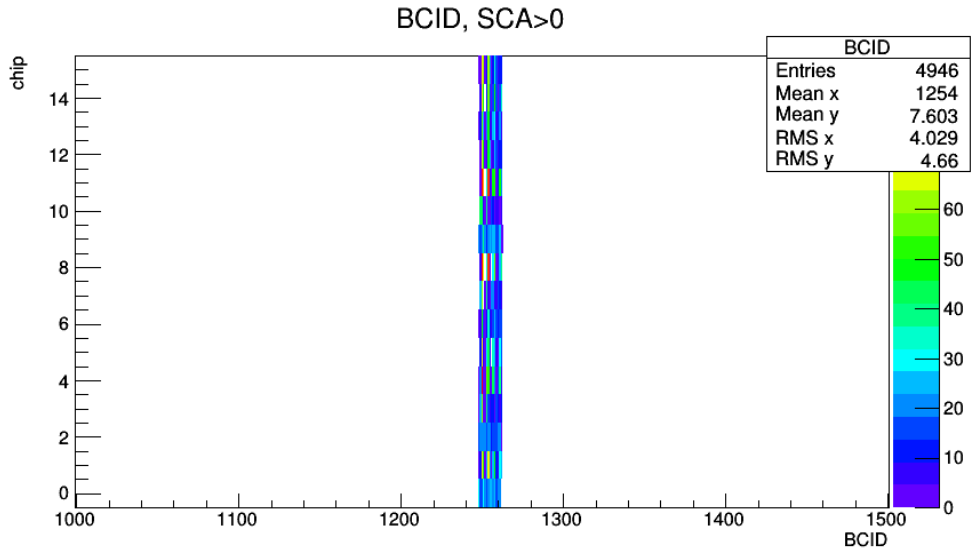
- I will work together with Frederic in the implementation of DQM4HEP in CALICOES
  - Not inmediately since this will take me some time.
- For the moment we have a rudimentary semionline Data Quality analysis framework that fulfills two functions:
  - Quick monitoring (chip and channel modules)
  - Quick analysis module manager: scurves, pedestal (ADC) extraction, MIP fit with pedestal subtraction, etc.
- It is under development: temporary repository https://github.com/airqui/tpecal/
- Is based in root and uses root files. Nothing else is needed (calicoes, pyrame, etc). To be run in the laptop (even though is not very well CPU usage optimized).
- Examples of Chip and Channel Monitor Modules:
  - Dif_1_1_1
  - Spill lenght = 0.5 ms

Chip Module: threshold = 190 DAC

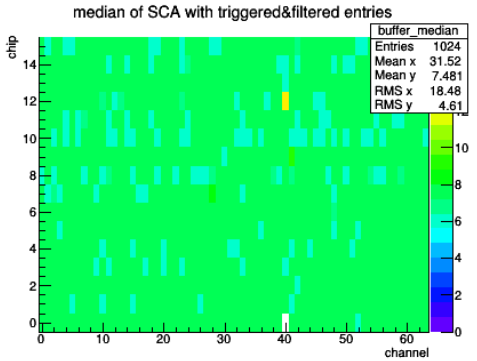




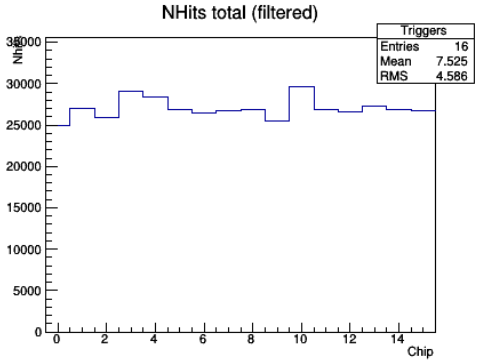


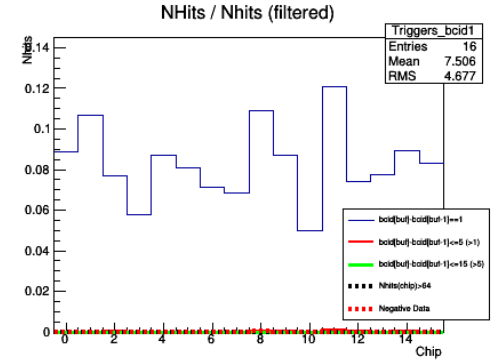


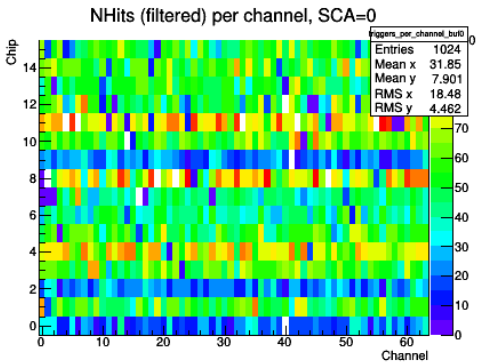
Channel Module: threshold = 190 DAC

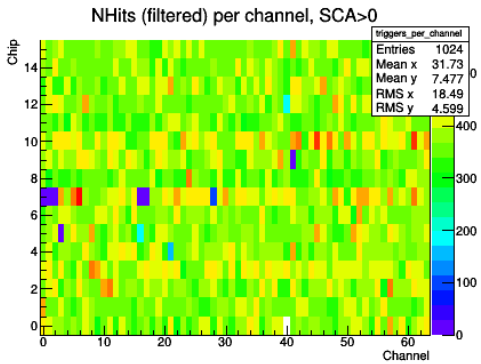


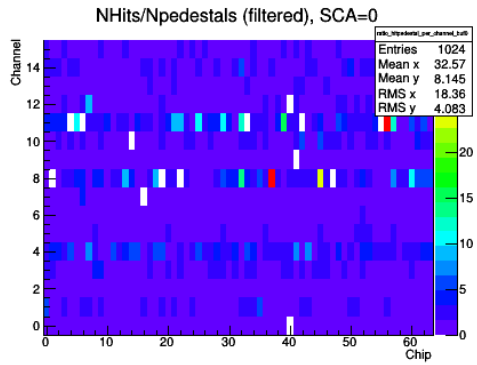
Filtered means:
charge>10,
nhits<64

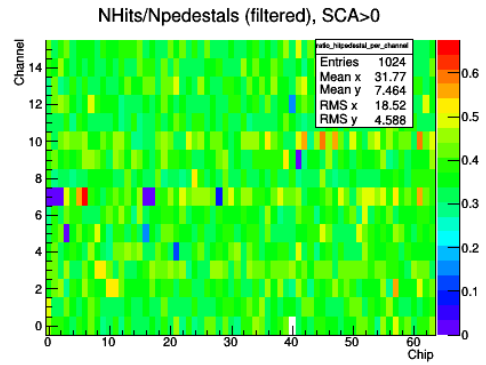


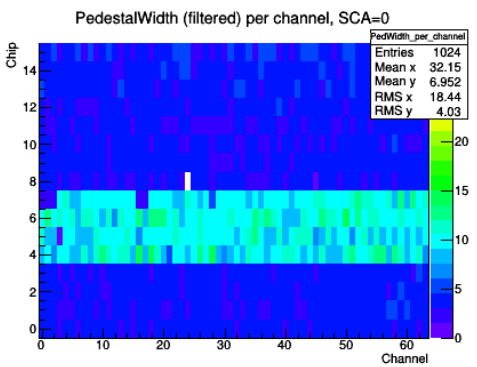


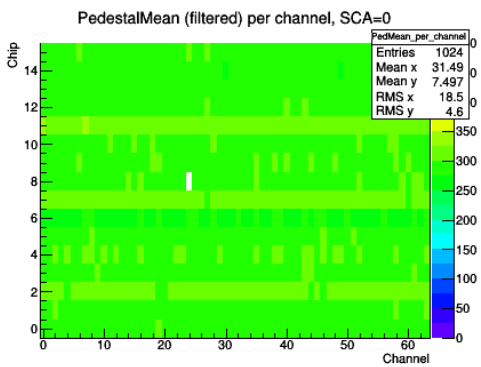


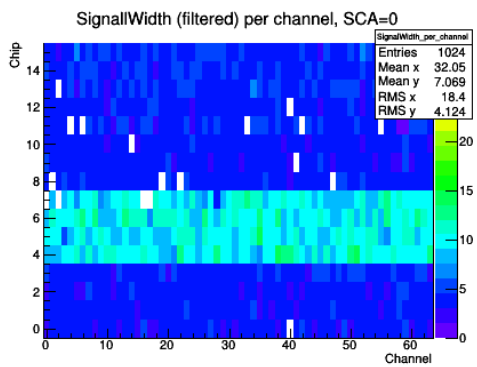


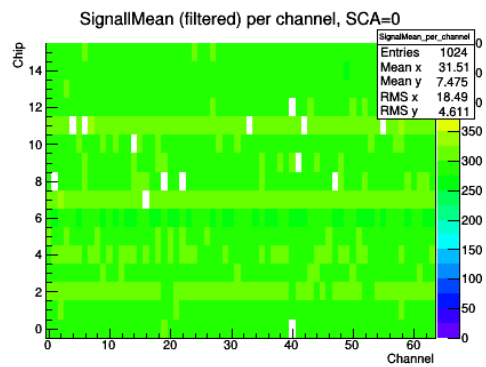




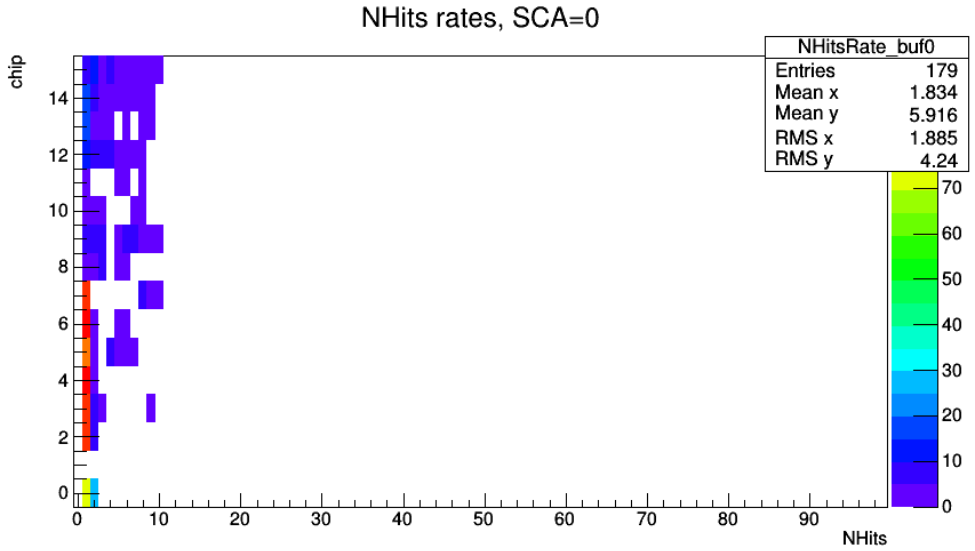


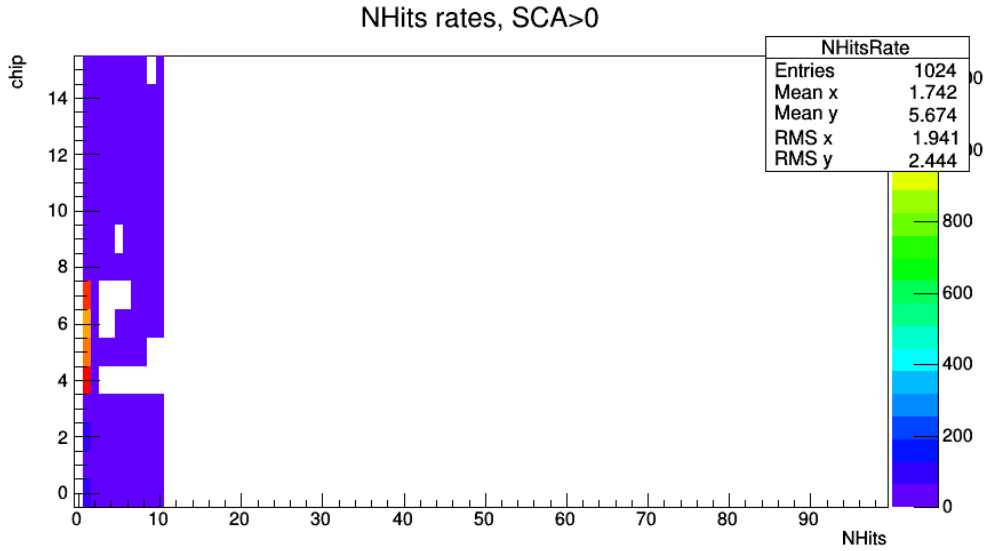


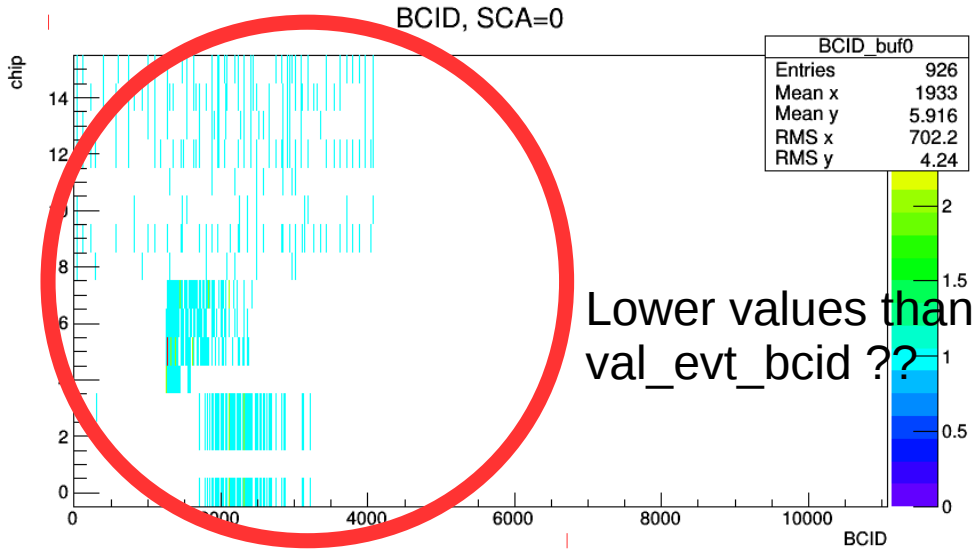




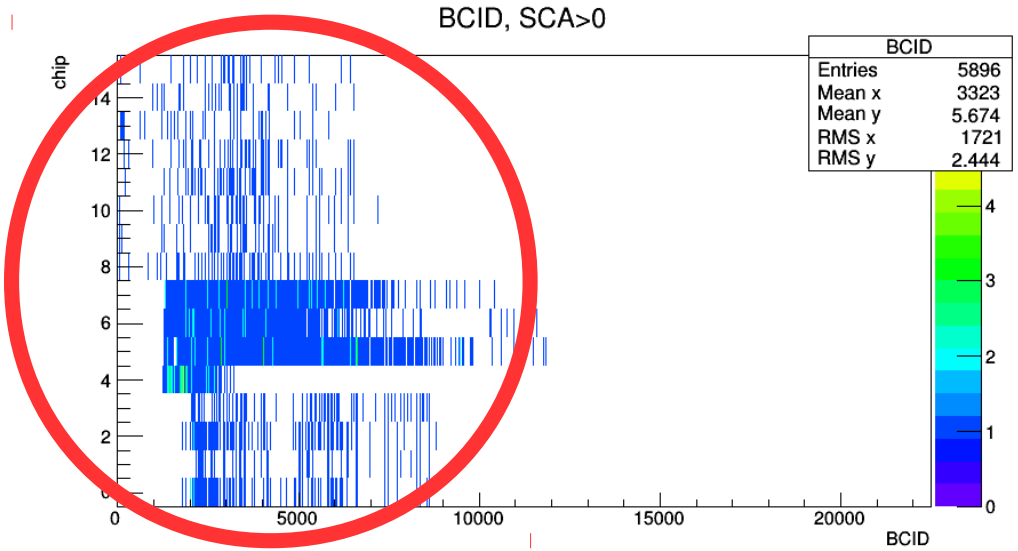
Chip Module: threshold = 250 DAC





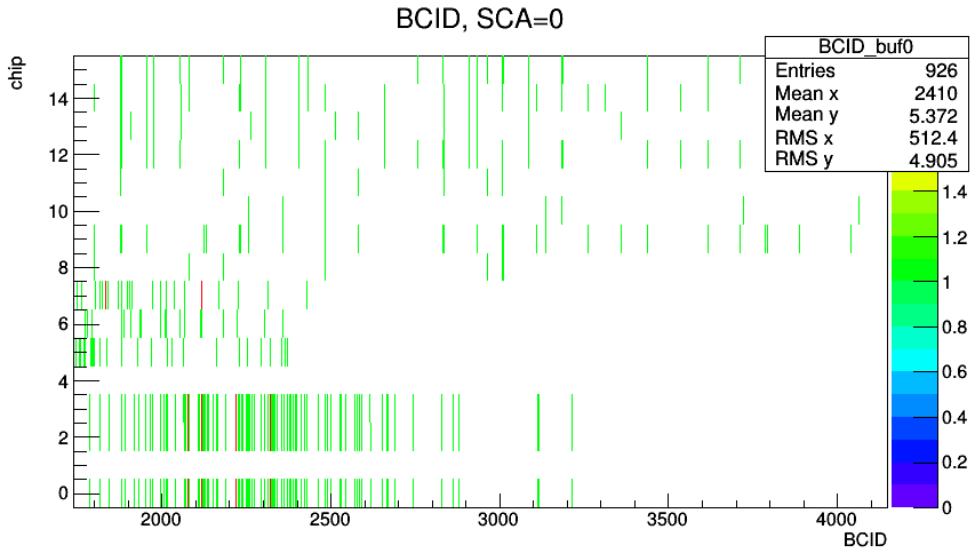


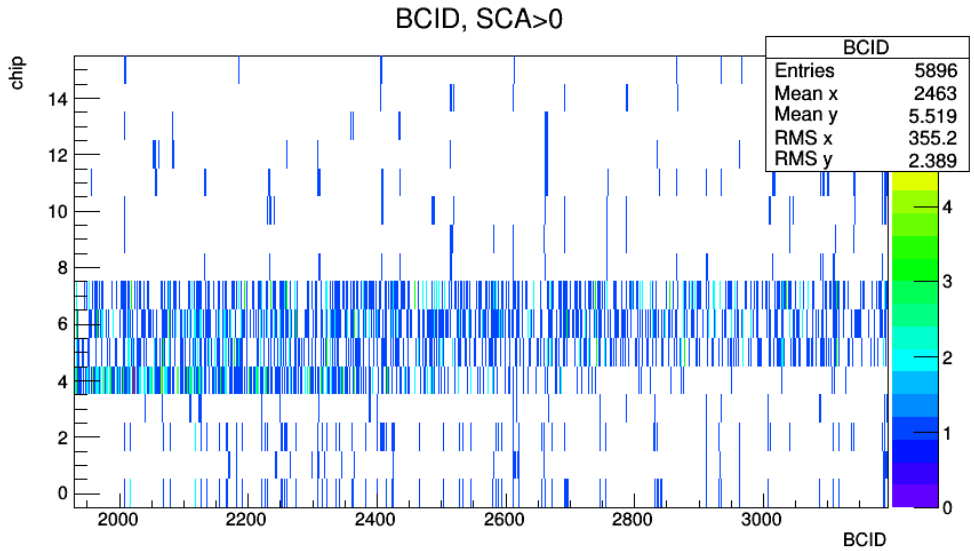
Lower values than val_evt_bcid ??



Chip Module: threshold = 250 DAC

Pattern ??



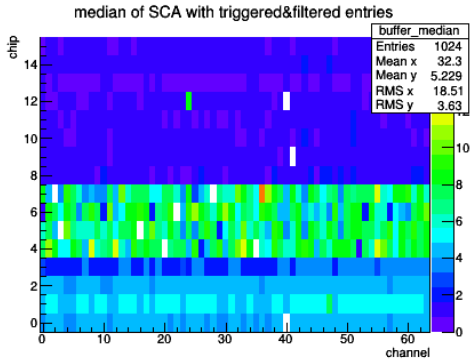


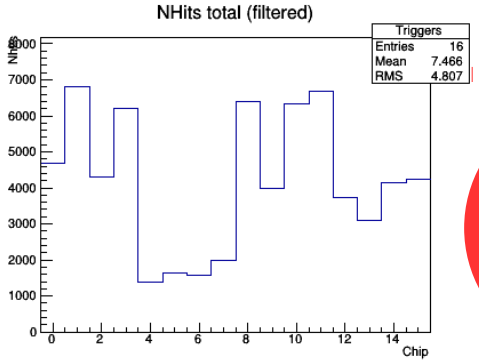
Somes Issues found

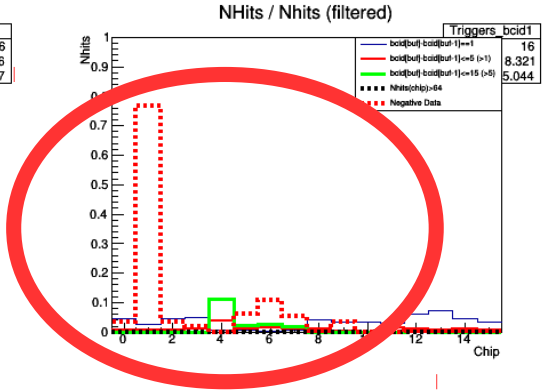
- The most puzzling to me is that the spill length was 0.5 ms
  - → 0.5 ms = 500 us = 2500 BCID tics.
- And that the val_evt_bcid was 1247...
- We should never see bcids lower than 1247...
  - except if the calculation of the corrected bcid is wrong (overrunnig bcid)
  - Which cannot be the case because the spill is too short.

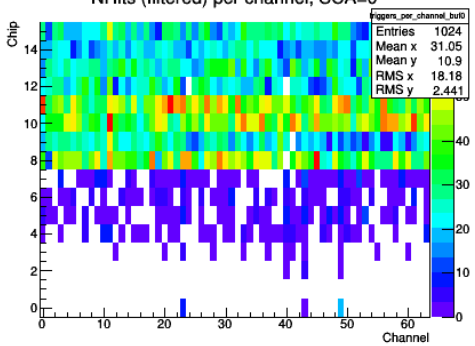
- I have checked the data on the fly, checking also the root file, looking at the spill generator saying that the length was 500 us.

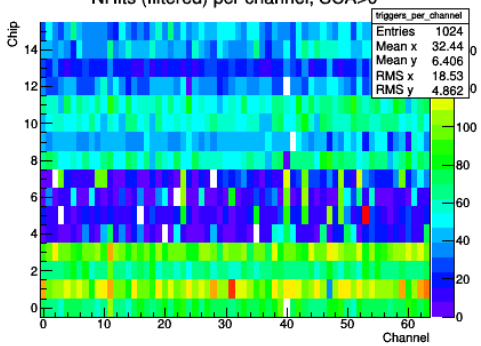
Channel Module: threshold = 250 DAC

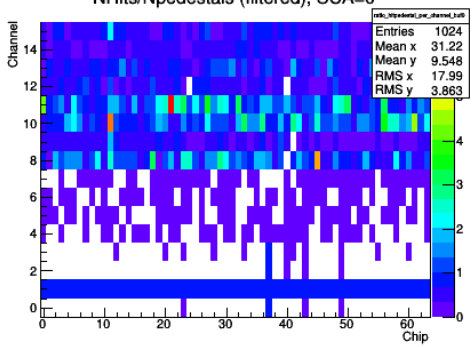


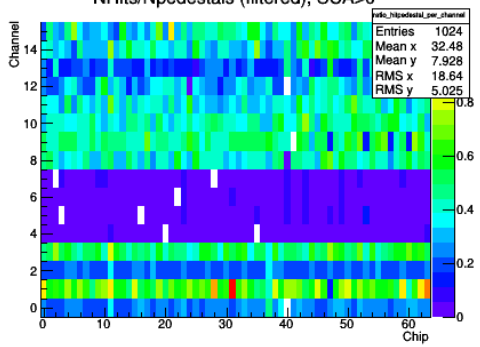


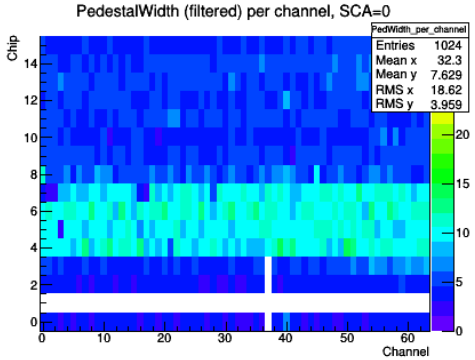


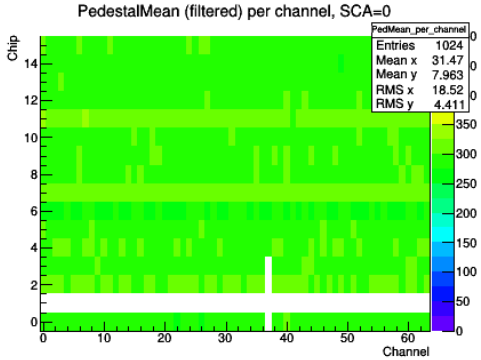


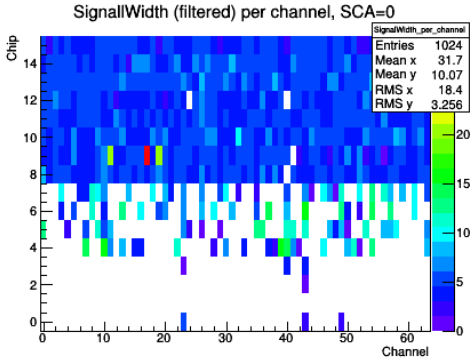


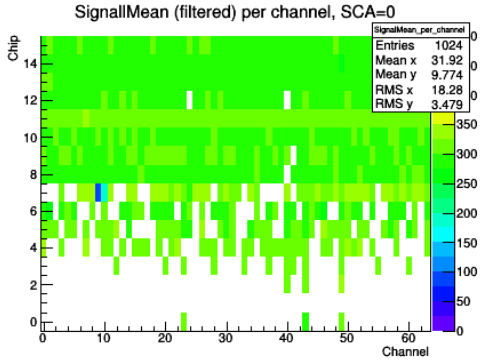












Ongoing taskes on the testbenches

- Understand the data
  - Spill issue?
- Debugging calicoes
  - Few bugs due to the new root version.
  - Data base (fixed?)
  - Etc... I am collecting a log with failures, fixes and log files for Miguel and Fred (in close contact with them)
- FEV8 testbench strange beaviour (related to the issues discussed here?)
  - Wrongly configured chips
  - Very strange BCID patterns.

- **The debugging has now really started at many fronts.**
  - Breakdown of the work?
  - I will focus on FEV8, prototype and DQM
  - Artur, sk2a and various testbenches at LLR?

To do (after understanding the data)

- Scurves:
  - Finish the analysis.
  - Repeat it with HV completely uplugged → dependency?
  - Decide a procedure.
- Full commisioning procedure development:
  - Hold value, gain value, noisy channels, pedestal (ADC) calculation.
- Others ?

Future meetings ?

- Next at LLR...
  - When? My personal inclination is to have a weekly meeting (at least at the beginning to speed up things) with as many expertises as possible in the room.
  - Suggestions?