Very forward vertexing

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[1]DESY, Hamburg

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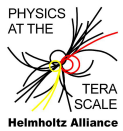
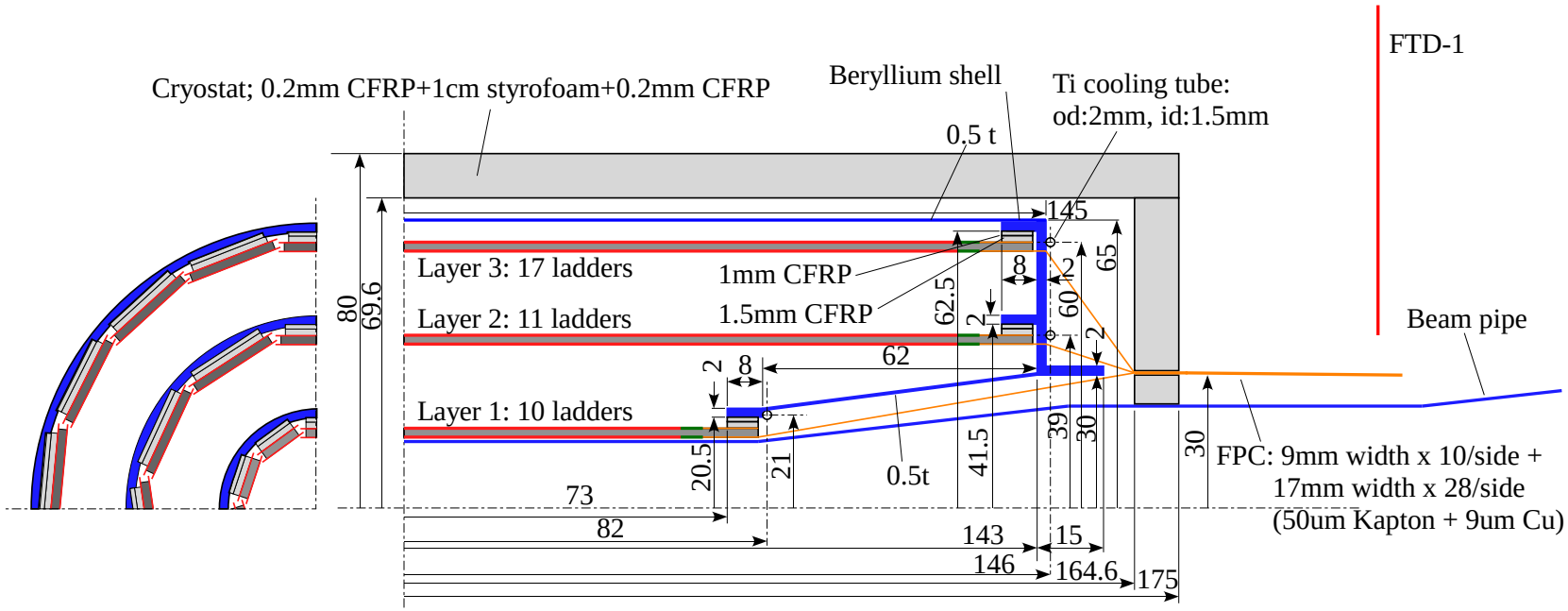


The Vertex Detector and the forward region



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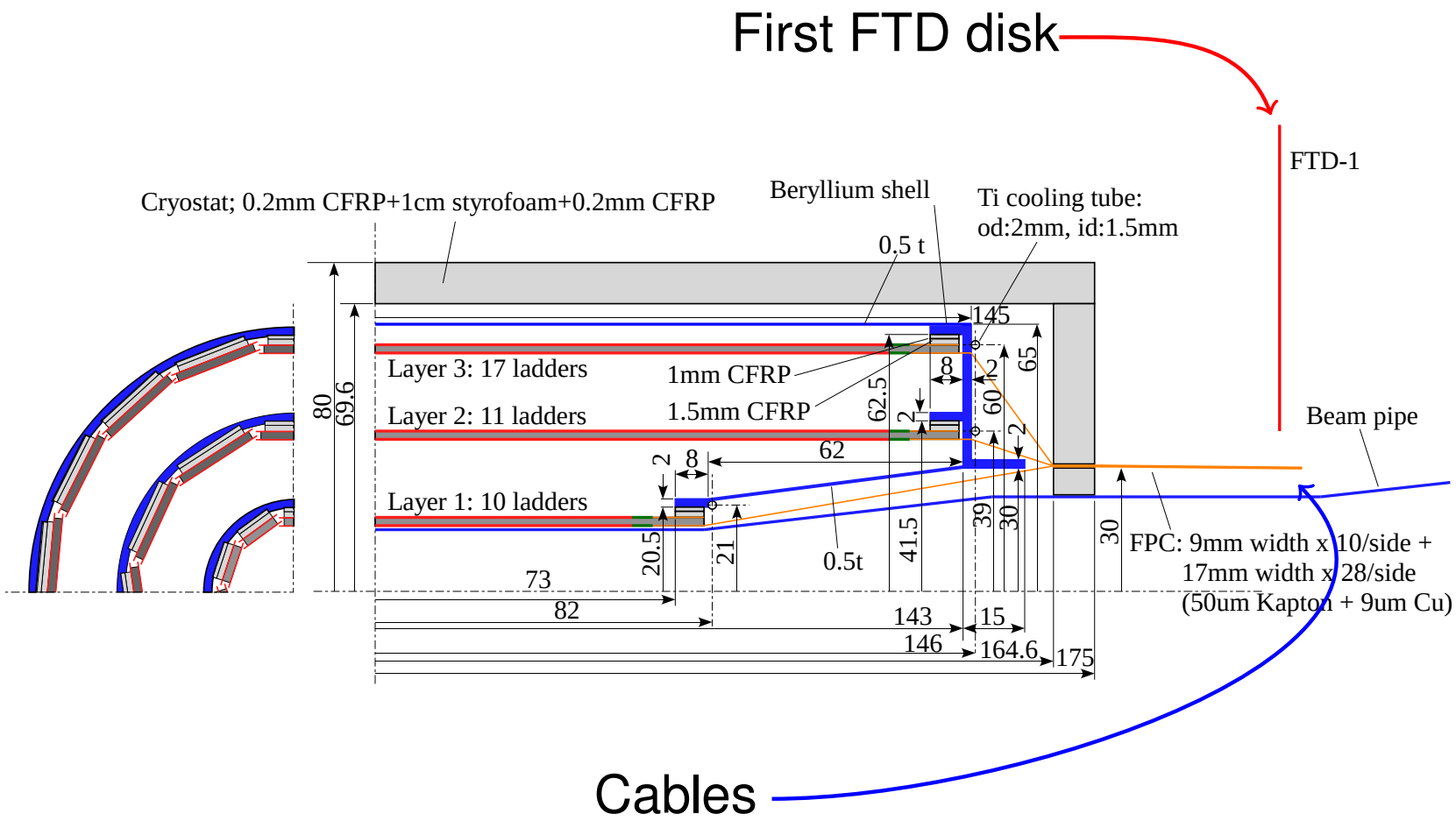

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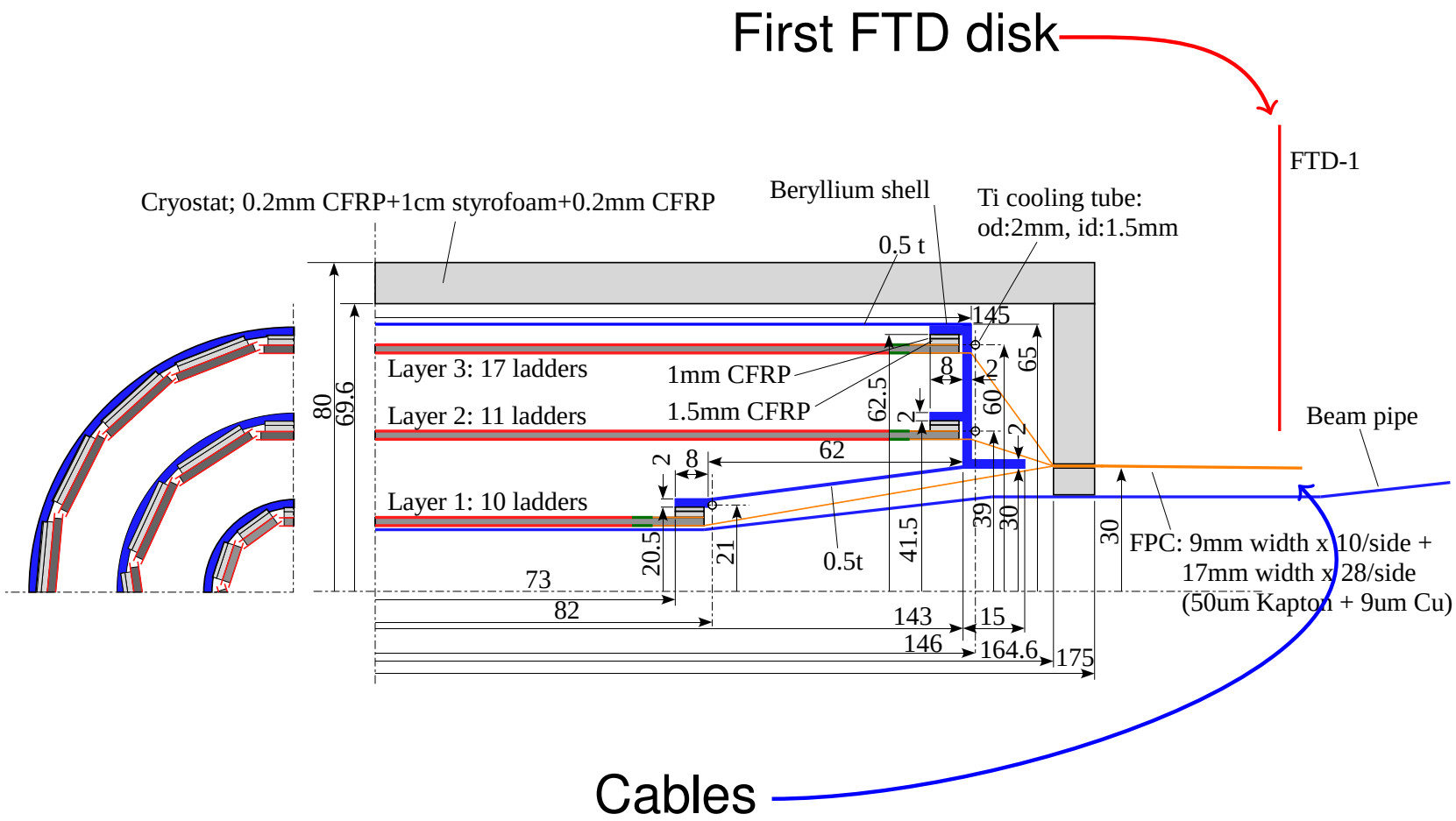

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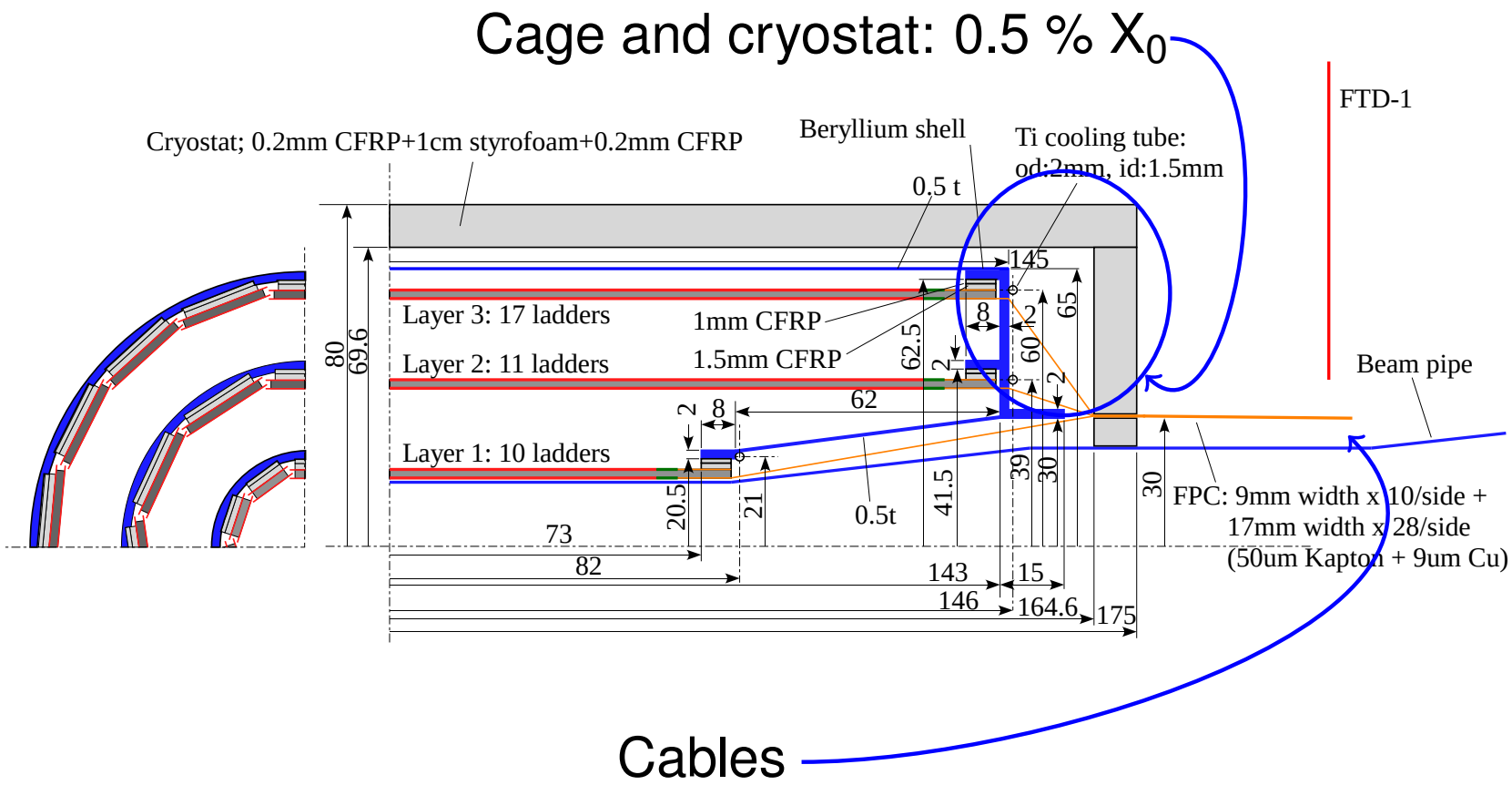

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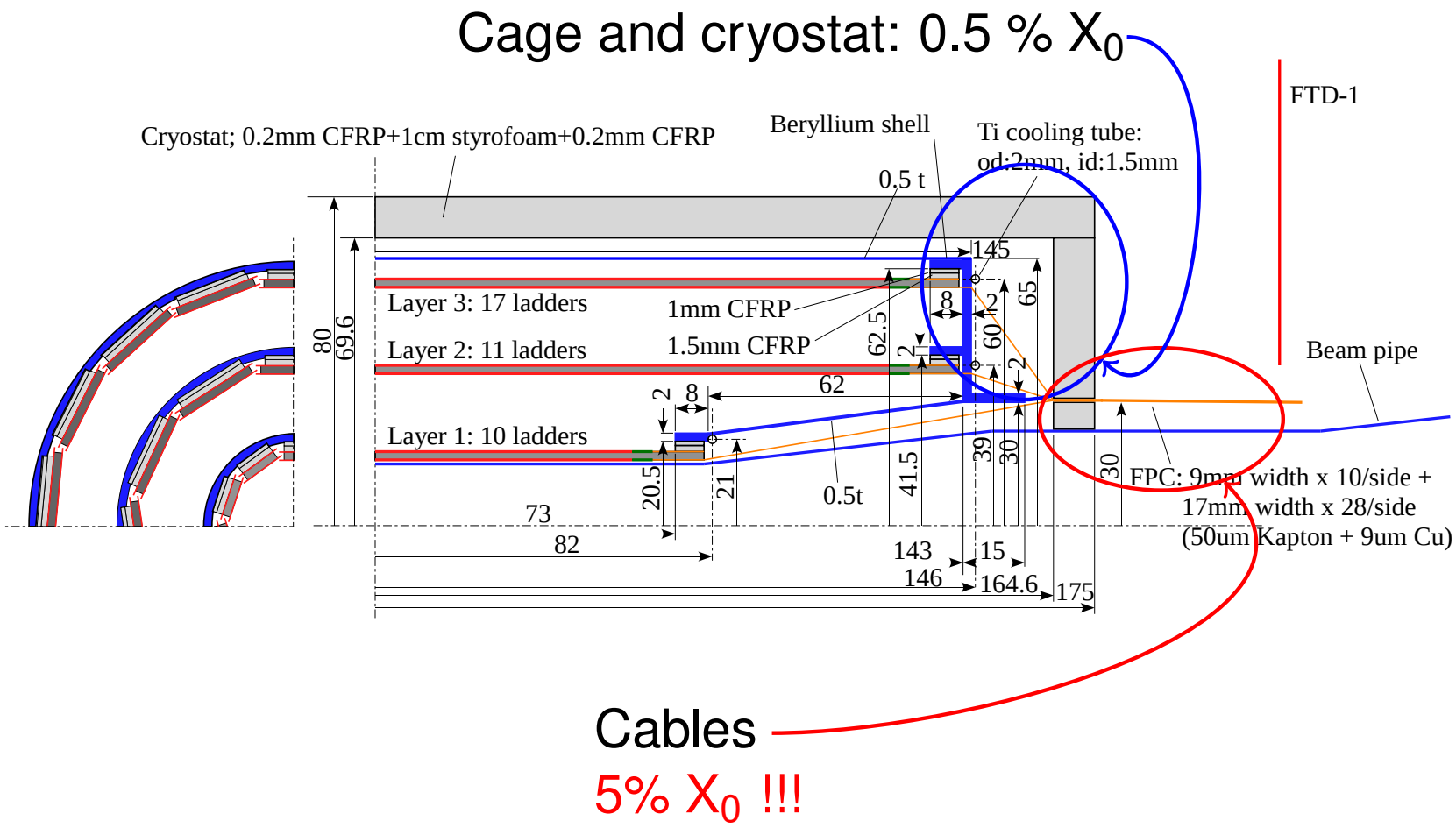
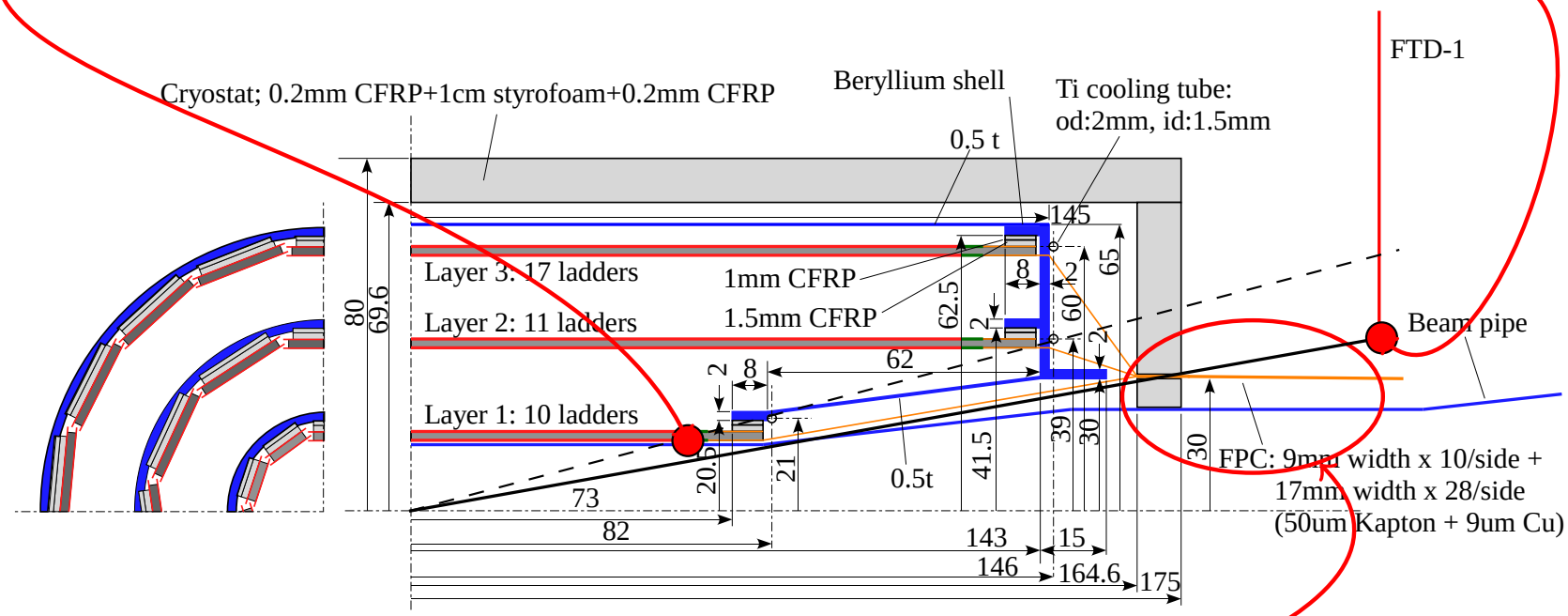


The Vertex Detector and the forward region

Hits VTX first: ∼ nothing in front

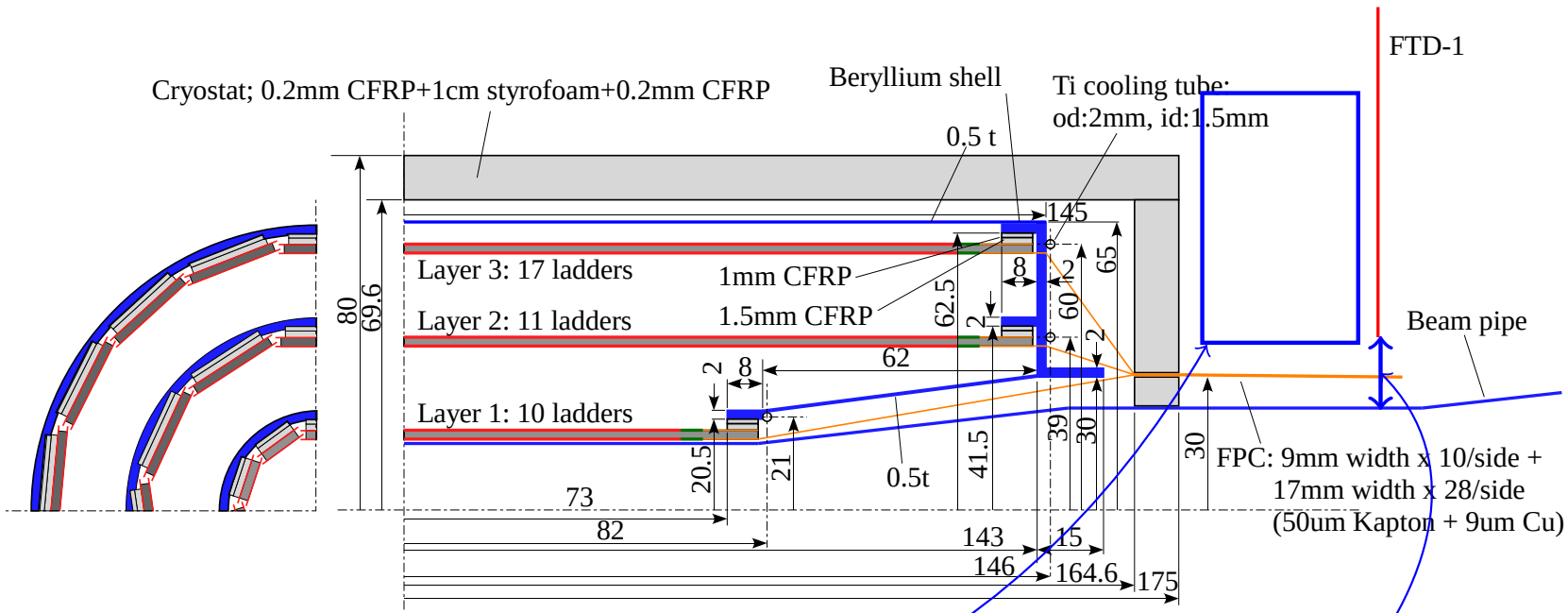
Hits FTD-1 first: lots in front



Cables

5% X_0 !!!

The Vertex Detector and the forward region



Nothing here !

Space needed for cables

Study effect of design on σ_{D0} @ low Θ with SGV

- Use SGV to calculate the covariance matrix in *scan* mode.
- Look at σ_{D0}, scanning in Θ.
- Fix p (not $p_\perp$!) to 2.5 GeV.
- Take geometry from the DBD text + cable estimates from C. Clerc.
- Then vary:
  - Cable routing from the VD (along beam-pipe or radially out)
  - FTD-1 inner radius (and position).
  - Adding "VTX-disks" inside the cryostat.
- A caveat: SGV can not handle cones, so the material-distribution is approximate : cones $\rightarrow$ combination of cylinders and planes covering the same angles.
  - In particular: The "small cone" = a disk covering the same angles, with X_0 corresponding to material seen. **NB** angle is only ~ 2 degrees $\Rightarrow$ 25 times the more X_0:s than at normal incidence !!!

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Comment on cable thickness (by a dilettante)

- Catherine's estimate: Withstands the peak current in a power-pulsed, 500 W(peak) design (with at most 10 % drop of the tension in the cables).
- Remember: This is *low voltage* $\Rightarrow$ several 100 A!
- $\Rightarrow$ need 80 mm^2 Cu $\Rightarrow$ 5 % X_0
- However, with the non power-pulsed FPCCD design: Continuous power is $\sim$ 40 W $\Rightarrow$ lower current $\Rightarrow$ lower^2 power dissipation in cables $\Rightarrow$ only 5 mm^2 Cu needed in innermost part $\Rightarrow$ 0.3 % X_0.
- In the same cables, CMOS/DEPFET would dissipate 100 times more power, but only $\sim$ 1 % of the time (Minute rise of T during the pulse)
- $\Rightarrow$ Will assume that also CMOS/DEPFET could live with such thin cables. Will show plots for both thick and thin cables.

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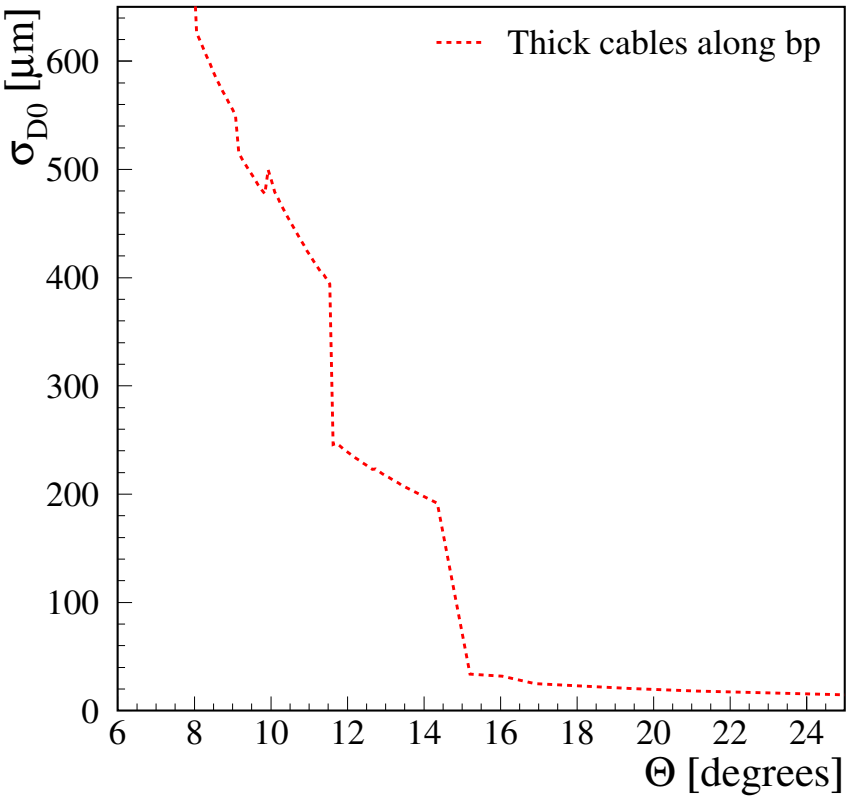
The effect on σ_{D0}

- σ_{D0} with thick cables *along the beam-pipe*
- ... and routed outside FTD-1 & FTD-2
- Same, with thin cables
- Add pixel-disks *inside the cryostat*, with point-res 2.8 μm
- Same...
- ... also with thick cables routed up.



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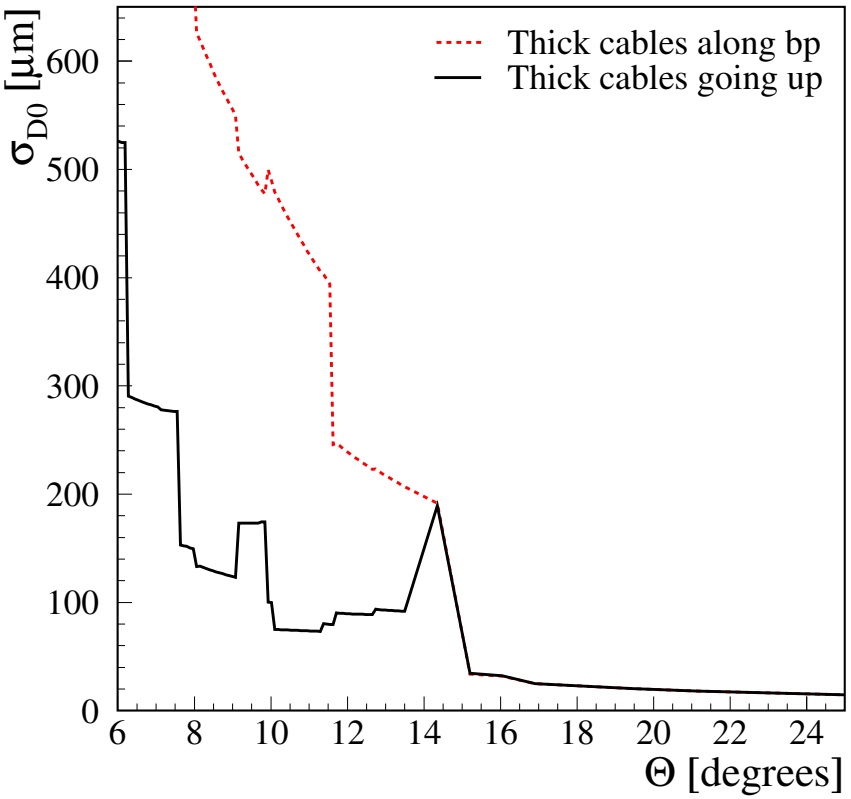

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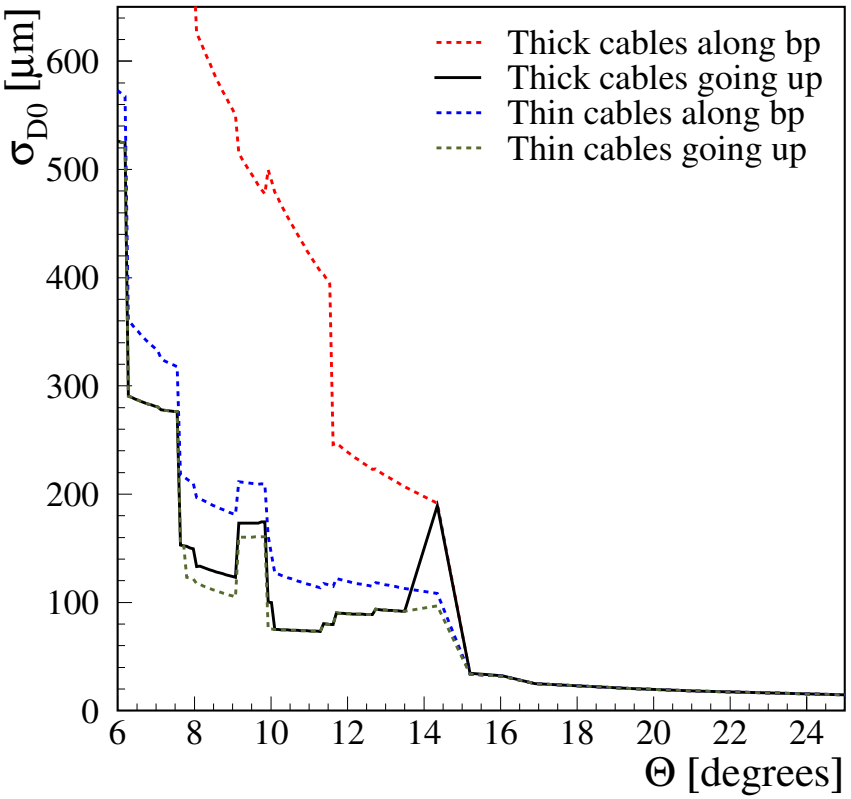

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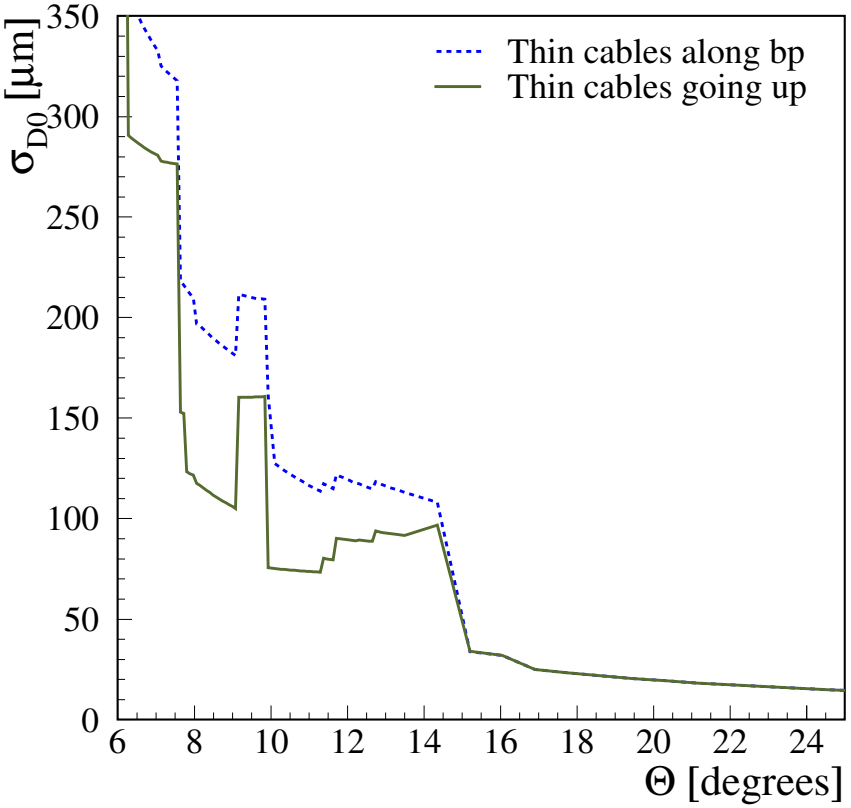

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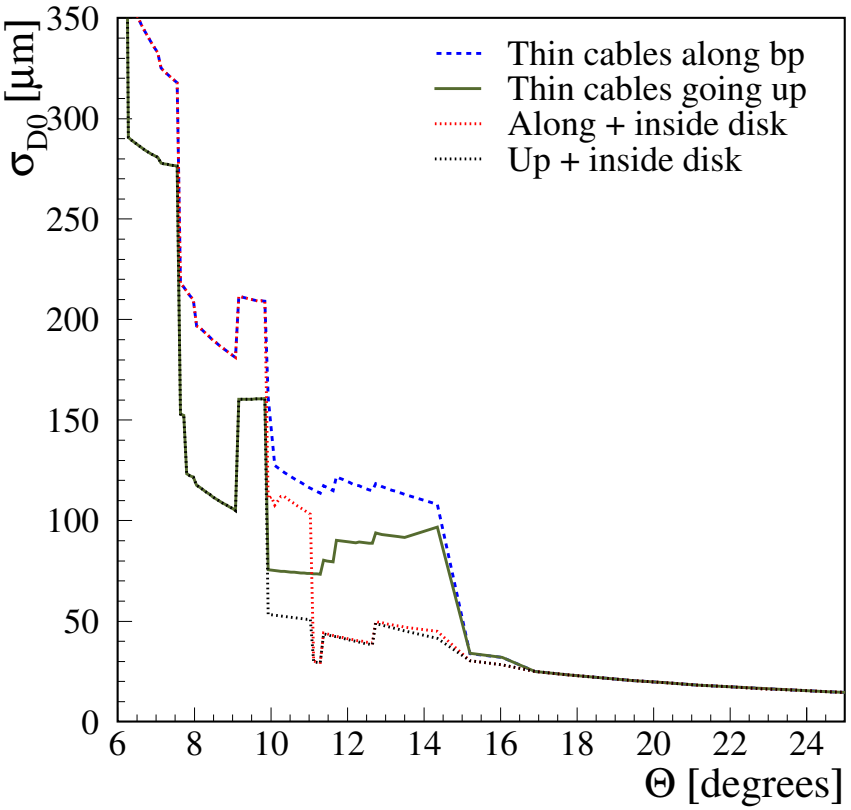

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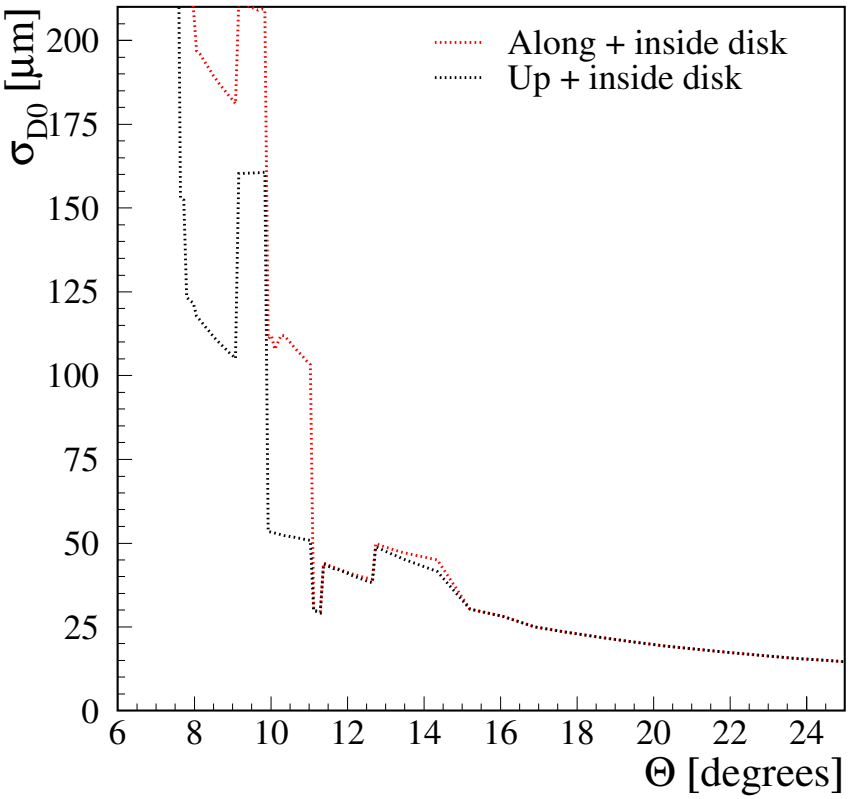

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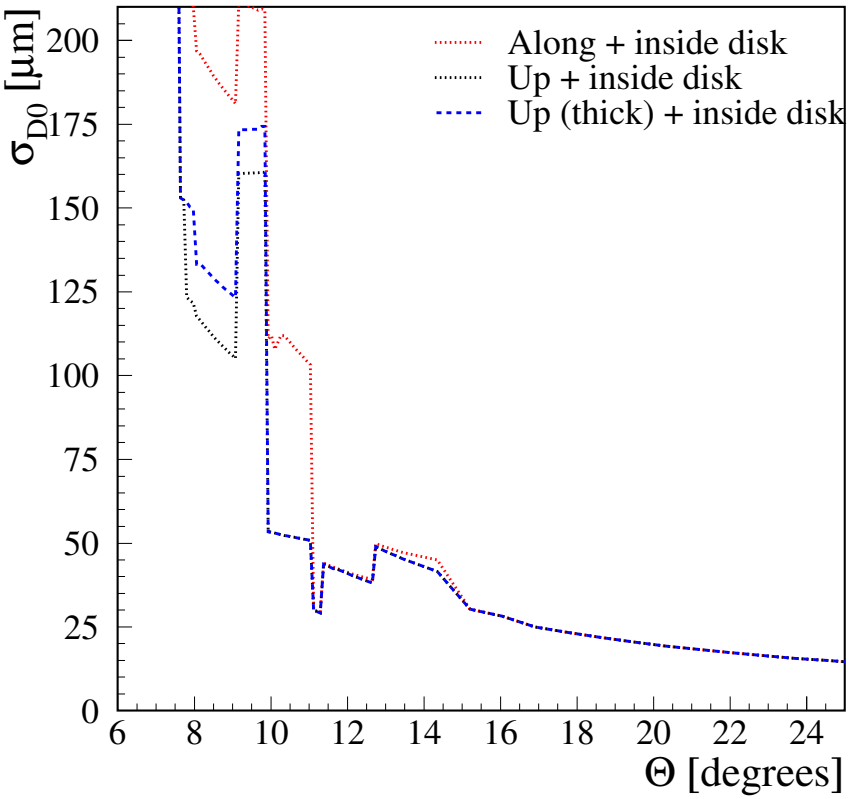

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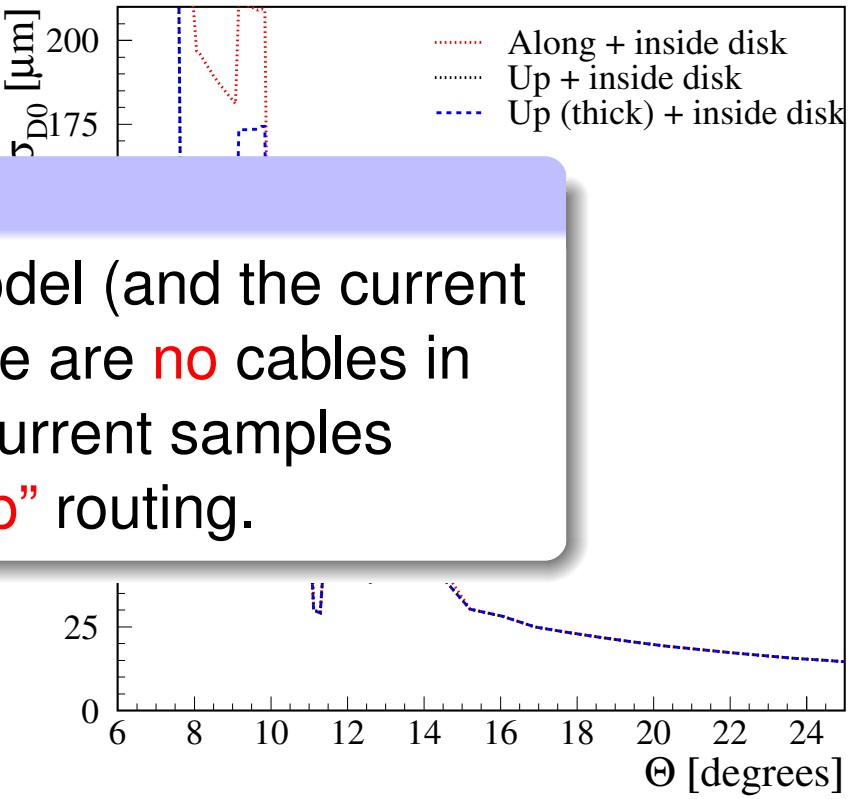

Note:

In the DBD Mokka model (and the current DD4HEP model), there are no cables in the critical region ⇒ current samples corresponds to the "up" routing.

Further comments

- Also checked "FTD1b" (an additional FTD-type pixel disk between FTD1 and FTD2):
  - Has $\sim$ no effect on σ_{D0}
  - (Might be useful for pat. rec., but SGV can't say anything about that...)
- Moving the first FTD disk closer helps a bit, but alas most of the benefit is shadowed by the small cone.
- The current idea on assembly of the inner region does not allow for the routing of the VTX cables outside the first FTD disks:
  1. Mount lower half of entire FTD and SIT in it's support.
  2. Separately, mount and cable the VTX on beam-pipe.
  3. Place beam-pipe+VTX assembly in assembled lower tube.
  4. Mount upper part of FTD and SIT.
  5. Close.

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Conclusions

- It would be possible to extend sub-100 μm *D*0 resolution to $\sim$ 9 degrees (from 16 degrees).
- For this, as little material as possible should be allowed in front of the first sensitive layer.
- For this, the last $\sim$ 10 cm of cables should be:
  - As thin as possible. (Is it possible to have so thin cables also for a CMOS/DEPFET design?)
  - And(preferably)/or routed out-of-the-way of the first FTD disk.
  - The latter means re-thinking the mounting procedure of the inner region.
- Sub-50 μm *D*0 resolution down to 11 degrees would be possible with VTX-style disks inside the VTX cage/cryostat. In this case, cable-thickness is less importrant.
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