Studying the “BCID issue” with the technical prototype

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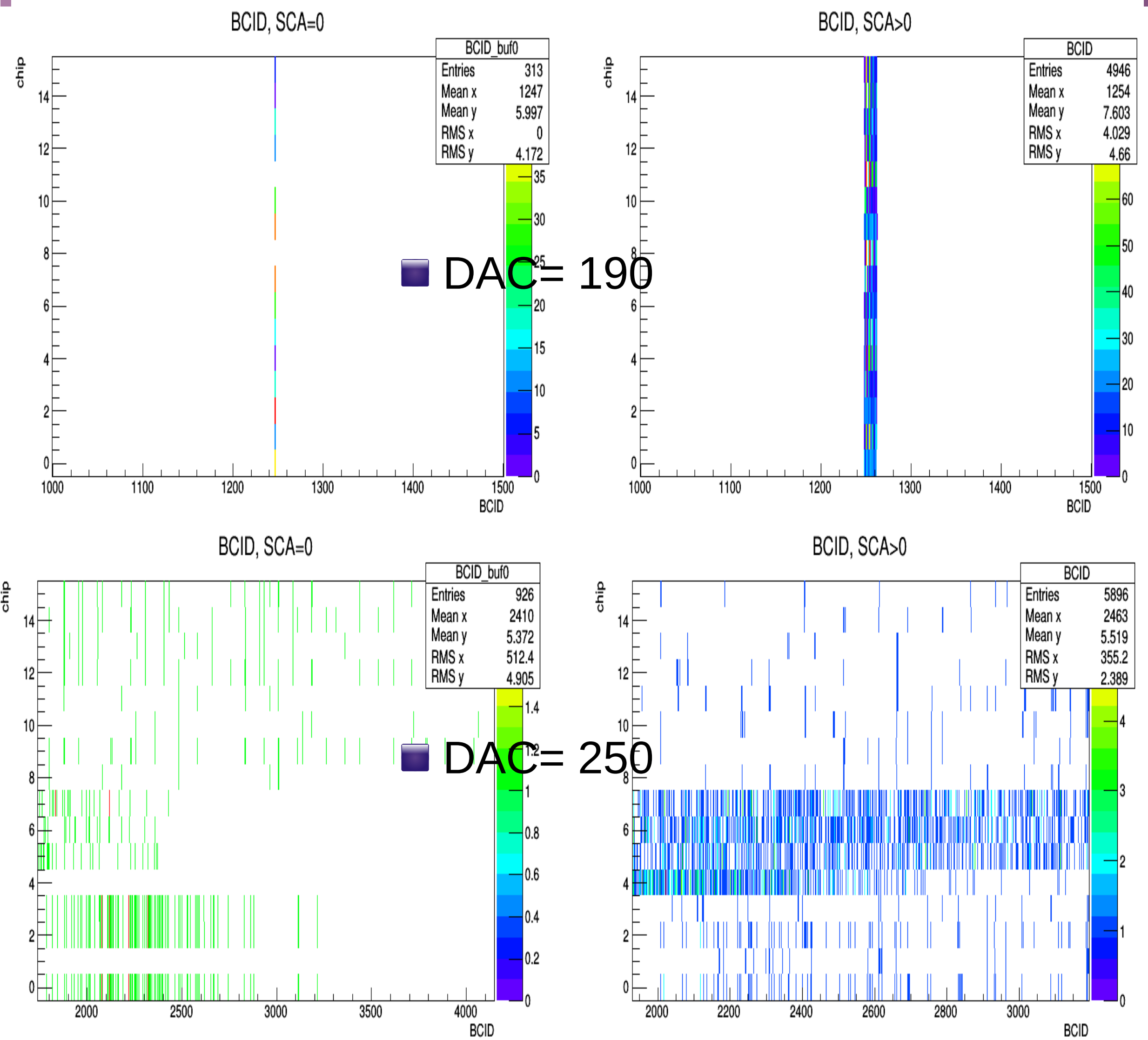
Orsay 15th Mars 2017

Prototype, same chip, same spill length (0.5 ms = 2500 BCID), 64 channels

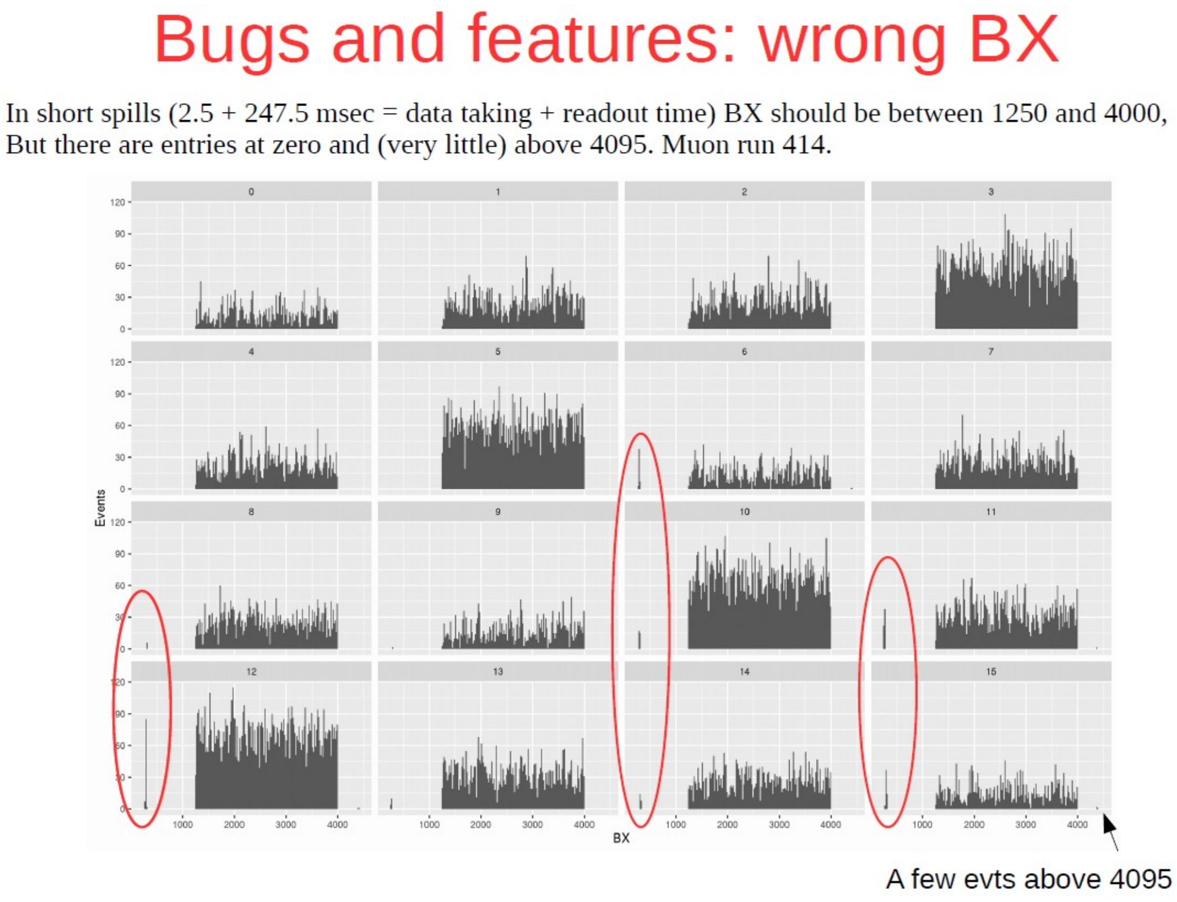


- DAC= 190
- DAC= 250

- **Summary from last week: Problem I.**
- The 190 DAC threshold run:
  - no values before val_evt, BCID =1245, (val_evt works ok)
  - No values after BCID ~1260 → all SCAs are full very quickly
- The 250 DAC threshold run:
  - Values after BCID 2500 → ??
- Assuming that BCID range is not fixed to 0-2500, then
  - Values before val_evt → can be because overrunning counter
  - very random distributions, meaning that if the first value is over 4096, the overrunning counter is still 0. It is reset every acq.

History:

- Already observed issue (Vladik) https://agenda.linearcollider.org/ev nt/6973/contributions/34374/attach ts/28329/42800/pedestals.pdf
- Same feature.



Bugs and features: wrong BX

In short spills (2.5 + 247.5 msec = data taking + readout time) BX should be between 1250 and 4000, But there are entries at zero and (very little) above 4095. Muon run 414.

A few evts above 4095

Cross checks

- Use Vladik converter → https://github.com/balagura/online_monitor
  - Same BCID range is observed.
- Check fev8_cob with skiroc 2 data from November (different DIF firmware, calicoes and converter)
  - The effect is also there for large threshold values (but we were using very long spills, so the effect is compatible with overrunning)

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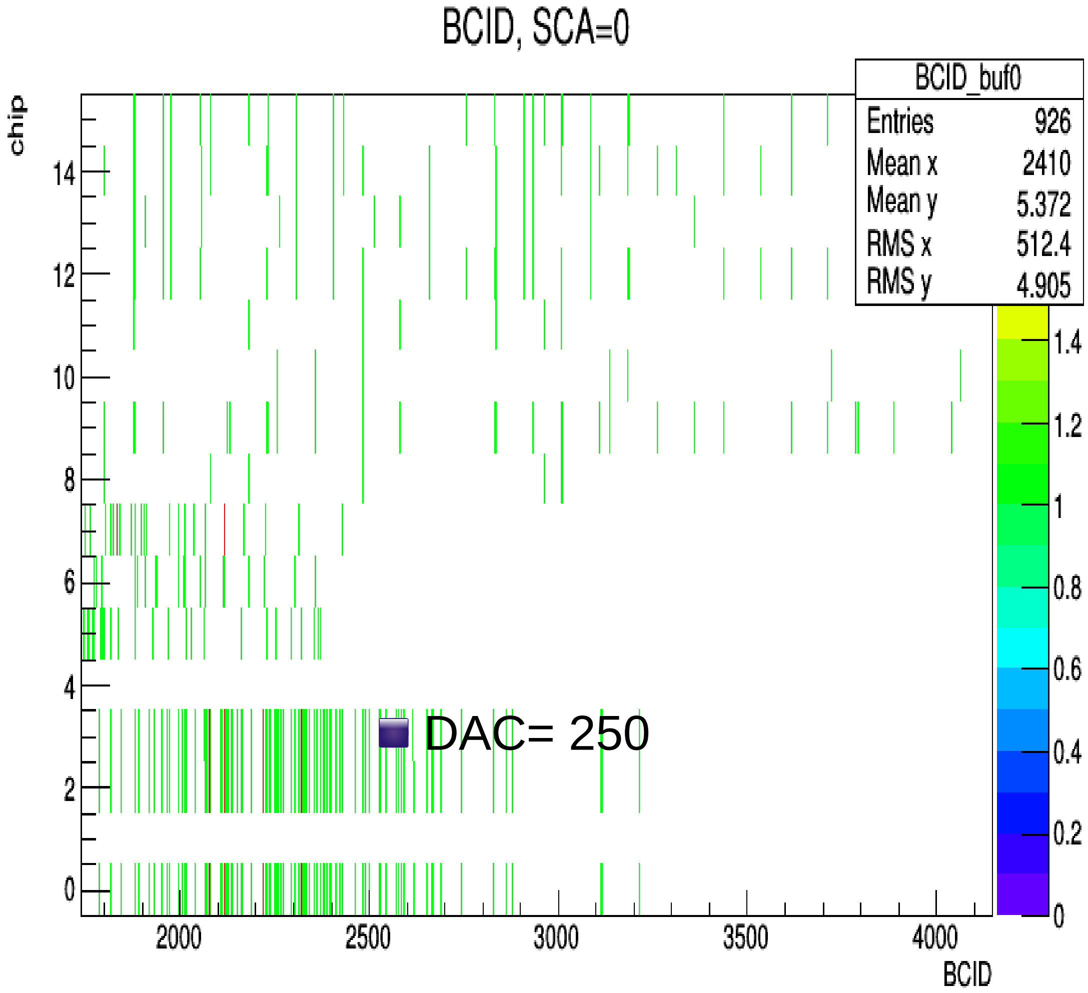

- DAC= 250

- **Summary from last week: Problem II.**
- Pattern → same BCID for all chips.
- Repeated with HV == off

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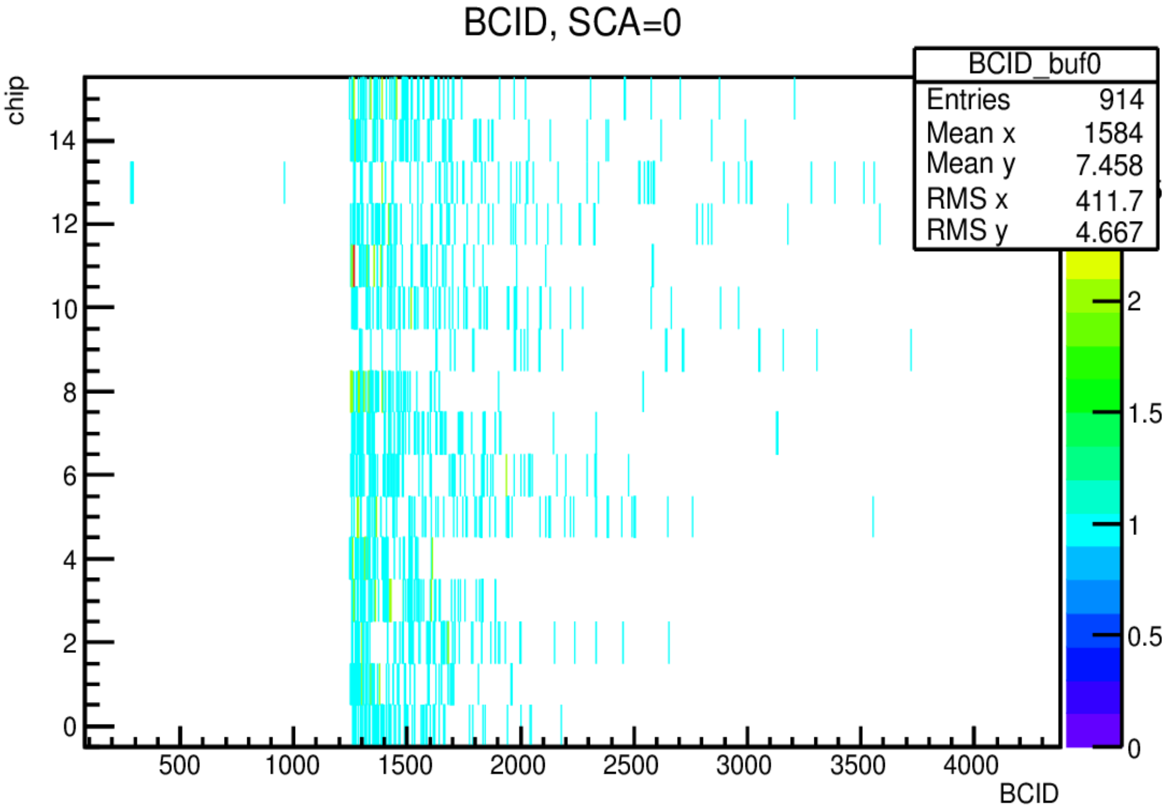

- **Summary from last week: Problem II.**
- Pattern → same BCID for all chips.
- Repeated with HV == off and a full power cycle
  - Much less noisy chips
  - **No pattern**
- **Ongoing: repeat full scurve analysis with and without HV.**

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