KLauS5, towards the 36-channel SiPM readout SoC

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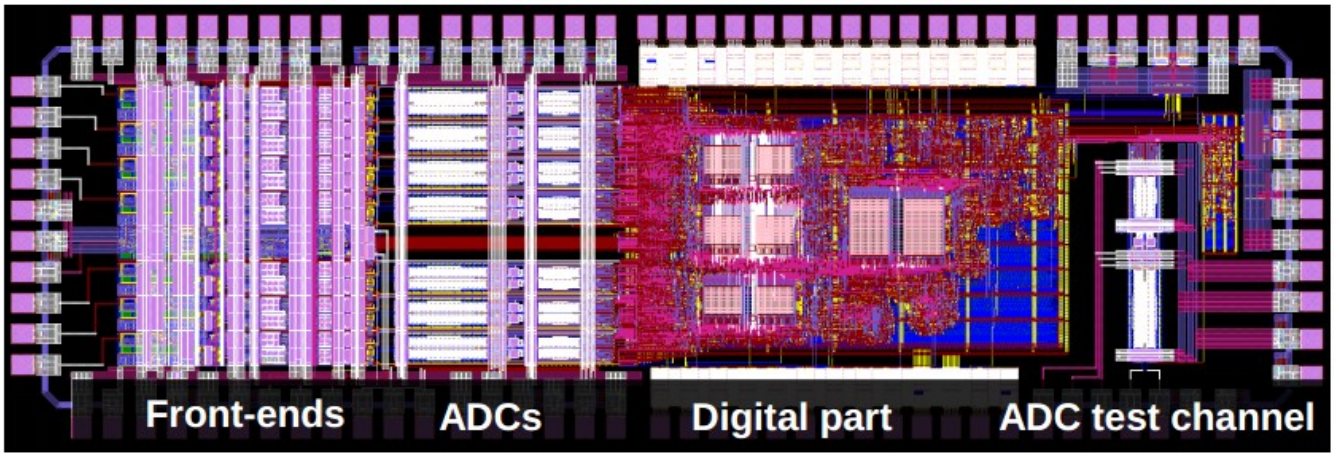
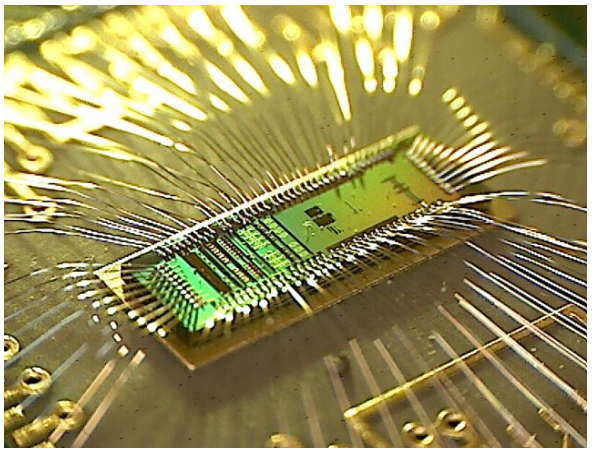
Contents

- Reminder and new results of KLauS4
- Development of KLauS5

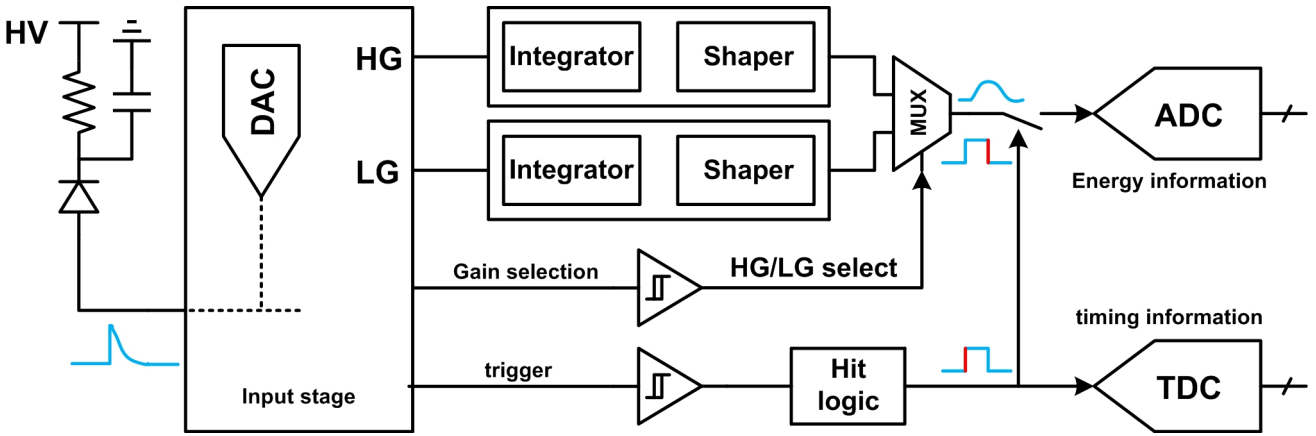
KLauS4: 7-channel prototype

Submitted in May 2016; Test-beam in Feb. 2017





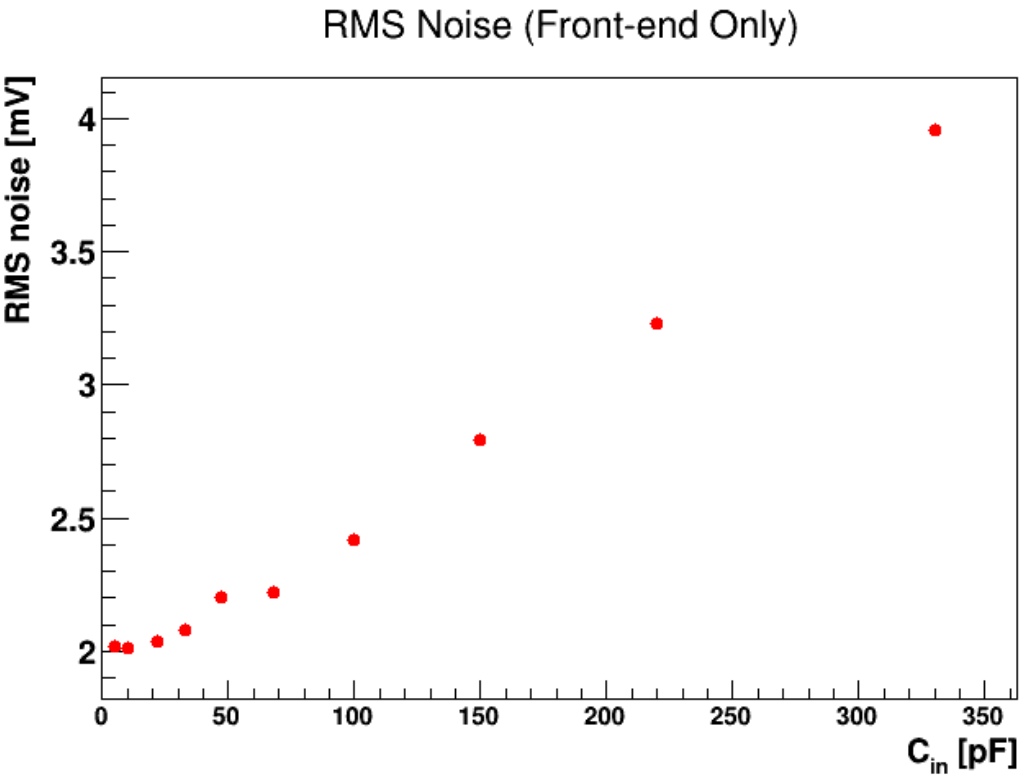
Analog blocks per channel



- Mixed-mode prototype
- UMC 180nm, 1.5 x 4.5mm^2
- TDC with 25ns binning, 12-bit
- LVDS or I^{2}C for data transfer
- SPI for slow control

Full chain: noise performance

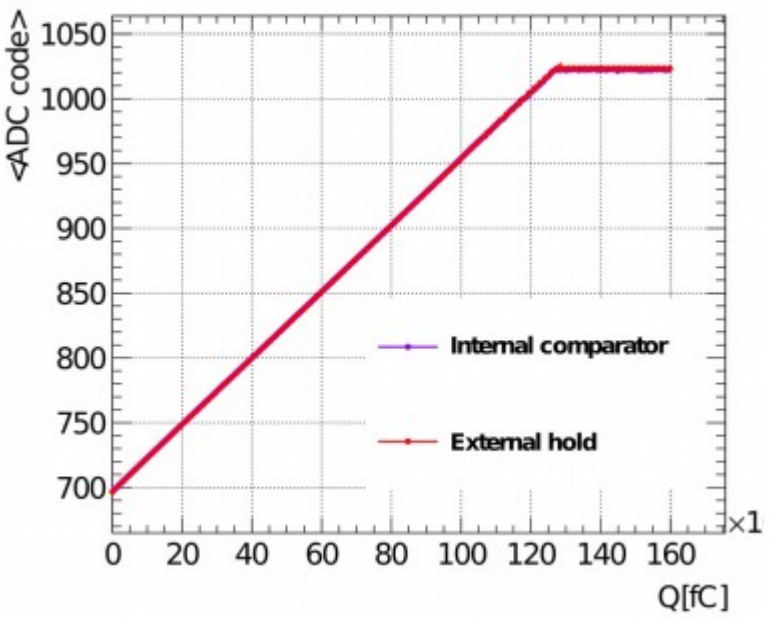
The RMS value of pedestal voltage

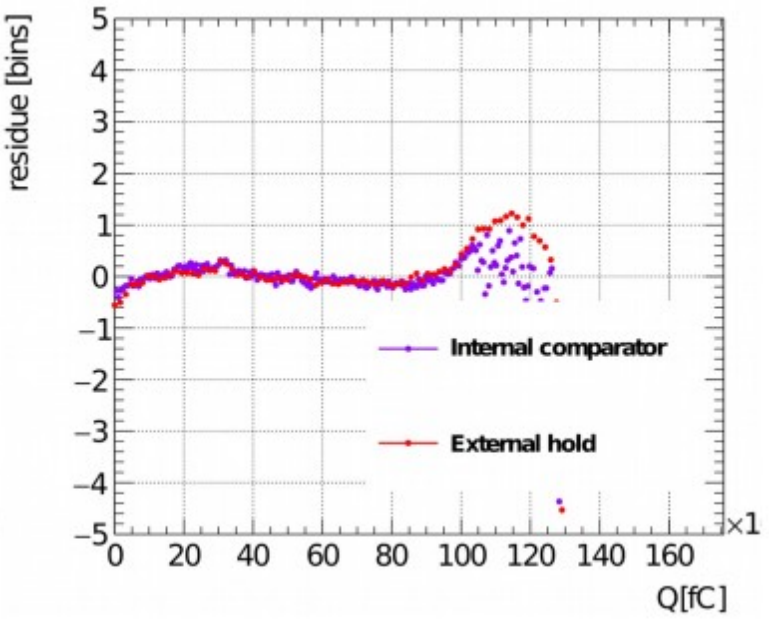


- Front-end only
  - Noise < 2.5mV (for Cin<100pF)
    - → **ENC < 6fC(Cin<100pF)**

- Full chain measurement, fixed charge input, code spans for 3~5 ADC codes
  - stddev around 0.6~0.8 bins(LSB=3.2mV)
    - → **The Front-end noise is dominant**

Full chain: linearity





Charge injection through 33pF capacitor

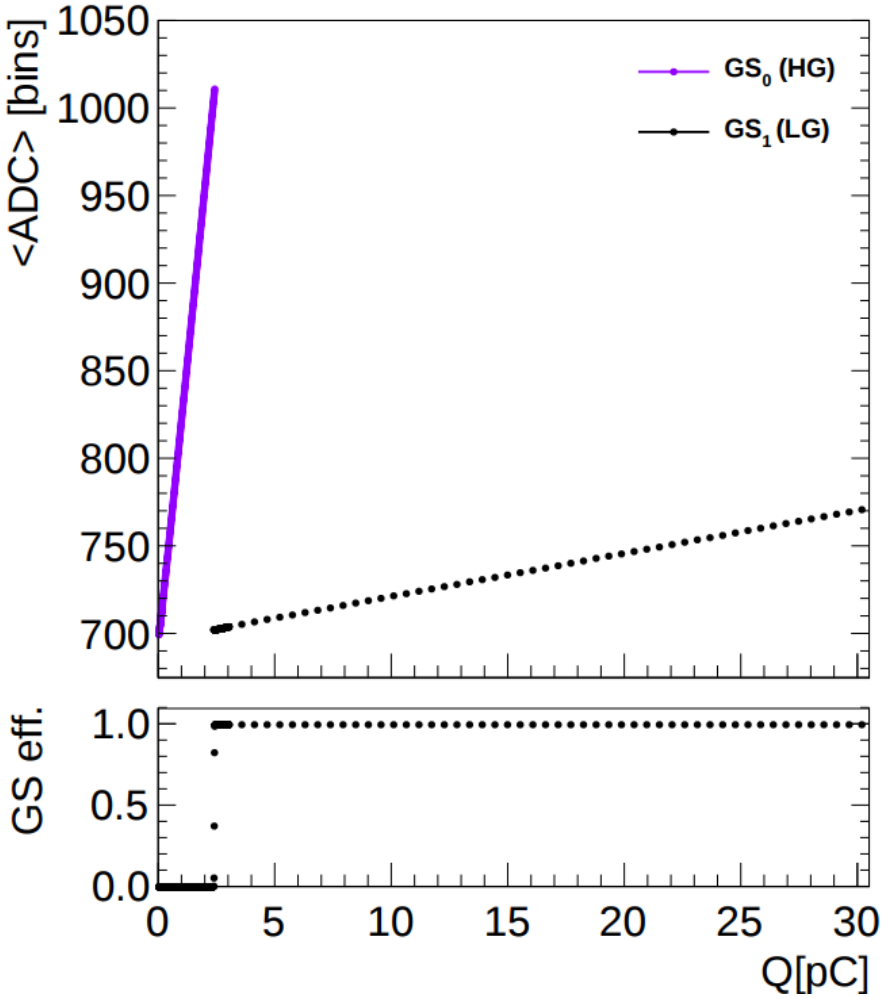
- Full chain measurement with 10-bit ADC
- Measurements with two type of hold
  - Internal generated hold (time walk)
  - External generated hold
- Dynamic range
  - HG scale → 2.3pC (2.7pC only FE)
  - LG scale → 130pC (136pC only FE)

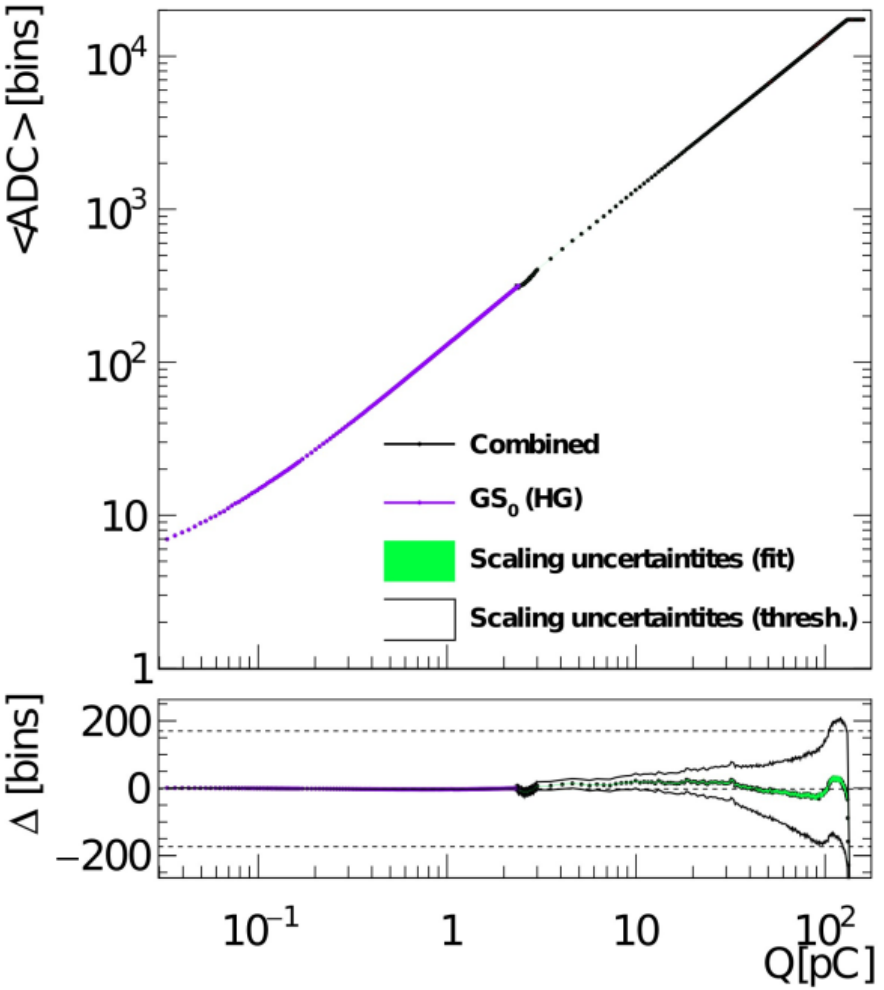
  Due to limited ADC dynamic range(1.6V)
- 1% FSR(Full scale range)

  (Residue: difference between the fitted data and the Measured result)

Auto-gain selection

Full chain linearity measurement using 10-bit ADC in auto-gain mode





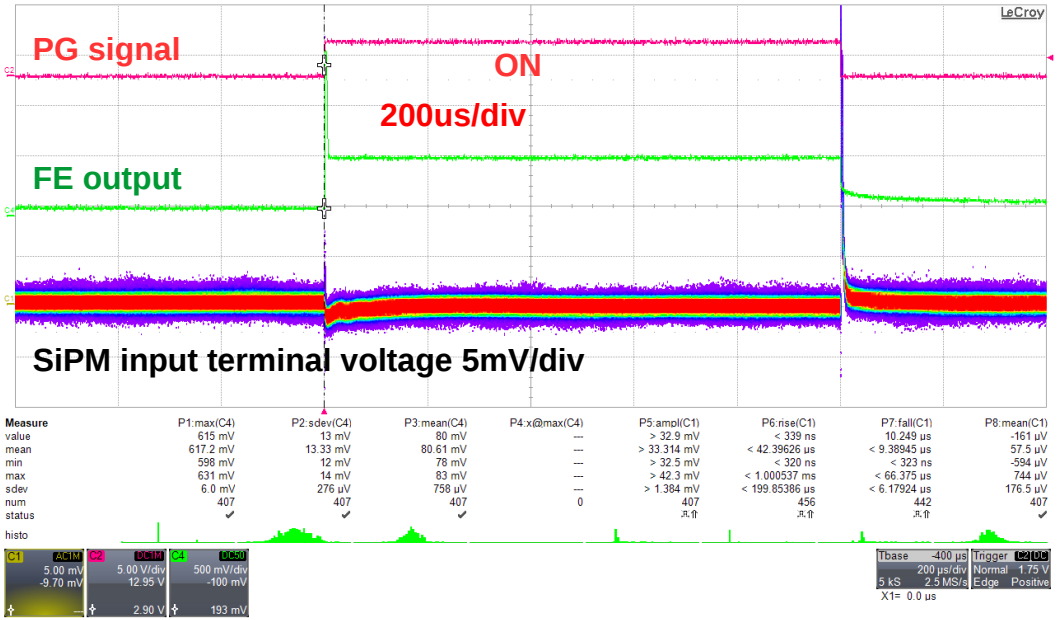
- The auto-gain selection works well (also verified in test-beam)
- Linearity is satisfactory: deviations < 1%(FSR), for charge smaller than 130pC

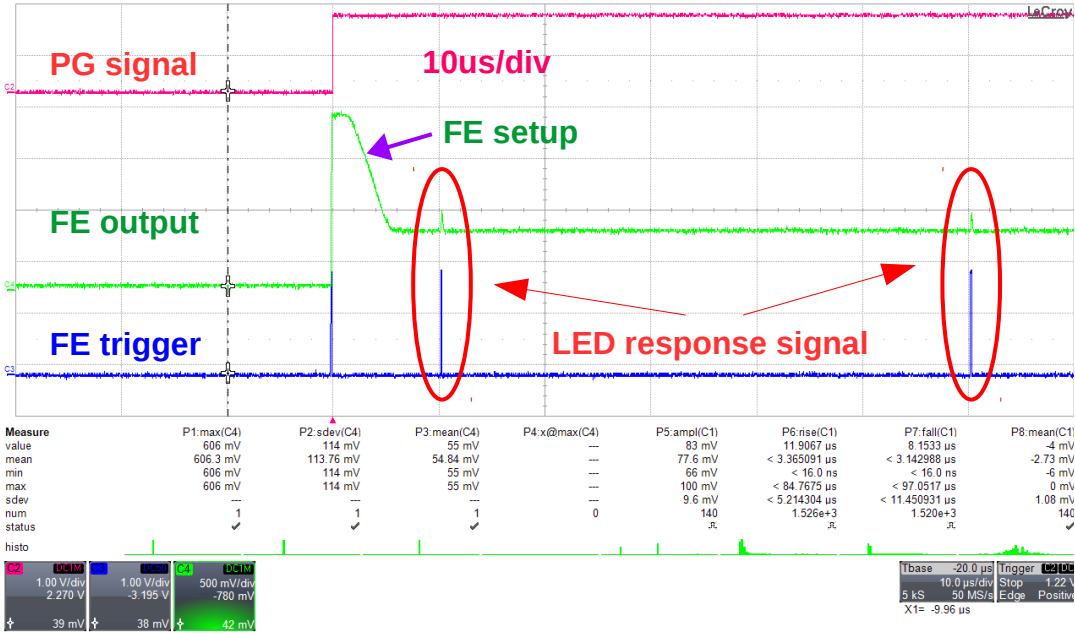
Power pulsing features

Analog signal behavior during power pulsing

- Power gating scheme:
  - Turn off ASIC when no events
  - 2.5mW/Ch→ 25uW/Ch(>0.5%)

- Key points:
  - **SiPM bias voltage**
    - Difference **< 20mV** for all settings
    - stable operation of SiPM
  - **Front-end fast setup**
    - Recover **< 10us**
    - further reduce the duty cycle of 1%



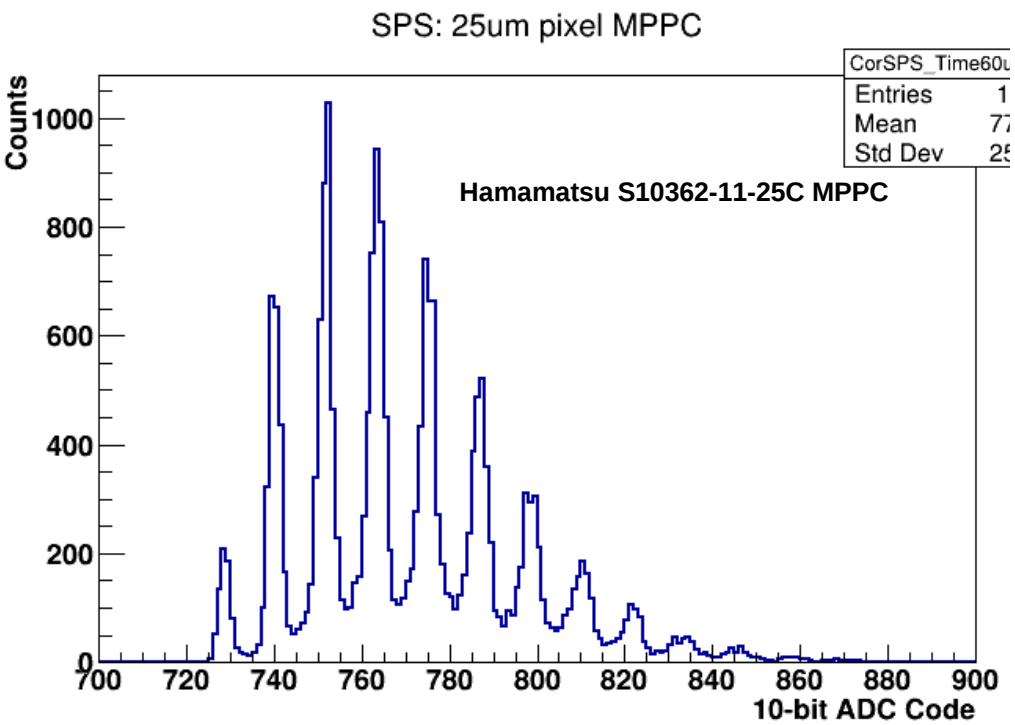


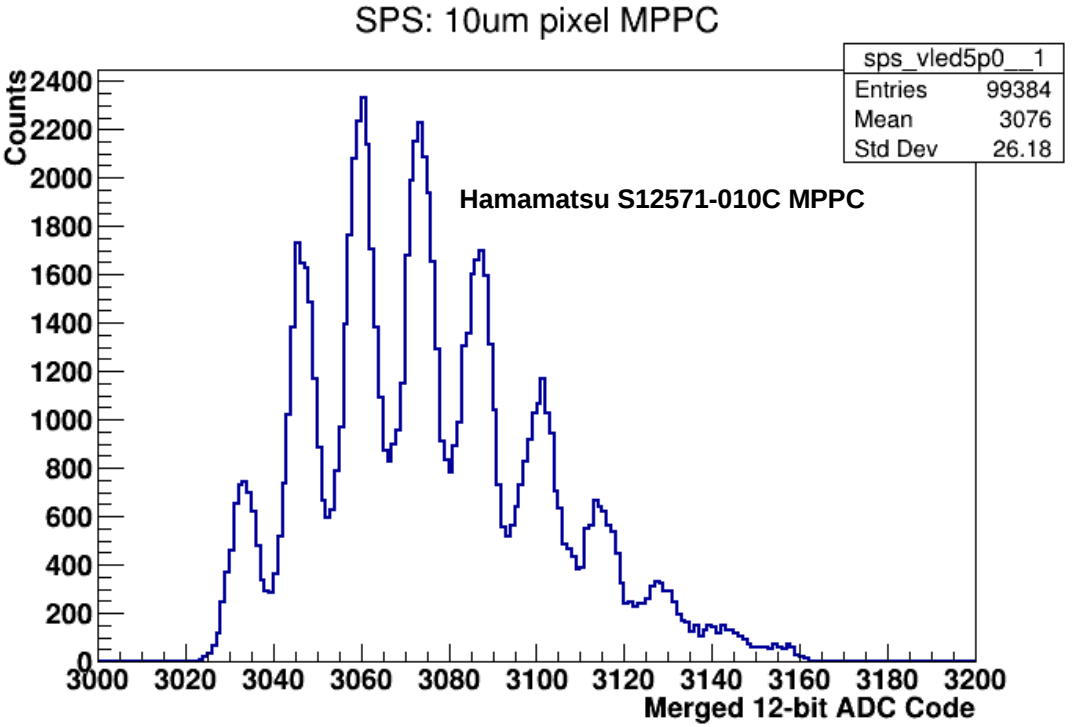
Measurements of the SPS

- Single photon spectra (SPS): SiPM with different pixel sizes
- Sensor illuminated by a pulsed LED

Spectra recorded in self-triggered mode
Large gain: 10b ADC sufficient
ADC DNL correction performed

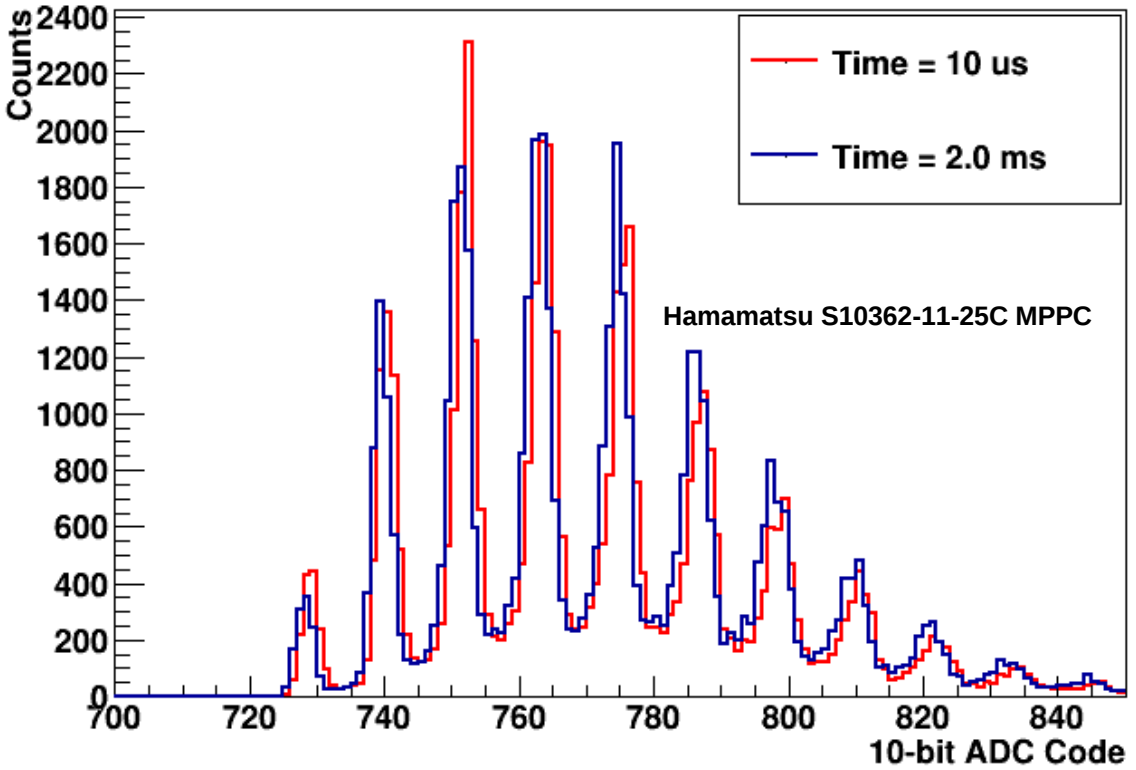
External triggered mode
Small gain: 12b ADC used
SiPM operated at nominal bias voltage
Gain = 1.35e5 (data-sheet)





Power pulsing features

- Single photo spectra with power pulsing
  - Different time delay between turn on ASIC and LED illumination
  - Almost no observable photo-peak displacement

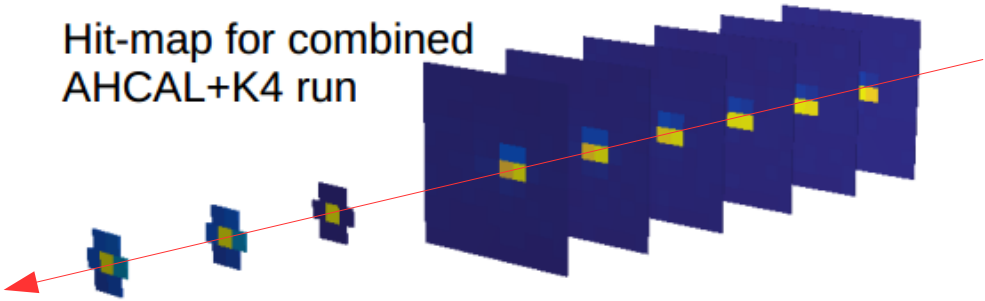


KLauS4 can work well with 10us delay after turn on during power-pulsing

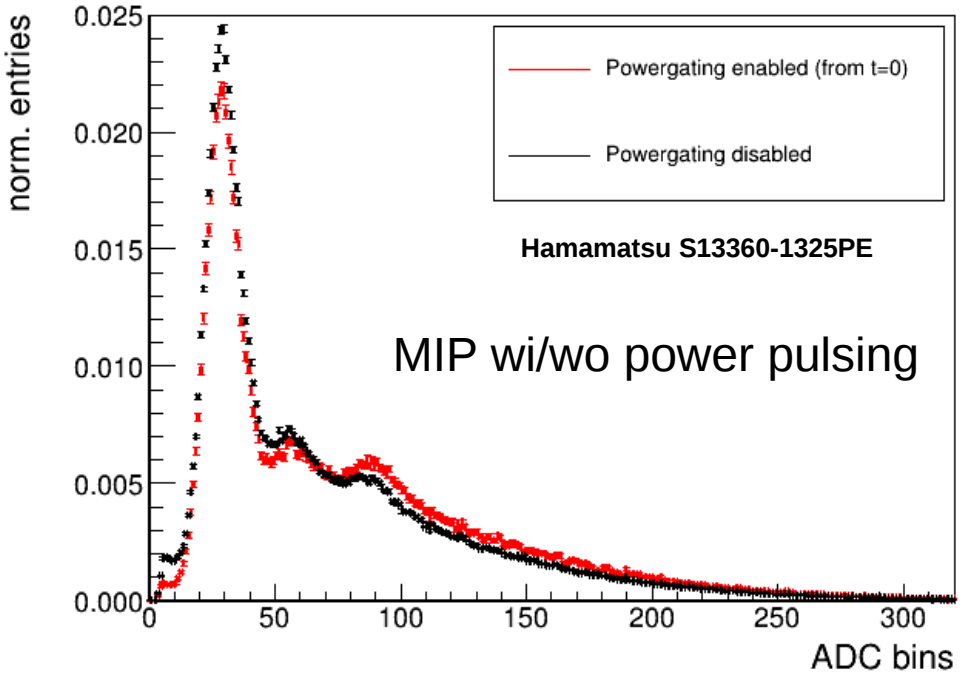
The duty cycle can reduced to slightly above 0.5%

Reminder of KLauS4 in test-beam

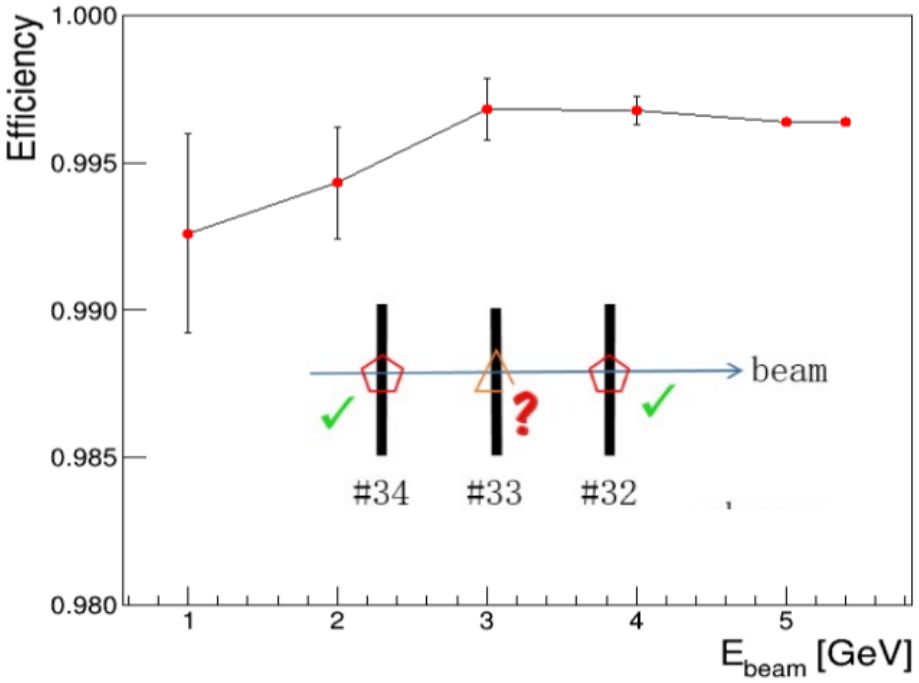
- Carried on Feb. 2017
  - Parasite to AHCAL DAQ tests
- 3-boards used
  - ✔ 1 board: single tile + SiPM in center
  - ✔ 2 boards: fully equipped (7 channels)



KLauS4 AHCAL HBU



The position of the MIP peaks is preserved



Efficiency > 99%

Summary of KLauS4

- **Current KLauS4 prototype**
  - ✔ Front-end and ADC working well
  - ✔ Successful measured of SPS for SiPM down to 10um pixel size
  - ✔ Validated the chip performance in the testbeam at DESY

	Performance		
SiPM bias voltage tuning range [V]	2.0		
SiPM bias voltage difference during power pulsing [mV]	< 20		
10-bit ADC DNL [LSB]	-0.52 / +0.14		
12-bit ADC DNL [LSB]	-0.44 / +0.36		
Crosstalk [dB]	< -80		
TDC	12-bit, 25ns binning		
	HG	MG	LG
Gain [mV/pC]	405	67	7.4
ENC [fC]	5.2	19.4	98.0
Dynamic Range [pC]	2.7	16.0	136

Contents

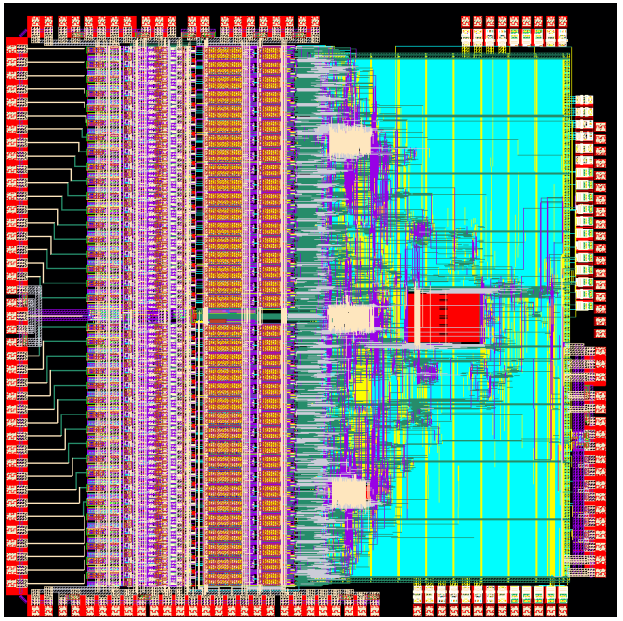
- Reminder and new results of KLauS4
- Development of KLauS5

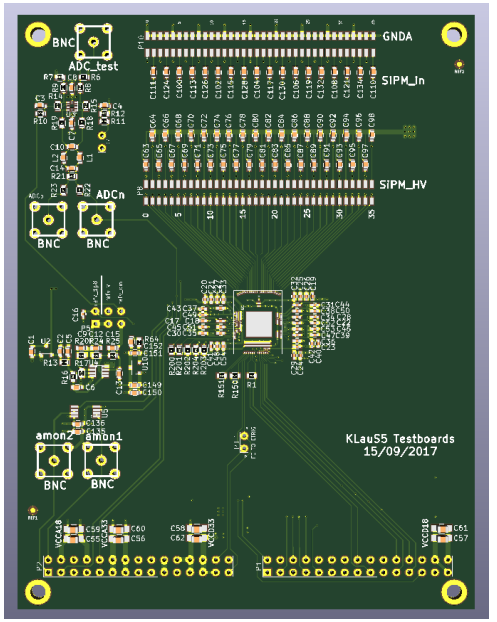
KLauS5: 36-channel prototype

Submitted in July 2017

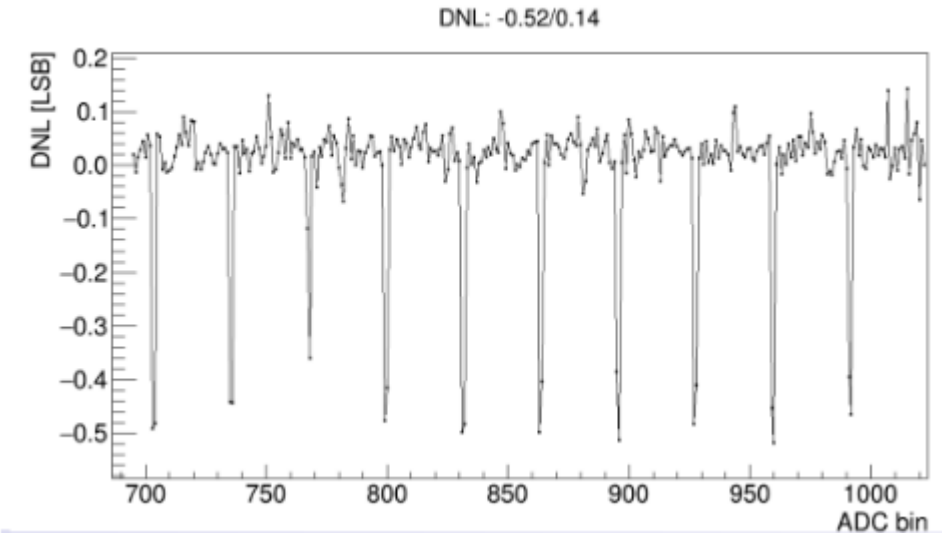
- Mixed-mode prototype (FE + ADC/TDC + Digital part)
- UMC 180nm CMOS technology, 5.0 x 5.0mm^2
- TDC with 25ns binning, *extended to 16-bit*
- Fast LVDS (160Mbit/s) or slow I^{2}C for data transfer
- SPI for slow control

Test-board prepared

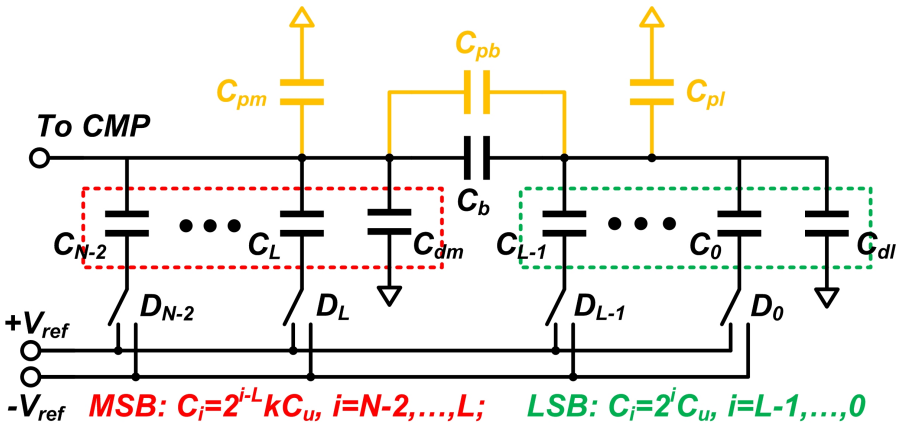




ADC



KLauS4



10-bit SAR ADC

Differential nonlinearity: spark every 32 bins

Large bridge capacitor (over-compensated)

Three layout versions in KLauS5 for trial and error

- ✔ Different compensated version implemented
- ✔ Reduce the parasitics at the LSB array, no compensation

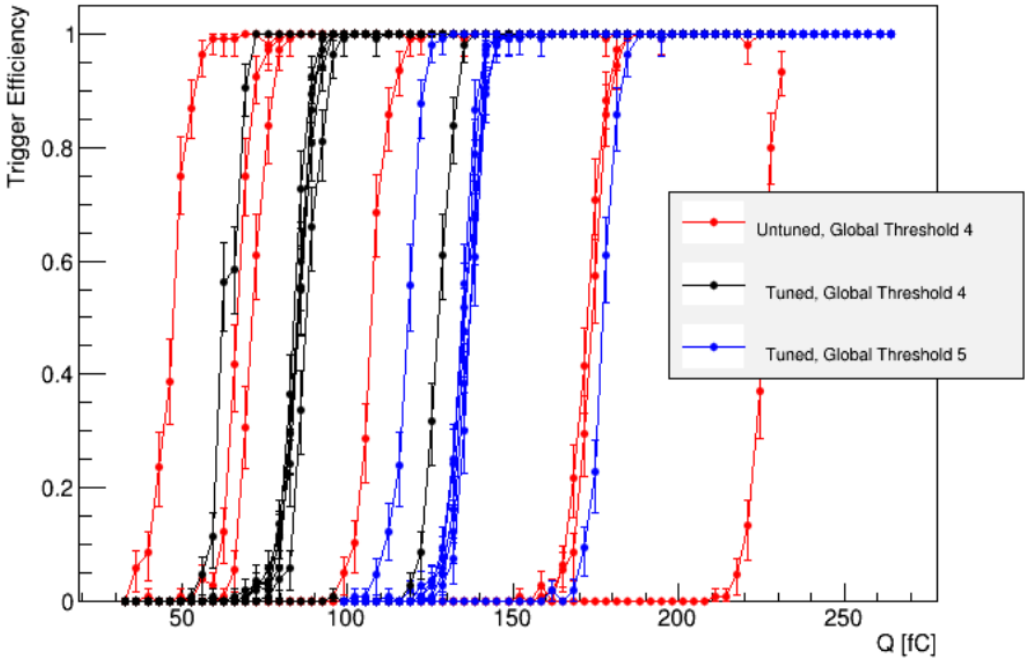
12-bit pipelined ADC

- ✔ Fix bugs in control logic

All ADCs are designed to be event-driven

Front-end

KLauS4



Comparator s-curves, 7 channels:
- No threshold tuning (same fine-tune setting)
- 2 global threshold settings after fine-tuning

Trigger comparator

Some outliers after fine-tuning

Would be worse in 36-channel

Mismatches among channels

Solution: extend the fine-tuning range

- ✔ Increasing the LSB current
- ✔ Increasing critical component size
- ✔ Adding a scaling control bit to double the LSB current (channel-wise)

Front-end

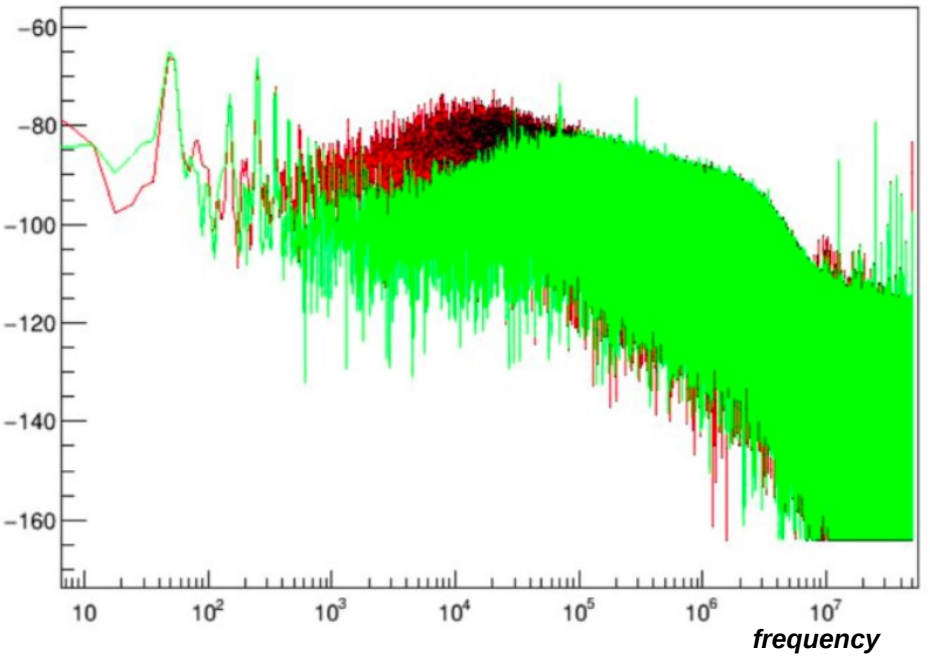
LFOTA

Low frequency feedback loop
to stabilize the pedestal

Gain-bandwidth plays a important role

Increase the gain-bandwidth
to suppress the noise

Pedestal PSD of KLauS4



Hold delay

Large delay dispersion among channels and cannot be totally fine-tuned
Size of critical components enlarged **to reduce the mismatch**

Low gain branch

Add a scaling setting to *extend the dynamic range to 400pC* (simulated)

Summary

- 36-channel KLauS5 submitted
- KLauS5 will be charactered once the chip is ready
- HBU and package will be discussed