R&D for the CLIC tracker

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On behalf of the CLICdp collaboration

International Workshop on Future Linear Colliders LCWS2017

Bundesministerium
für Bildung
und Forschung

universitätbonn

Outline

- Introduction
- Technology consideration
- Test beam
- SOI test chip
- HR CMOS Investigator test chip
- Fully integrated HR-CMOS chip for the CLIC tracker
- Summary & outlook

Requirements for the CLIC tracker

To achieve high precision measurement of track momentum:

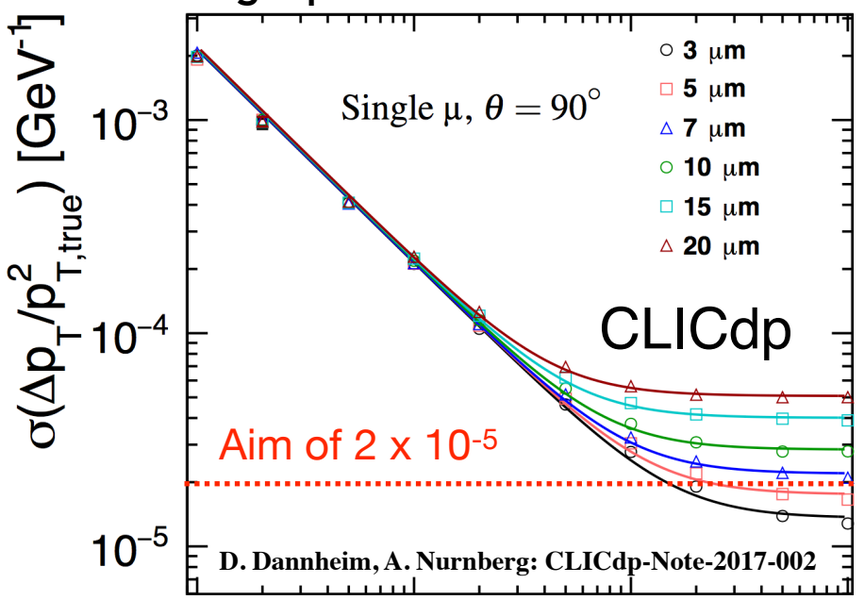
- Need single point resolution of ~ 7 μm (high momentum tracks):
  - Small pitch ~ 30 μm
- Material budget of 1 - 1.5 % X_0 per detection layer (low momentum tracks, photon conversion):
  - Silicon thickness of < 200 μm

To suppress beam-beam background:

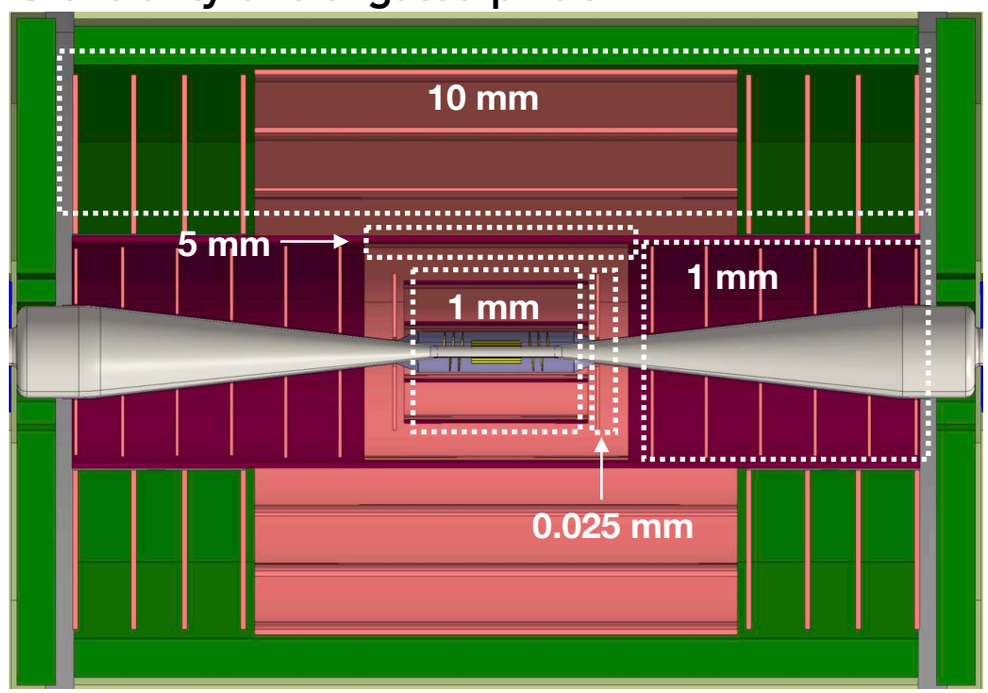
- Large surface silicon tracker with elongated pixels/small strips:
  - Granularity in barrel of 1 mm x 50 μm - 10 mm x 50 μm (depending on layer)
  - Inner tracker disc with 0.025 mm x 50 μm granularity required from pattern recognition, granularity of 10 mm in other disks
- Time slicing of 10 ns

Note: moderate radiation environment of 10^{-4} times lower than LHC

Momentum resolution for different single point track resolution:



Granularity of elongated pixels:



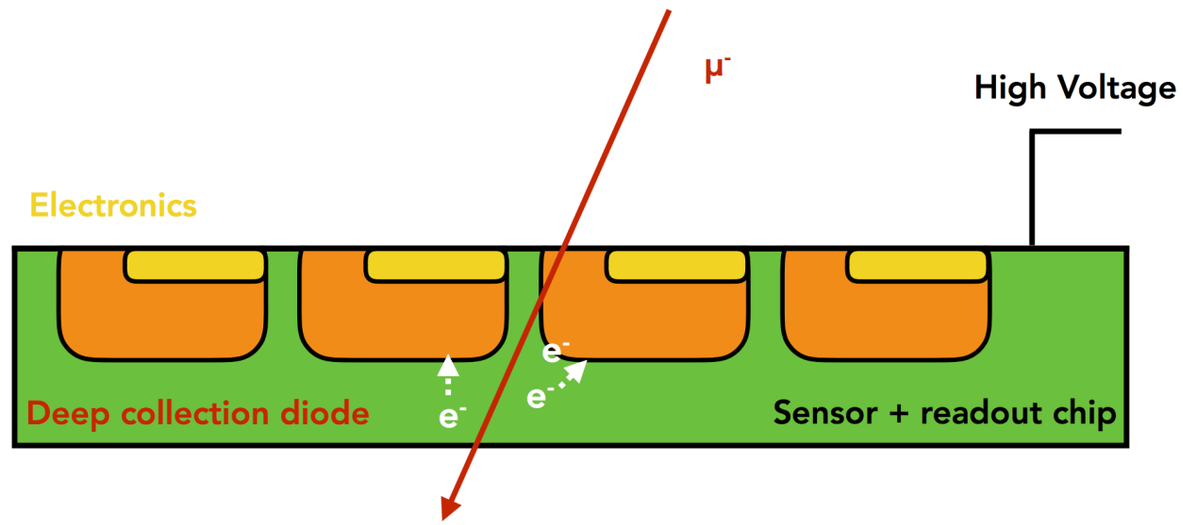
See note by D. Dannheim, A. Nurnberg: Requirements for the CLIC tracker readout (CLICdp-Note-2017-002)

Technology considerations

Integrated technologies are interesting candidates especially in view of large scale production & low material budget

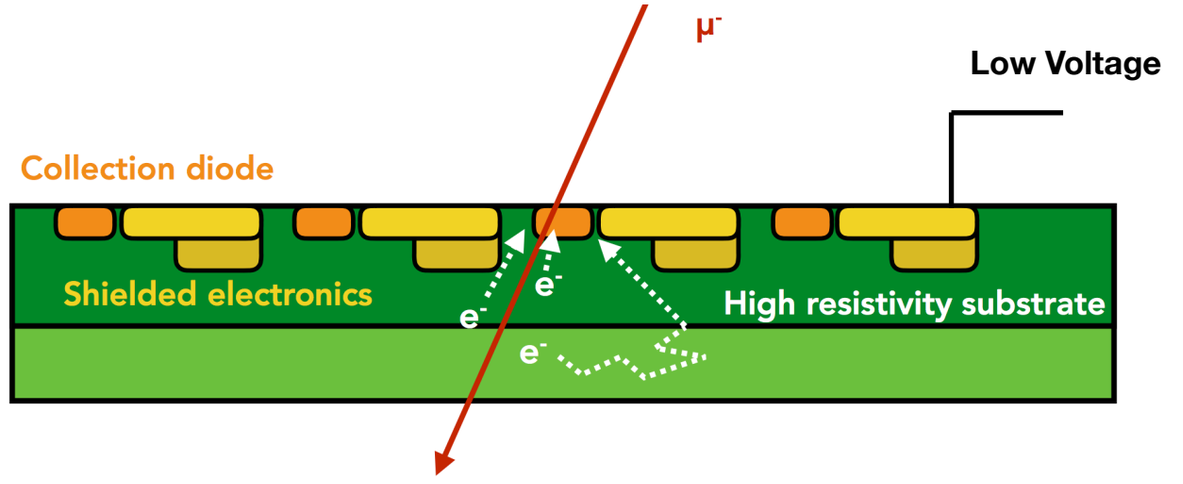
Integrated High Voltage (HV) CMOS:

- Electronics integrated in large deep collection diode (large capacitance)
- High voltage (frontside bias, backside bias possible)
- High resistivity possible



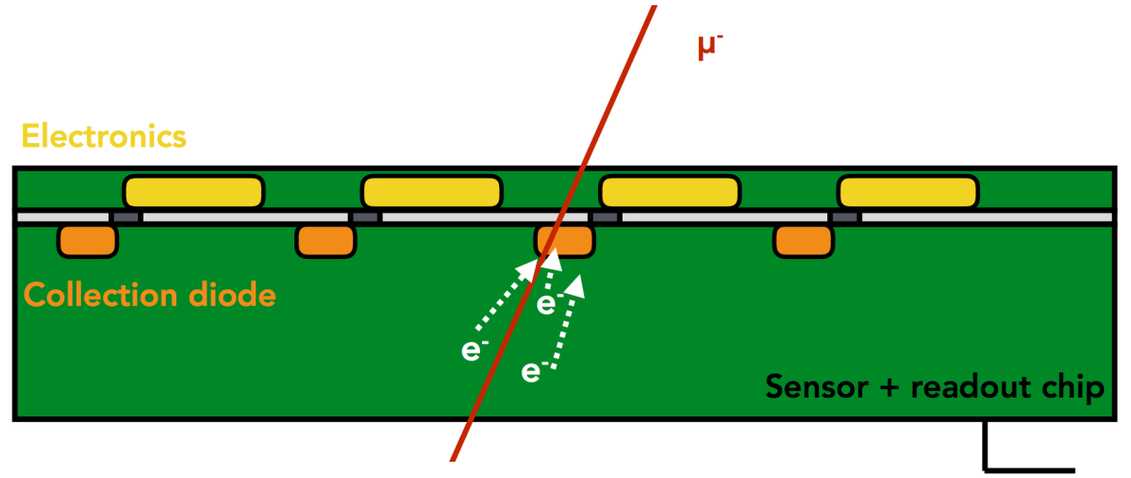
Integrated High Resistivity (HR) CMOS:

- Electronics integrated in separate wells (small collection diode → small capacitance)
- Low voltage (frontside bias)
- Recent process modifications achieve full depletion and allow for backside biasing with higher voltage



Silicon On Insulator (SOI):

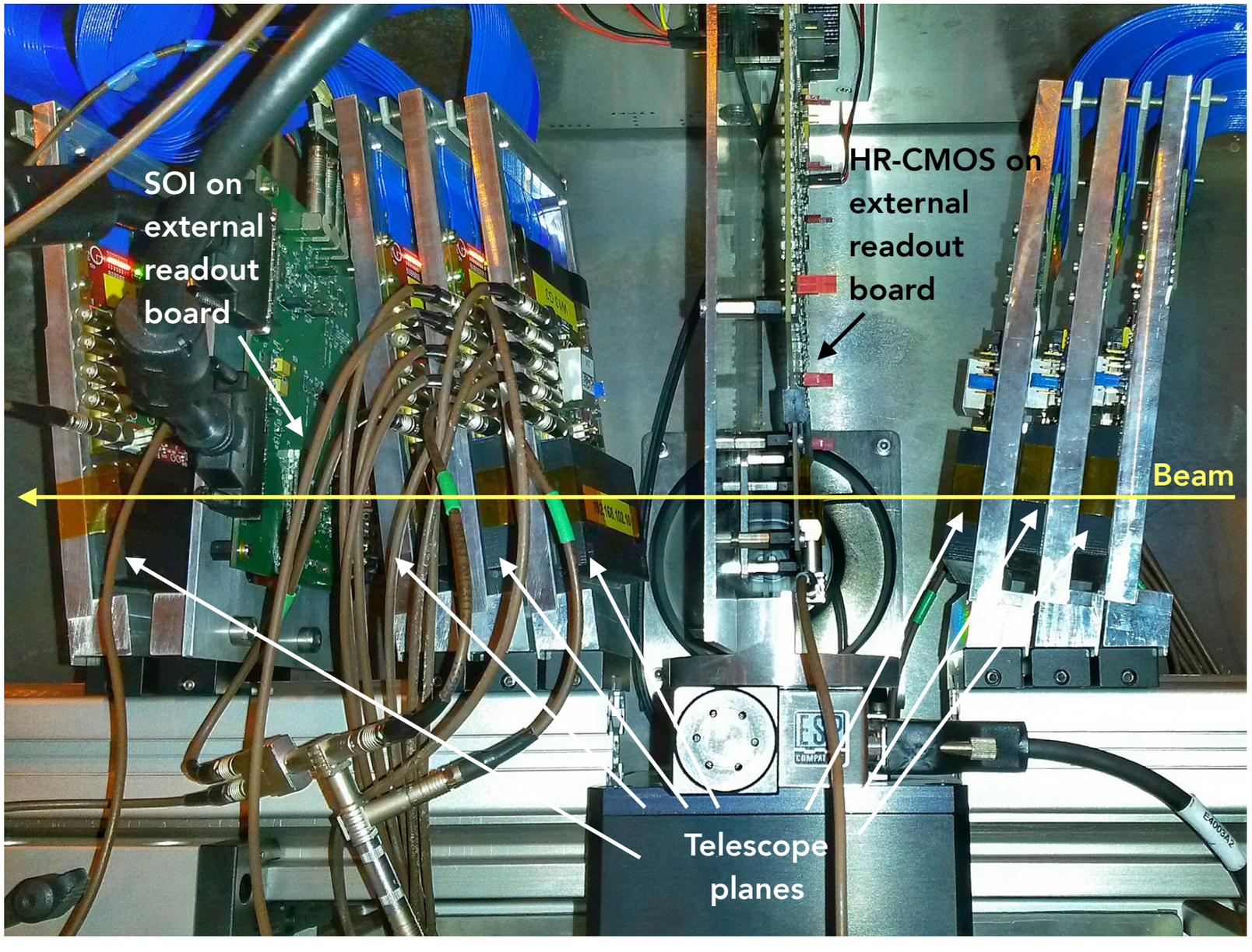
- Electronics separated by insulation layer
- High backside voltage (full/homogenous depletion)



Test beam

Test chips of various technologies considered for the CLIC tracker (integrated HV-CMOS, integrated HR-CMOS, SOI) have been integrated in CLICdp Timepix3 telescope:

SOI and HR-CMOS test chips in CLICdp Timepix3 telescope:



CLICdp Timepix3 telescope:

- Permanently installed at end of H6 beam line in SPS north area
- Excellent tracking performance:
  - Spatial resolution of 2 μm (on the centre DUT)
  - Timing resolution of < 1 ns (on the centre DUT)

Studied HV-CMOS - ATLASpix_simple

180 nm HV-CMOS process:

- Fully integrated chip designed for ATLAS ITk upgrade
- Fabricated on wafer with resistivity of 80 Ω cm
- Analogue part in pixel (charge amplifier, discriminator)
- Digital logic in periphery (point to point connection):
  - Simultaneous ToT and ToA readout

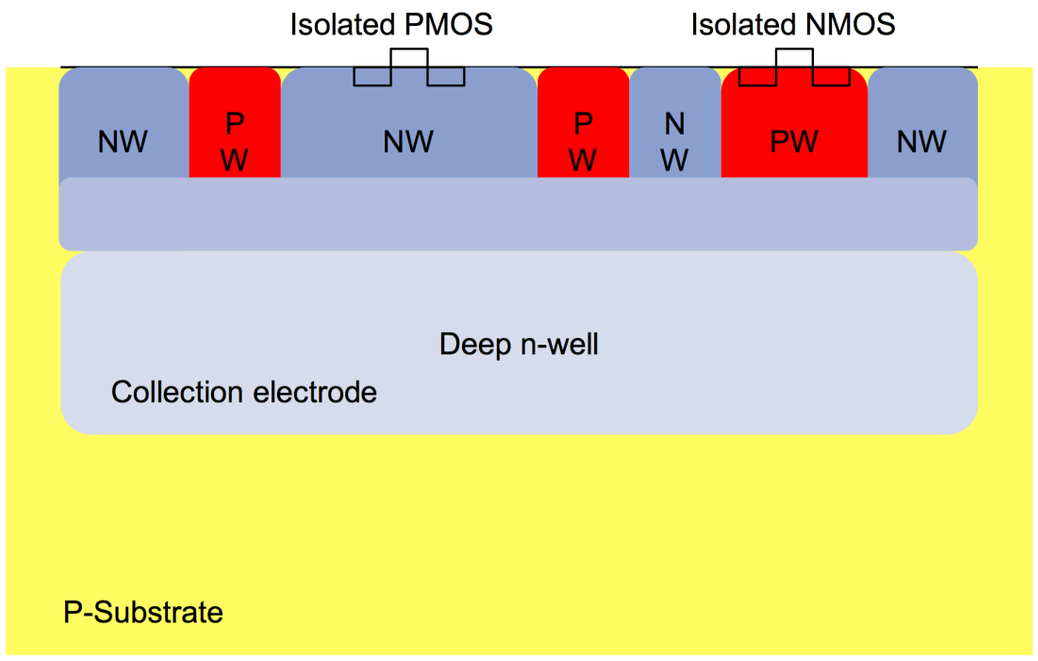
Layout:

- 25 x 400 pixels, 130 µm x 40 µm pixel size
- Attractive for elongated pixels for CLIC tracker

First results:

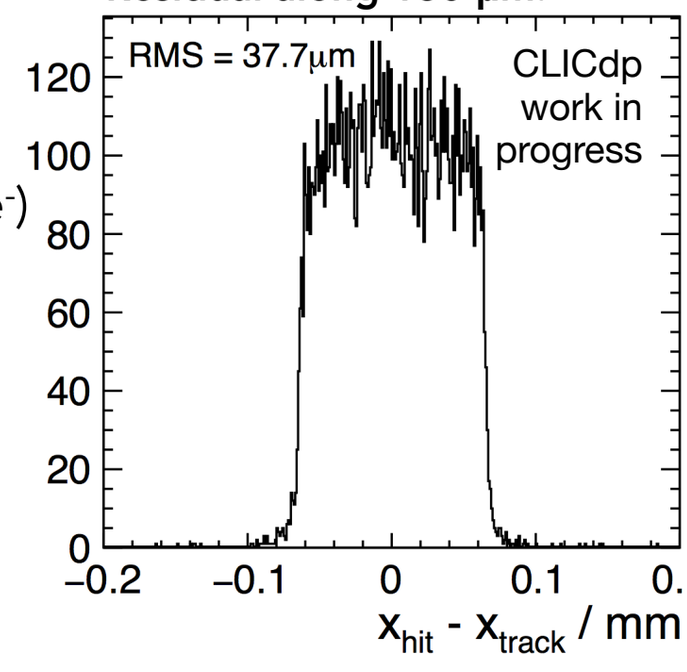
- Almost no charge sharing (threshold ~ 3000 e^-)
- Residual distribution show RMS of pitch/√12
- Measured with ATLAS FE-I4 telescope (threshold ~ 1000 e^-):
  - Efficiency ~ 99.7 % (preliminary)

Process cross section of ATLASpix:

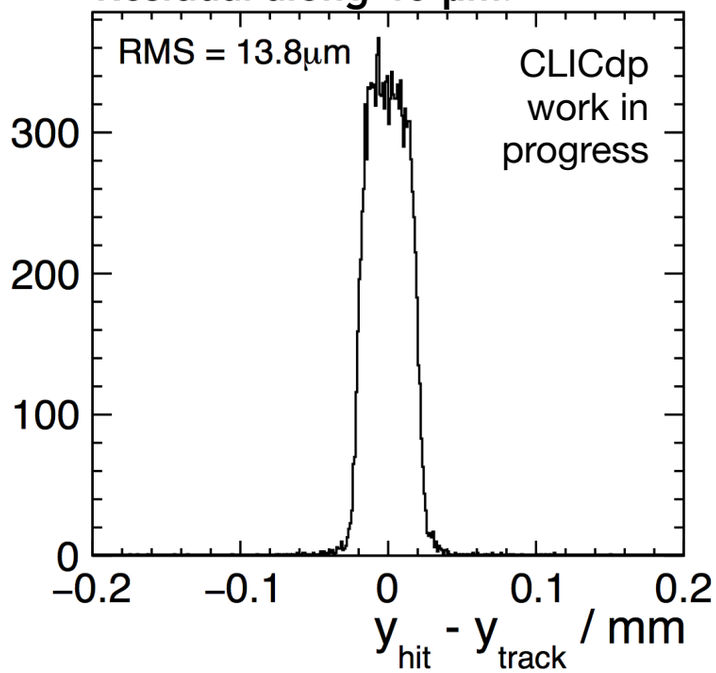


I. Peric, 12th Trento Workshop, 2017

Residual along 130 µm:



Residual along 40 µm:



Studied Silicon On Insulator (SOI) process

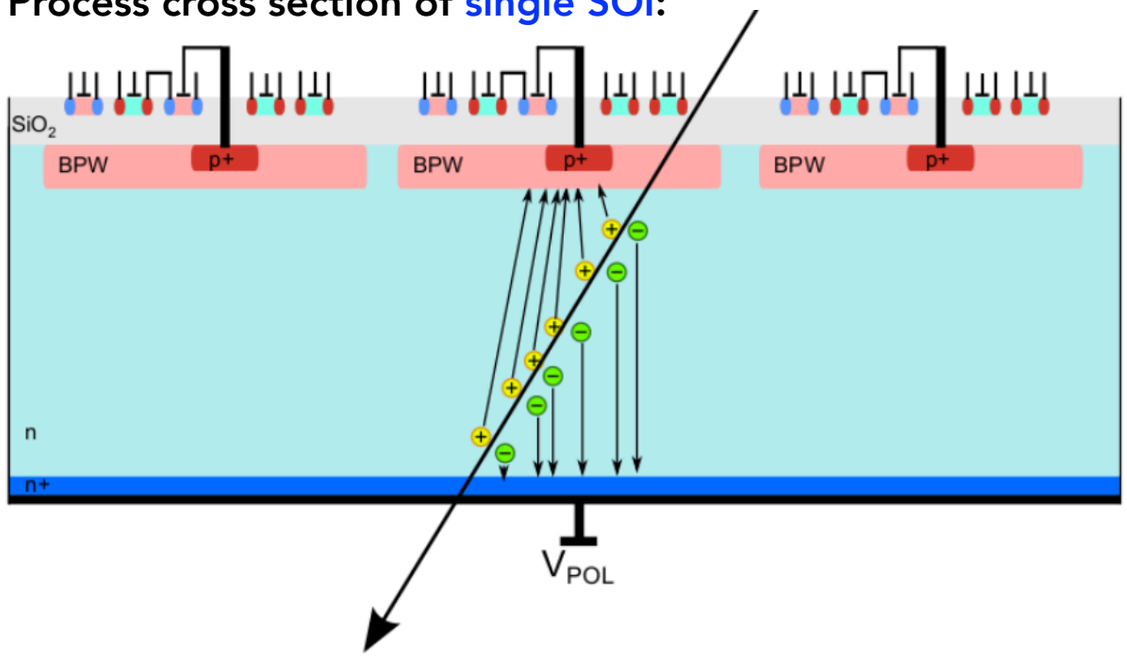
200 nm CMOS-SOI process:

- Studied chip designed by AGH & IFJPAN-Crakow group
- Fabricated on High Resistivity (HR) wafer
- Sensor and electronics integrated on a single wafer
- Electronics shielded by insulation layer and **B**uried **P-W**ells (BPW):
  - High voltages applicable:
    - Full depletion and fast timing
  - Reduction of parasitic capacitance:
    - Maximise signal/noise
    - Low analogue power consumption & fast timing

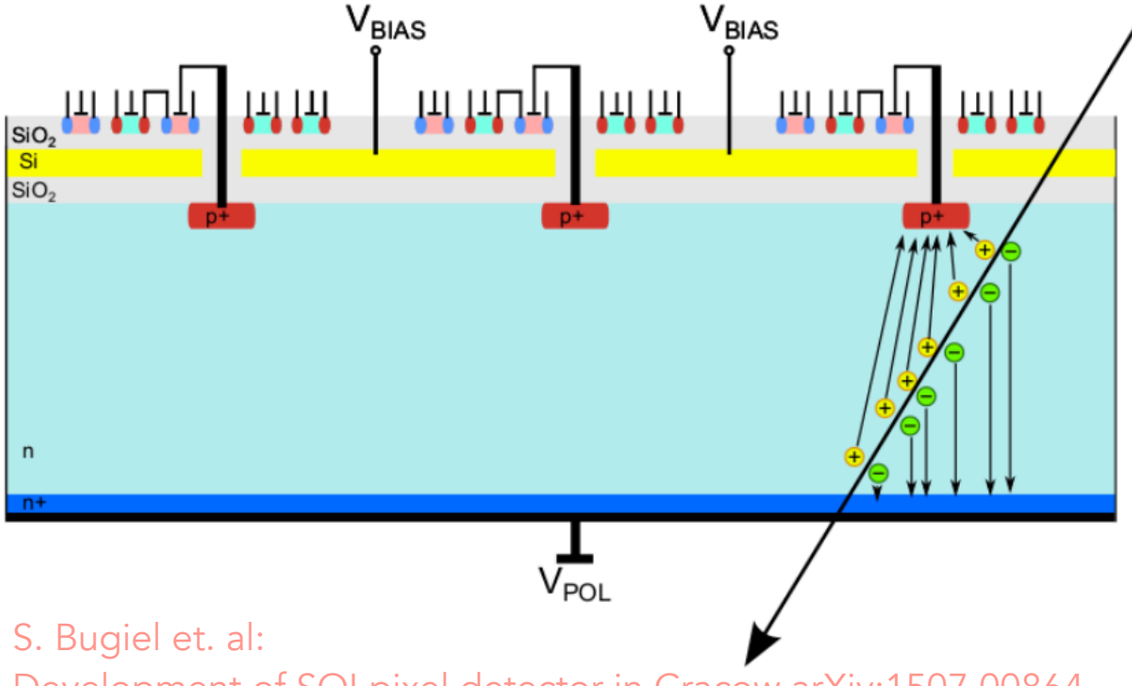
Improvement:

- Additional biased silicon layer in insulation layer:
  - Compensated threshold shift in CMOS transistors from radiation
  - Also serves as additional shielding of electronics
  - Additional capacitance from silicon layer

Process cross section of single SOI:



Process cross section of double SOI:

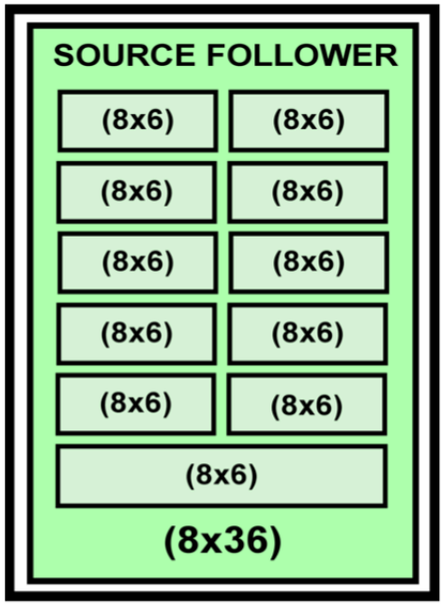


S. Bugiel et. al:
Development of SOI pixel detector in Cracow arXiv:1507.00864 [physics.ins-det])

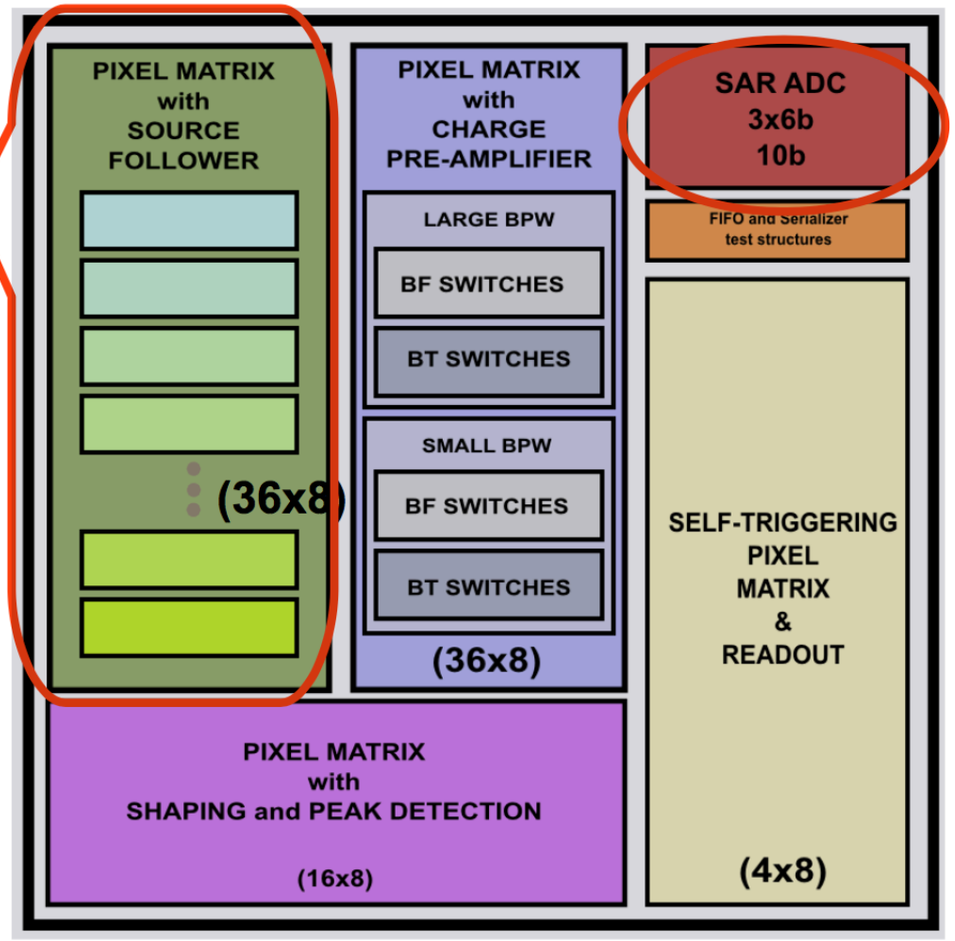
SOI test chip

Test chip with different pixel layouts:

- Different sections with pixel circuitry containing source follower or charge preamplifier
- For each section various matrixes with 8 x 6 pixels are implemented (different pixel, BPW and transistor sizes)



SOI chip layout:



S. Bugiel et. al:
Development of SOI pixel detector in Cracow
arXiv:1507.00864 [physics.ins-det])

- Analogue response of amplitude sent to external ADCs

Different substrates:

- Variation of:
  - Thickness (300 - 500 µm)
  - Doping (n/p)
  - Resistivity (700 Ωcm, 2 kΩcm, 7 kΩcm)
  - Materials (FZ(n), FZ(p), CZ(n))
  - Process (SOI, double SOI)

Results presented for a 500 µm thick FZ(n) wafer type SOI chip

SOI test beam results

Bias scan for source follower matrix with a pitch of 30 µm on single SOI chip:

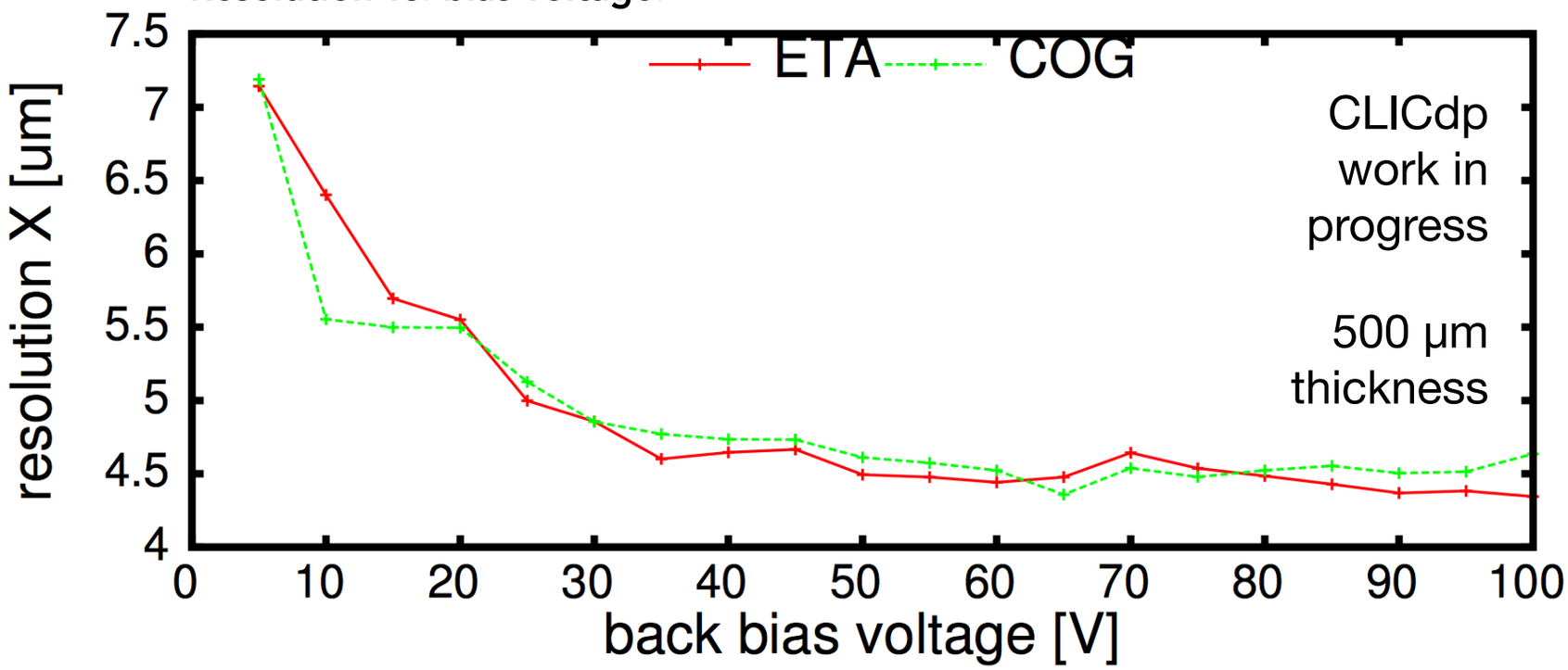
For bias voltages ≳ 50 V:

- Fully efficient
- Resolution of ~ 4.5 µm

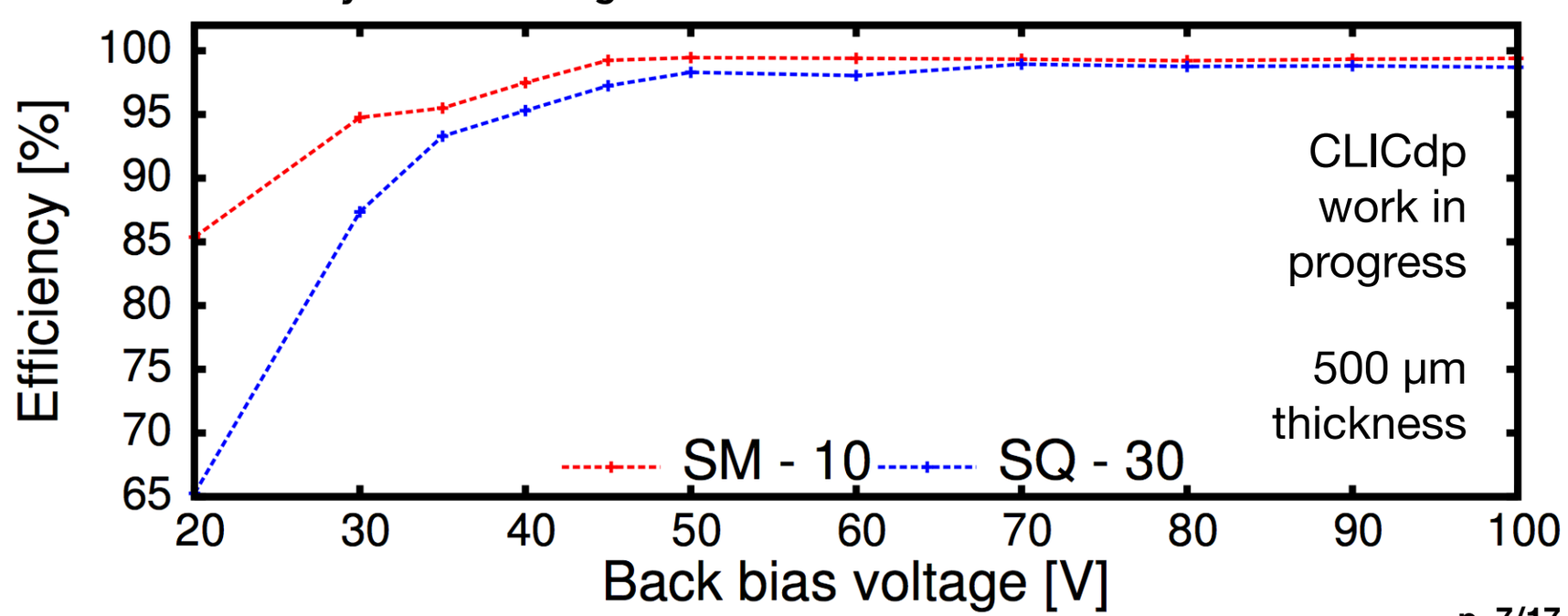
- Proof of good performance of investigated design

- Further studies with thinner sensors needed to evaluate performance with respect to requirements of CLIC tracker

Resolution vs. bias voltage:



Efficiency vs. bias voltage:



SOI test beam results

Comparison of different pixel designs:

- Investigated different in-pixel circuitry (source follower or charge preamplifier) and different shielding (BPW)

Results for matrix with 30 µm pitch on a single SOI FZ(n) chip:

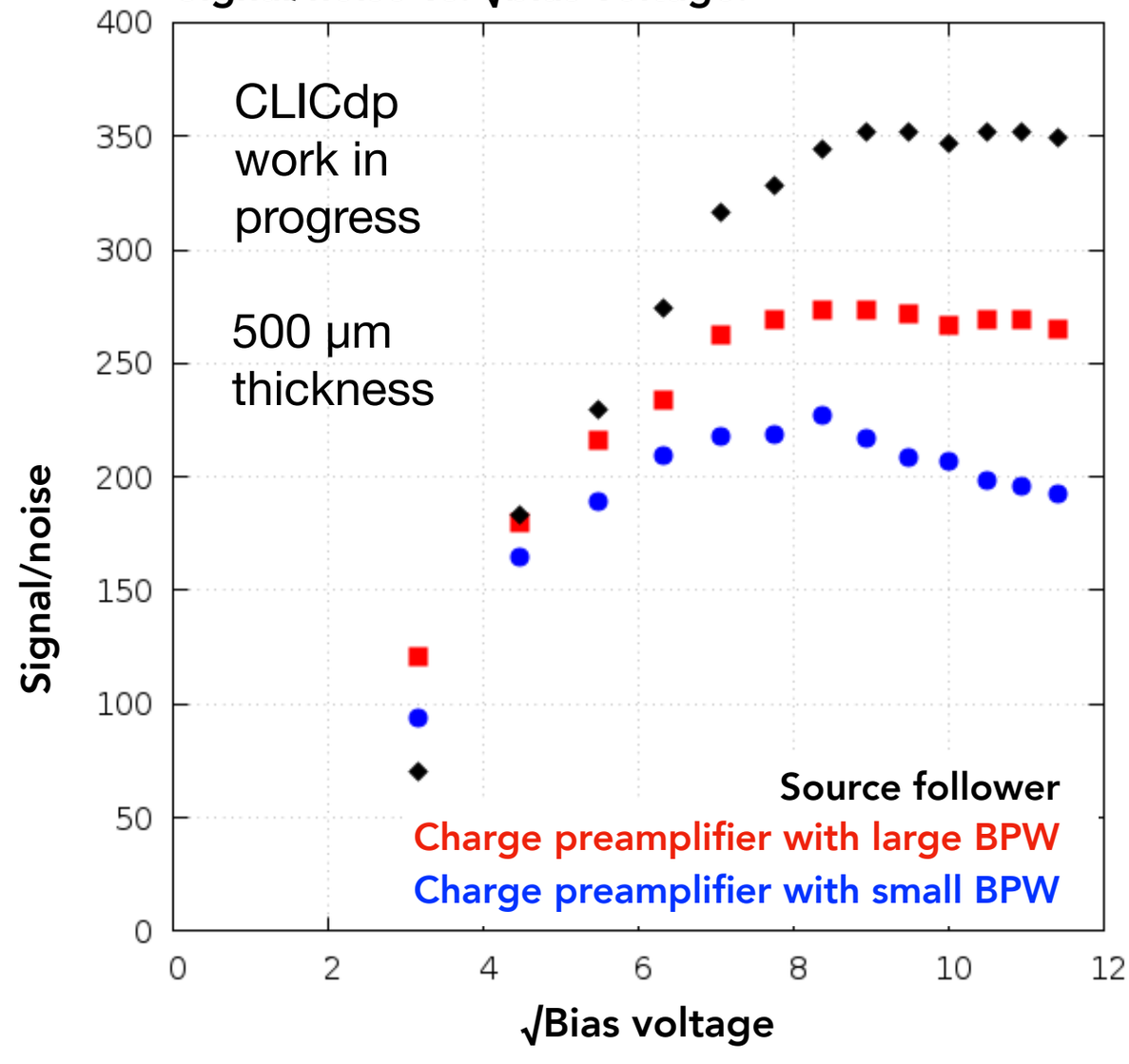
Larger signal/noise for source follower:

- More simple design for source follower (fewer transistors)
- Less noise

Larger signal/noise for large BPW:

- Better shielding of CMOS logic
- Lower noise

Signal/noise vs. √bias voltage:



New chip w.r.t. results presented on previous slide:

- Larger matrices with better s/n ⟶ expect improved performance due to lower threshold

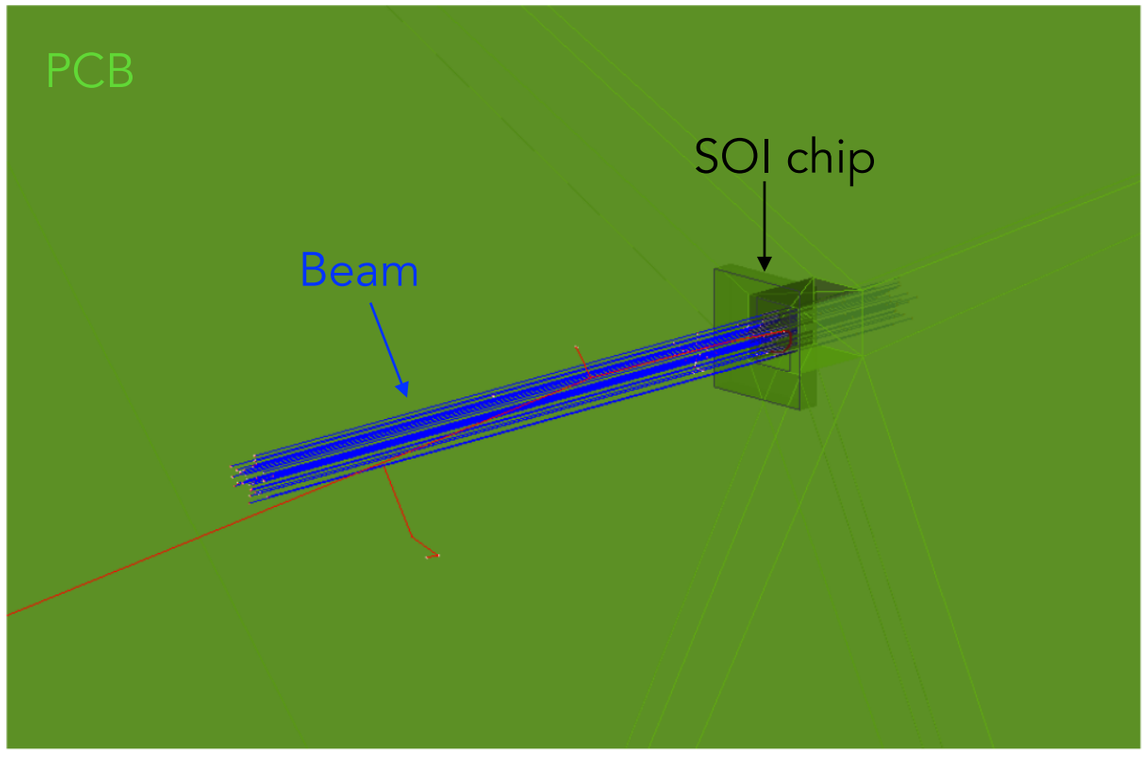
SOI simulations

Allpix Squared simulation framework used to model SOI response:

See talk by D. Dannheim, R&D for the CLIC vertex detector

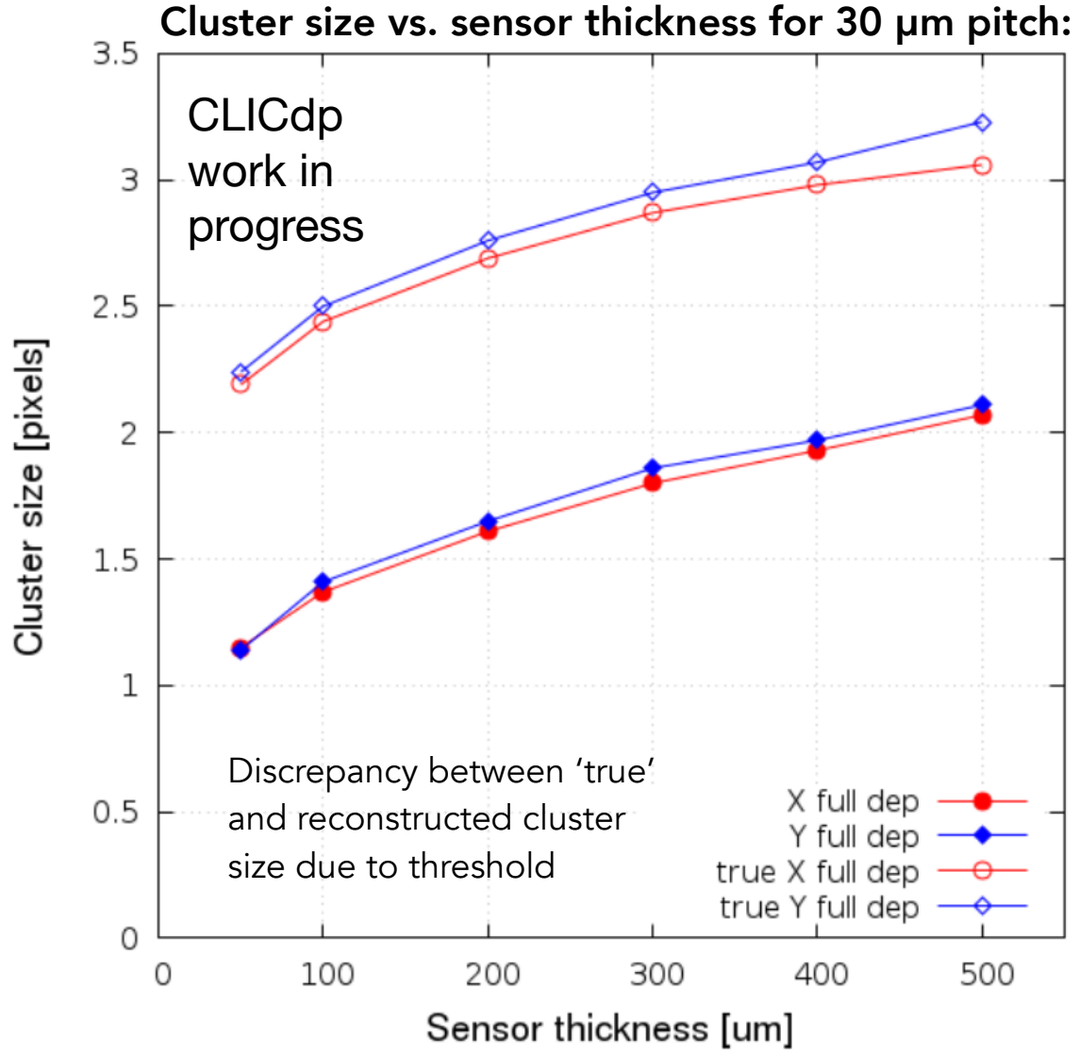
- Implementation of setup (PCB, chip geometry)
- Implementation of chip parameters (noise, gain, threshold)
- Simulate planar sensor as active material

SOI chip modeled in Allpix2:



- Evaluation of charge sharing for different sensor thicknesses at full depletion:

Cluster size vs. sensor thickness for 30 µm pitch:



Studied HR-CMOS process

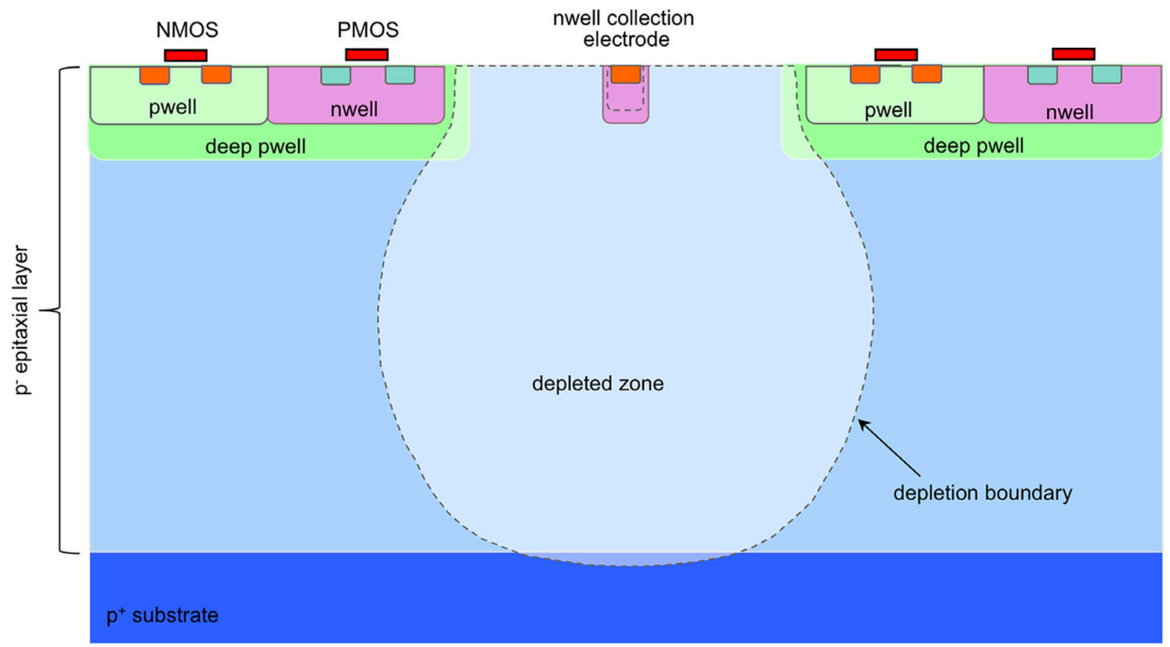
180 nm HR-CMOS process:

- Studied Investigator test chip designed as part of ALICE ITS upgrade (W. Snoeys et. al)
- Thin HR epitaxial layer (15-40 µm)
- CMOS circuitry placed and shielded by separated deep P-well
- Small collection diode small capacitance:
  - Maximise signal/noise
  - Low analogue power consumption and fast timing
- Frontside biasing:
  - Bias voltage limited by CMOS transistors to - 6 V

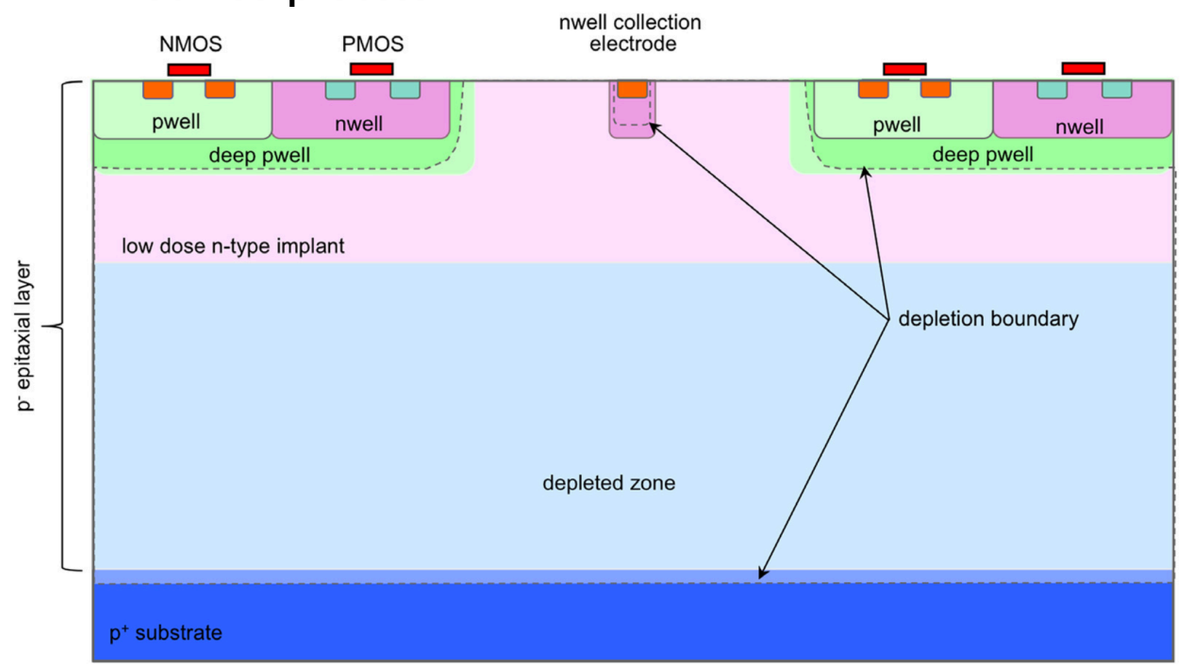
Improvement:

- Additional low dose N-implant to achieve full lateral depletion:
  - Improved radiation tolerance
  - Faster timing capability (?)
  - Backside biasing possible (not limited to - 6 V)

Standard process:



Modified process:



W. Snoeys et. al:
A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance (http://dx.doi.org/10.1016/j.nima.2017.07.046)

Investigator test chip

Test chip with different pixel layouts:

- Different mini-matrices with 8 x 8 pixels and various pixel layouts (variation of e.g. pixel size, collection electrode size)
- Each pixel contains a source follower

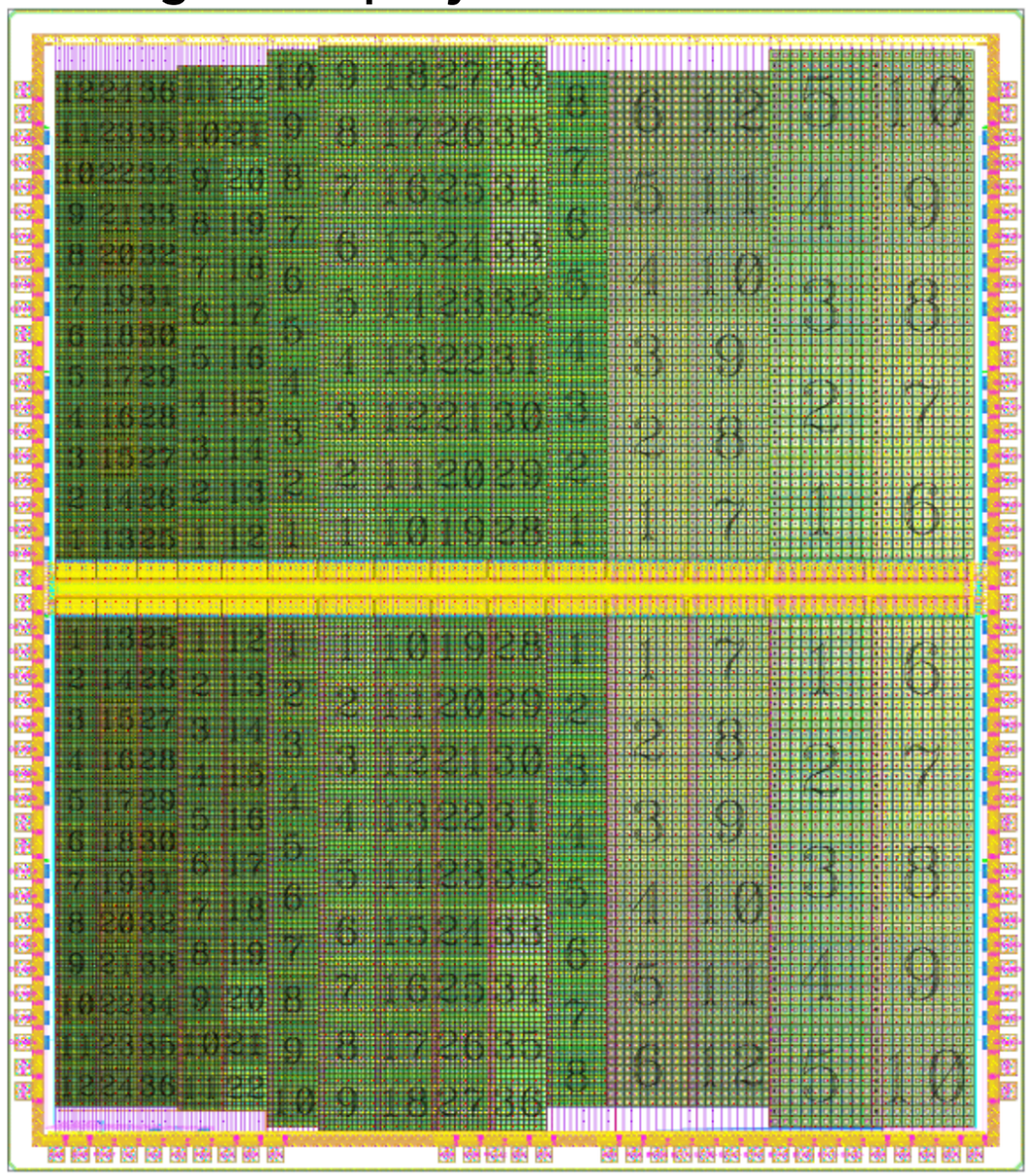
Digital logic not on chip:

- Analogue response sent to external ADCs
- One ADC per pixel (65 MHz sampling)

Different productions:

- Variation of:
  - Epitaxial layer thickness (15-40 µm)
  - Resistivity (1-8 kΩcm)
  - Process (standard, modified)

Investigator chip layout:



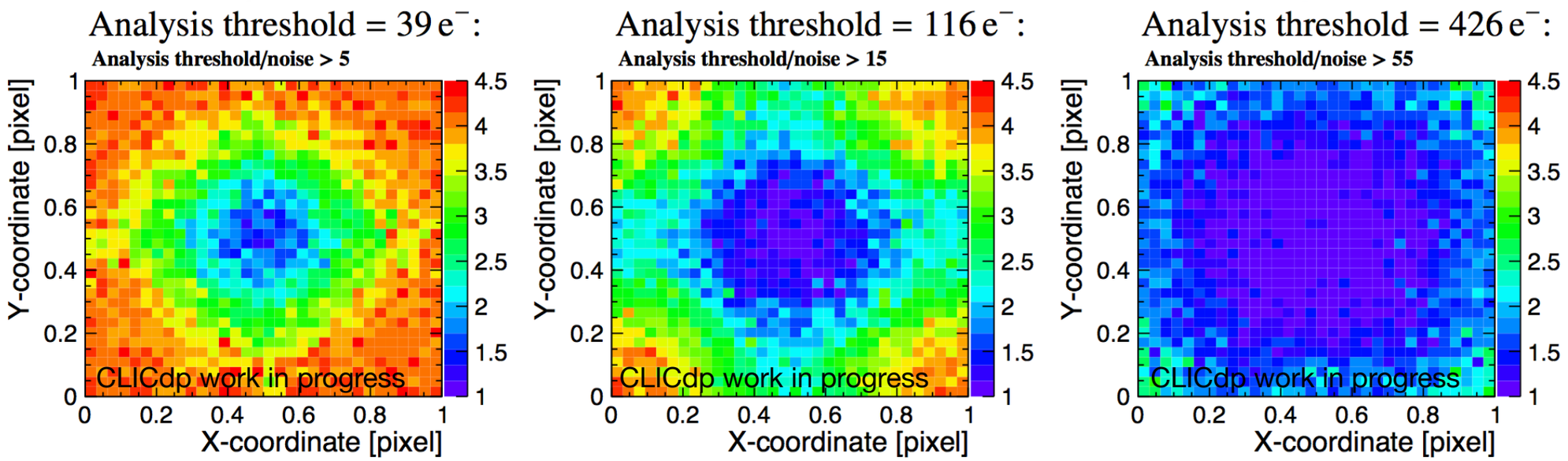
Chips with an epitaxial layer thickness of 25 µm (depletion depth of ~ 18 µm) have been studied for the standard and modified process

W. Snoeys et. al:
A process modification for CMOS monolithic active pixel sensors for enhanced depletion, timing performance and radiation tolerance (http://dx.doi.org/10.1016/j.nima.2017.07.046)

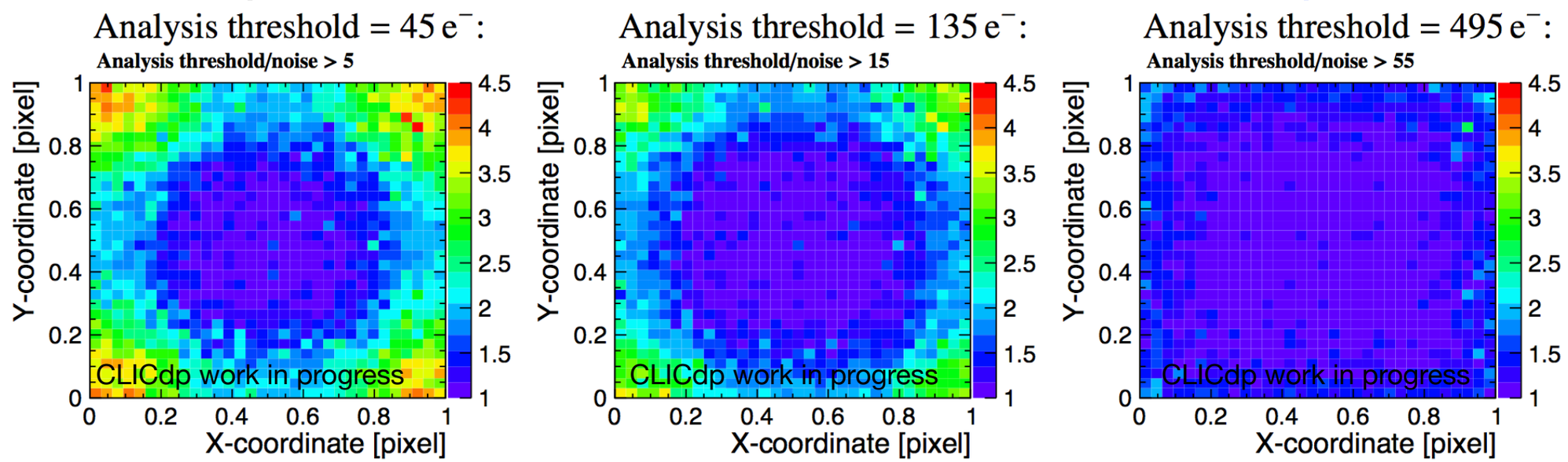
Investigator test beam results

Charge sharing studies (pitch of 28 µm, bias voltage of - 6 V):

In-pixel cluster size at different thresholds for the standard process:



In-pixel cluster size at different thresholds for the modified process:

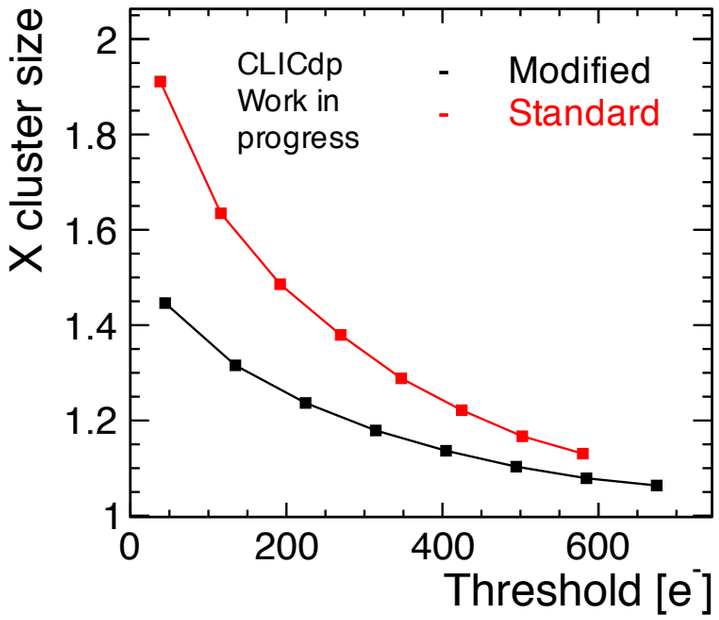


→ Significantly more charge sharing for standard process, as expected from diffusion.

Investigator test beam results

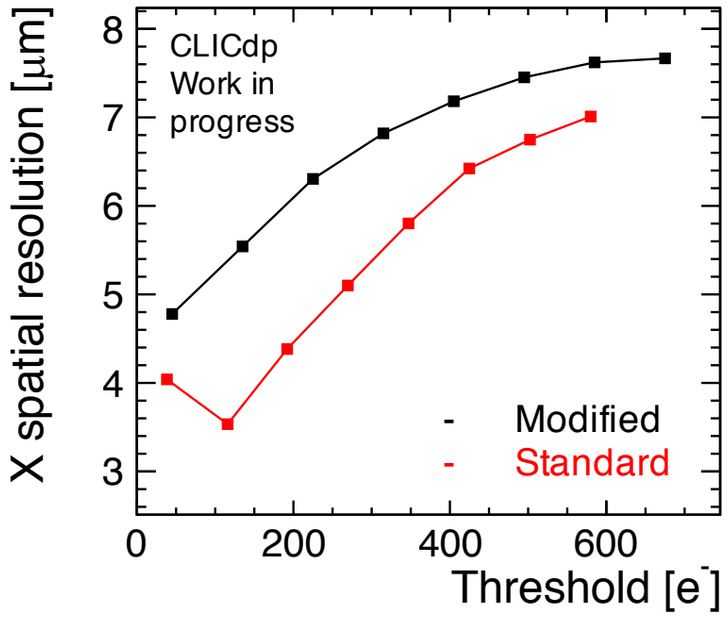
Impact of charge sharing on spatial resolution and efficiency for standard & modified process (pitch of 28 µm, bias voltage of - 6 V):

X cluster size vs. threshold:



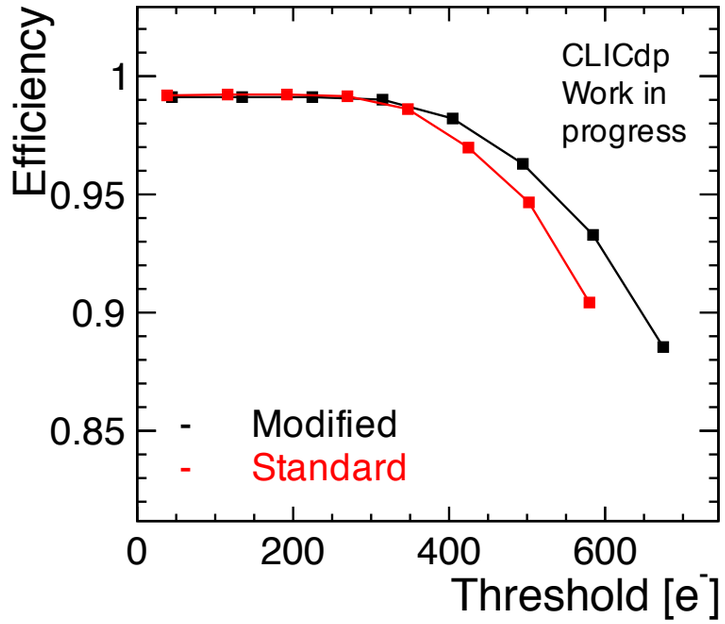
- More charge sharing for standard process
- Expected from non depleted regions (diffusion)

X resolution vs. threshold:



- Better spatial resolution for standard process down to ~ 3.5 µm

Efficiency vs. threshold:



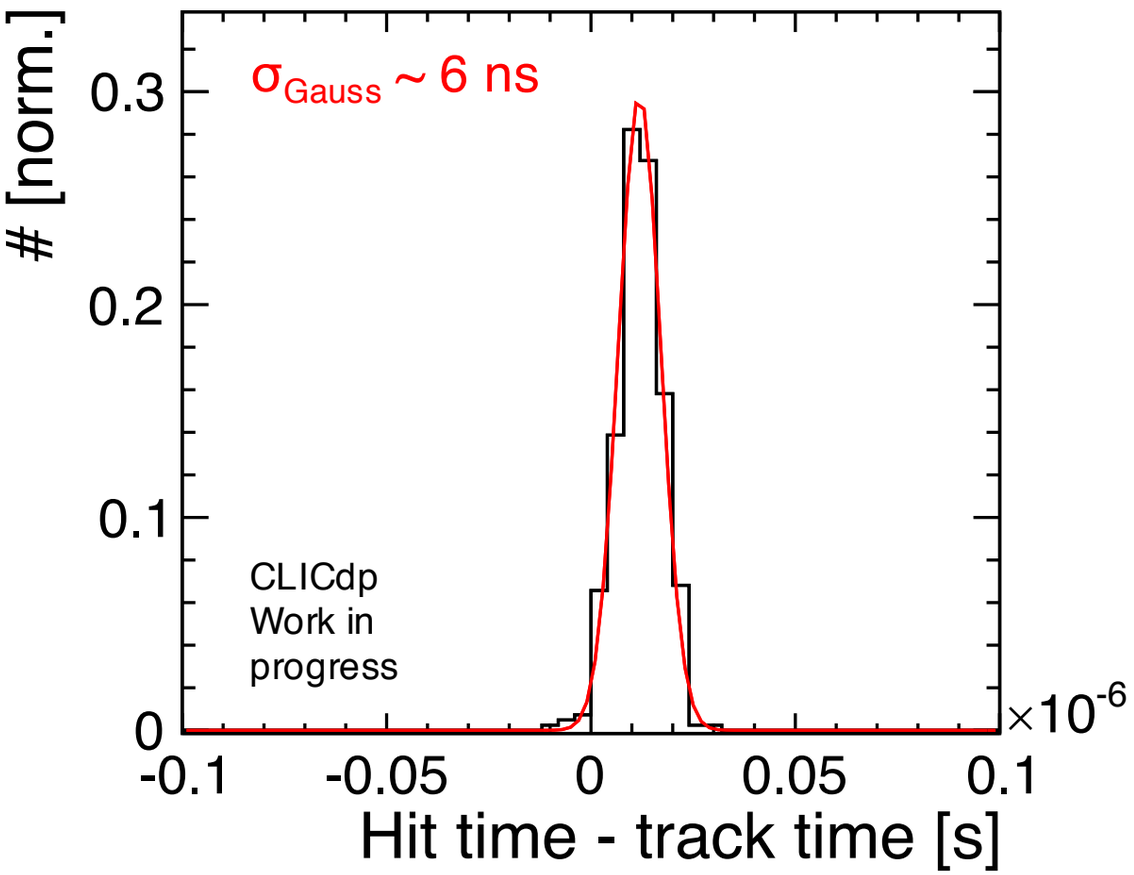
- Earlier drop of efficiency (at lower thresholds) for standard process

→ Efficiency & spatial resolution for both process variants within requirements for CLIC tracker.

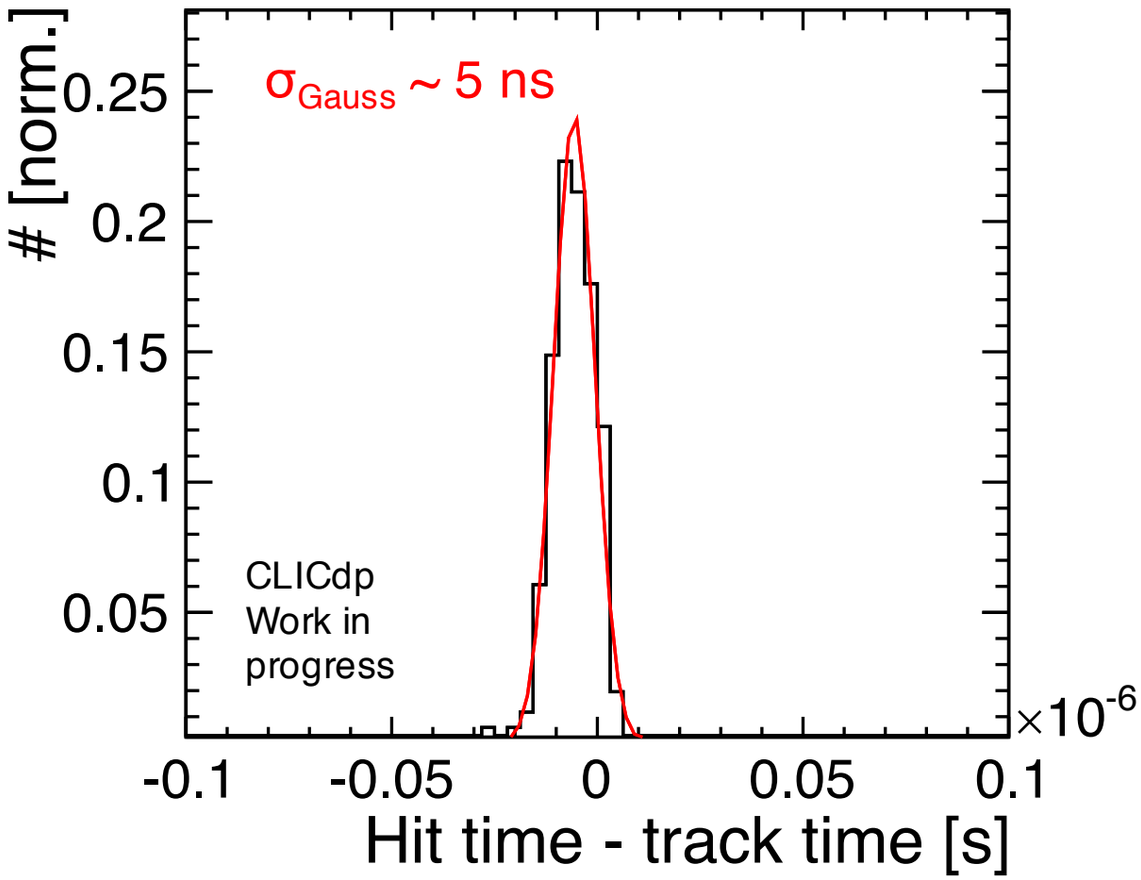
Investigator test beam results

Timing resolution for standard & modified process
(pitch of 28 µm, bias voltage of - 6 V):

Standard process:



Modified process:



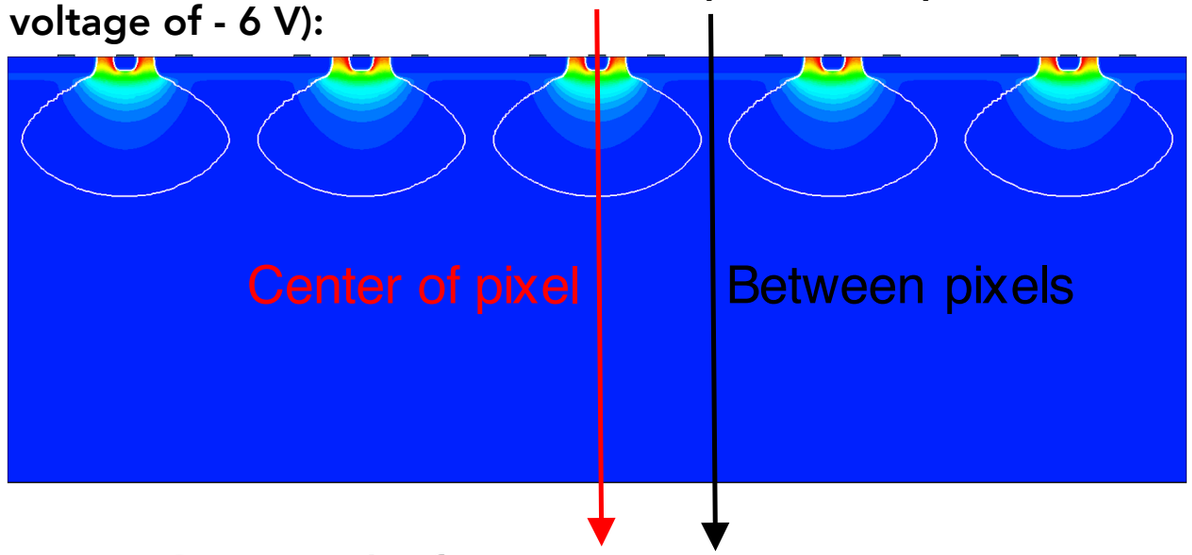
→ Comparable timing resolution for both processes

(Probably limited by used setup, readout sampling frequency of 65 MHz)

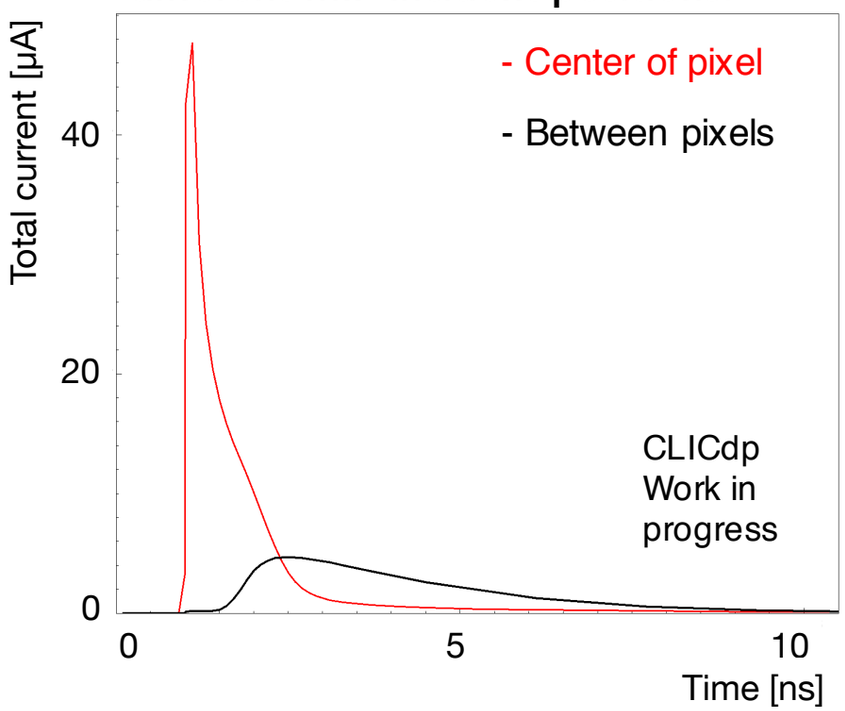
Investigator 2d-TCAD simulation

Standard process:

2d-TCAD simulation of electric field (pitch of 28 µm, bias voltage of - 6 V):

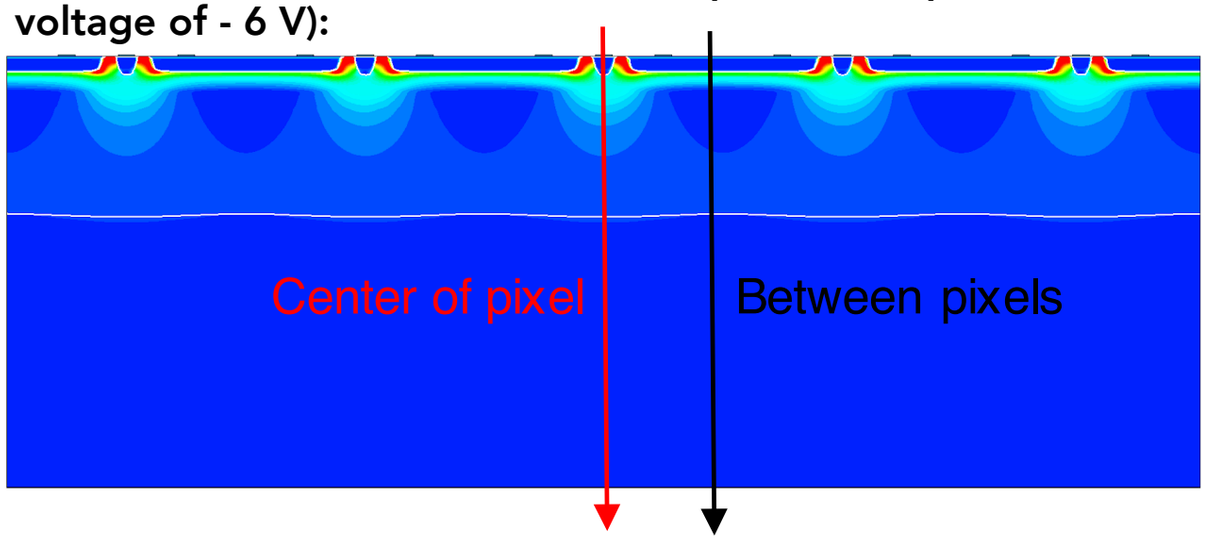


Current pulse for different MIP incident positions:

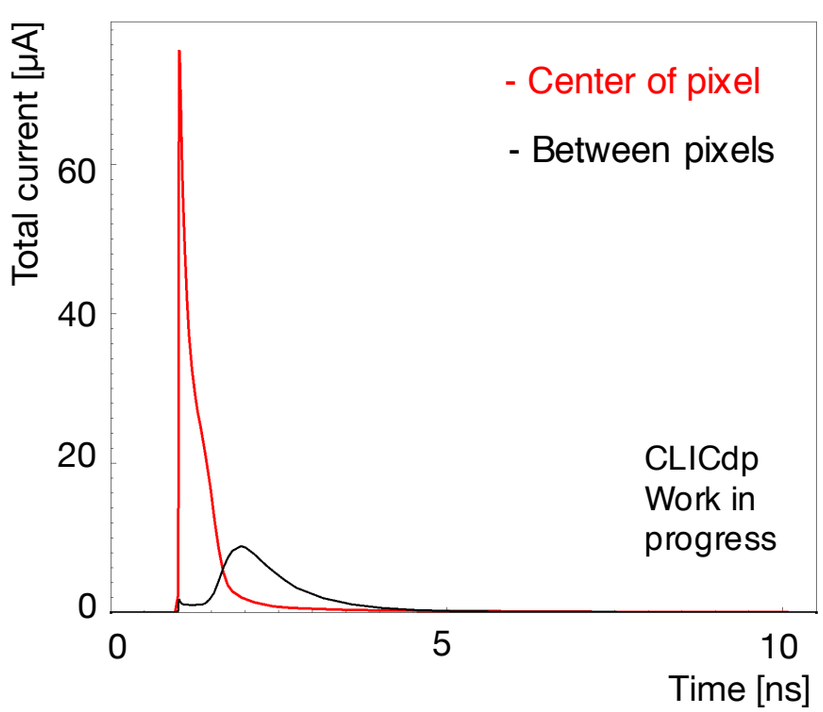


Modified process:

2d-TCAD simulation of electric field (pitch of 28 µm, bias voltage of - 6 V):



Current pulse for different MIP incident positions:



- Fast rise of current pulses for both process
- Slower component for standard process visible in non depleted regions between pixels

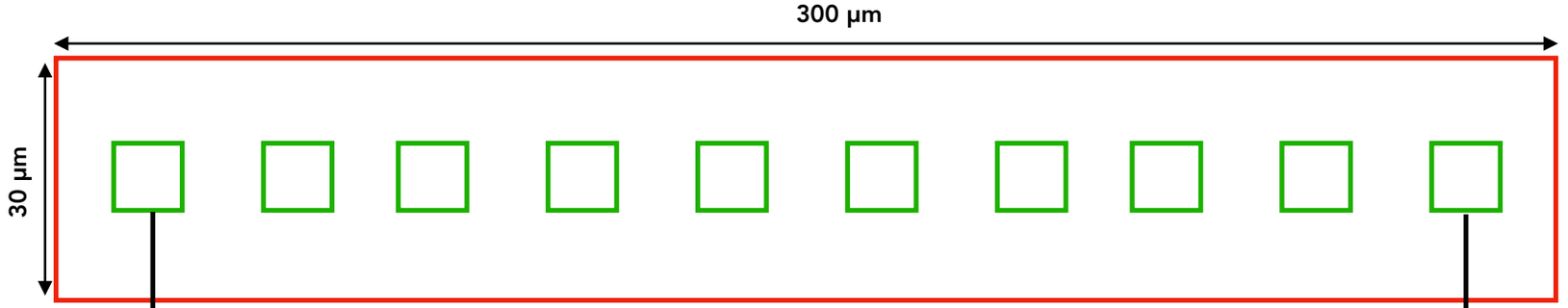
CLICTD - design of a fully integrated chip for the CLIC tracker

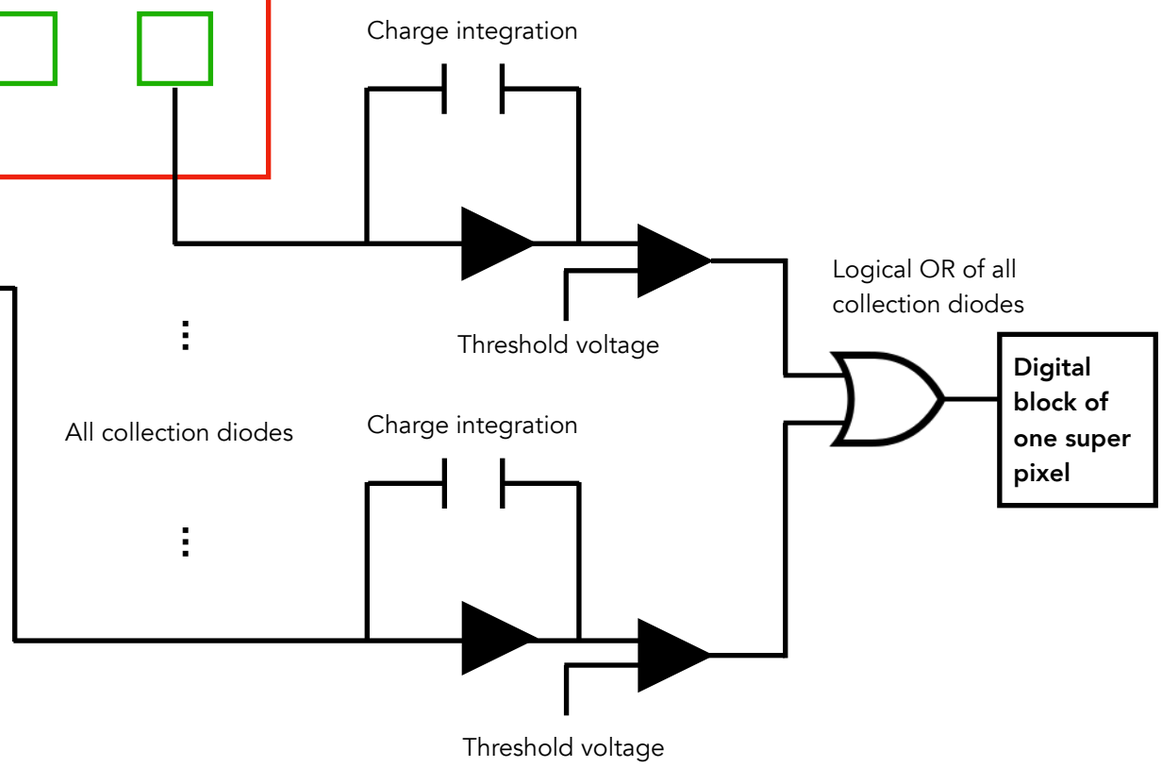
Motivation:

- Promising performance of studied HR-CMOS technology with respect to requirements of CLIC tracker
- Technology used in next phase of R&D to design a fully integrated chip for the CLIC tracker

CLIC Tracker Detector (CLICTD) - main idea/concept for elongated pixels/small strips:

- Design super pixel structures to maintain advantages of small collection diode (prompt and fully efficient charge collection) while reducing digital logic





CLICTD - some specifications:

- Discriminator output of each of the 10 collection diodes combined in logical OR
- Output of logical or passed to digital part:
  - Simultaneous 8-bit ToA and 5-bit ToT measurements
  - 100 MHz clock to achieve 10 ns time slicing

Summary and outlook

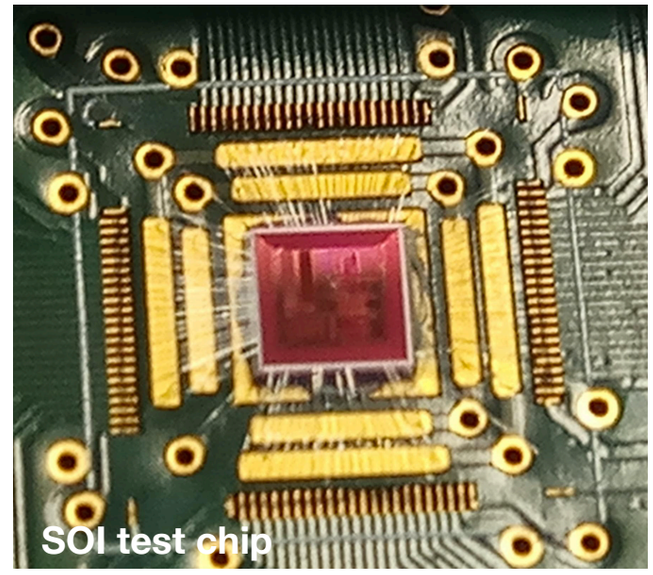
Prototypes of various integrated technologies under investigation for the CLIC tracker:

Integrated HV-CMOS:

- *MuPix and ATLASpix integrated in CLICdp Timepix3 telescope*

SOI HR-CMOS:

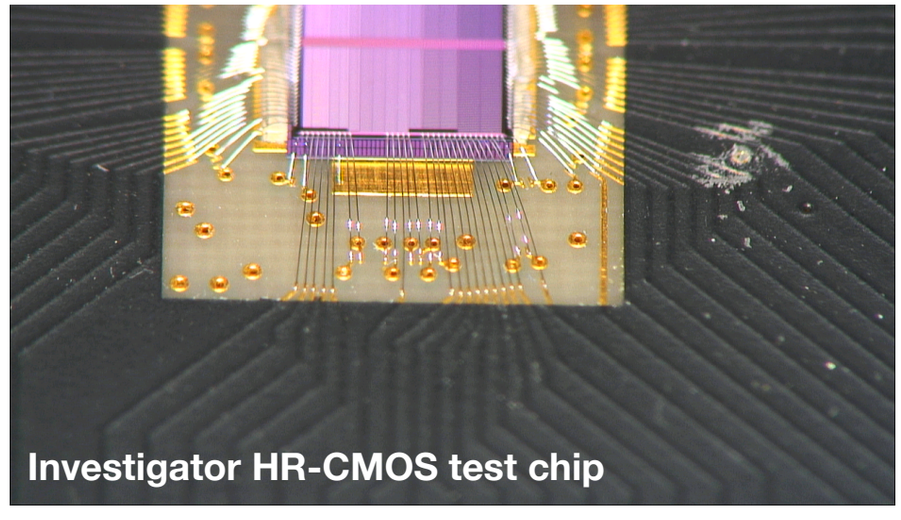
- Test beam studies of various pixel layouts and substrates
- *Good performance of investigated Cracow design for 500 µm thick prototypes*
- Further studies with thinner prototypes to evaluate performance w.r.t. requirements for CLIC tracker


SOI test chip

Integrated HR-CMOS

- Test beam and simulation studies of two different submissions
- *Promising analogue performance of 50 µm thin prototype (25 µm thin epitaxial layer) w.r.t. requirements for CLIC tracker:*
  - Efficiency > 99 %, spatial resolution down to 3.5 µm, timing resolution ~ 5 ns (28 µm pitch)

See note: Study of the ALICE Investigator in view of the requirements at CLIC (CLICdp-Note-2017-005)


Investigator HR-CMOS test chip

Fully integrated chip for the CLIC tracker:

- *HR CMOS technology used in next phase of R&D to design a fully integrated prototype chip for the CLIC tracker*

Thanks to all people that provided material to this talk!

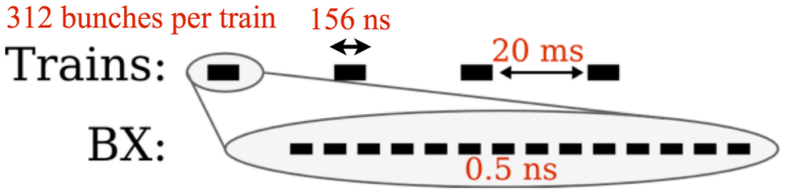
Backup

CLIC tracker - experimental environment and layout

Experimental environment:

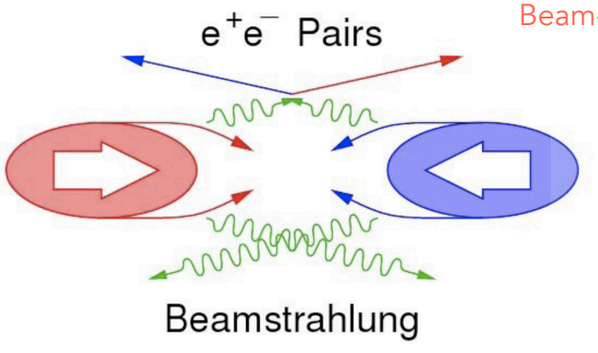
CLIC beam at 3 TeV:

Luminosity	6 x 10^{34} cm^{-2} s^{-1}
Bunch separation	0.5 ns
Bunches / train	312
Train duration	156 ns
Repetition rate	50 Hz
Duty cycle	~ 10^{-5}
Beam size x,y	45 nm x 1 nm
Beam size z	44 μm



Beam-beam interactions:

See talk by D. Arominski, Beam-induced backgrounds at CLIC

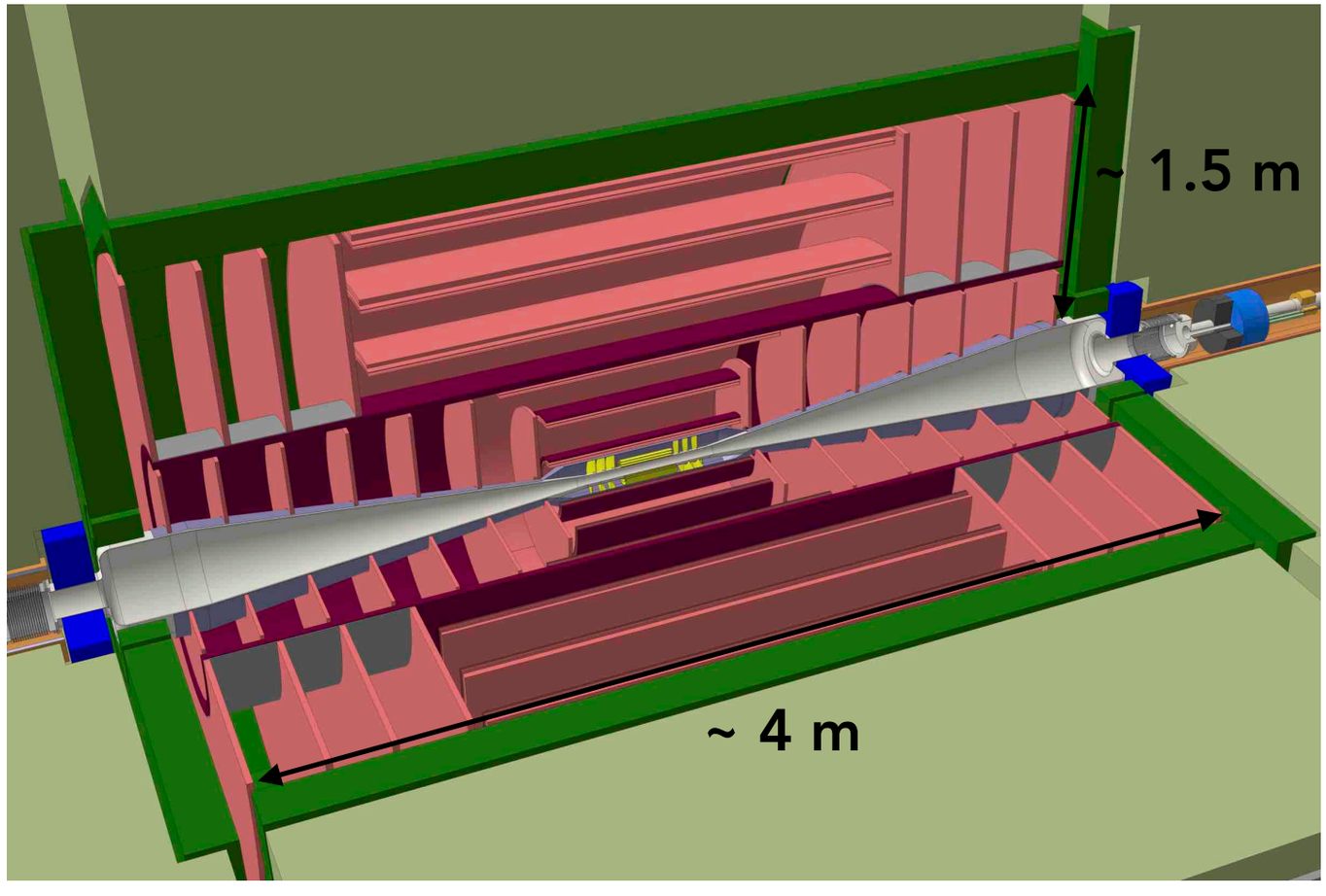


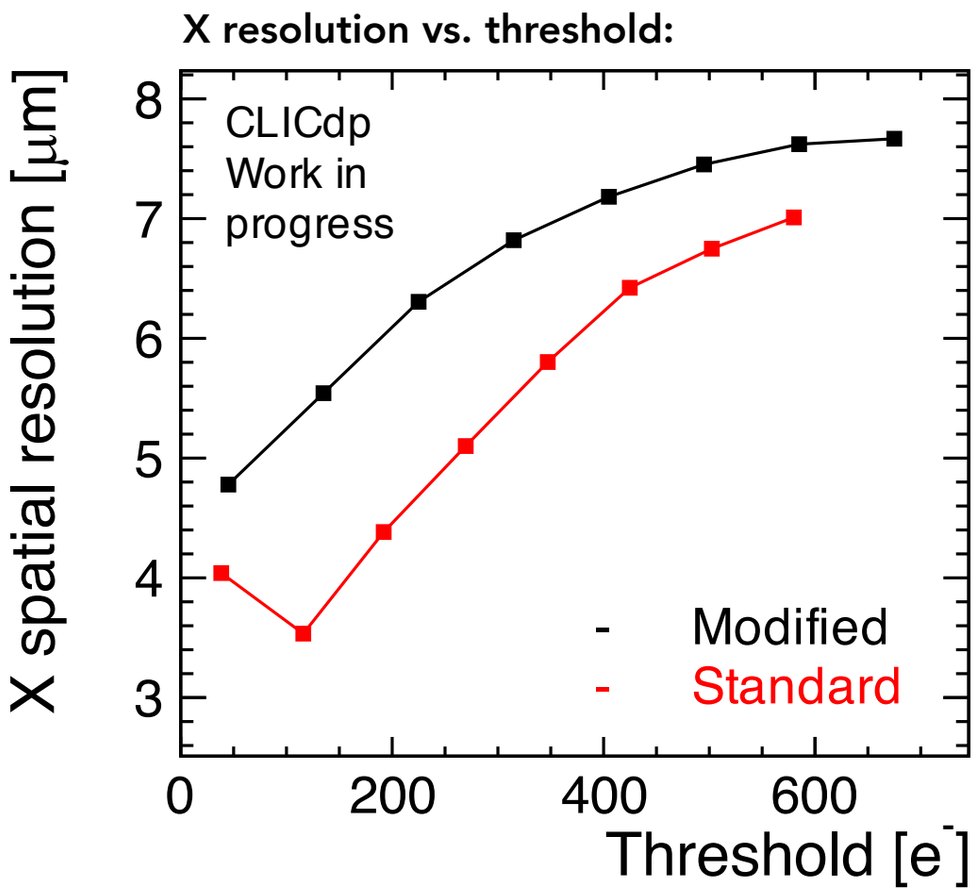
- Dominant contribution from incoherent e^+e^- pairs and $\gamma\gamma$ -> hadrons

CLIC tracker layout:

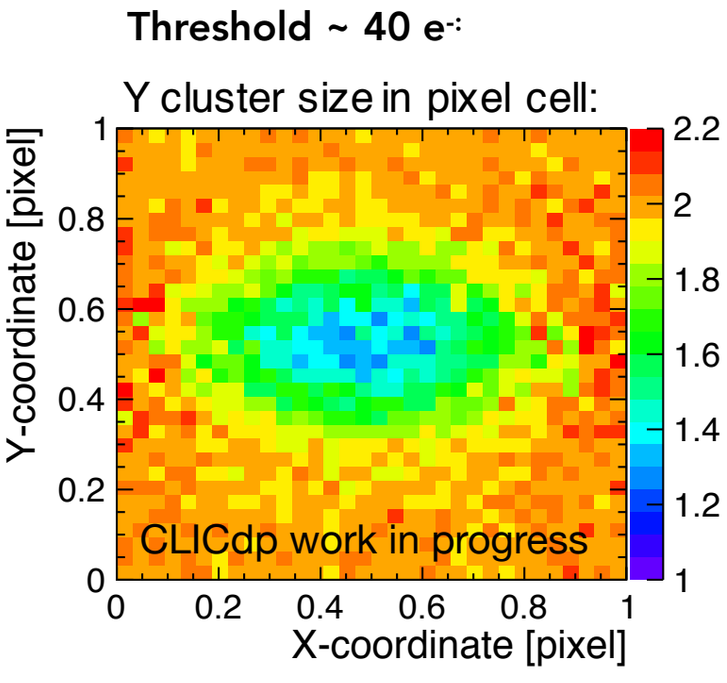
- Large surface ~ 100 m^2 all silicon tracker
- Layout optimised to achieve good coverage:
  - Outer and inner tracker separated by support tube of beam pipe

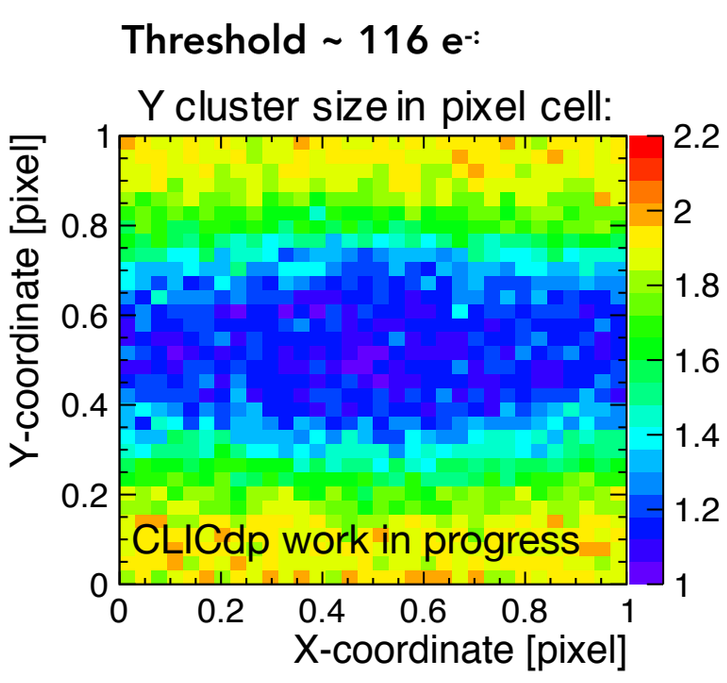
CLIC tracker layout:

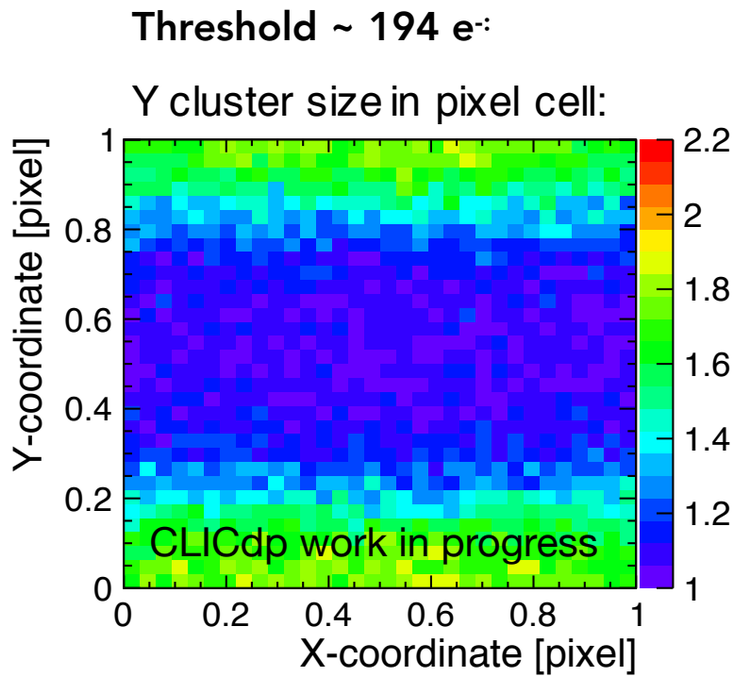




Y-cluster size for the standard process at different thresholds:

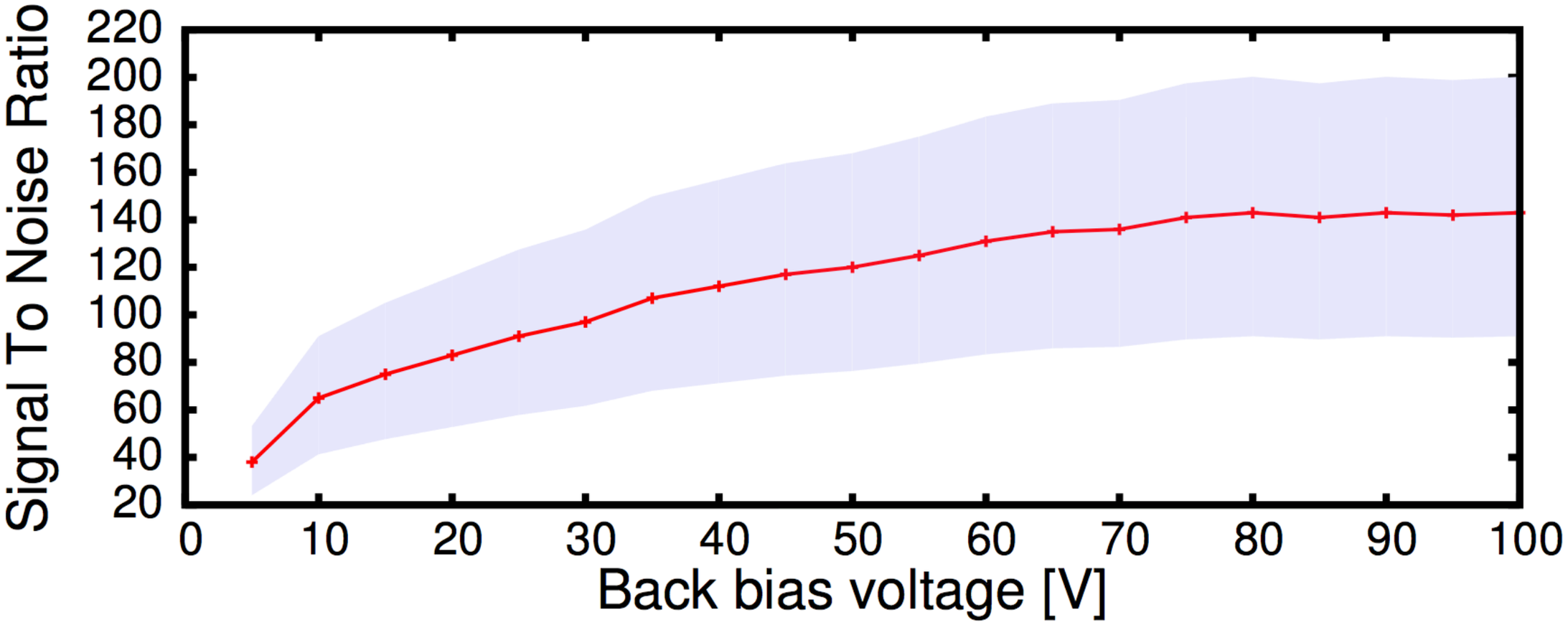






SOI test beam results

S/N variation of for results shown in slide 4.:



SOI test beam results

Comparison single and double SOI on FZ(n) wafer with 500 µm thickness: