

Interface Control Document Template

TPC

Prepared by	Signature
D. Tsionou,....	

Accepted by	Signature
xx TPC integration officer	

Approved by	Function	Date	Signature
Paul Colas, Akira Sugiyama	ILD TPC conveners	Xx/xx/xx	

Summary	The TPC interfaces to SiECAL and VDET are described. Its structure...
Annexes	

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1. INTRODUCTION

1.1. Scope of the document

The purpose of this version of the document is first to assemble all elements that may be relevant for the TPC. The document doesn't claim however neither exactness nor completeness at this stage.

Very preliminary

Note: Unless otherwise against, this document does not address software interfaces.

1.2. Applicable Documents (AD)

Applicable Documents (AD)			
AD	Title	Reference	Version
DBD	ILD DBD	arxiv: 1306.6329	v1
XML	Change in size and small option		
2017			

1.3. Reference Documents (RD)

Reference Documents (RD)			
RD	Title	Reference	Version

1.4. Details of change to the previous design

Indicate (if necessary) the changes compared with the previous version of design. This section may become obsolete but since the reference of the document is the DBD and there are unavoidable changes since then we would like to record them here

- SiECal thickness increased to 223 mm from 185 mm with respect to DBD due to more realistic layer structure. The consequences on the TPC are a small reduction of the radius.

1.5. List of abbreviations

List of Abbreviations

FC	Field Cage		
LV	Low voltage		
HV	High voltage for detectors		

1.6. Nomenclature

Nomenclature

Module	Module with its electronics	Field Cage	Gas-tight double cylinder equipped with a voltage degrader to insure a uniform electric field (figure)
Web	The support of the endcap detector modules	Patch panel	Panel to receive cables/fibres from the detectors and to the concentrators, and from the HV and LV supplies to the detectors.
Membrane	Thin metallized film stretched in the middle of the field cage		

1.7. Block diagram

The Figure 1 shows a primitive block diagram for one column of SiEcal slabs.

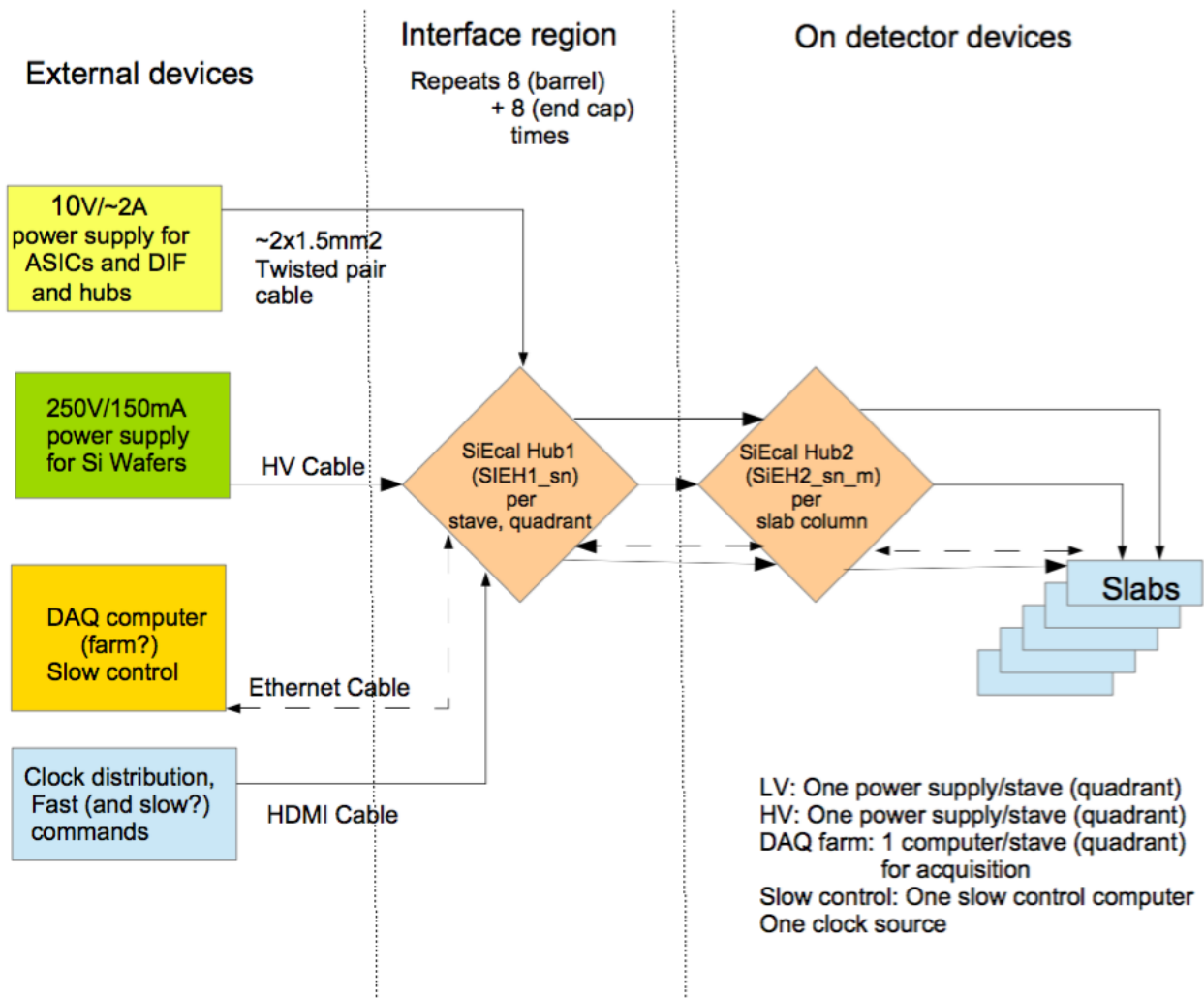


Figure 1 : Schematic view of power distribution and distribution and concentration of other relevant signals and data for one column of slabs.

The cables that arrive or leave from the Hub of type 1 have the following purpose:

- Low voltage power supply for the readout electronics and the powering of the active hubs
 - In going cables
 - 5 V/few A power supply (Voltage drop may not be correctly taken into account)
 - Optical fibre for the signal
- High voltage power supply for the gaseous amplification
 - Standard “red” HV cables (fw 100 V, few nA, in going)
- Optical fibers for data transmission and detector control
 - Out going and in going
- Clock distribution

In the following the interfaces are described:

- Power (the type of power [regulated, unregulated, heating-, number of lines for each type]):

At the Hub1 the power arrives directly from supplies sitting in the electronics trailer,
Low voltage (~5V, few A) for the operation of the readout system
High voltage (few 100V, few nA) for the gaseous amplification device.

- Remote control: control type (relays, digital ...), the number of each type of control:
Layers will be switched off by remote control, in principle the layers should be part of a GPIB bus system of which the master card is integrated. Each master card receives commands via Ethernet.
- Insulation:
Standard HV cables.
- Other interfaces: clock, other instruments, ...
Further interfaces are the clock distribution and transmission of fast commands (both within one micro-HDMI cable), Slow control and a standard Ethernet cable for data transmission to the DAQ computer.

For convenience the original instructions are listed below:

It should indicate all electrical interfaces, including redundancies:

- power: the type of power (regulated, unregulated, heating), number of lines for each type;
- remote control: control type (relays, digital ...), the number of each type of control
- insulation;

Other interfaces: clock, other instruments, ...

1.8. Connection diagram

For convenience the original instructions are listed below:

This is a general wiring diagram showing the names of cables, connectors, equipment, ...

1.9. List of Connectors

- USB type Connector
- Standard HV Connector
- Standard Ethernet Connector
- Standard HDMI Connector

For convenience the original instructions are listed below:

This is a general wiring diagram showing the names of cables, connectors, equipment, ...

For each connector on should indicate:

- The location (eg equipment A);
- the name of the connector;
- type (manufacturer's name + complete reference);
- the general function (eg power ...)
- coded pins, keying;
- the precise limits of the respective supplies;
- the principle of shield connections and grounding policy.

1.10. Cabling and connecting sheets

For every connector and every pin it will be specified:

- the signal type (analog, digital, power, RF, ...),
- the waveform (period, duty cycle, maximum value, minimum value)
- a graphical representation for complex signals (ramp, modulation ...),
- the category (transmitter or receiver)
- the reference of the pinning of the connector,
- the electrical diagram of the interfaced circuit.

1.11. Electrical grounding scheme

A diagram will indicate how are connected or isolated mechanical grounds, shieldings ...
The maximum contact resistance will be defined.

1.12. Power Consumption

(For the following it will be assumed that the Detector Interface (DIF) Cards that are part of an SiEcal layer will be power pulsed as the rest. In this case they will not add significantly to the power budget. Note that this is currently not the case and e.g. the cooling system is based on a steady DIF power consumption between 0.3 and 3 W. Already the lower limit will lead to a permanent current of 643 A in the SiEcal system. This should be avoided!)

The principle of power pulsing implies that the bias currents at the ASICs (and also of the DIF cards?) are enabled with a duty cycle of 1%.

The total average electrical power consumption is about 1.6 kW. The barrel is expected to consume between 1.2kW and the end caps about 0.4 kW.

The peak power consumption is therefore about 100 times higher.

The peak current in a detector layer is of the order of 10 A (around 7080 layers exist in total). However, the external connections and power supplied are not affected since the power pulsing will be realized via large capacitances (typically super capacitances of 400 mF with 16 mΩ ESR). In the current scheme the capacitances will be located on top of each column of slabs.

Note finally that bias voltage to the silicon wafers does not add significantly to the power budget (O(10 W)).

1.13. Other electrical interfaces

For the moment we use this section to describe what is inside the electronic trailer.

- HV power supplies
- 16 LV power supplies (type Lambda devices)

- Computer Farm (typically 16 DELL Poweredge),
- Connected to central storage of Central DAQ system for event building?
- Alternative direct SiECal data immediately to central DAQ system

For convenience the original instructions are listed below:

This section defines all other electrical interfaces (clock s, other instruments ...).

2. GENERAL DESCRIPTION OF SUBSYSTEM

The TPC is a gas-tight vessel at atmospheric pressure closed by 2 endplates carrying the detector modules.

Several options are retained during the R&D and costing periods. The baseline radius, and a reduced radius (so-called ‘small’ option). The segmentation of the baseline option can be in 4 or 8 “wheels” depending on how large can be the modules, and 3 to 6 wheels for the small option. Several technologies are under study.

3. GENERAL INTERFACE DESCRIPTION

The following items are considered:

Dimensions

Mechanical interface : support of the TPC and support of the ISS and Vertex Detector in the TPC.

Matter obstruction for the calorimeter (thickness of the FC)

Services (cooling, LV and HV supplies, signal)

Very High Voltage for the field cage.

Gas for the TPC.

4. MECHANICAL INTERFACE

The TPC is supported by 2x3 ribbons...

5. ELECTRICAL INTERFACE

The guiding line for the TPC is to have as few connections to the outside world as possible. There will be one or a few HV and LV cables per module, and optical fibres for the signal and the electronics settings. To ease the separation of the detector from the supplies and concentrators, there will be patch panels on each side (A and B).

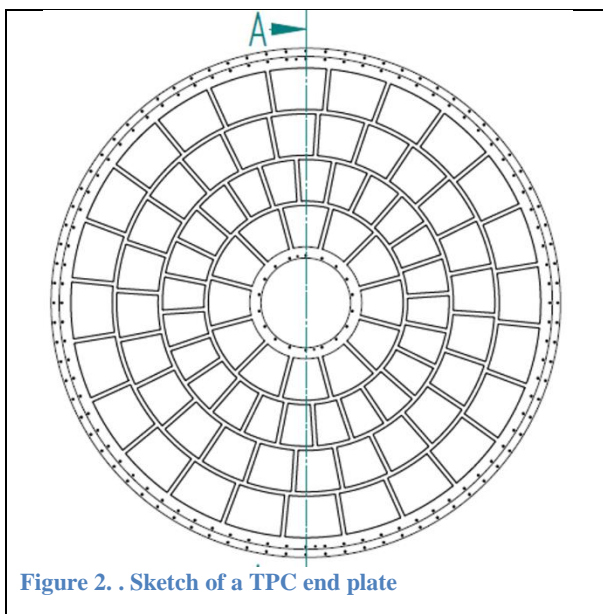


Figure 2. . Sketch of a TPC end plate

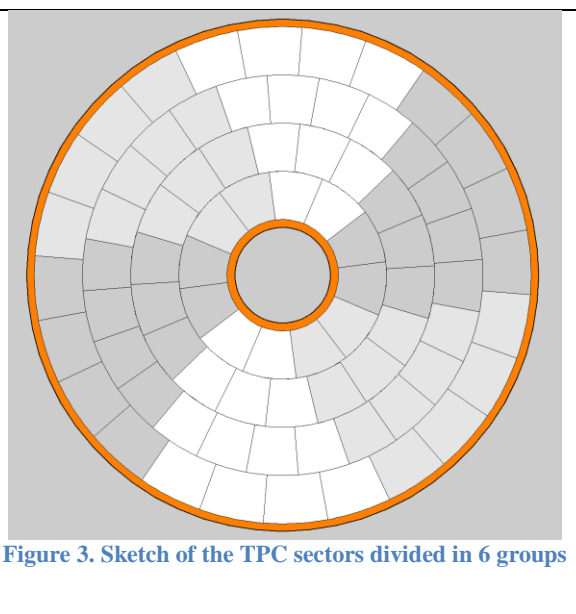


Figure 3. Sketch of the TPC sectors divided in 6 groups

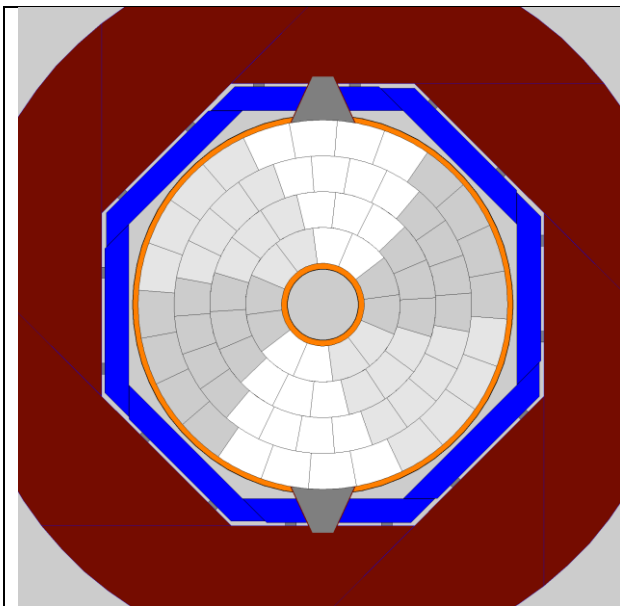


Figure 4. The TPC is shown hanging from the HCal. The ECal barrel is also represented with its rails.

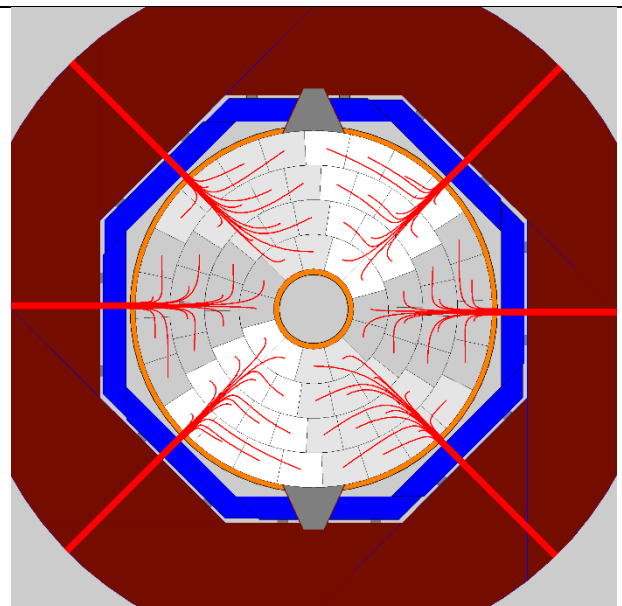


Figure 5. Getting the services out of the TPC. An example.

6. FLUID INTERFACE

If the 2PCO₂ cooling solution is retained, the cooling fluid will be circulated in 1mm diameter pipes in the modules (or the PCB will be equipped with microchannels), under a pressure of 50 to 100 bars.

- the flow,
- the purity constraints of the fluid.

1.14. Gas system Interface

The detector gas mixture will be brought and expelled by 2 cm diameter pipes.

1.15. Liquid system Interface

The information here and in Sec. 8 are extracted from a detailed study of the cooling system that is available under [xxx].

The TPC will be cooled by a diphasic CO₂ system. A compressor is located outside *about 30 m off the beam axis of the ILD Detector* and the cooling fluid will be brought to and away from each endplate. From there it is further distributed to the individual modules by manifolds. Possibly several modules (maybe four?) can be served in series.

Error! Reference source not found. shows the general concept of the cooling system.

7. THERMAL INTERFACE

For the subsystems:

- Thermal dissipation: in and out of operation

The SiECal will evacuate all its produced heat by means of the cooling system. The only sources of heat dissipation are the cooling pipes in which water with a temperature of around 20°C will be flowing. Out of operation there is no heat dissipation at all.

- Limit temperatures: during standby mode, for switching power, in operation 60 °C.

8. INTERFACES FOR DETECTOR TESTING

These are the specific interfaces related to the test equipment:

- MSE interfaces: mechanical assembly test ... ;
- ESE interfaces: electrical interfaces with the test and verification systems;
- OSE interfaces: reference cubes, or targets for the surveys ...

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