VTX: Technological status and ongoing studies

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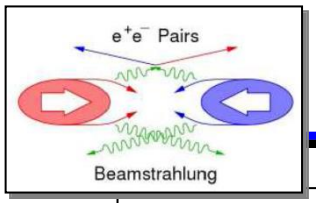
With inputs from Marcel Vos, Akimasa Ishikawa and VTX R&D groups
(thanks also to L.Andricek, K. Hara)

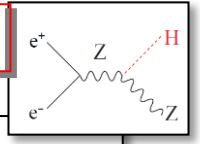
- Technology R&D status
  - Requirements
  - DEPFET
  - CMOS
  - FPCCD
  - SOI
- Miscellaneous open questions
  - Cooling, beam background, Faraday cage

Technology R & D

Reminder: VTX requirements

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$



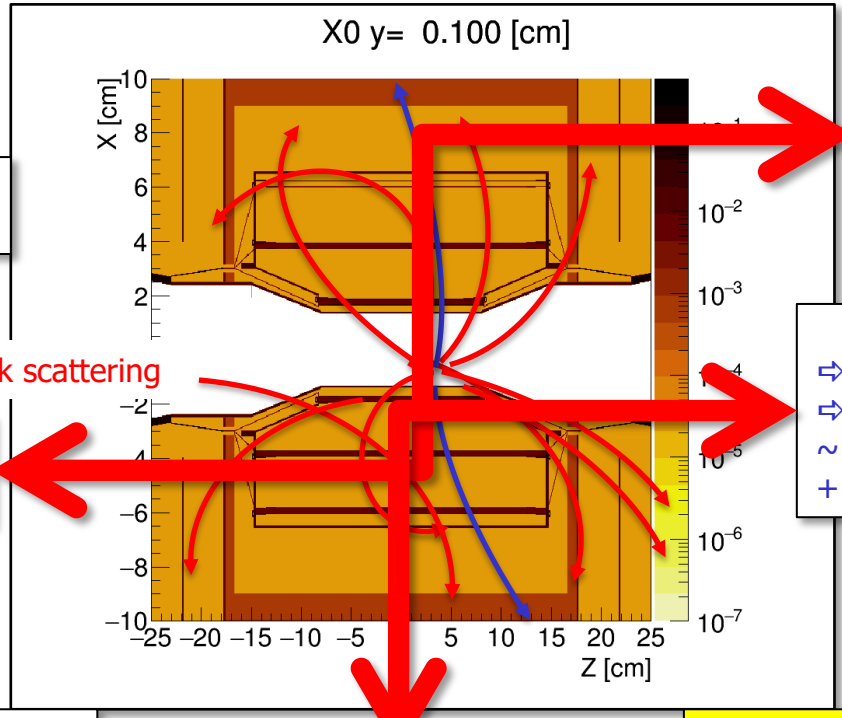


Physics
⇨ Flavour tagging
⇨ Low pT tracks

Beam background

Physics (<Hz/cm²)

Beam background (~ 5 hits/BX/cm² on layer 0)



Vertex reconstruction
⇨ granularity
⇨ Pitch ~17 um
⇨ (σ_{sp} ~3 um)

Radiation hardness
O(100kRad/an) & O(10^{11})neq/an

Rad.Tol. devices

Material Budget
⇨ ~ 0.15% X_0 / layer
⇨ < 1% X_0 for the whole VTX
~ 900 μm Si
+ ~0.14% X_0 for the beam pipe

Read-out speed
O(1-10 μs)

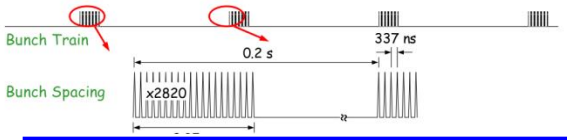
Power consumption
~< 50mW/cm²

Fast read-out & low Power architectures

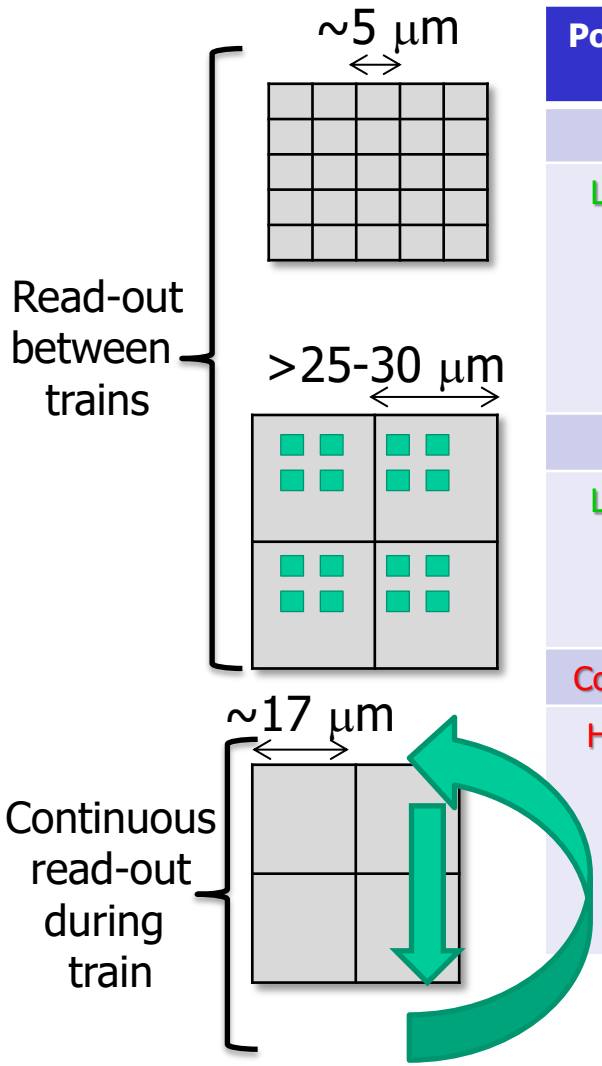
Cooling
Stiffness / Alignment

Low material detectors & supports structures

Challenge : meet the requirements all together



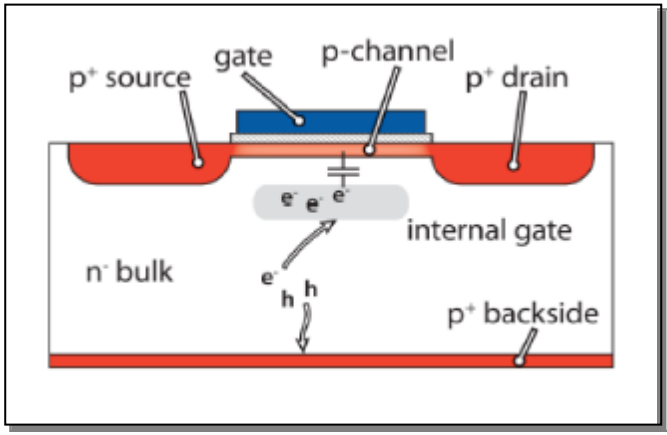
Read-out strategies vs resolution/occupancy

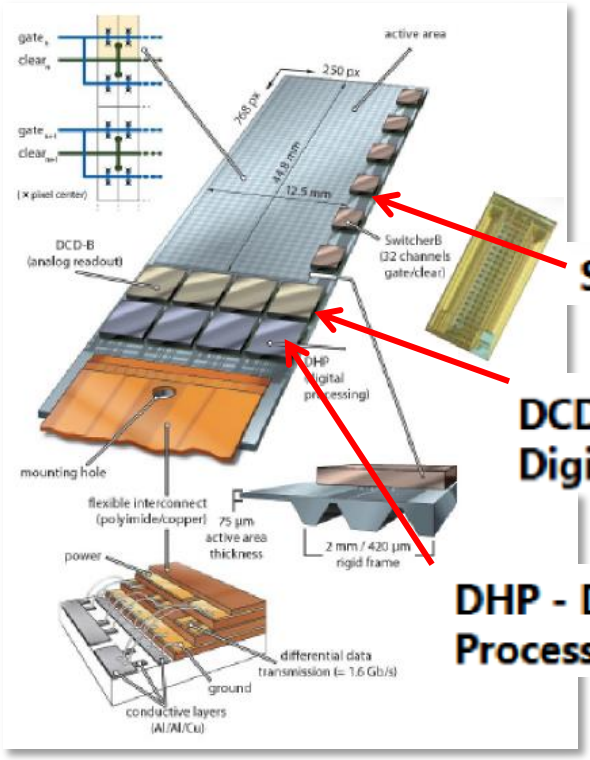


Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^5 grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.
⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

DEPFET





SwitcherB - Row Control

DCDB - Drain Current Digitizer

DHP - Data Handling Processor

DEPFET pixel:

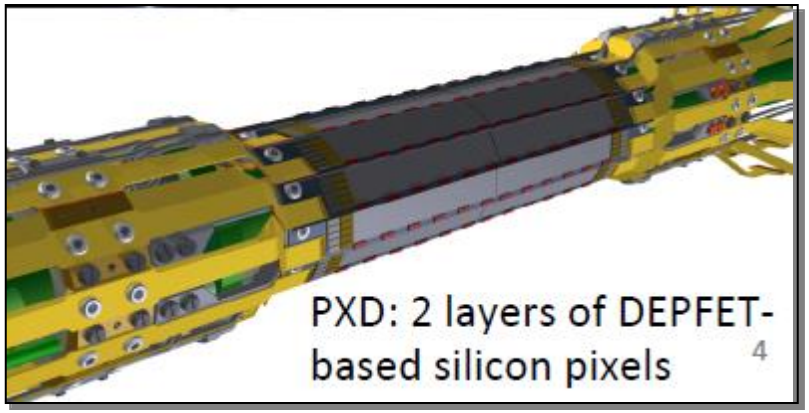
- Pixel = p-channel FET + full depletion bulk
- Internal gate capacitively coupled to FET gate
- Clear process to remove stored charges
- Rolling-shutter read-out

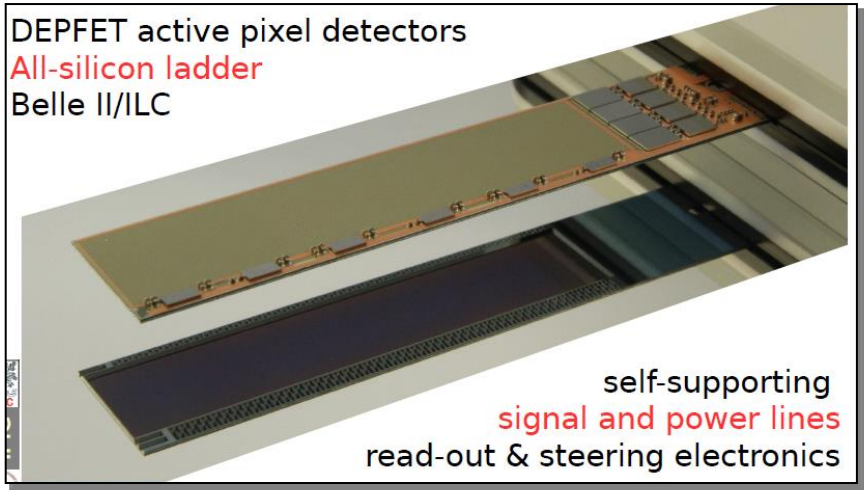
Detection and internal amplification

Small intrinsic noise

Low power consumption

DEPFET for Belle II PXD





DEPFET PXD	L1	L2
# ladders	8	12
Distance from IP (cm)	1.4	2.2
Sensitive thickness (μm)	75	75
#pixels/module	768x250	768x250
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (μm²)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Total sensitive Area (cm²)	89.6	176.9

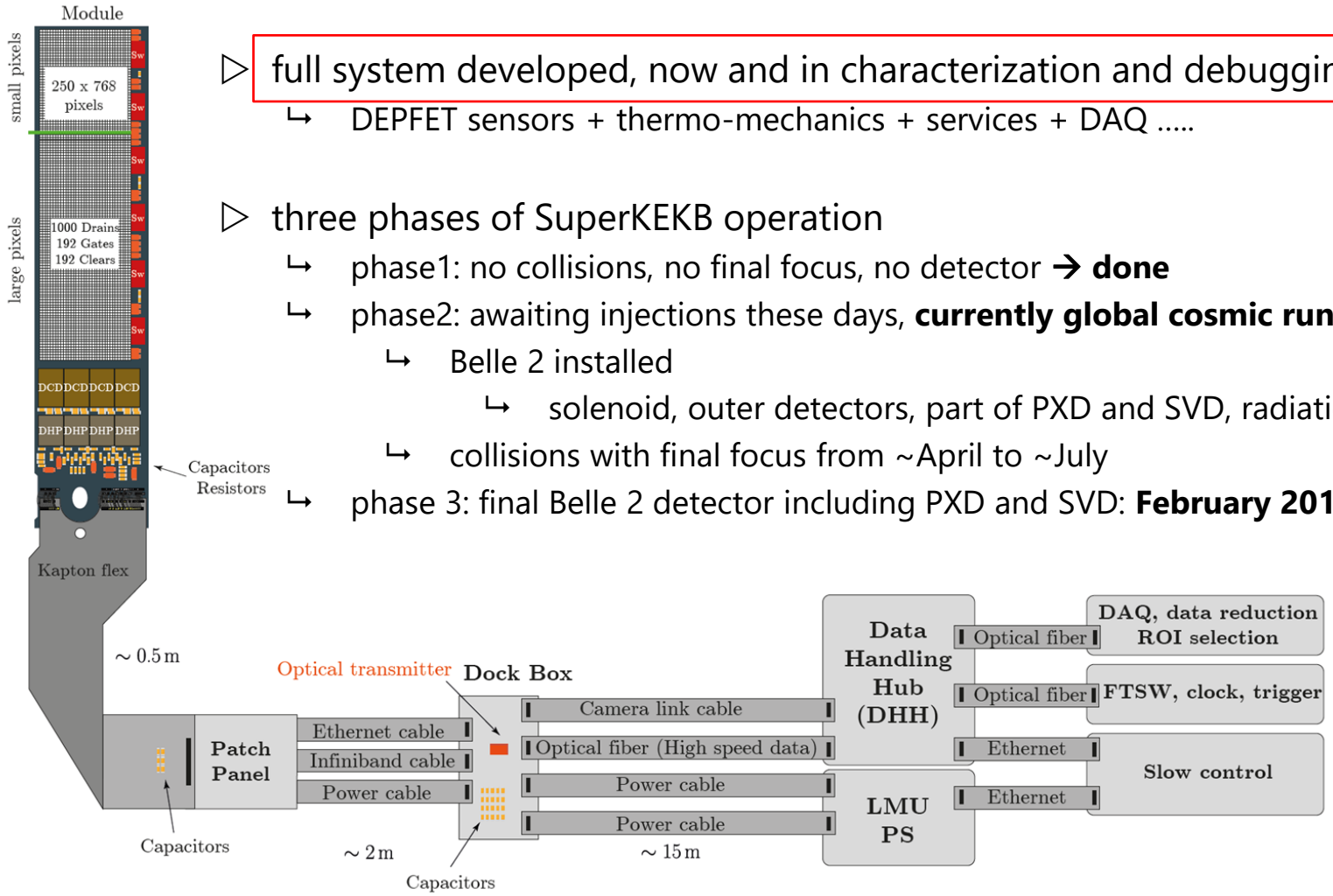
	Belle II PXD
Occupancy	0.4 hits/μm²/s (< 3%)
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Frame time	20 μs
Momentum range	~ 70 MeV - few GeV
Angular acceptance	17° - 155°
Material budget	0.21% X_0 per layer
Resolution	15 μm (50×75 μm²)

DEPFET PXD Status

- DEPFET collaboration is in the final phase of construction of the Belle 2 PXD
  - two layer pixel detector: 20 ladders, ~8 Mpx, 20µs readout time

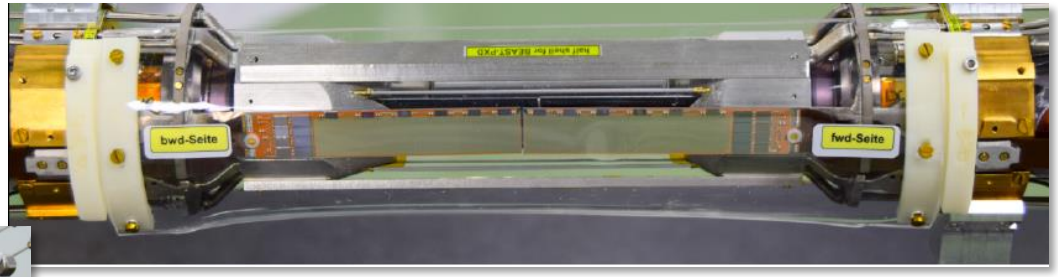
- full system developed, now and in characterization and debugging phase
  - DEPFET sensors + thermo-mechanics + services + DAQ .....

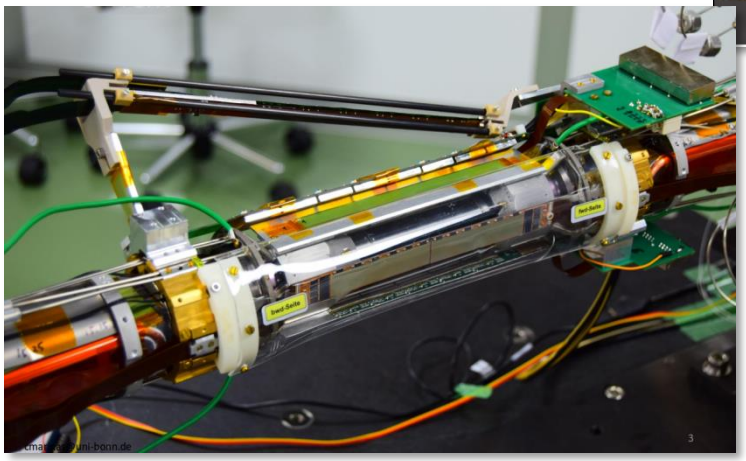
- three phases of SuperKEKB operation
  - phase1: no collisions, no final focus, no detector → **done**
  - phase2: awaiting injections these days, **currently global cosmic run ongoing**
    - Belle 2 installed
      - solenoid, outer detectors, part of PXD and SVD, radiation monitors
    - collisions with final focus from ~April to ~July
  - phase 3: final Belle 2 detector including PXD and SVD: **February 2019**



BEAST (beam commissioning)

- Motivation
  - Machine commissionning and beam parameters optimization
  - Check rad. safety for VXD
- Beast II installed in the VXD volume
  - 4 PXD Modules DEPFET
  - PLUME ladders
  - Other radiation monitors

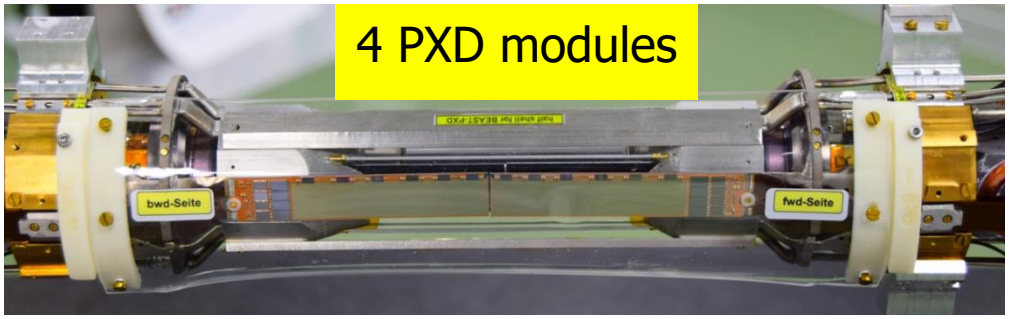


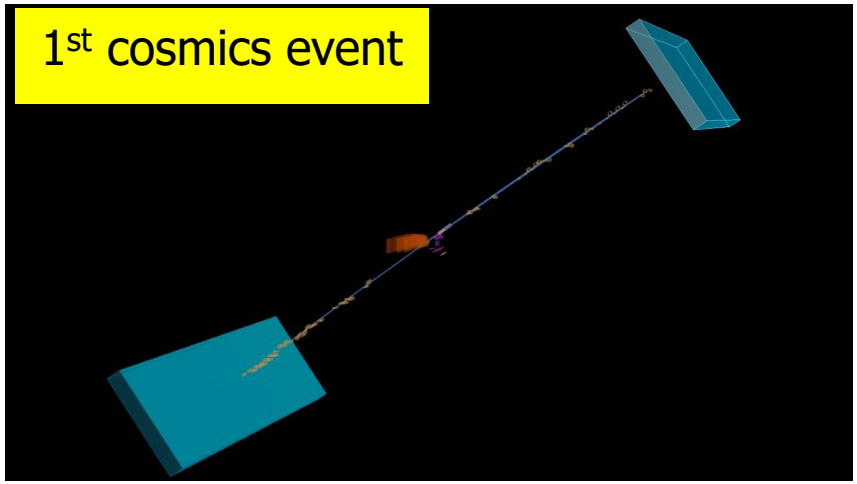


First collisions: March 2018 (until June/July 2018, int. lumi. ~ 20 fb^{-1})

PXD @ phase 2

- 10% of final PXD (4 modules in final configuration)
- installed into IR of Belle 2
- cosmic data taking ongoing





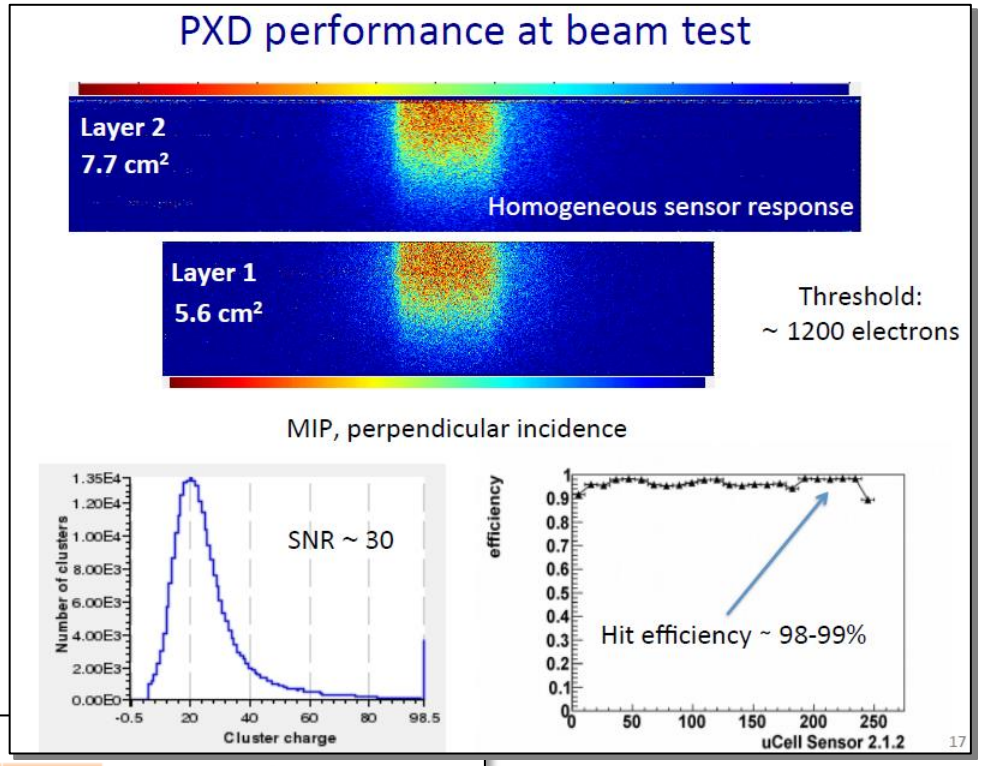
towards phase 3 (Final BelleII detector)

- Module and ladder production ongoing
  - main module production almost done
  - L1 ladders done, L2 ladder in progress
  - full PXD to be at KEK in June 2018

8 ladders for PXD L1

PXD milestones

- VXD combined beam test
  (@ DESY e^- 4 GeV beam in 2017)
  - 1 T solenoid field
  - Full acquisition chain
  - Belle II Slow control
  - CO_2 cooling
- Performances validated
  - Homogeneity response
  - SNR ~30
  - Hit efficiency ~ 99%
- Production



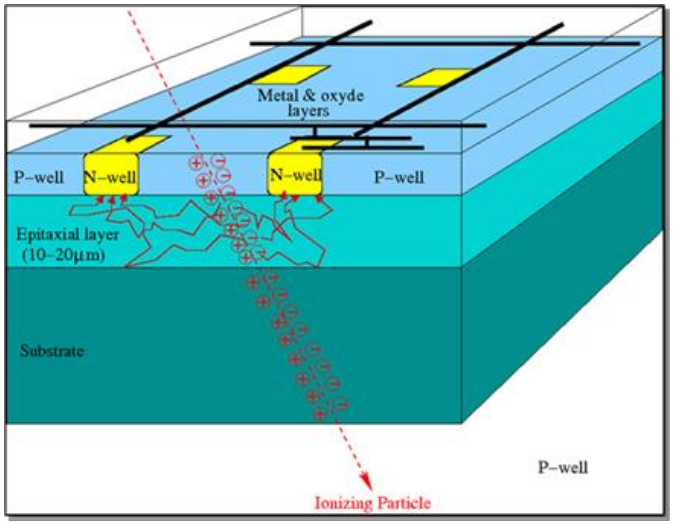
Sensor production status

	REQ	G99	G98	G95	M99	M98	M95
Inner Forward	8	17	3	0	1	0	0
Outer Forward	12	26	6	2	3	1	0
Outer Backward	12	22	3	1	4	0	0
Inner Backward	8	13	3	0	3	1	0

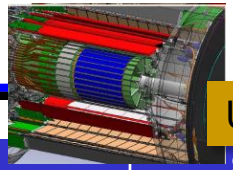
G: good
M: medium
B: bad
The number behind gives the minimal percentage of live pixels on the sensor

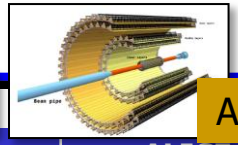
- Belle II
  - PXD @ KEK June 2018
  - Data taking early 2019

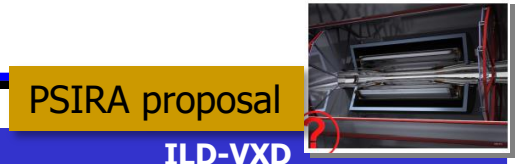
CMOS Pixel Sensors (CPS)



Evolving CPS



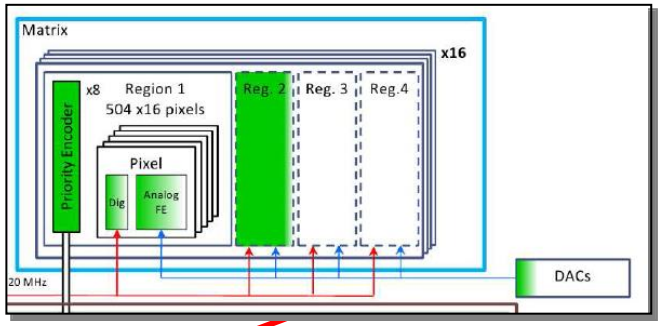


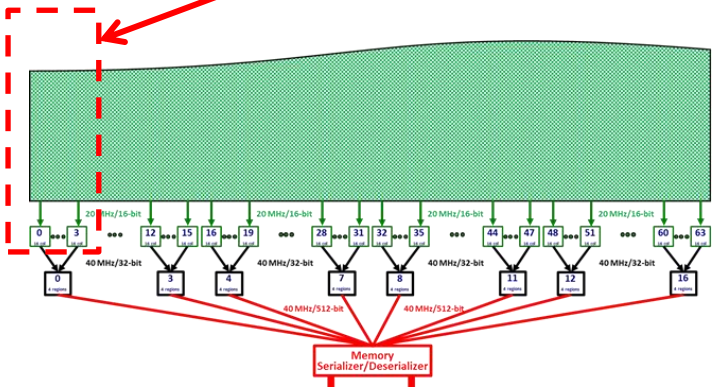


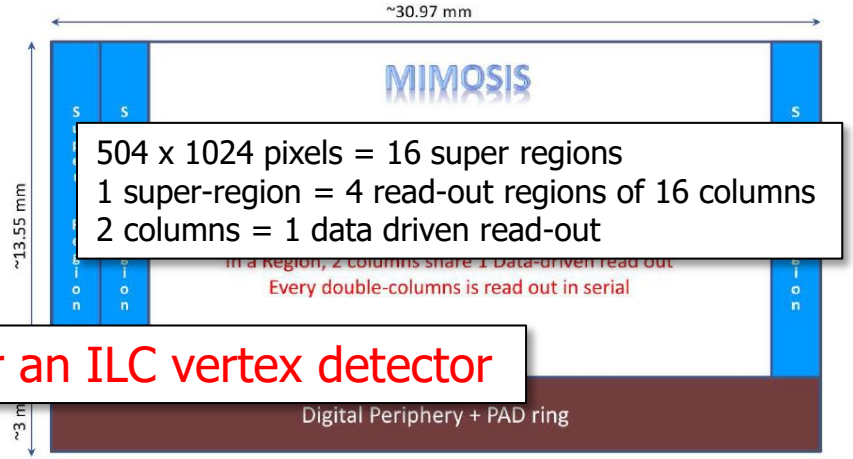
	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35	**0.18 μm**	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	**Asynchronous r.o.** **In pixel discri.**	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm²) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 18 x 18 / ~ 3 (inner) ~ 22 / ~ 4
Time resolution (μs)	~185	**5-10**	5	**1 - 4**
Data Flow		~10^6 part/cm²/s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7 x 10^5 /mm²/s **>2 Gbits/s output** **(20 inside chip)**	~375 Gbits/s (instantaneous)
Radiation	O(50 kRad)/year	2x10^{12} n_{eq}/cm² 300 kRad	3x10^{13} n_{eq}/cm²/yr & 3 MRad/yr	O(100 kRad)/year & O(1x10^{11} n_{eq}(1MeV)) /yr
Power (mW/cm²)	< 150 mW/cm²	**< 35 mW/cm²**	< 200 mW/cm²	~ 50 mW/cm²
Surface	2 layers, 400 sensors, 360x10^6 pixels 0.15 m²	7 layers, 25x10^3 sensors **> 10 m²**	4 stations Fixed target	3 double layers 10^3 sensors (4cm²) 10^9 pixels ~0.33 m²
Mat. Budget	~ 0.39 % X_0 (1st layer)	~ 0.3% X_0 / layer		~ 0.15-0.2 % X_0 / layer
Remarks	1st CPS in colliding exp.	(with CERN)	. Vacuum operation	Evolving requirements

MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - Back from foundry
  - Test under preparation (2018)
  - Test pixel Radiation hardness and priority encoder frequency
    - Radiation hardness design (SEU)
    - Testability
- MIMOSIS-1: 1st prototype of complete sensor
  - (sub. Q2 2018)
- MIMOSIS-2:
  - (sub. Q2 2019)
- MIMOSIS-3: final pre-production sensor
  - (~2020)







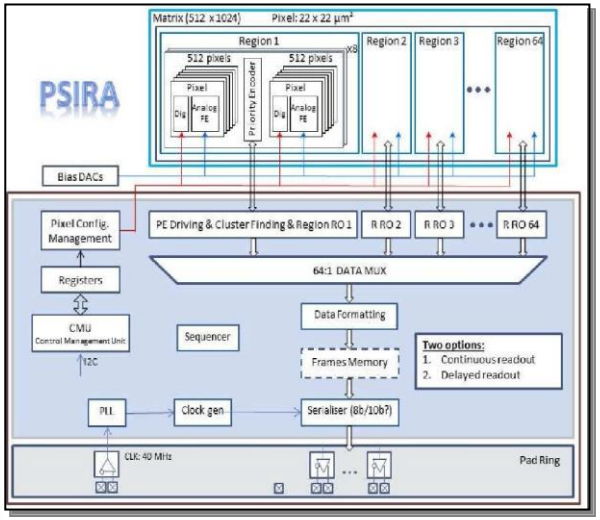
⇨ architecture adaptable to a fast sensor for an ILC vertex detector

Extension of MIMOSIS to ILC vertexing and tracking

- Conservative approach
  - Minimize changes w.r.t. MIMOSIS
    - Keep TJ 0.18 μm technology & a similar architecture
  - 2 sub-systems targeted
    - Vertex detector & Silicon inner trackers (SIT @ ILD)
  - Performances targeted
    - ~ 20% better spatial resolution (vertexing)
    - Read-out time: 2-4 μs (ILD-VXD) and 1 μs (ILD-SIT)
    - Faster = higher Power consumption

⇨ PSIRA

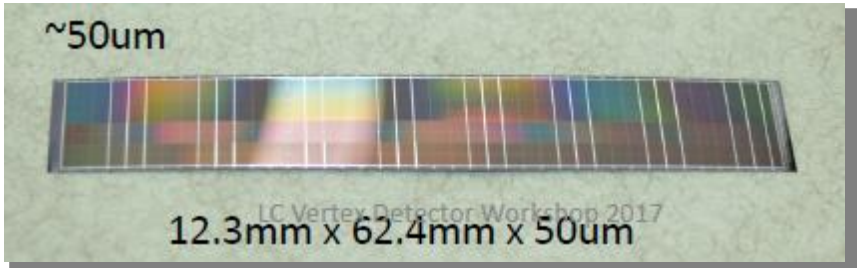
⇨ Finalize CPS ~2025



- Expected Performances
  - σ_{sp} ~4 μm ⇨Use double sided ⇨ σ_{sp} ~2.8 μm
  - Signal peaking time ~ 2 μs
  - Single pixel adress read-out = 50 ns
    - (with 20 MHz clock)
  - Sustainable occupancy (~5 pixels/hits)
    - ~ 4 hits/region/μs ~ 100 hits/cm²/μs
- Explore smaller feature sizes 180 nm ⇨110 nm
  - Motivations
    - Smaller pixel dimensions & faster read-out
    - Reduced power consumption

- Elementary read-out region:
  - 8 pairs of columns (512 rows)
  - Pitch 22 x 22 μm² ⇨ region ~ 4 mm²

⇨ Smaller feature size offers opportunities to get closer to ILC bunch tagging



FPCCD

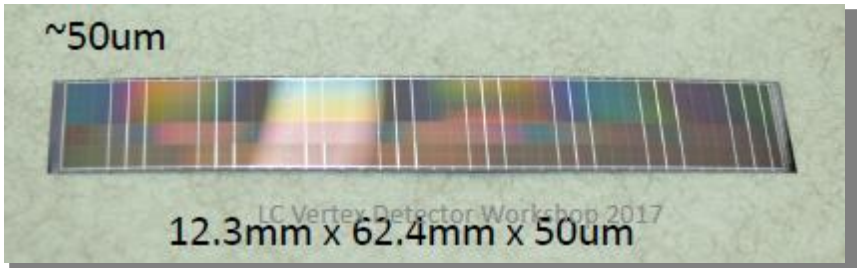
- Fabricated by Hamamatsu
- Able to provide small pixel size (~5 um) over large surface
- Thin, double layer structures
- Needs cryostat to operate (-40°C)
- Low power readout ASIC

FPCCD

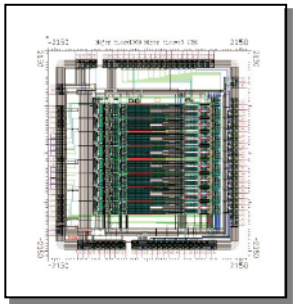
- Prototypes
  - Small scale
    - Different register sizes
    - Performance studies
  - Large Scale

Real size sensor for 1st doublets 12.3mm x 62.4mm

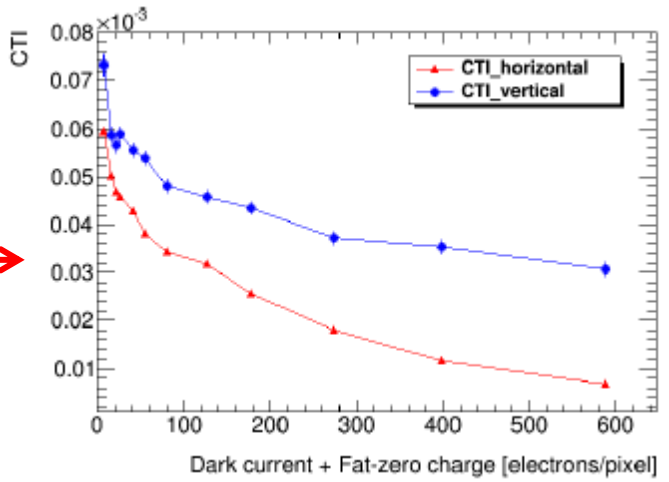
125 x 13000 pixels with 16 readout node



- Readout chip
  - 3 prototypes fabricated
    - 8 bits ADC
    - 10 MHz, 6 e- noise, < 6mW/channel

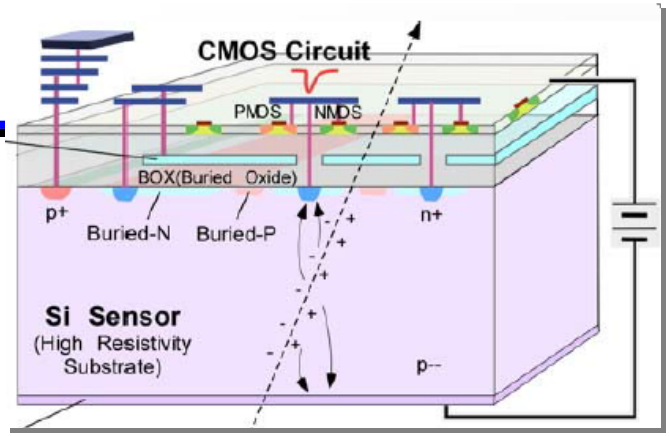


- Neutron irradiation test
  - Up to Fluence: $1.78 \times 10^{10}\ n_{eq}/cm^2$
  - Charge Transfer Inefficiencies
    - Improved by Fat-zero charge injection →

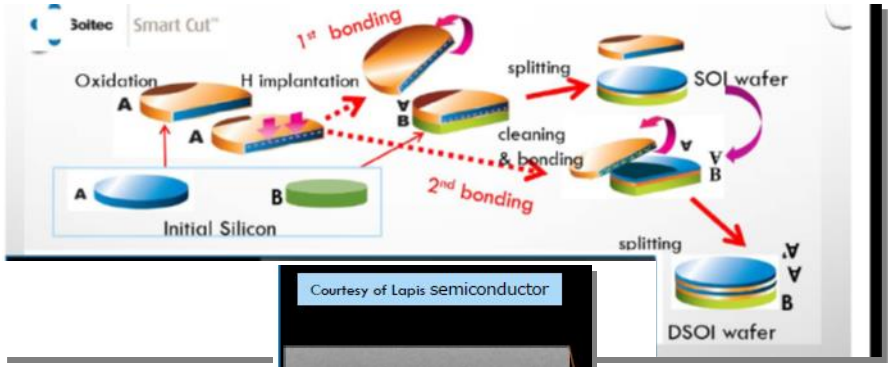


SOI

SOI



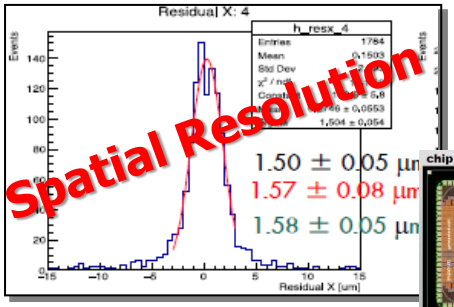
- Silicon On Insulator (SOI) added values
  - Monolithic
  - Room temperature operation
  - Can chose substrate & circuitry « independantly »
    - Full depletion
    - Potentially high density circuitry
    - Potentially 3D
  - Well suited for a time stamping read-out strategy
    - Time & signal memories while keeping pitch small
- Double SOI →
  - Solves back-gating, trapping & cross-talk
  - Improve radiation tolerance
- Challenge
  - Accessibility to the technology options

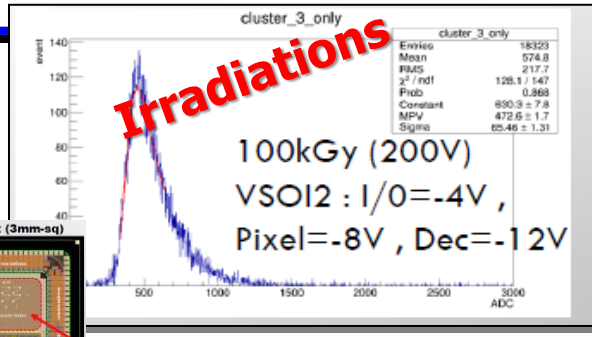


(K. Hara Vertex 2017)

SOI (cf Hara @ VERTEX 2017)

- Prototypes : (different wafers explored)
  - FPIX2 (8μm pitch, 128x128)
    - Test spatial resolution (charge spread)
    - Test Radiations hardness
  - SOFIST V1
    - Analog signal memories
    - Tested in beam
  - SOFIST V2
    - V2: 0 suppr. Logic
    - time stamp memories
  - SOFIST V3:
    - 3 time & signal memorie
    - 1MGy achieved



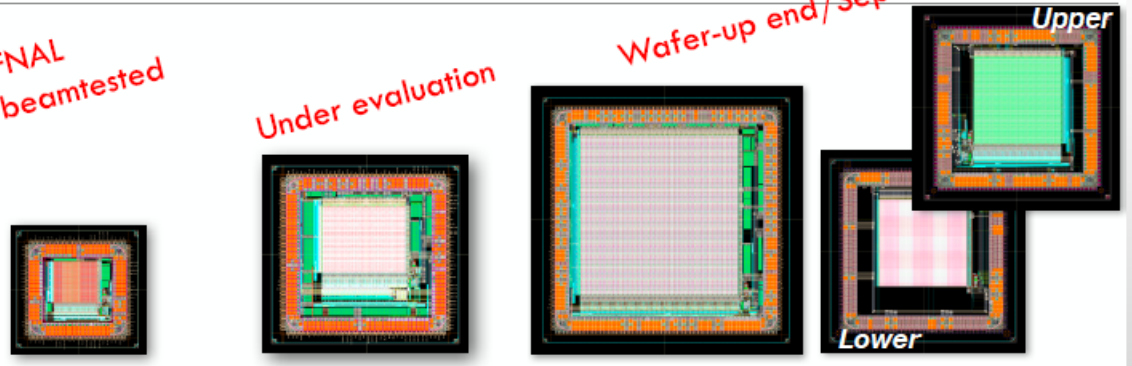


- 3D stacking being investigated

Lower pixel
- Pre-amp
- Comparator

Upper pixel
- Shift-register
- Analog memory x3
- Timestamp x3

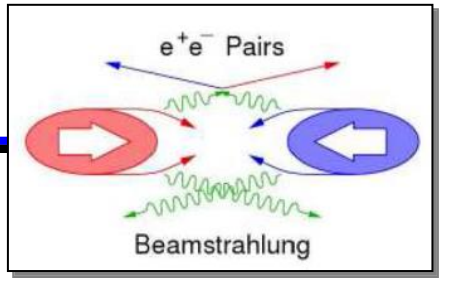
	MX1850	MX2040	MX2166	
SOFIST	ver.1	ver.2	ver.3	ver.4 (3D)
	FNAL beamtested	Under evaluation	Wafer-up end/Sept.	



Chip Size (mm^2)	2.9 x 2.9	4.45 x 4.45	6 x 6	4.45 x 4.45
Pixel Size (μm^2)	20 x 20	25 x 25	30 x 30	20 x 20
Pixel Array	50 x 50	64 x 64 (Time Stamp) 16 x 64 (Analog Signal)	128 x 128	104 x 104
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF x 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ-cm)	2≤	1≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Under evaluation	Delivered (Jan. 2017)	Submitted (Jun. 2017)	Submitted (Jun. 2017)

Miscellaneous open questions

Beam background



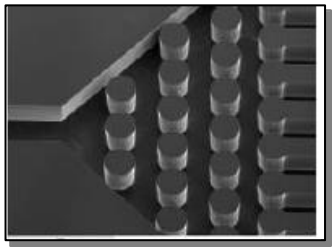
- DBD ~5 hits/cm^2/BX on first layer

5 part/cm^2/BX ⇨17x17 μm^2 pitch, cluster mult. ~5, 50 μs read-out time @ 0.5TeV on Layer 1 ⇨ ~ 1 %

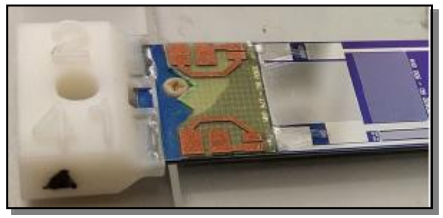
- Recent estimates not necessarly consistent between each other
  - Safety factors are mandatory ! (~x5)
- √s = 500 Gev ⇨ √s = 250 GeV ~ factor 2.
  - Partly compensated by enhanced luminosity
- Backscattered particles
  - Typically ~< 20% of the total background
    - Anti-DID choice NOT governed by VTX occupancy
- Joined effort with SiD could be useful
  - Define common plots to facilitate comparisons ?
- See dedicated Claude Vallée's talk

Cooling options

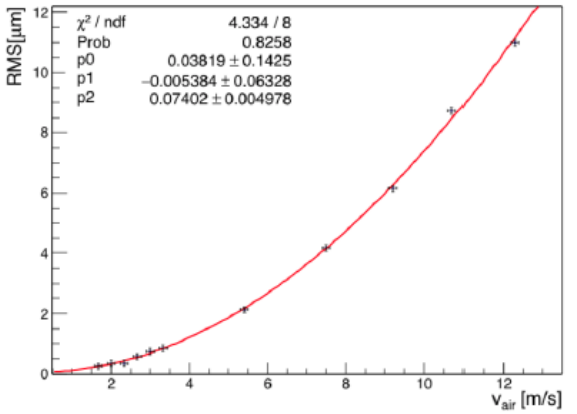
- Technology dependent (Room temp. OR -40°C operation)
- Air cooling
  - STAR HFT: (P ~150 mW/cm^2), air flow ~9 m/s
    - No alignment issue (lower requirements w.r.t. ILC)
  - Belle II mock-up studies



- Micro-channel cooling
  - NA62 GigaTracker (working), LHCb VELO upgrade, etc.
  - (AIDA, Bonn, MPG-HLL, IFIC) ⇨ MCC for DEPFET in the handle wafer
    - Thermo-mechanical studies, connectors, gluing, leaking tests, etc.



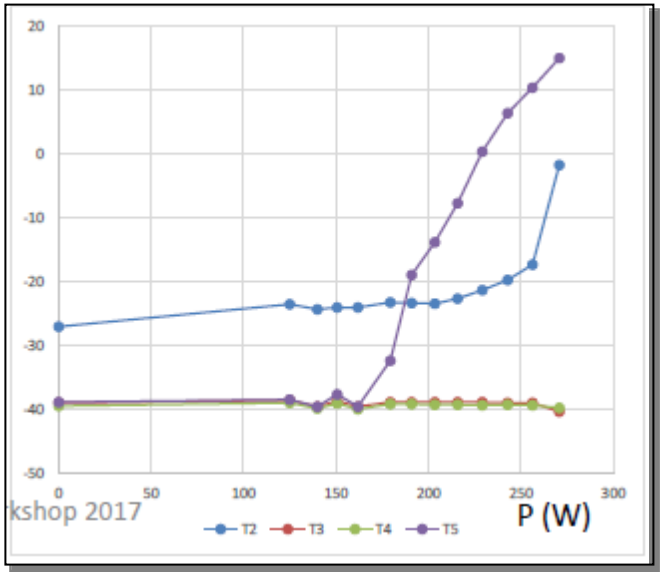
  - Results : very efficient local cooling
    - Up to ~ 25 mW/cm^2 for $\Delta T = 10^o$
    - (mono-phase cooling liquid)
  - Goal: extend cooling capabilities to the whole module

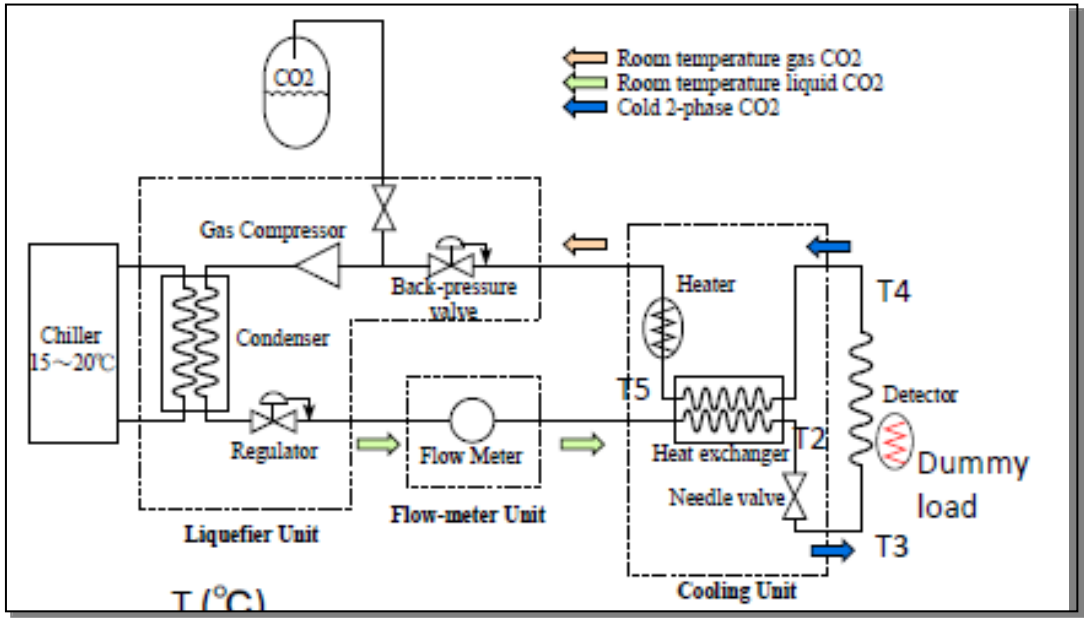


Cooling (FPCCD)

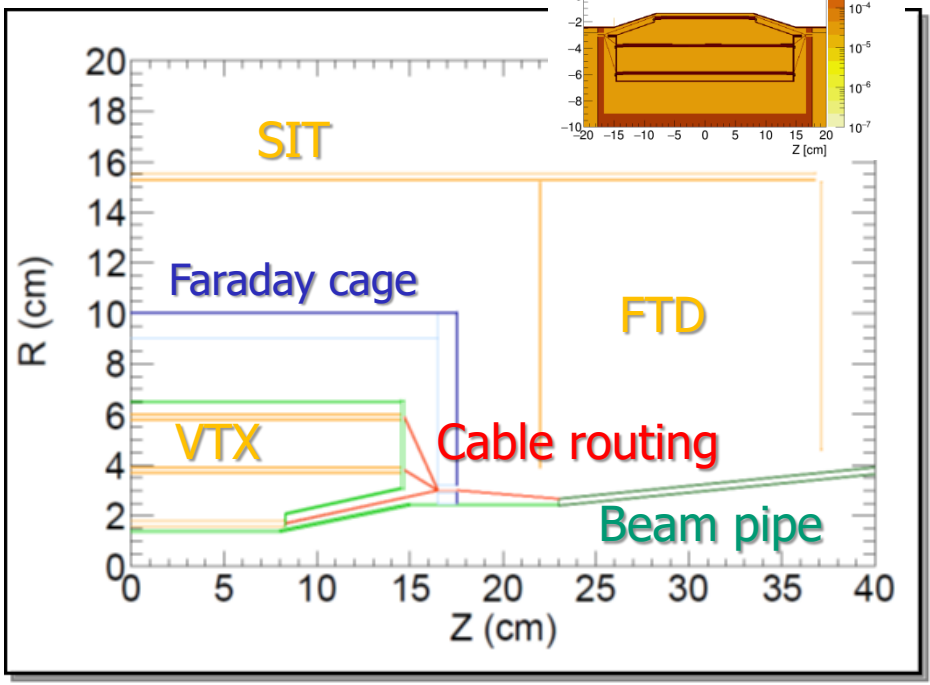
- Cryostat and Liquid CO_2 (and gas N_2) cooling system
  - Should be cool down to –40° C⇨ Cryostat (styrofoam + CFRP)
  - Inter-train readout → Larger power consumption than CMOS/DEPFET
  - About 50W inside the cryostat, about 200W junction box
- Gaz compressor system
  - Don't need strict thermal insulation for transfer tubes

Cooling power measurement using dummy load





The Faraday cage



- Faraday cage role
  - Stopping e.m. waves with an hermetic cage
    - See shielding effect next slide
    - Doesn't protect from internal noise source !
  - 500 μm aluminium (+ styrofoam cryostat)
    - ~ 0.55%X0 (+0.05%X0)
- Requirements
  - Electric continuity mandatory
  - Connexion to the mass mandatory
    - Connexion to the TPC ?
  - Any holes reduces its efficiency
    - Holes / cables (Cooling, Power, Data, control)
    - Propagation through cables
    - Small holes always better

⇨ Any change in the cable routing needs to be evaluated

- Questions
  - Radius of the Faraday cage ?
    - Can it be reduced ? Air flow cooling ?
  - Isolate/Shielding beam pipe with gold ?
    - 20 μm Au = 0.6% X_0 (beam pipe ~ 0.15% X_0) ⇨ Too much material
    - 25 μm thin foil of titanium against background from synchrotron radiation ?
  - E.M. spectrum ?
    - ~100 kHz – 100 MHz ?

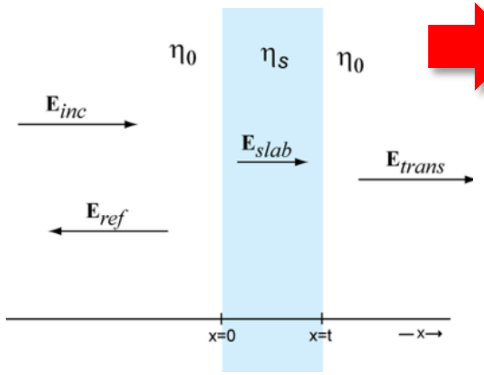
⇨ Cf Dr. Fernando Arteche talk @ Ringberg workshop, (ITAINNOVA Aragòn)

Faraday cage, Skin effect, Shielding effect

- Shielding effect (S.E.) in dB

$\eta_0 = \sqrt{\mu_0/\varepsilon_0}$ is the intrinsic impedance of free space (~377 ohms).

$$|\eta_{cu@100\,MHz}| = \sqrt{\frac{2\pi f\mu}{\sigma}} = \sqrt{\frac{2\pi(10^8)(4\pi\times10^{-7})}{5.7\times10^7}} = 3.7\times10^{-3}\ \Omega$$



Shielding effect (S.E.)

$$S.\,E. = 20\log\left|\frac{E_e}{E_i}\right| \quad [\,dB\,]$$

E_e = *Electric field (exterior)*

E_i = *Electric field (interior)*

$$S.E. = 20\log\frac{\eta_0}{4\eta_s} + 20\log e^{t/\delta} = R(\mathrm{dB}) + A(\mathrm{dB})$$

- Faraday cage : Skin effect:

$$\delta = \sqrt{\frac{2\rho}{(2\pi f)(\mu_0\mu_r)}} \approx 503\sqrt{\frac{\rho}{\mu_r f}}$$

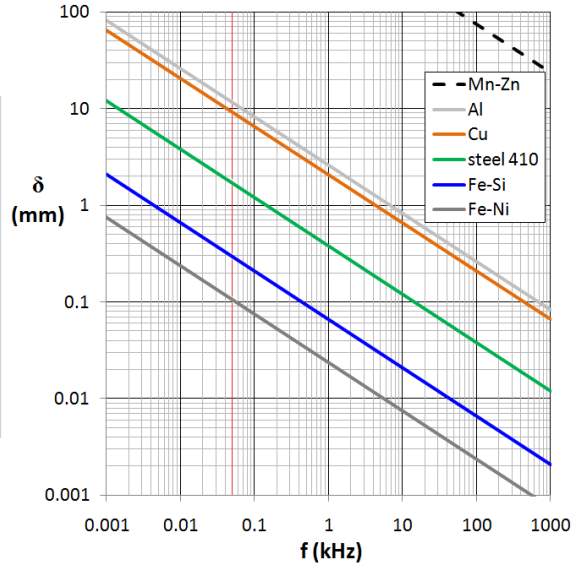
where

δ = the skin depth in meters

μ_r = the relative permeability of the medium (for copper, μ_r = 1.00)

ρ = the resistivity of the medium in Ω·m, also equal to the reciprocal of its conductivity: $\rho = 1/\sigma$ (for copper, ρ = 1.68×10^{-8} Ω·m)

f = the frequency of the current in Hz



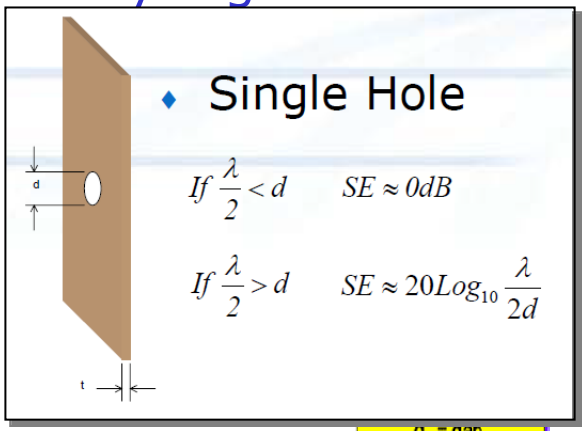
Freq.	S.E. (dB) 500 μm Al.	S.E. (dB) 25 μm Au.
1 kHz	138	137
10	131	127
100	133	118
1 MHz	159	110
10 MHz	264	106
100 MHz	617	116
1 GHz	1756	169
10 GHz	5380	358

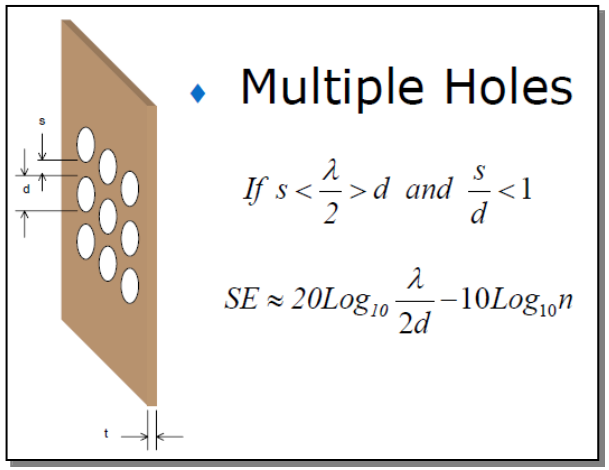
S.E. (Ideal case)

500 μm Al seems largely enough (+ stiffness role)

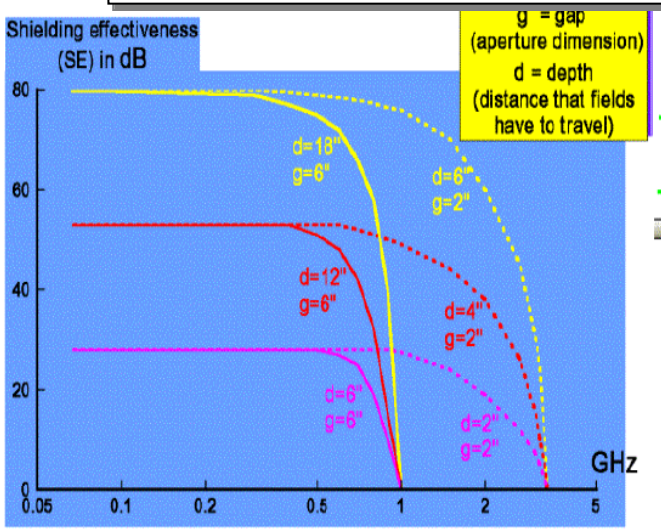
Faraday cage: Holes

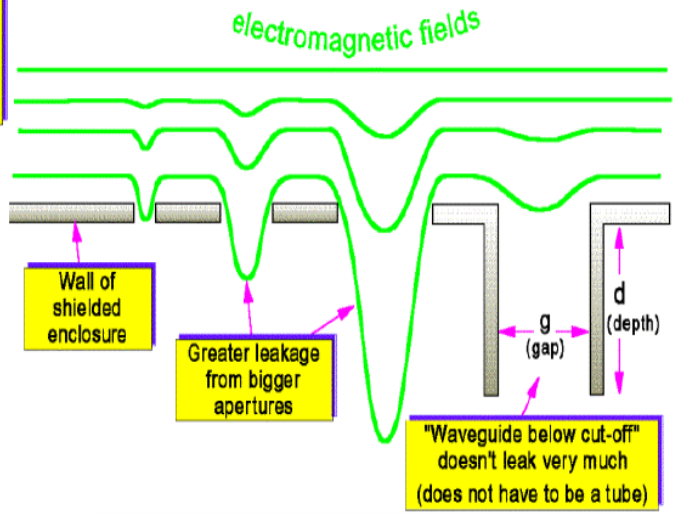
- Faraday cage :





t = Material thickness
n = Number of Holes
s = edge to edge hole spacing





Is a gap of ~ few mm ok ?

100 dB reached with d/g ~ 3.5

f_{cut} ~ 150 / gap [mm] GHz

SE [dB] ~27 d/g
d = depth
g = gap

summary

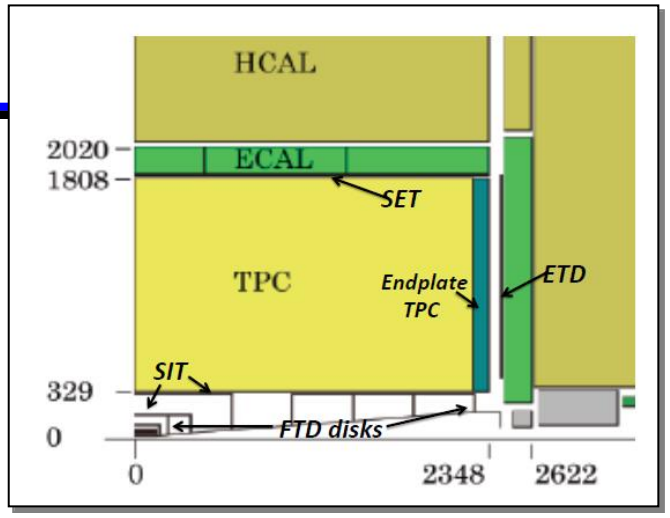
- The VTX ILD requirements
  - Several technologies are close to ILD requirements
  - VTX should be thought as a part of the central system:
    - VTX + SIT + FTD + beam pipe + Faraday cage + TPC
    - Final geometry should be revisited (disks, cable routing, Faraday cage, etc.)
    - Devil is in the details
- However…
  - The technology choice calendar is not defined yet.
  - Many integration questions remains (manpower issue)
  - We should prepare to welcome new groups
- Lots of benefits from other HEP experiments (STAR, ALICE, BELLE II, etc.)
  - Experience learned
  - Keep know how for ILC
  - Funding
- Interface document for ILD
  - Preliminary version exists. Keep working in it.

backup

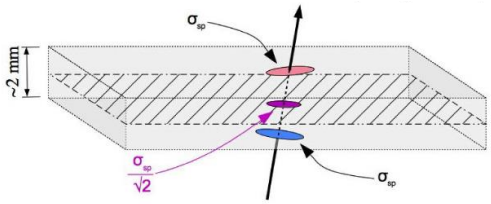
Materials

- Beryllium:
  - resistivity ρ = 4 - 9 x 10^{-8} Ω.m
  - Density = 1.85 g.cm^{-3}
  - Radiation length X_0 = 65.19 g.cm^{-2} ⇨ 35.28 cm
- Copper:
  - resistivity ρ = 17 x 10^{-9} Ω.m
  - Density = 8.96 g.cm^{-3}
  - Radiation length X_0 = 12.86 g.cm^{-2} ⇨ 1.436 cm
- Aluminium:
  - resistivity ρ = 28 x 10^{-9} Ω.m
  - Density = 2.7 g.cm^{-3}
  - Radiation length X_0 = 24.01 g.cm^{-2} ⇨ 8.897 cm
- Silicon:
  - Density = 2.33 g.cm^{-3}
  - Radiation length X_0 = 21.82 g.cm^{-2} ⇨ 9.370 cm
- Optical fibers
  - 1 mm diameter (25 Gbits/s)
  - Density = 1.19 g.cm^{-3}
  - Radiation length (acrylic) X_0 ⇨ 33 cm
- Gold
  - resistivity ρ = 2.4 x 10^{-8} Ω.m
  - Density = 19.3 g.cm^{-3}
  - Radiation length = 6.46 g cm^{-2} ⇨0.3344 cm
  - 20 um gold = 0.6 % X0
- Styrofoam
- Titanium
  - resistivity ρ = 6 x 10^{-7} Ω.m
  - Density = 4.506 g/cm^3
  - Radiation length = 16.16 g cm^{-2} ⇨ 3.560 cm

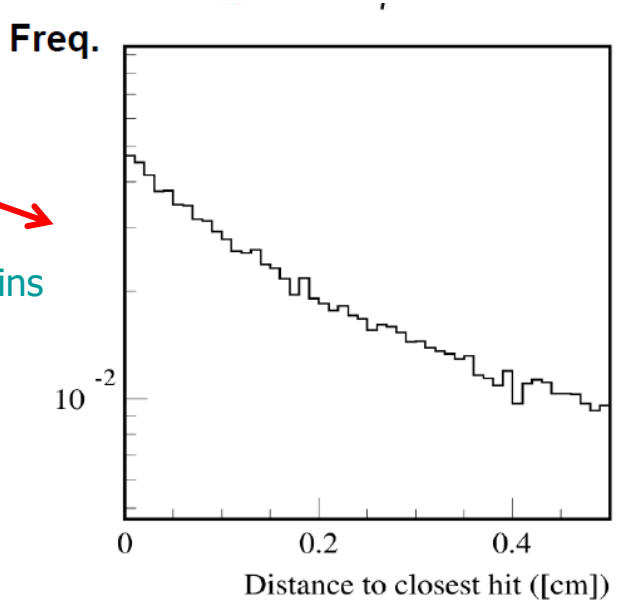
PSIRA for Pixelated SIT



- Concept
  - 2 double-sided layers
    - Improved spatial resolution & track seeding
  - Baseline:
    - $\sigma_{R\phi,Z}$ = 5 μm
    - Δt = 1 μs



- Expected occupancies
  - Beam background ~10^{-2} hits/cm^2/μs
    - Negligible impact on r.o. time
  - Physics hits
    - e.g.: If 5 hits/region/μs ⇨ ~ 750 ns to read it.
    - This actually governs the minimal read-out time !
    - Monte-Carlo input needed
  - Data stored in buffers on the chip and transfered inbetween trains
- Accelerating read-out speed ? (below 1μs)
  - At the expense of Power consumption
    - Needs shrinking peaking time 2μs ⇨ ~300 ns
    - x 5 Power consumption (8 mW/cm^2 ⇨ 40mW/cm^2)
- Potential improvements
  - Clock freq. 20 MHz ⇨ 40 MHz ⇨ 25ns pixel read-out
  - Priority encoder architecture



Dimensions and VXD asumptions

- VXD asumptions: sp.res = 4μm; time resolution = 4 μs -> pitch = 23 x 23 μm^2
- Chip sizes:
  - L0/1: 11mm x 31. mm ?
  - L2/3/4/5: 22 mm x 31. mm ?
- Ladders sizes:
  - 4 chips x 31mm ⇨ 12.5 cm length
  - Layers 0/1: Radii (1.6/1.8cm); length: 12.5 cm; ladders: 10
  - Layers 2/3 : Radii (3.6/3.8cm) ; length: 2x12.5 cm ; ladders: 11x2
  - Layers 4/5 : Radii (5.8/6.0cm) ; length: 2x12.5 cm ; ladders: 17x2
- Surfaces:
  - L0: ladders: 1.1 x 12.5 x 10 = 137.5 cm^2 ⇨ cylinder surface: 2 π x 1.6 x 12.5 = 126 cm^2
  - L1: ladders: 1.1 x 12.5 x 10 = 137.5 cm^2 ⇨ cylinder surface: 2 π x 1.8 x 12.5 = 141 cm^2
  - L2: ladders: 2.2 x 12.5 x 2 x 11 = 605 cm^2 ⇨ cylinder surface: 2 π x 3.6 x 25 = 565 cm^2
  - L3: ladders: 2.2 x 12.5 x 2 x 11 = 605 cm^2 ⇨ cylinder surface: 2 π x 3.8 x 25 = 597 cm^2
  - L4: ladders: 2.2 x 12.5 x 2 x 17 = 990 cm^2 ⇨ cylinder surface: 2 π x 5.8 x 25 = 911 cm^2
  - L5: ladders: 2.2 x 12.5 x 2 x 17 = 990 cm^2 ⇨ cylinder surface: 2 π x 6.0 x 25 = 942 cm^2
  - TOTAL : ladder surfaces = 3461 cm^2 ⇨ cylinder surface = 3282 cm^2

"Physical limitations to the spatial resolution of solid-state detectors", M. Boront et al., IEEE TNS 62-1, p381 (2015)

"a simple formula $\sigma \sim p/(S/N)$ saturates due to δ electrons at higher S/N"

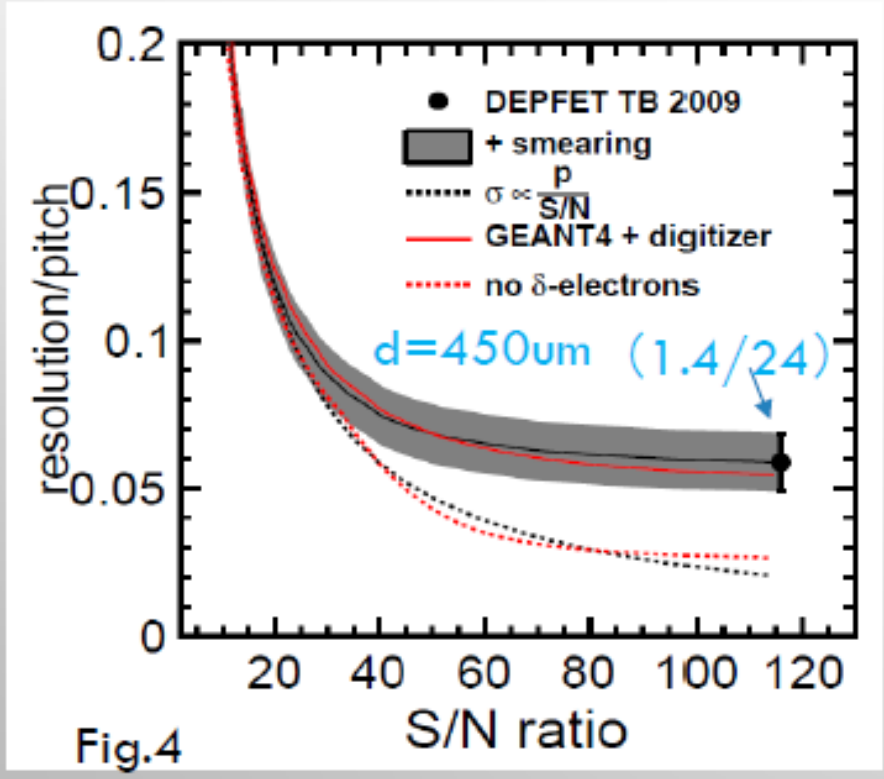


Fig.4

FPCCD Electronics and Readout

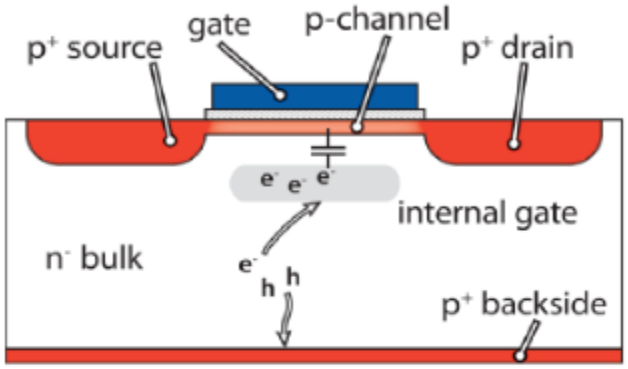
- Data transfer
  - Data size 135MB/train assuming 500GeV ILC and 32bit information per hit
  - 16 ASIC channels are serialized to single cupper cable and sent to junction box located very forward region (close to FTD1 (or 2) and beampipe)
  - Zero suppression is done by ASIC in the junction box, then data is sent via optical cable to local VTX DAQ system at platform.
    - Number of optical cables are 6 per side → in total 12 cables
- Power supply
  - Power supply and control cables via junction box.
  - Power supply are located on platform.
    - Two power supply for clock generation
    - Three power supply for CCD
    - Three power supply for readout circuit
    - 16 x 8mm2 cables per side → in total 32cables
- Clock and drivers
  - Three serial cable per side for upper/lower : in total 12 cables
    - Master clock 100MHz
    - Accelerator clock
    - Control clock
  - CCD driver and clock driver are inside the junction box

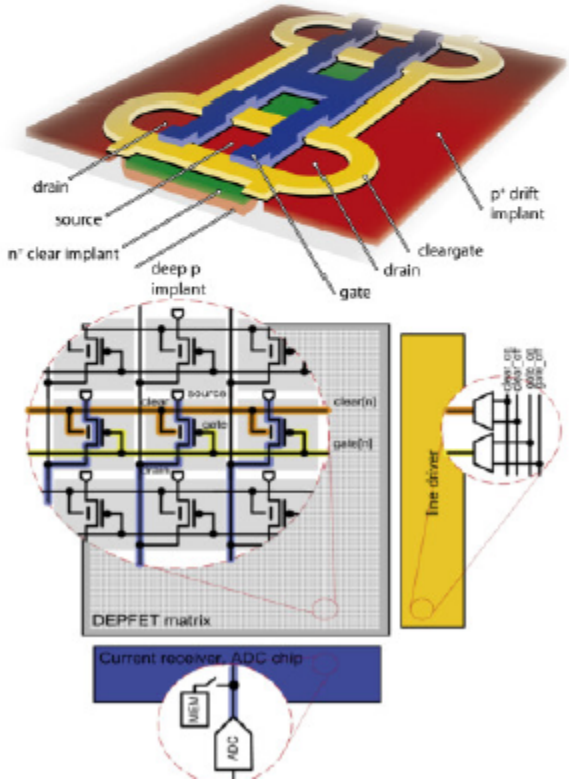
Rack and Cooling

- Number of Rack at platform
  - 1 x 19inch rack for power supply
  - 1 x 19inch rack for adding address information
  - 4 x 19inch rack for DAQ and online monitoring
- Cryostat and Liquid CO_2 (and gas N_2) cooling system
  - Should be cool down to -40degree
  - Inter-train readout → Larger power consumption than CMOS/DEPFET
  - About 50W inside the cryostat, about 200W junction box
    - FPCCD 10mW/channel (heating is larger for readout side)
    - ASIC 5mW/channel
    - ASIC and FPCCD readout side can be directly cooled down via CFRP for doublet ladder
  - CO_2 : 1g/sec per side (note. cooling power 300J/g)
    - 1 x 2mm cable per side → in total 2 cables
    - CO2 cable is attached to endcap and cool down the air inside
  - N_2 : 6litter/min (or less)
    - If air flow is further needed to cool down the FPCCD for not-readout side, N_2 cooled down by CO_2 is flowed to cryostat.
  - outer wall : 0.2mm^t CFRP + 1cm^t Styrofoam + 0.2mm
    - Carbon Fiber Reinforced Polymer (**CFRP)**
    - Styrofoam (polystyrene)
  - Inner wall : similar one but styrofoam thinner

DEPFET pixel sensor

Jochen Dingfelder
University of Bonn
Vertex 2017, Las Caldas, Sep. 12, 2017





- Each pixel is a **p-channel FET** integrated in a fully depleted bulk
- Deep **n-implant** creates **potential minimum** under FET gate (**internal gate**)
- Internal gate capacitively coupled to FET gate
- **Drain current** is proportional to **number of electrons** collected in internal gate

  Internal gain: g_q~ 500 pA / electron
- Charge collection in "off-state", readout on demand (rolling-shutter, 4 rows at a time)
- Clear process to remove stored charges

- Detection and internal amplification
- Small intrinsic noise
- Low power consumption

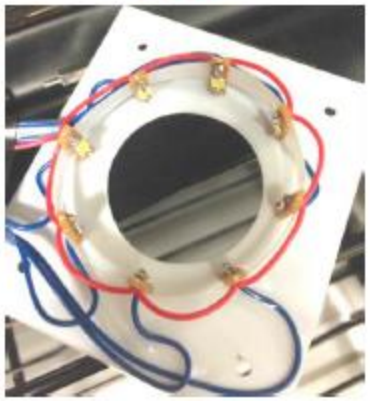
Improvement of CTI by Fat-zero charge injection

- Improvement of CTI
  - Degradation of CTI is caused by lattice defect

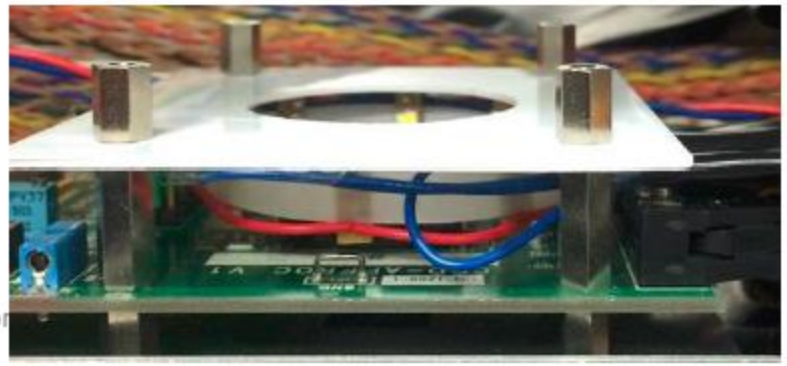
  ⇒ Additional charge are injected to fill up the lattice defects before transferring signal.

- Fat-zero charge injection
  - Fill lattice defect by background current
  - In this study, LED was used to fill the gap.

LED



CCD



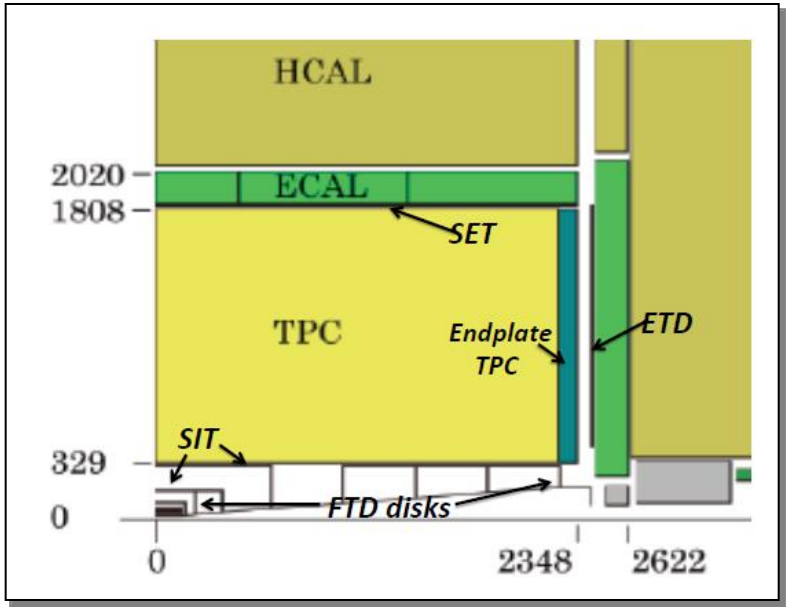
Typical occupancy rate (layer 1, with DBD rates)

Pixel pitch	σ_{sp}	Read-out Time / time resolution	Assumed average cluster multiplicity	Lumi Mode (bunch Per train)	BX time spacing	√s	Assumed Expected Background	Expected background with safety factor 5	Occupancy	remarks
(μmxμm)	μm	(μs)	# pixels	B/train	ns	GeV	#hits/cm²/BX		w.o./w safety	
17x17	~3	50	5	Baseline (1312)	554	500	6	30	$8x10^{-3}$ / $4x10^{-2}$	DBD
17x17	~3	50	5	Upgrade (2625)	**366**	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Lumi upgrade
17x17	~3	50	5	1312	554	**250**	3	15	$4x10^{-3}$ / $2x10^{-2}$	250 GeV
17x17	~3	50	5	2500	366	**1000**	10	50	$2x10^{-2}$ / $1x10^{-1}$	1 TeV
17x17	~3	**25**	5	Baseline (1312)	554	500	6	30	$4x10^{-3}$ / $2x10^{-2}$	DBD X 2 faster
22 x 22	**~4**	4	5	Baseline (1312)	554	500	6	30	$1.5x10^{-3}$ / $8x10^{-3}$	Async. Read-out
25 x 25	**~5**	**1BX**	**3**	Baseline (1312)	554	500	6	30	$1x10^{-4}$ / $5x10^{-4}$	Bunch stamping
5 x 5	**~1**	**1 train**	**6**	Baseline (1312)	554	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Fine pixel BB tagging

Occupancy = (#hits/cm²/BX) x <mult> x (pitch)² x (r.o.time) / (BXtime) x safety

5 part/cm²/BX ⇨17x17 μm² pitch, cluster mult. ~5, 50 μs read-out time @ 0.5TeV on Layer 1 ⇨ ~ 1 %

ILD dimensions



Barrel system						
System	R(in)	R(out)	z /mm	comments		
VTX	16	60	125	3 double layers	Silicon pixel sensors,	
				layer 1:	layer 2:	layer 3-6
				$\sigma < 3\mu m$	$\sigma < 6\mu m$	$\sigma < 4\mu m$
Silicon						
- SIT	153	300	644	2 silicon strip layers	$\sigma = 7\mu m$	
- SET	1811		2300	2 silicon strip layers	$\sigma = 7\mu m$	
- TPC	330	1808	2350	MPGD readout	$1 \times 6\text{mm}^2$ pads	$\sigma = 60\mu m$ at zero drift
ECAL	1843	2028	2350	W absorber	SIECAL	30 Silicon sensor layers, 5×5 mm^2 cells
					EcECAL	30 Scintillator layers, 5×45 mm^2 strips
HCAL	2058	3410	2350	Fe absorber	AHCAL	48 Scintillator layers, 3×3cm^2 cells
					SDHCAL	48 Gas RPC layers, 1×1 cm^2 cells
Coil	3440	4400	3950	3.5 T field	2λ	
Muon	4450	7755	280	14 scintillator layers		

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1811	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65

ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2420	0.985-0.799	x:σ=7.0	0.65

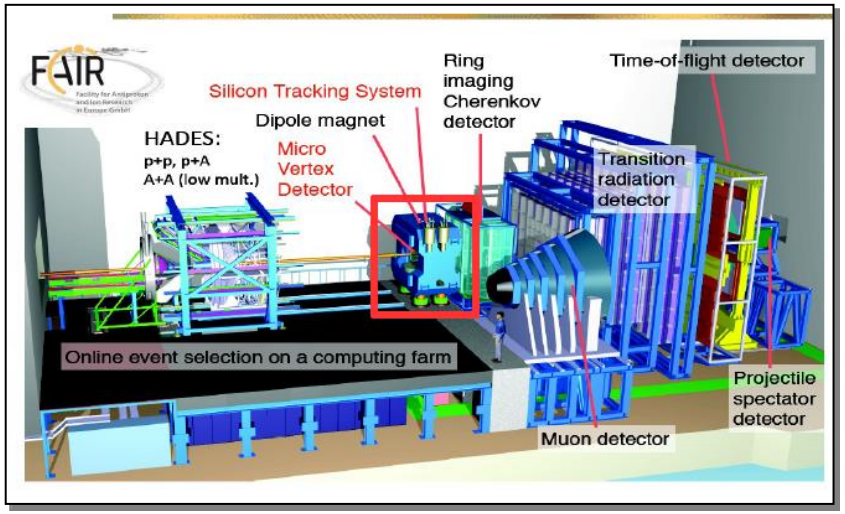
FTD characteristics (design baseline: pixels for two inner disks, microst				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802		0.25-0.5
49.6-164	371.3	0.991-0.914	σ=3-6	0.25-0.5
70.1-308	644.9	0.994-0.902		0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998	σ=7.0	0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65

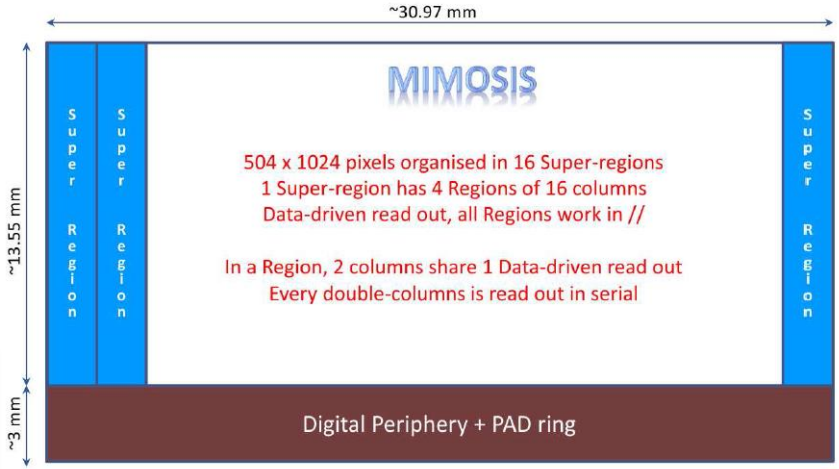
CBM-MVD: MIMOSIS sensor

- CBM-MVD @ FAIR (~2019-2020)

  0.18 μm deep P-well, based on ALPIDE design.

  - MIMOSIS sensor
  - Requirements & Design
    - Pitch ~ 27x33 μm^2 ⇨ σ_{sp} < 5 μm ;
    - In-pixel discrimination
    - Binary charge encoding
    - Data driven read-out
    - Time resolution = 5 μs
    - 4 stations of CPS
    - x2 Data transmission rate (up to x10 for local hit density)
    - peak hit rate @ ~10^8 /cm^2/s ⇨ >1 Gbits/cm^2/s output (20 inside chip) ⇨ more buffer & serializer
    - Rad.tol. x 10 w.r.t. ALICE-ITS : 3x10^{13} n_{eq}/cm^2/yr & 3 MRad/yr (with replacement every year)
    - P < 200 mW/cm^2
    - Vacuum compatible & Negative temp. operation





504 x 1024 pixels = 16 super regions
1 super-region = 4 read-out regions of 16 columns
2 columns = 1 data driven read-out

⇨ architecture adaptable to a fast sensor for an ILC vertex detector