QUAD development a TPC building block

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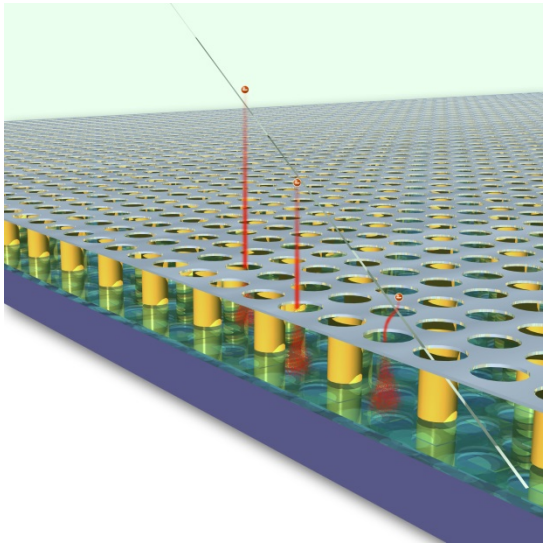
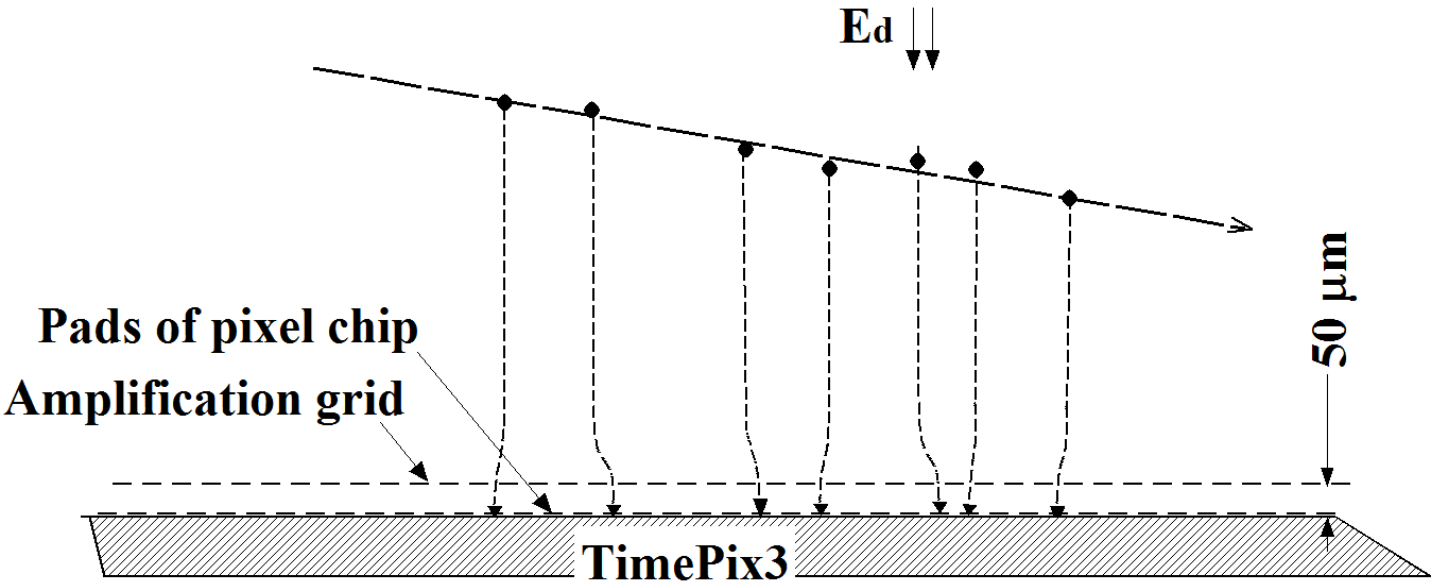
GridPix technology

- Pixel chip with integrated Micromegas (InGrid)
- Very small pixel size
- => Mostly detecting **individual electrons**

- Optimal statistics
- => **best possible track position resolution** by a gaseous detector

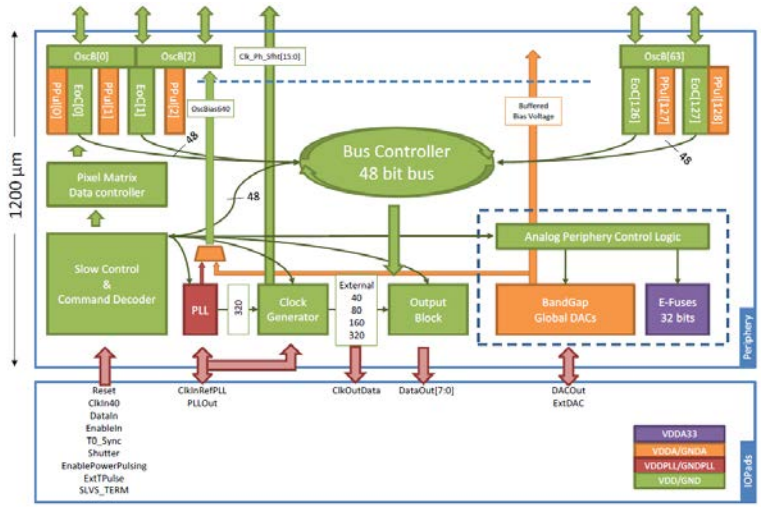


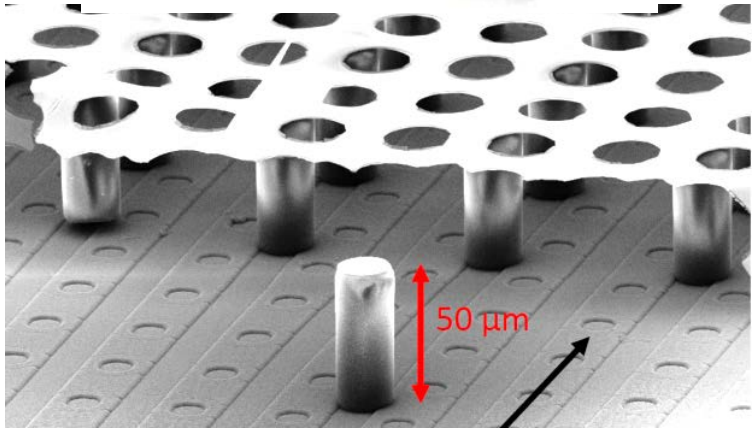


GridPix chip

TimePix3

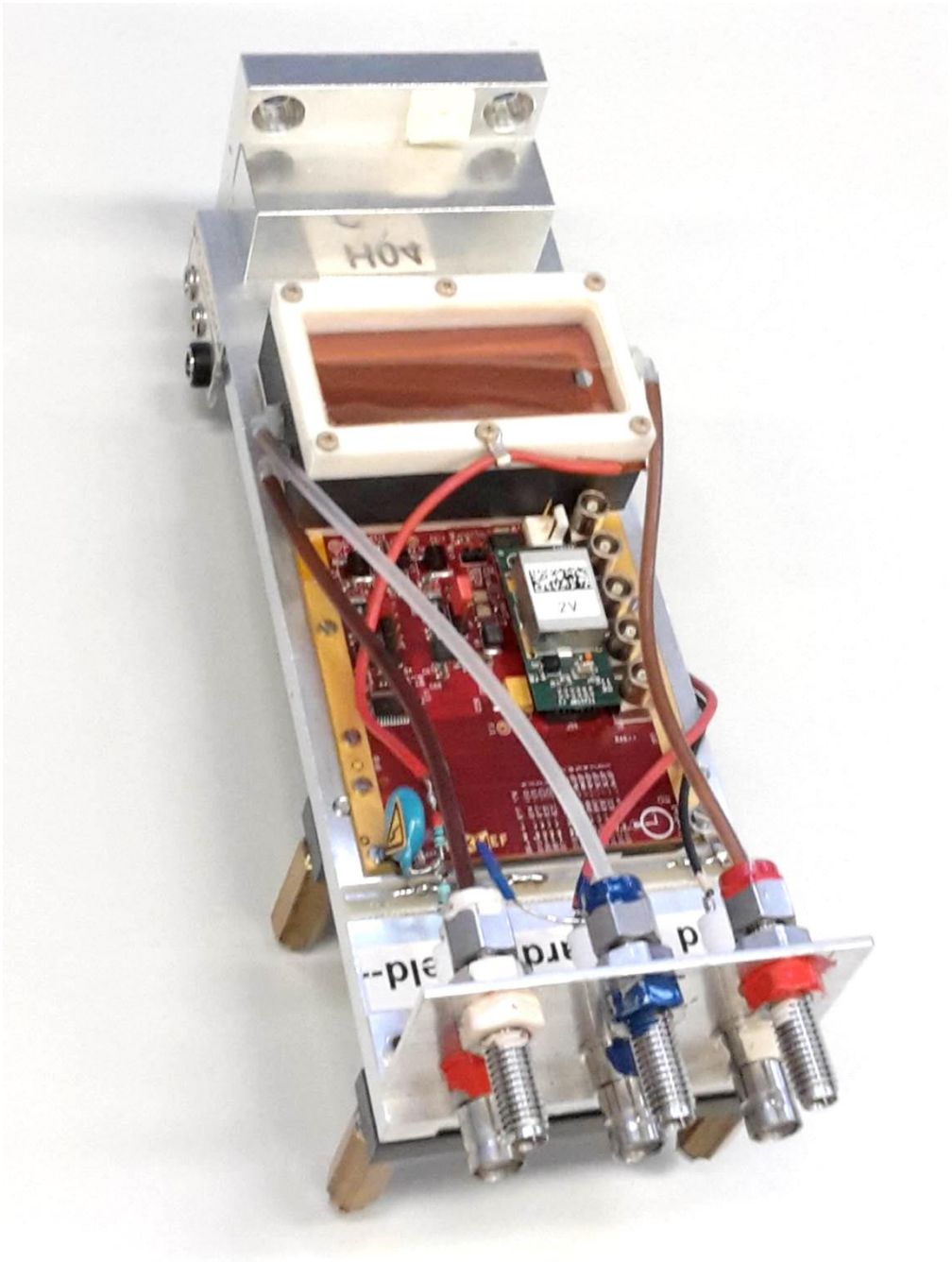
- 256 x 256 pixels, 55 x 55 µm pitch, 14.1 x 14.1 mm sensitive area
- TDC with **600 MHz clock (1.7 ns)**
- Presently used in the data driven mode
  - Trigger added as additional time stamp
  - Running in triggered mode is possible
- Simultaneous registration of arrival time (ToA) and amplitude by ToT measurement
  - => **Compensation of time walk**
- High power consumption
  - Up to 2.5 A @ 2 V (5W), depending on hit rate
  - => good cooling is an issue
- Equipped with InGrid produced at IZM by photolithography (wafer postprocessing)
  - Aluminium grid (2- 3 µm thick) with 35 µm wide holes
  - Supported by SU8 pillars 50 µm high
  - Grid surrounded by SU8 dyke (200 µm wide solid strip) for mechanical and HV stability





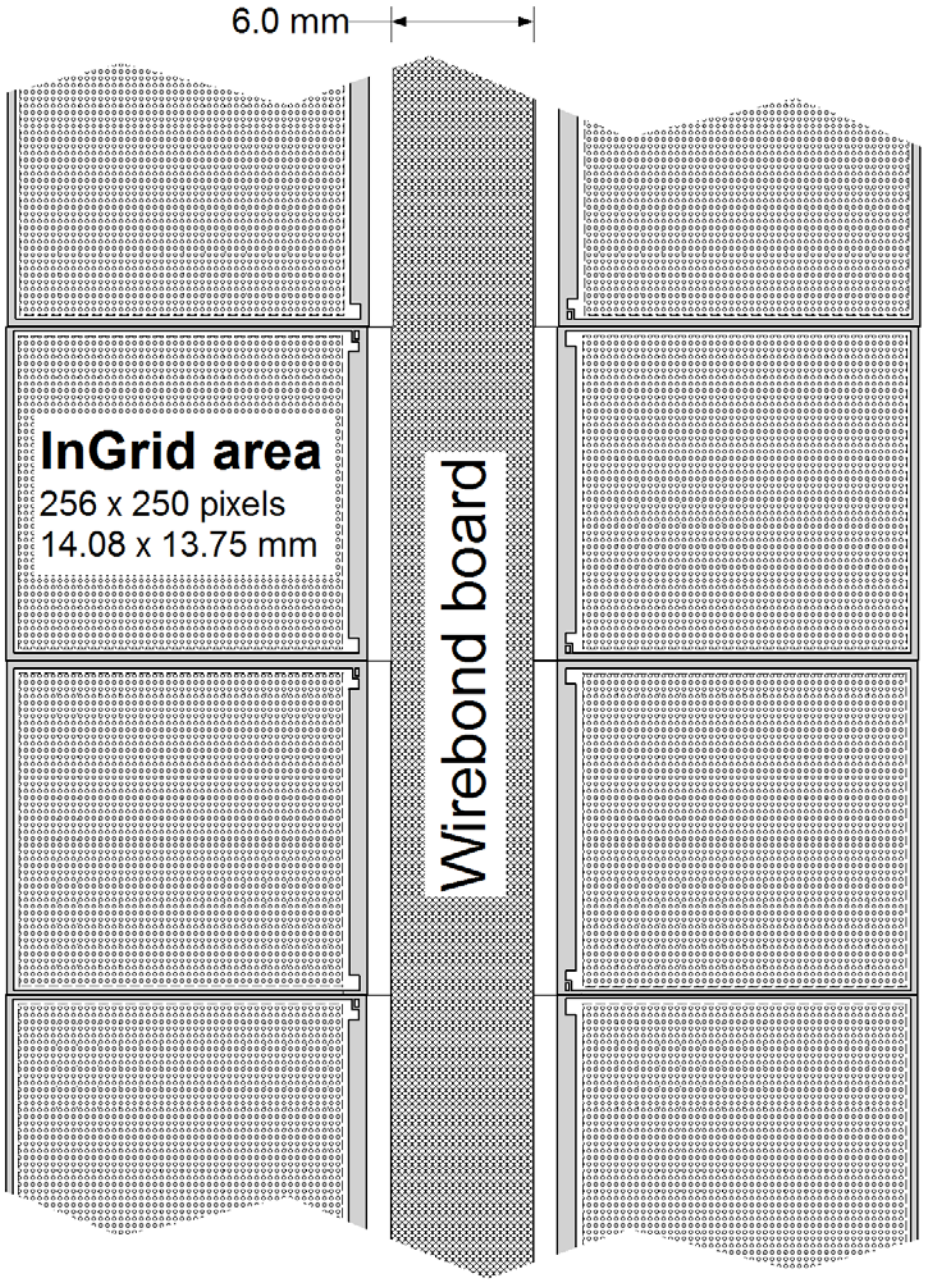
Single chip GridPix detector

- See talk Kees Ligtenberg
- Active area
  - 1.2% (whole structure)
  - 2.4% (PCB)



How to design a detector with the biggest active surface?

- Smallest insensitive area: use a central wirebond board



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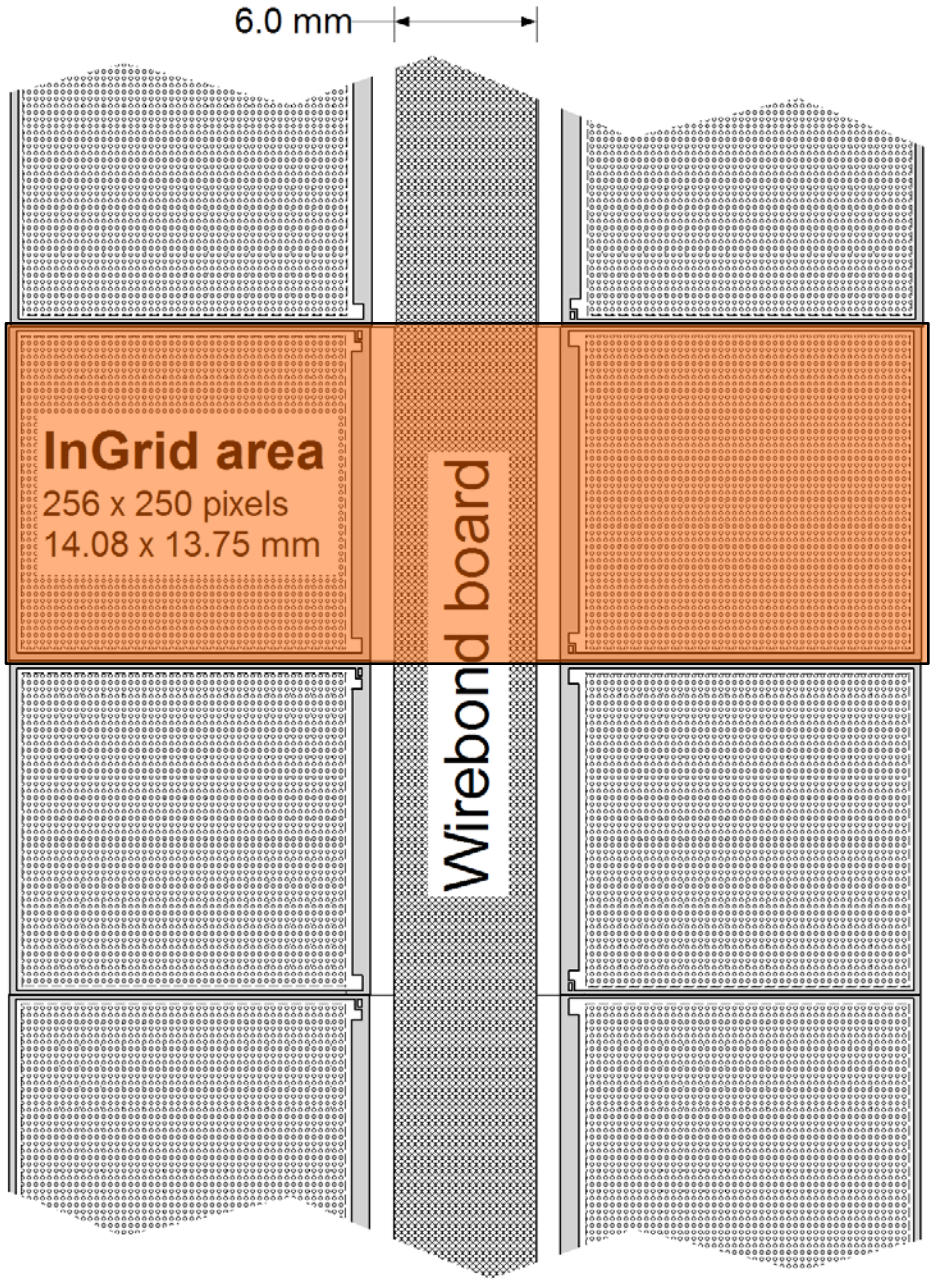
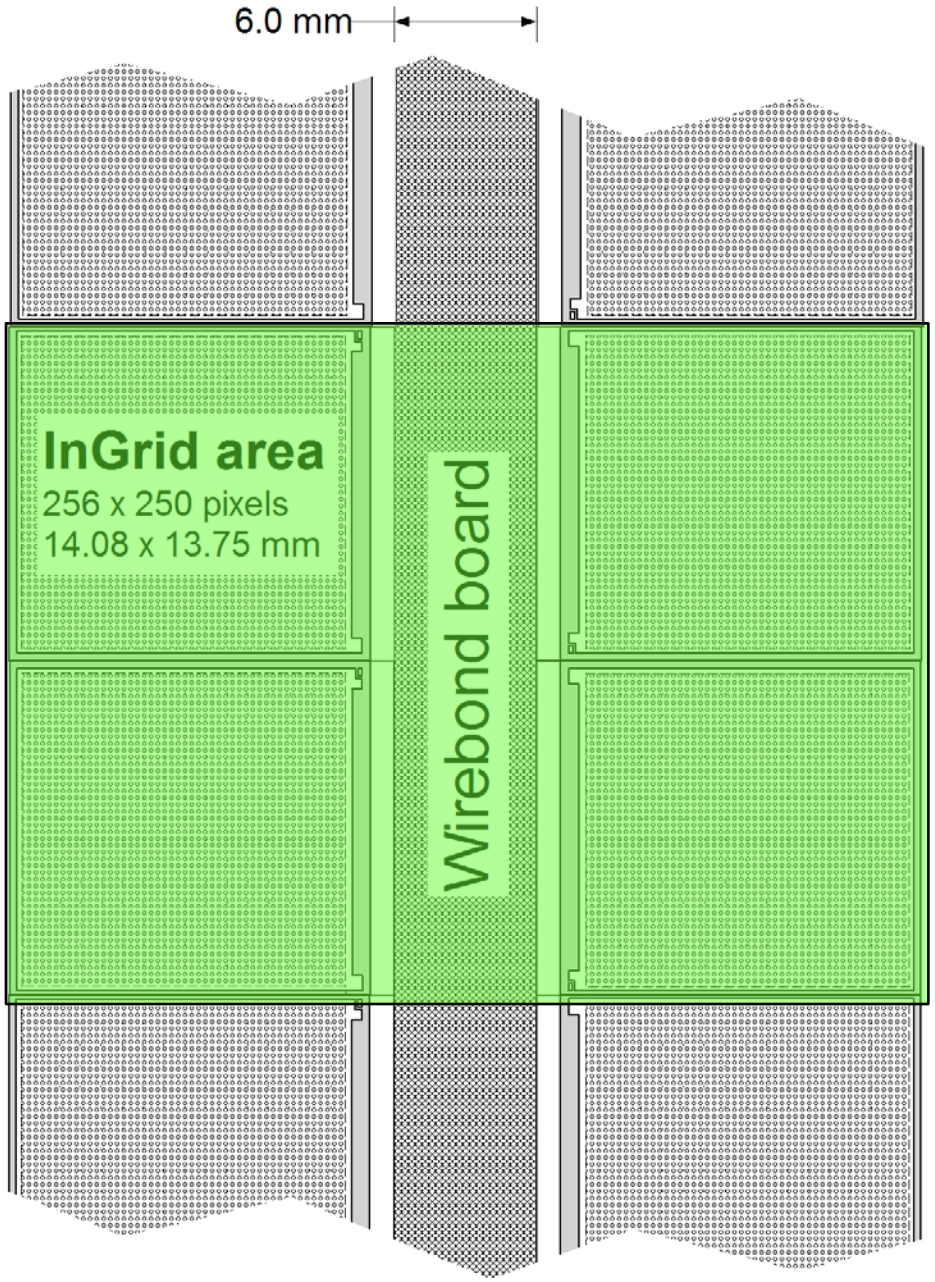
- So we may have as a basic unit:
- 1 x 2 chips
  - Not sufficient space (14 mm) for a LV stabilisation and a data RO



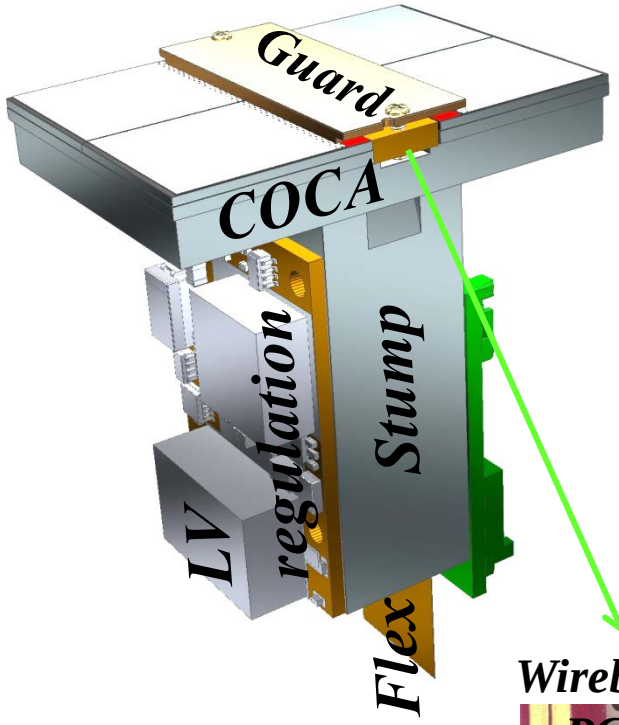
How to design a detector with the biggest active surface?

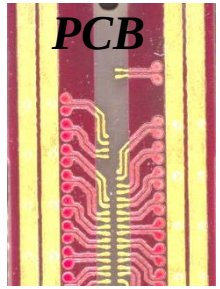
- Smallest insensitive area: use a central wirebond board
- So we may have as a basic unit:
- 1 x 2 chips
  - Not sufficient space (14 mm) for a LV stabilisation and a data RO
- **2 x 2 chips (QUAD)**
  - All fits
- ≥ 3 x 2 chips
  - Less flexible, lower yield, more handling risk



The building block QUAD

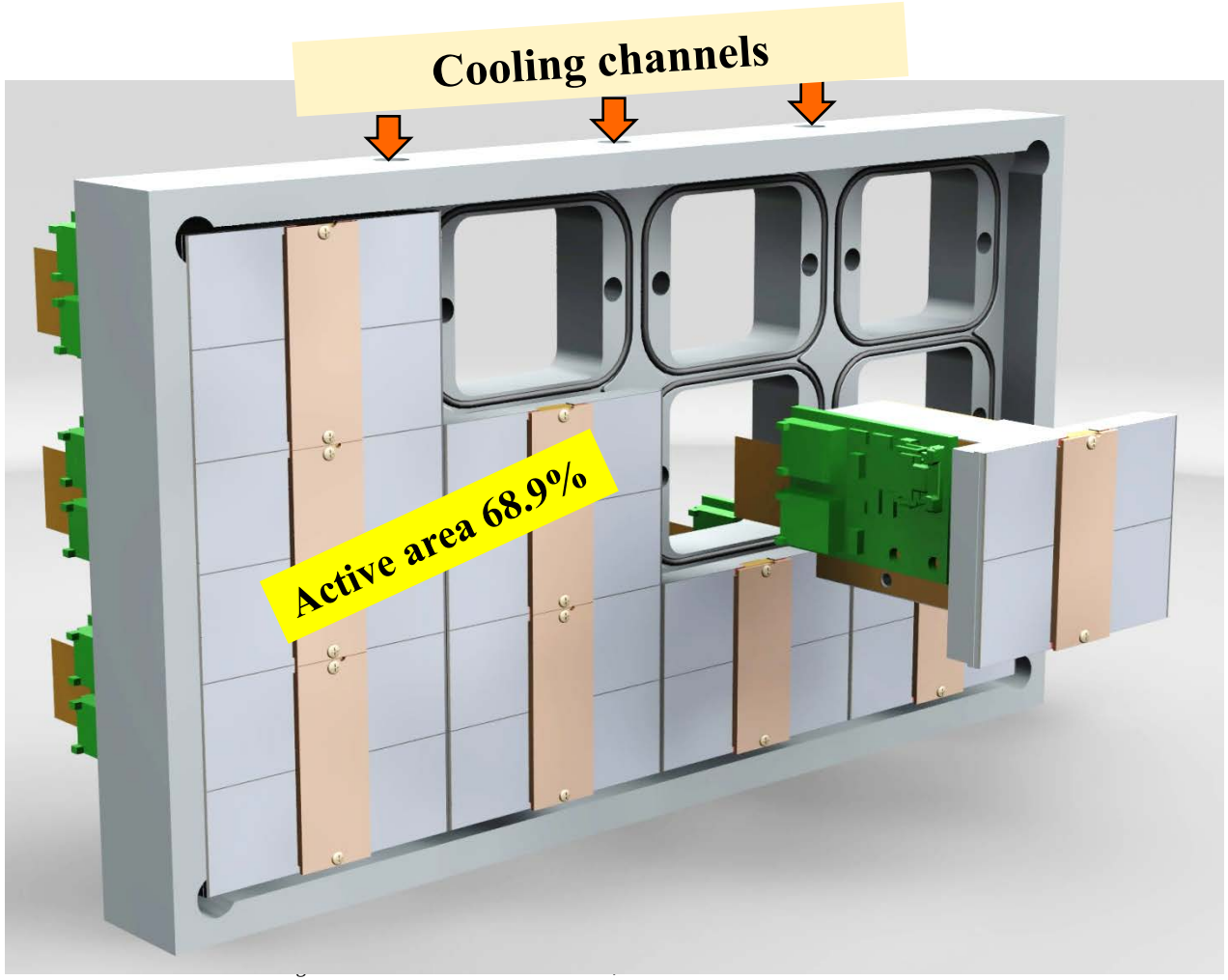
- 4 GridPix chips on a **COld CArrier** plate (COCA)
  - **39.6 x 28.38 mm**
- Connected to a common wirebond **PCB**
- Avoiding space and material for connectors
  - => flex connection to LV regulation board
  - => long **flex** to IO/control connector
- Central carrying structure (**stump**)
- LV board to stabilize the power voltage
  - Up to 10 A @ 2 V
- **Guard** electrode covering the wirebonds to define a homogeneous electrical field
- **All services fit under the active area**

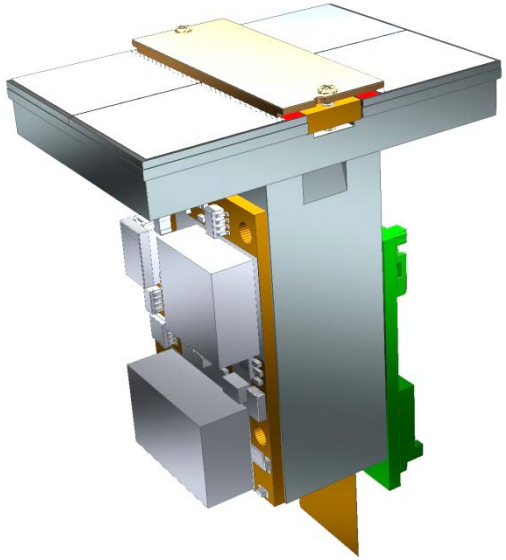




QUAD as a building block

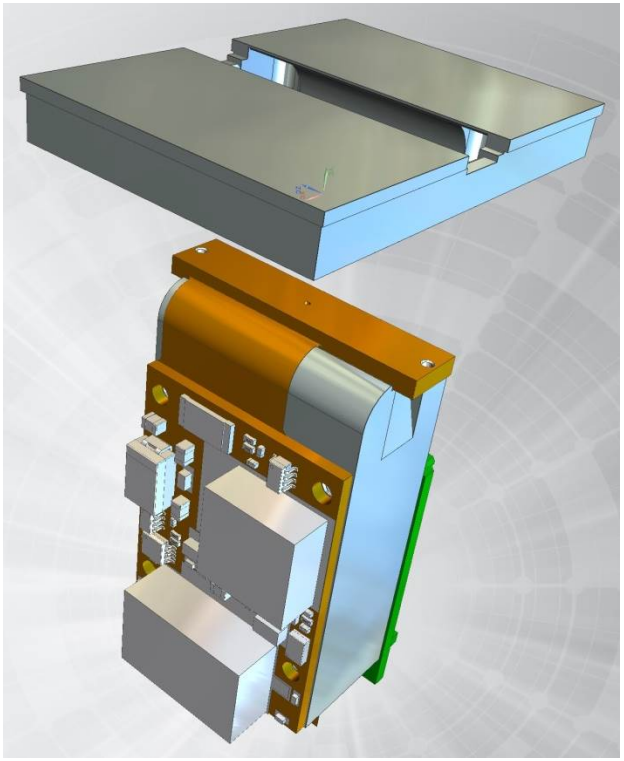
- Unlimited surface may be covered
- Plug in QUADs into a base plate
- Push them from two sides to a mechanical reference
- Also cooling (up to 20 W/QUAD) by base plate

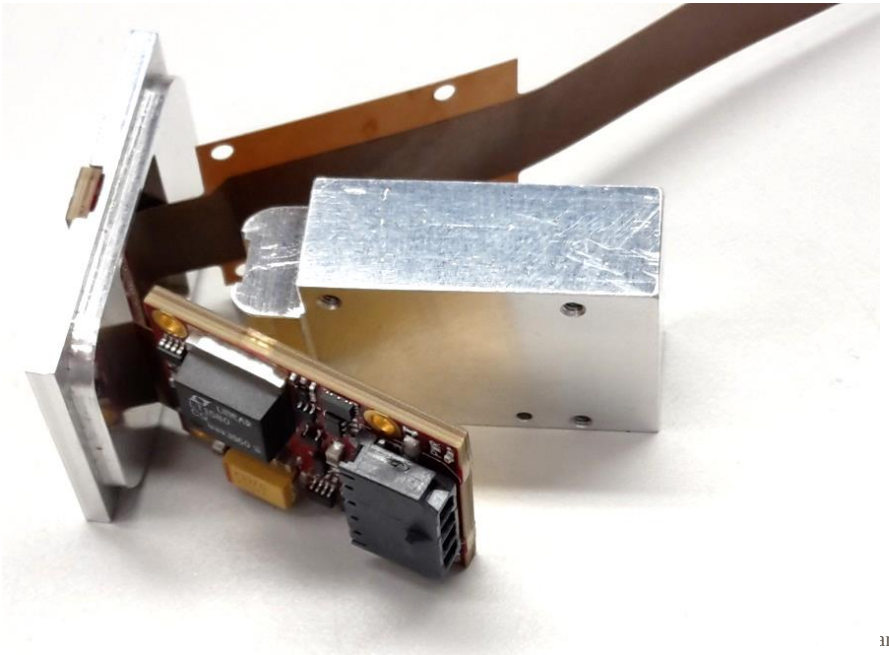


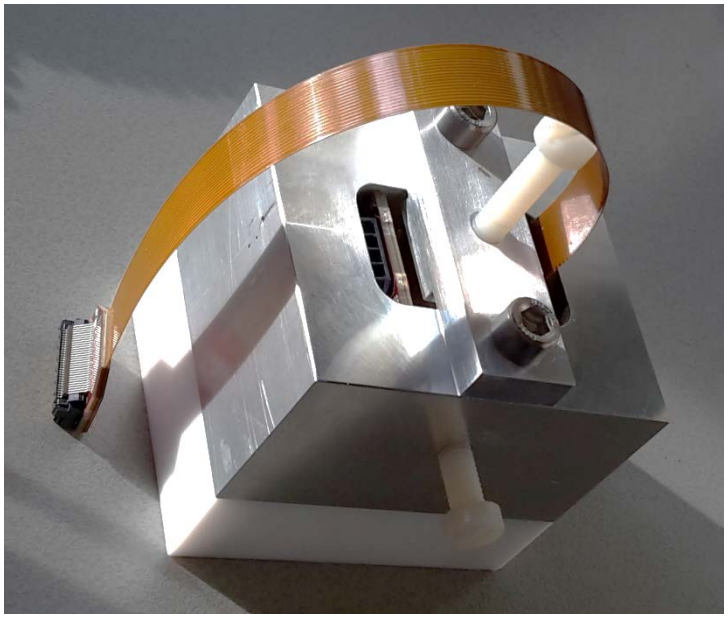


QUAD assembly 1st step

- Glue COld CArrier (COCA) together with wirebond PCB and stump
- Using dedicated jig
- Glue: Araldite 2020 (low viscosity) + Boron-nitride (1.3 ml + 1 g) for good thermal conductivity

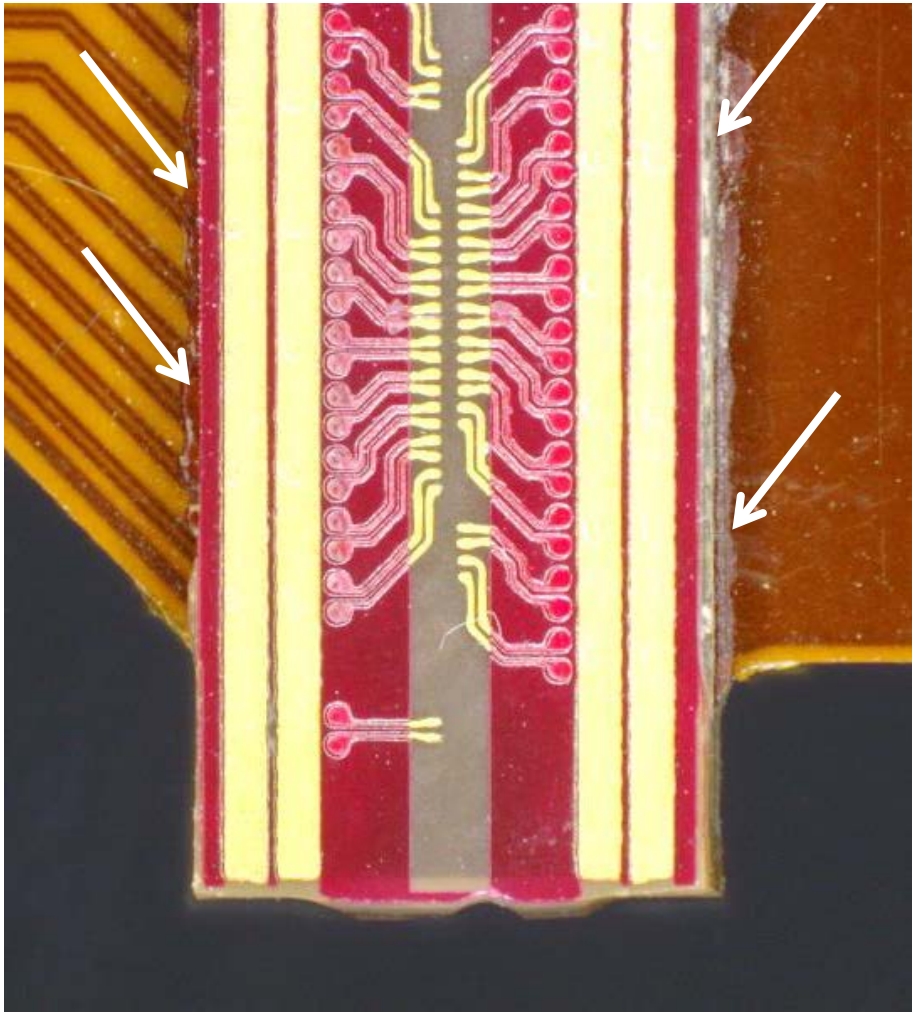






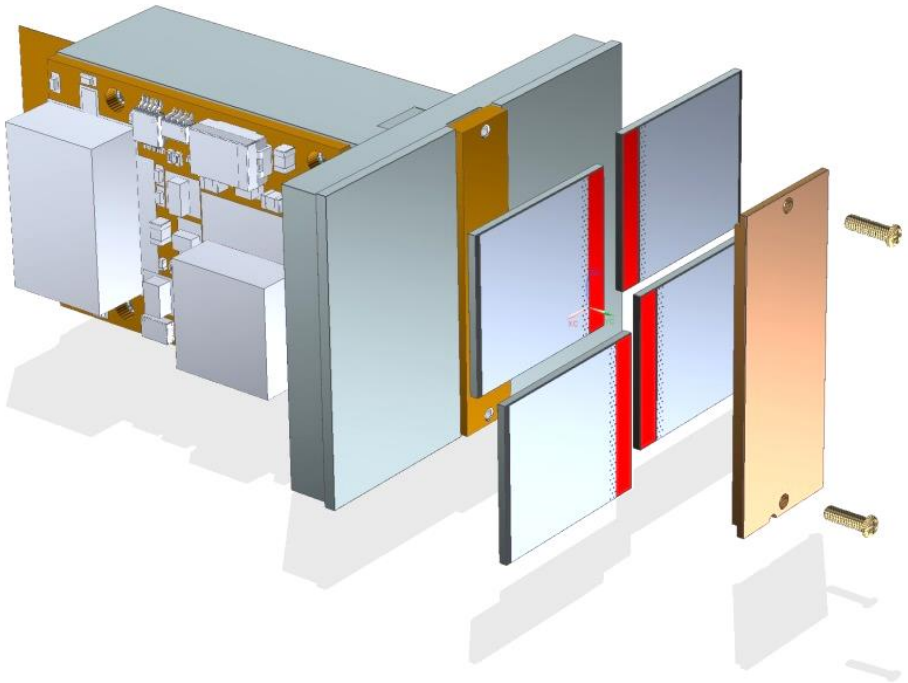
Problem

- Wirebond board badly dimensioned
  - Does not fit into the COCA
  - Needs high precision machining under microscope



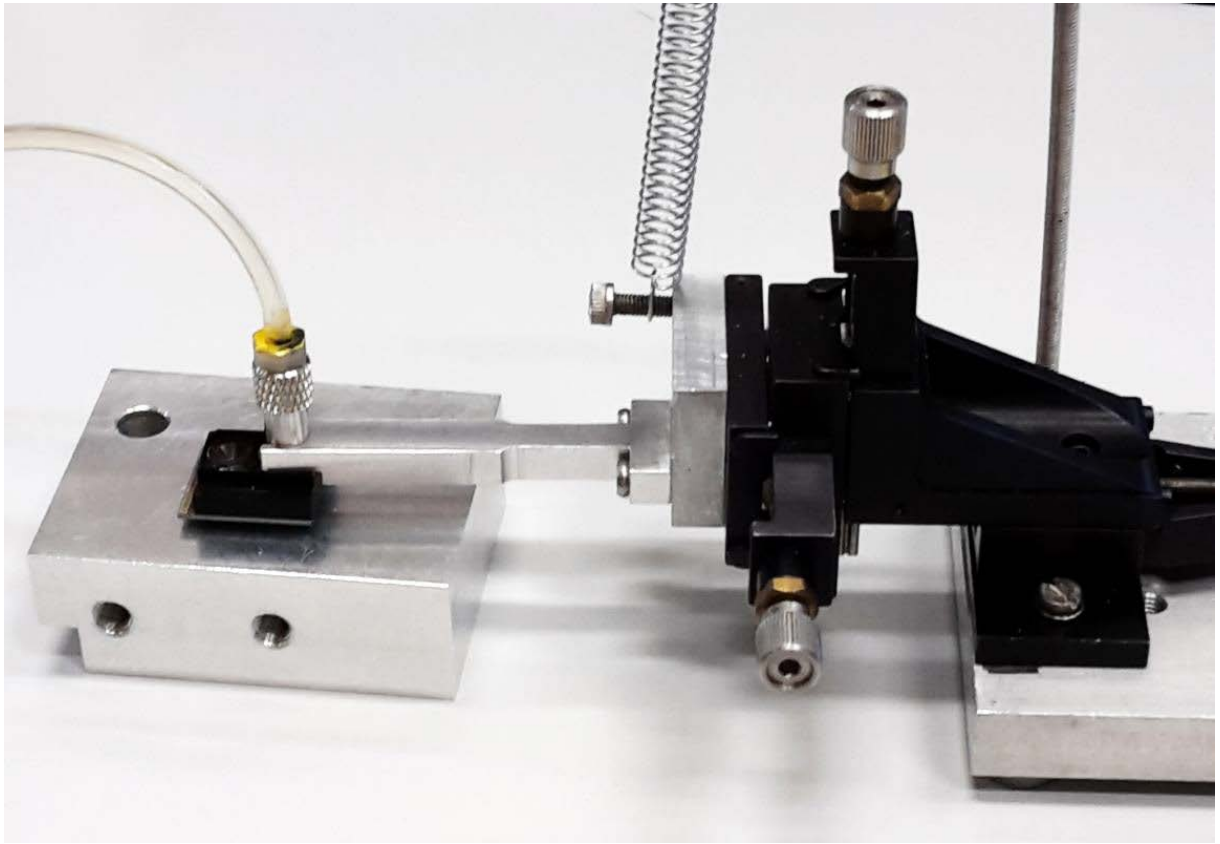
Adding the GridPix chips

- Problem: how to handle the chips with the extremely fragile grid
- Using a dedicated vacuum pickup tool touching the dykes only
  - Vacuum slowly rising and falling



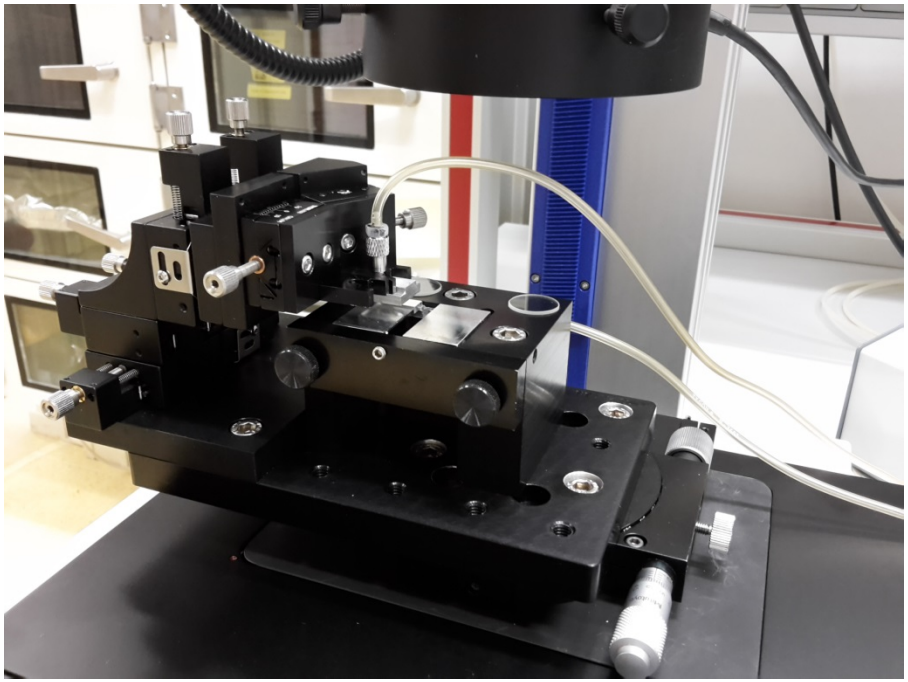
Picking up the GridPix chip

- Precisely aligning the tool to the chips
- Using XYX stage



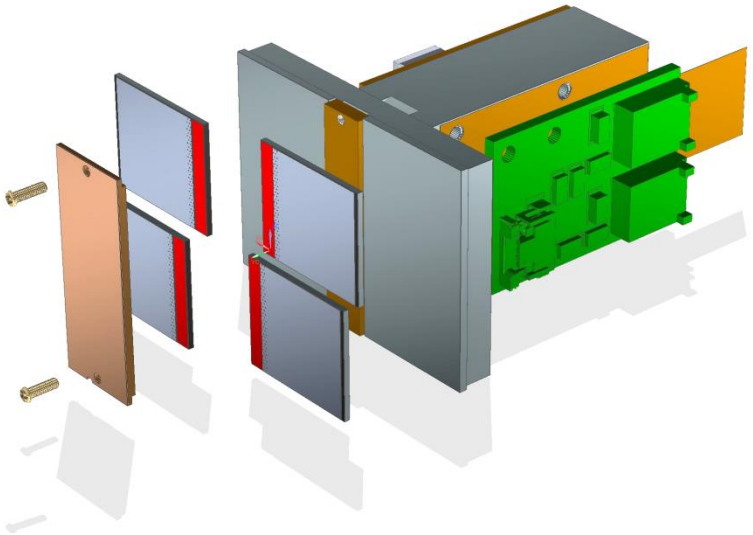
Aligning GridPix chips onto the QUAD

- Using Zeiss Axiozoom microscope
  - Precise Wetzlar XY stage under LabVIEW control
- Manually adjusting the chips in X,Y, Z and θ
  - QUAD: referring to the precise edges of the COCA
  - Chips: referring to the bonding pads
- Aimed accuracy 20 µm in X,Y and Z



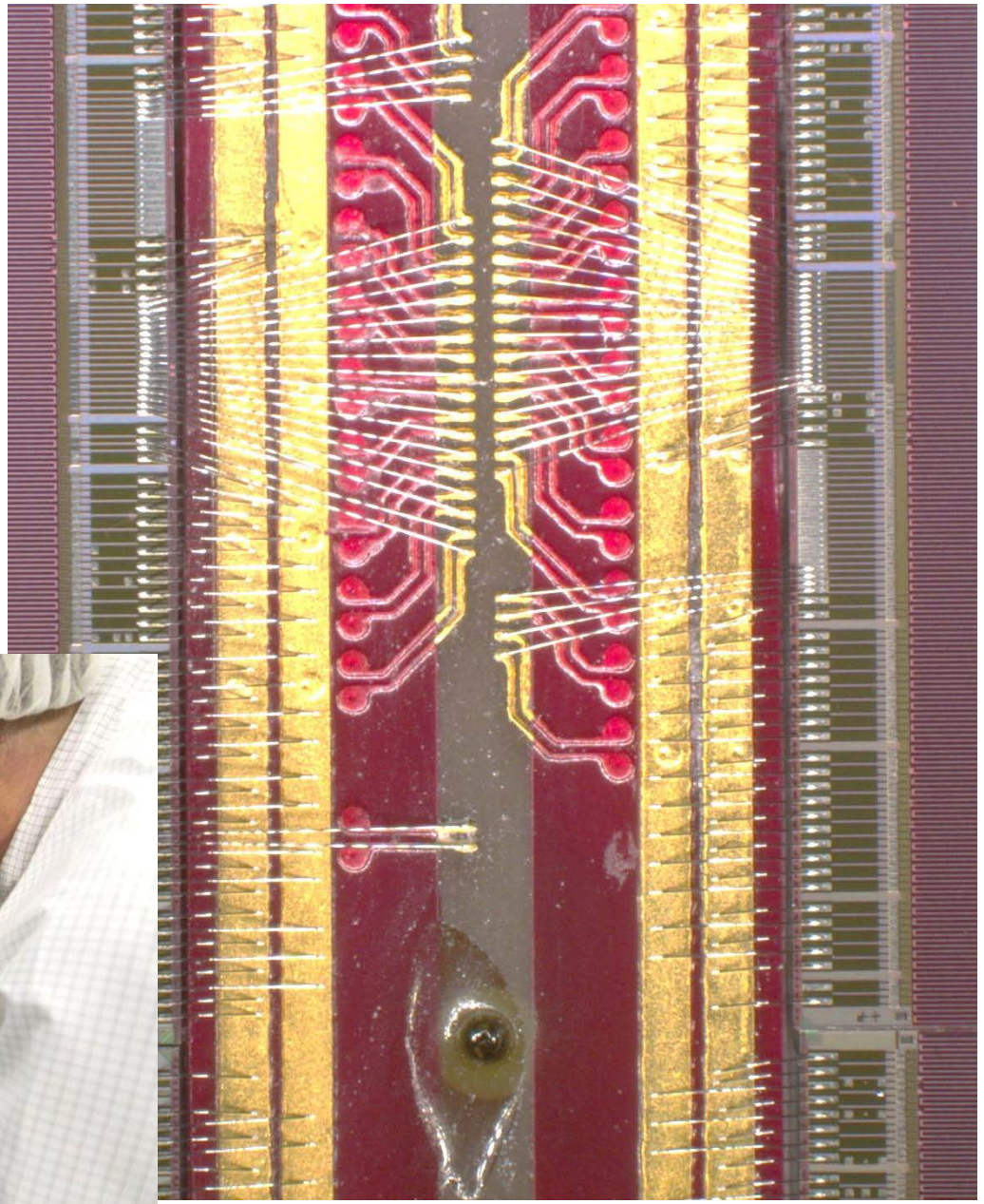
Attaching the chips to the COCA

- Requirements
  - Good adhesion and mechanical stability
  - But it should be possible to replace a broken chip
- Both chip and COCA extremely flat
  - => very thin glue layer
  - Several glues tried
  - For all glues impossible to remove a chip without damaging COCA surface and neighbouring chip
- We are using now sticky thermal foil (3M 8940)
  - 0.13 mm thick
  - Good adhesion
  - Chip easily removed after applying some alcohol



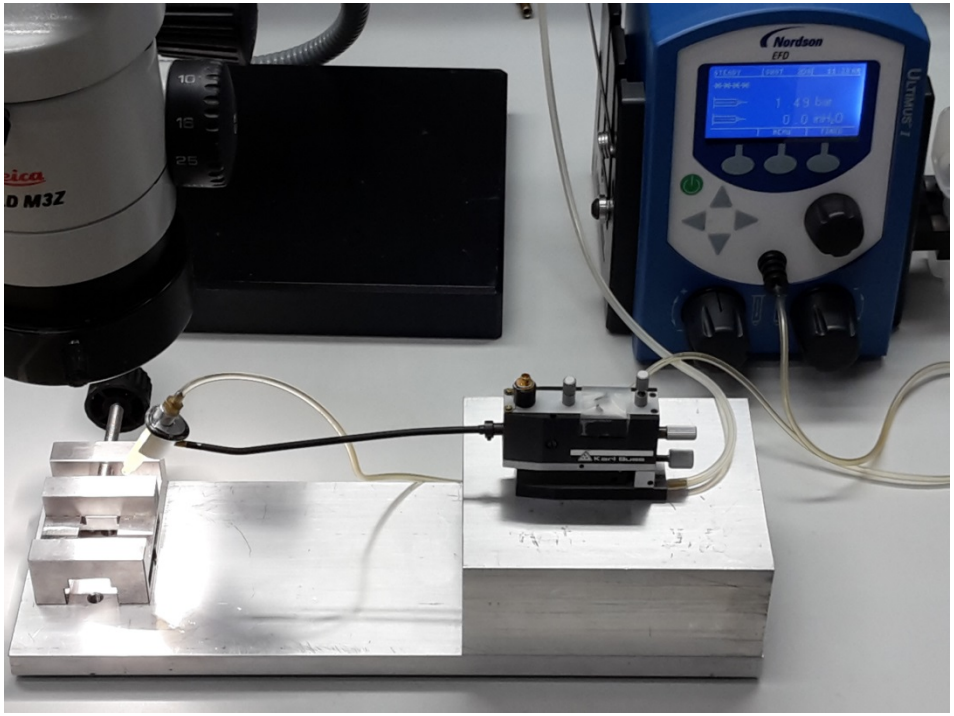
Wire bonding

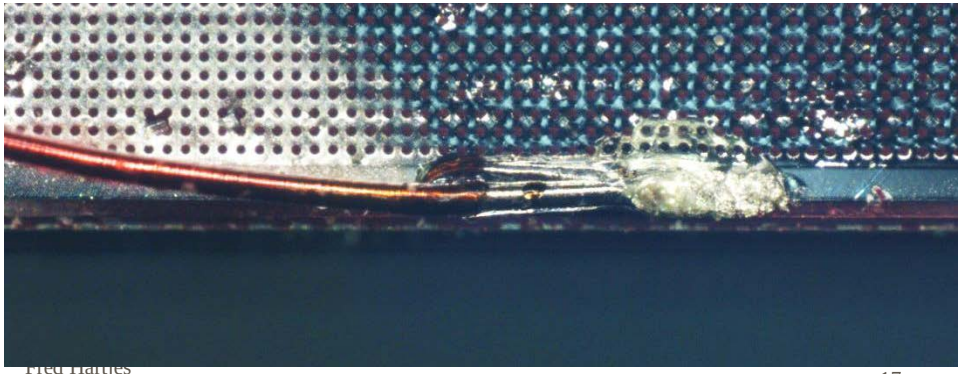
- Using automatic machine
- Fast procedure



Connecting the grid to HV

- Grids individually connected by 100 MΩ resistors to HV supply
  - Minimizing the energy of a spark discharge
- Using 80 µm insulated wire
- Wire bend to just above the dyke
- Electrical contact by silver glue
  - Tra duct
  - Avoiding flowing into grid hole (short cut)
  - Micromanipulation using XYX probe
- Mechanical strength by adding Araldite
- **In total 4 days involved (3 glue steps)**

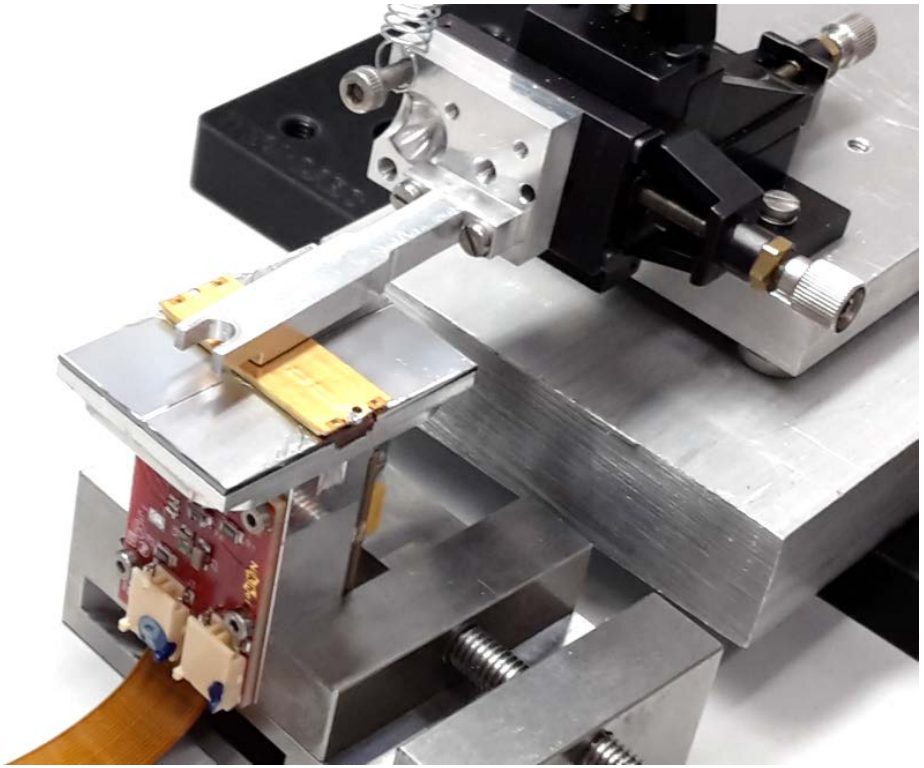




- Next generation of grids will have a wide dyke at the wirebond side

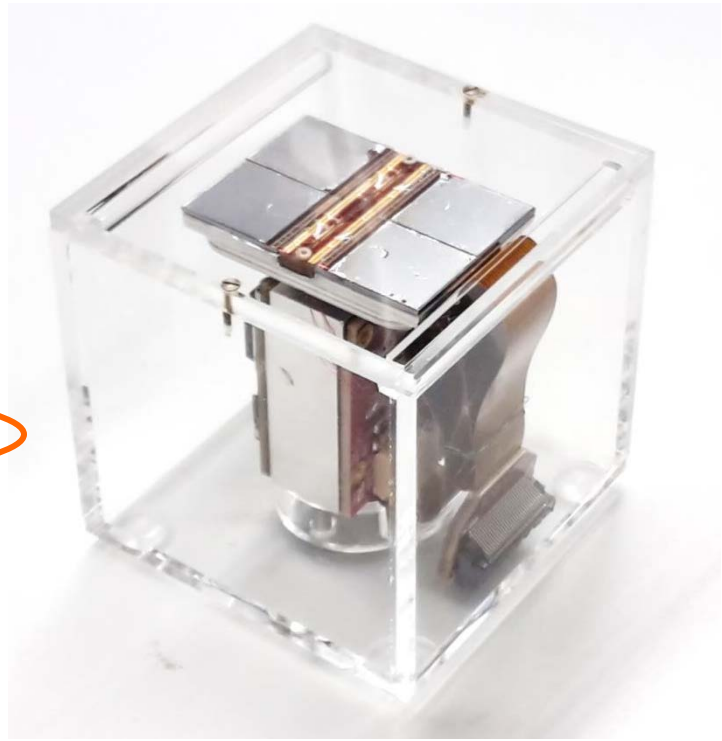
Assembling the guard electrode

- Covering the wirebond board
- Positioning by XYZ stage
- Attached by two M1.2 peek screws



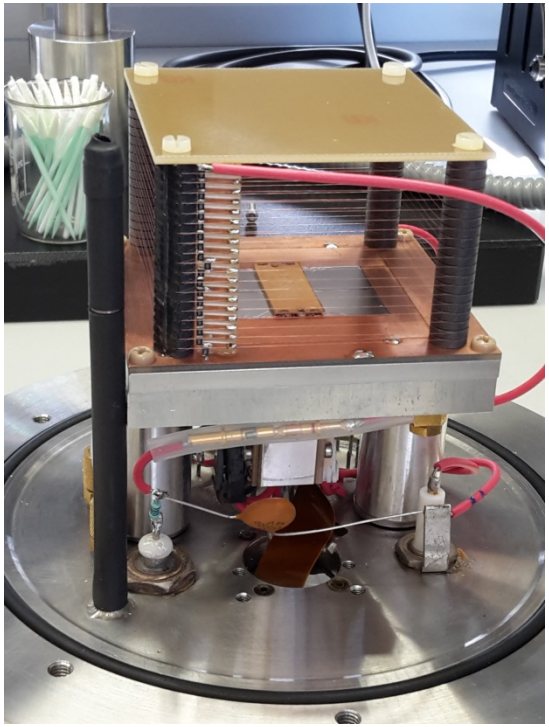
Status

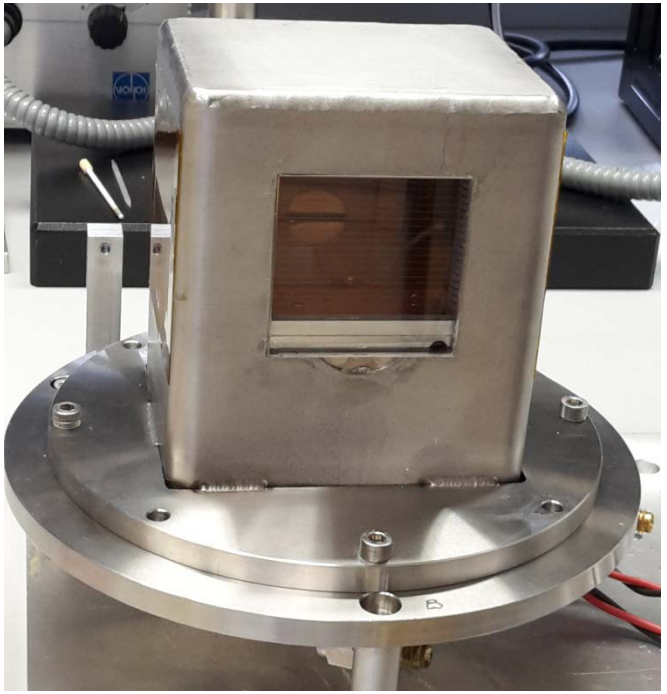
- One mechanical prototype assembled
  - Broken chips, bad grids
- Electrical prototype #1 assembled
  - Passed DAQ test
  - Damaged grids
- Electrical prototype #2 assembled
  - Passed DAQ test
  - Grid HV tested until 300 V
  - **Flex broken while improving the test box**
- Electrical prototype #3 being assembled
  - Presently software problems with DAQ test
  - One chip not functioning
    - Labelling error (Class K instead of class C)
- At present we have no PCBs and only a few chips
- New components (chips + PCBs) expected March 2018



Testbox for UV laser and test beam

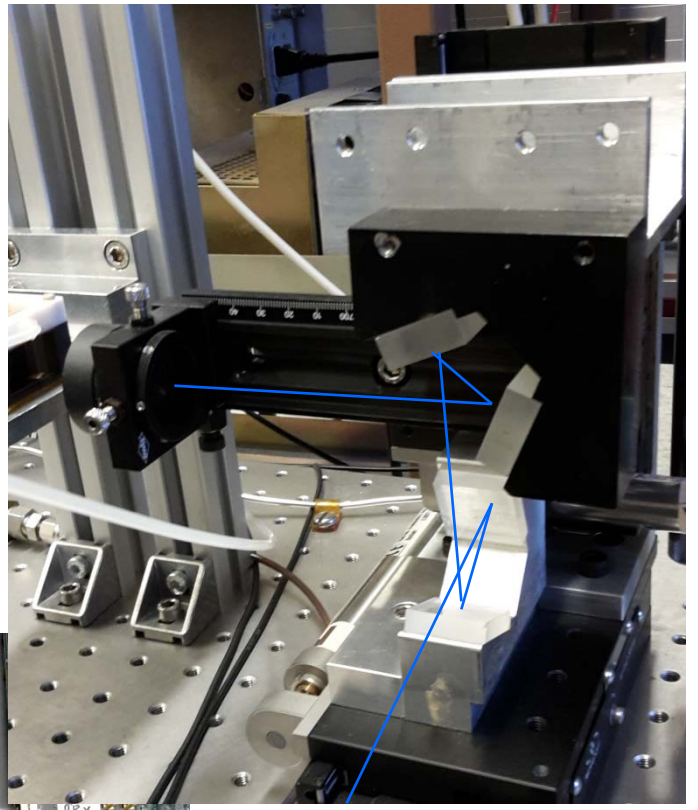
- SS box with UV-laser window and field cage
- Kapton foil windows at both sides

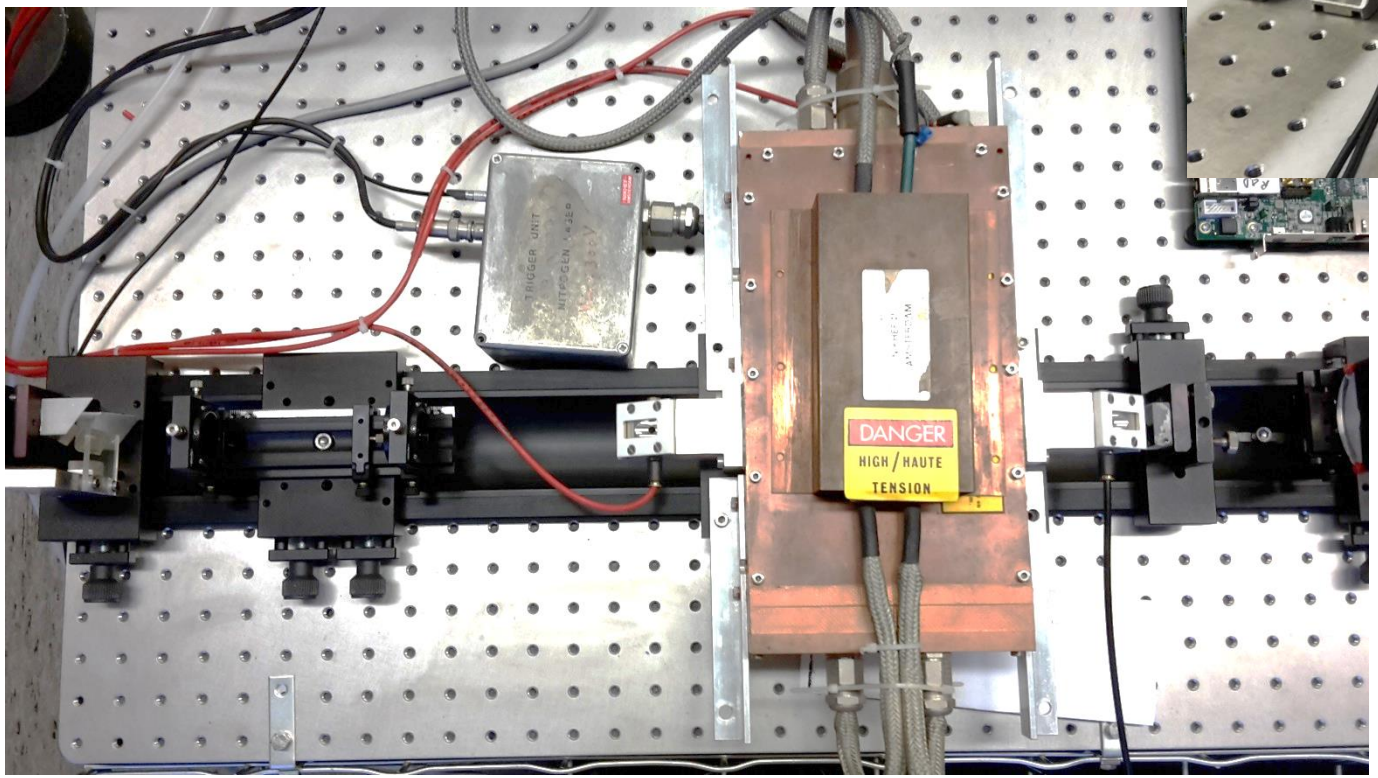


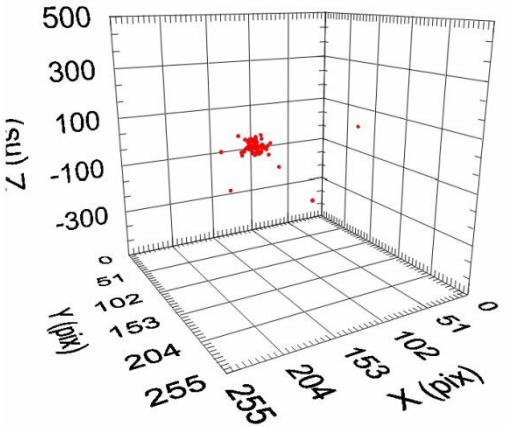


UV laser test bench

- Ionization cluster at the focal point
- Precise mirror control in X, Y and Z
- Ionization cluster can be positioned everywhere in the field cage



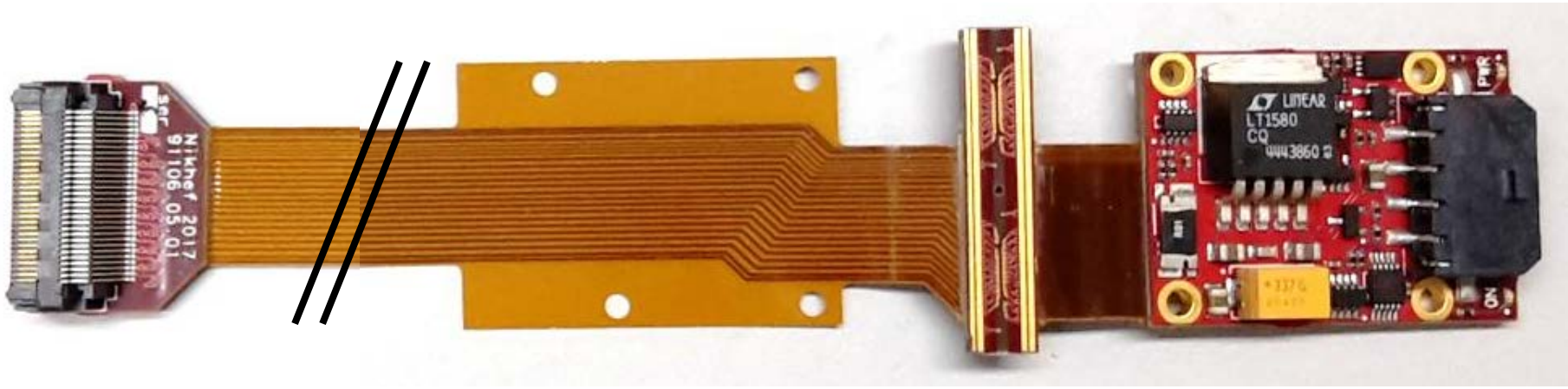




Future development

- **Problem**: presently extremely high price of wirebond board + flex
  - For prototyping 1100 – 1900 euro per QUAD, depending on quantities
  - Manufacturer: PCB Technologies Ltd (Israel)
  - High price caused by:
    - Special flex-rigid construction with 75 µm feature size
    - Blind-buried construction and filled vias
    - Worldwide only few companies can make such a product (not yet in China)

- We will widen the dyke (up to 1 mm) at wire bond side for next generation InGrids
- Greatly simplifying grid HV connection
  - Reducing guard width (11 => 9.5 mm)

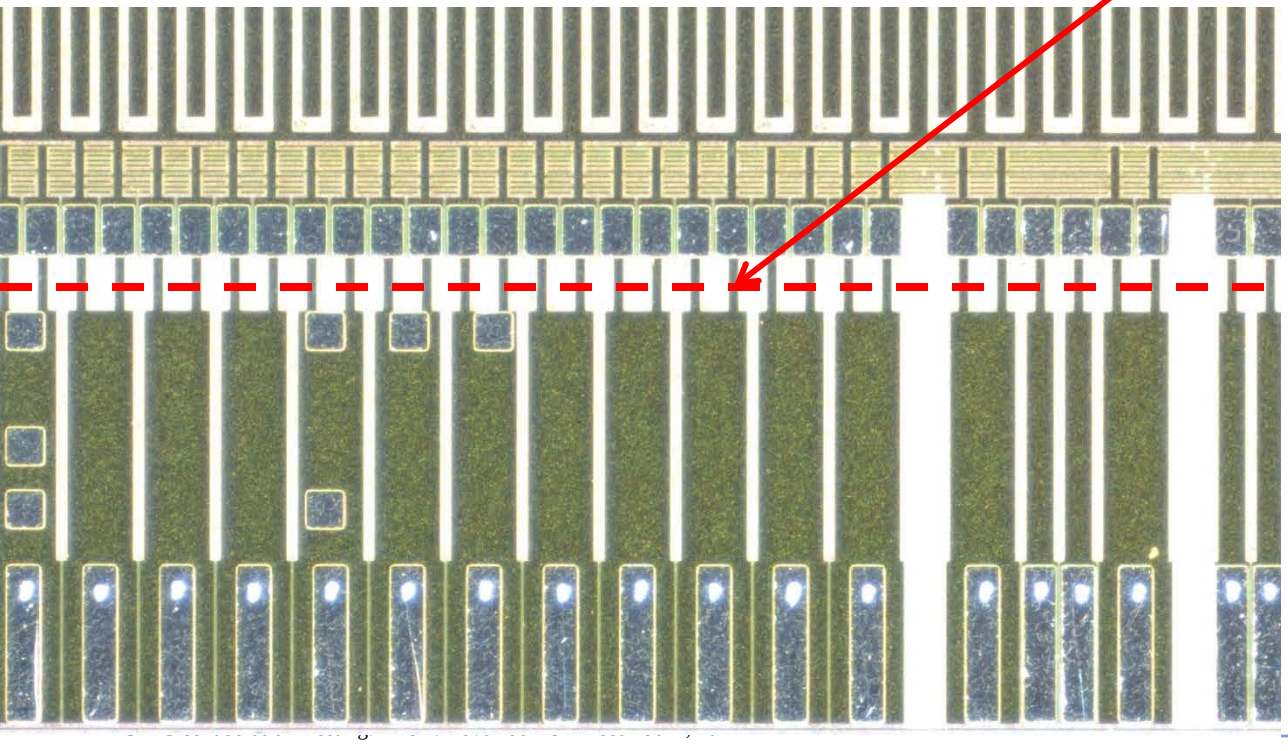


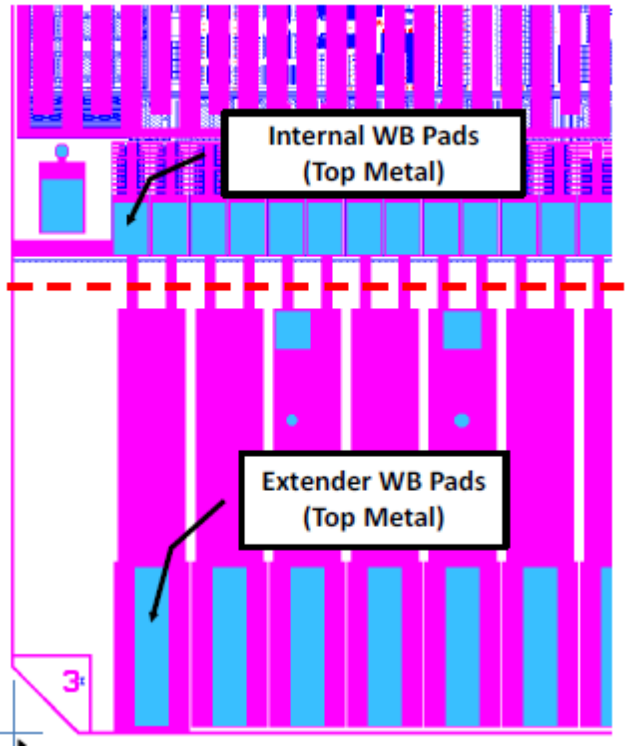
Through via option

- Alternative: use through-via option of the TimePix3
  - Probably cheaper PCB
  - Advantages
    - Reducing chip width by ~0.9 mm
    - Omitting the 6 mm wide wirebond PCB
  - => Reduce the width of the guard from 11 to ~3 mm
  - => **Active area** 68.9% => **86.4%**

In development at MediPix collaboration

Cutting line





Conclusions, outlook

- Assembly of QUADs is going quite smooth nowadays
  - For small prototype series (~20 items) ≥ 2/week looks feasible
- New production of QUADs to start March 2018
  - 10 PCBs planned
- Presently software problems with chip configuring and DAQ
- Critical grid HV connection on narrow dyke will be greatly facilitated at the next grid design (wide dyke at bonding pad side)
- In future we have to redesign the mechanics
  - Reduce the stump material
  - Use carbon composites instead of aluminium
- Applying **through via** technology will yield significant saving in costs and enlarging active are (> 86%)