Asian GEM module

Overall status

Budget of this fiscal year is very limited

what we can do is analysis and discussion

Analysis of Beam test data 2016

resolution

dE/dx (Aiko will report)

w/ Gate and w/o Gate

Gate R&D is not Asian module specific issue

No new R&D (waiting the result from beam data)

but we may need some production

to keep production technique at Fujikura

Simulation study will be reported by T.Ogawa

GEM R&D

better geometry

Simulation by T.Ogawa suggest wider hole diameter
for 100um thick

better material

Y.Kato continue GEM stability test
CERN, Scienergy, Laytech, Ceramic GEM ….

Module R&D

No progress

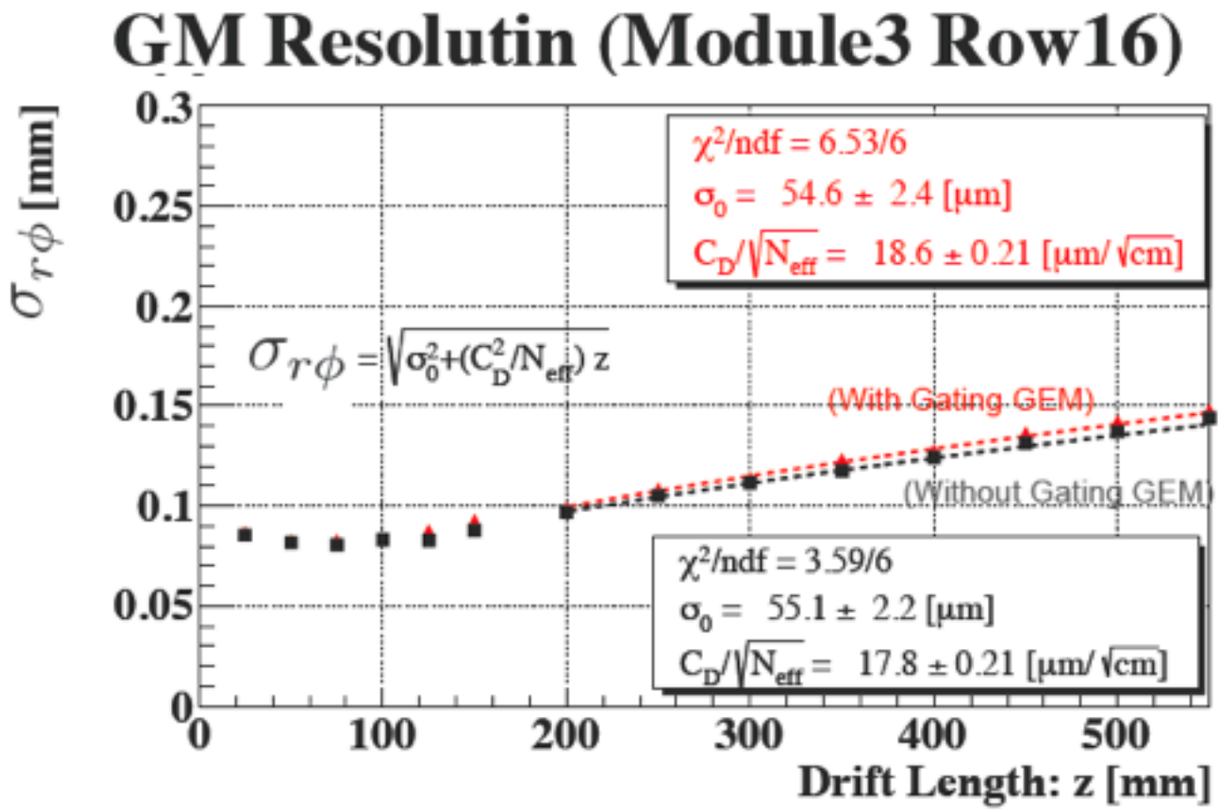
discussing issue
ion leaks from Gate/GEM
validity of our concept

Cooling R&D group wide issue

will be discussed by T.Fusayasu

Analysis of Beam test data 2016

Resolution study by Yumi Aoki



Resolution of w and w/o Gate behave similar

Cd/√N -> transmission of electron ~90%

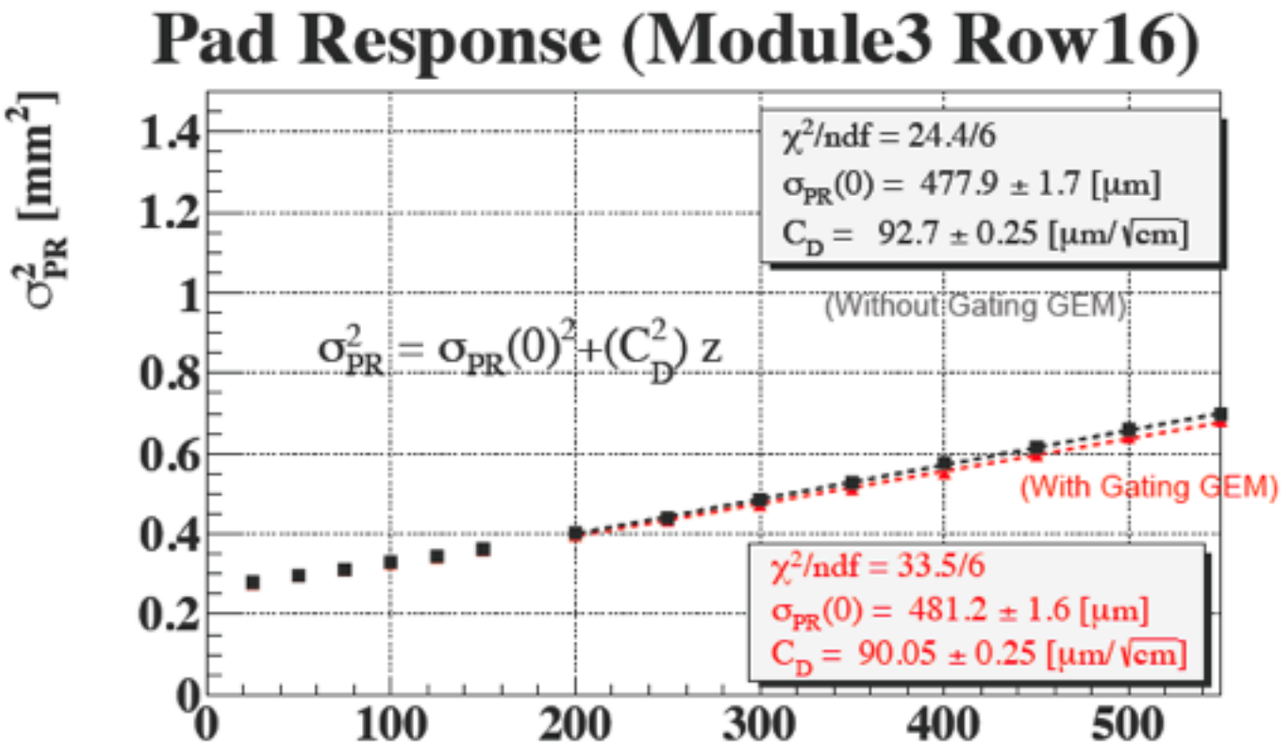
very rough number but almost consistent with test chamber

with Gate Cd/√Neff=18.6 ± 0.21 μm/√cm

without Gate Cd/√Neff=17.8 ± 0.21 μm/√cm

But.. ..

Cd should not be changed by Gate



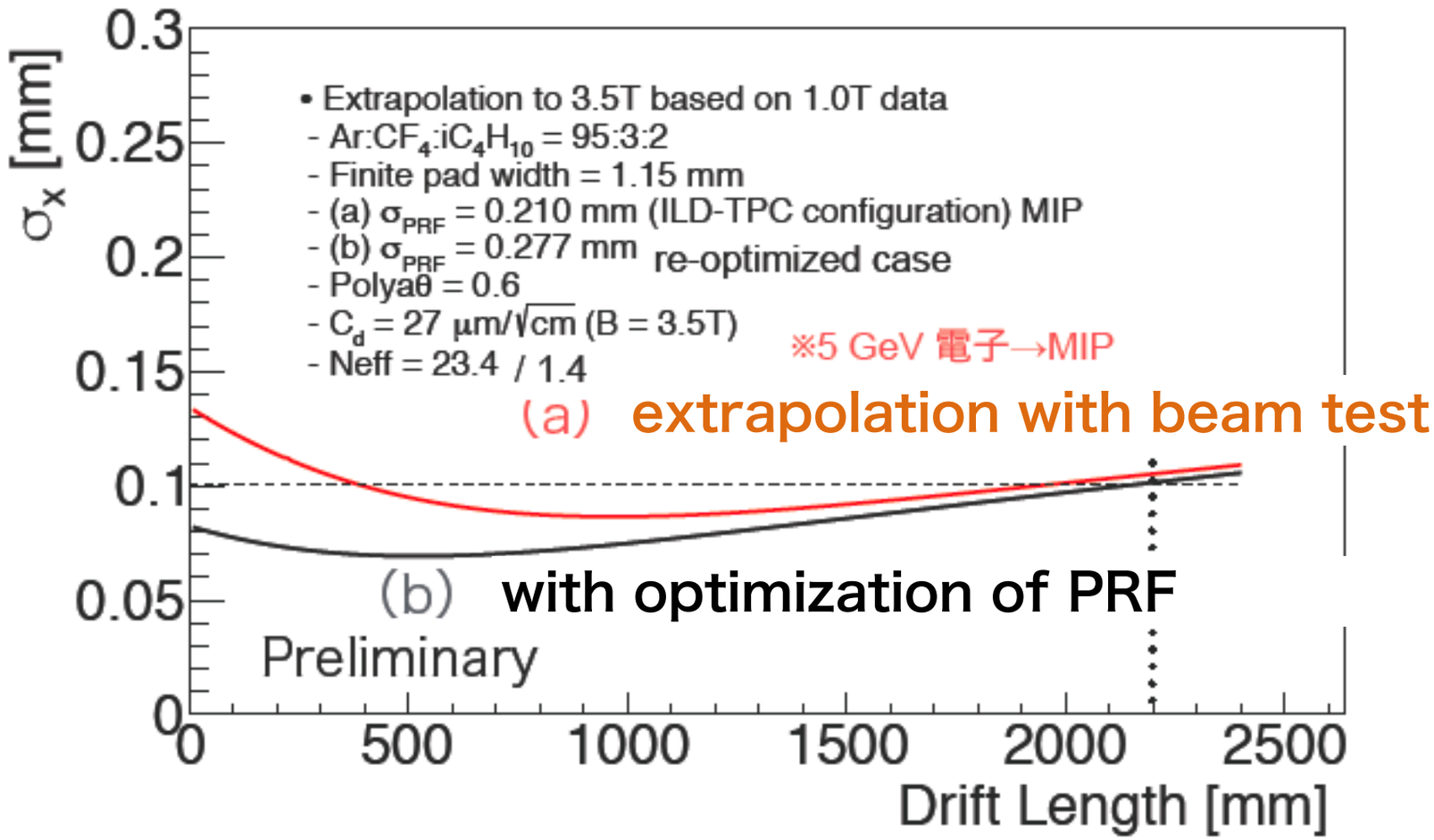
Cd w/o Gate is systematically larger than that w/ Gate.
for diff. pad-row, diff run

If we use obtained value transmission is ->

	with Gate	without Gate	
Cd [μm/√cm]	90.05±0.25	92.7±0.25	
Cd/√Neff	18.6±0.3	17.8±0.3	
N_{eff}	23.4±0.6	27.2±0.8	86.4±3.1

Investigation of Cd difference is on going

Extrapolation to ILD condition



>80% Gate + GEM system can provide required performance at ILC

3.5T mag. field reduce PRF (increase of 1 pad hits)

Cd @transfer region is high and ~plateau

increase amp. region? 6mm->10mm ????

any other methods?

this must be considered when we design the next module

Module Design

Gate-MPGD distance: need exact number of ion drift velocity

1cm or 5mm?

Diffusion coefficient is much smaller than electron

but ion drift velocity much smaller than selection

diffusion of ion is almost equal to thermal limit.

T.Ogawa's estimation is about 300um?@1cm drift under ILD

Ion leak happen? to us (no side frame) between Gate-GEM

Increase of MPGD introduce a risk of ion leak?

GEM/Gate holding structure

no progress at all

No side frame can reduce dead region?

no progress at all

Towards LOI (202x)

Demonstration of LCTPC
using realistic components

Module GEM + Gate
RO electronics + cooling system

connection between PCB and RO electronics
is essential for module design
sAltro16 MCM are based on small high-pitch connector
(LP1 conn. has X talk > 10% btw neighbor channel)
in order to save space for chips mount on BS as well as FS

Real TPC can use higher density chip
space limit can be compromised (?)
-> SACLEY's connector may have more potential
small connector and may have some room for cooling

Do we prioritize demonstration w sAltro?

What is the next module design to be ?

for demonstration ?

for future design ?

When Technology choice(GEM or Micromegas) happen?

When GEM module is unified? (before above)

No summary