

Status report on the SALTRO16 chip

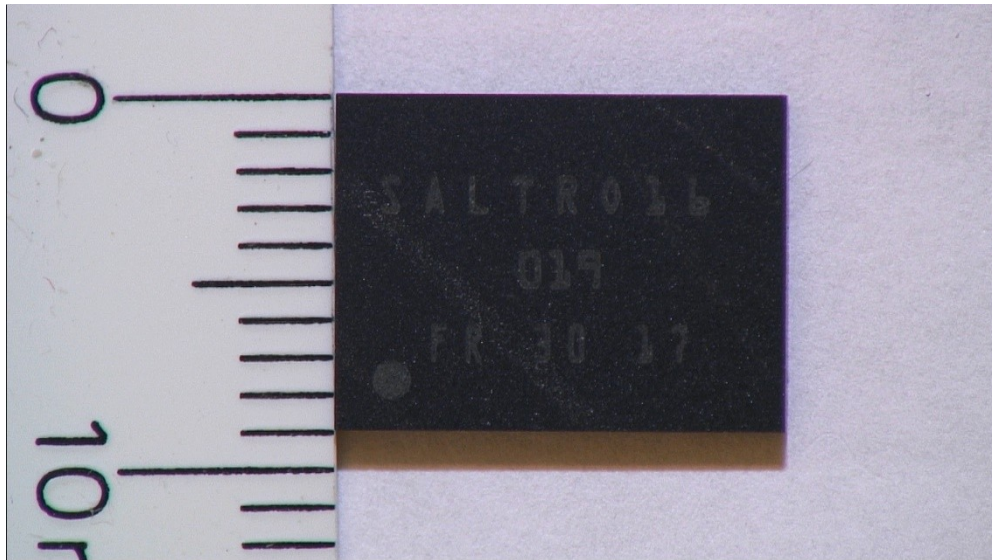
LCTPC Collaboration Meeting
29.11.2017

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Lund University

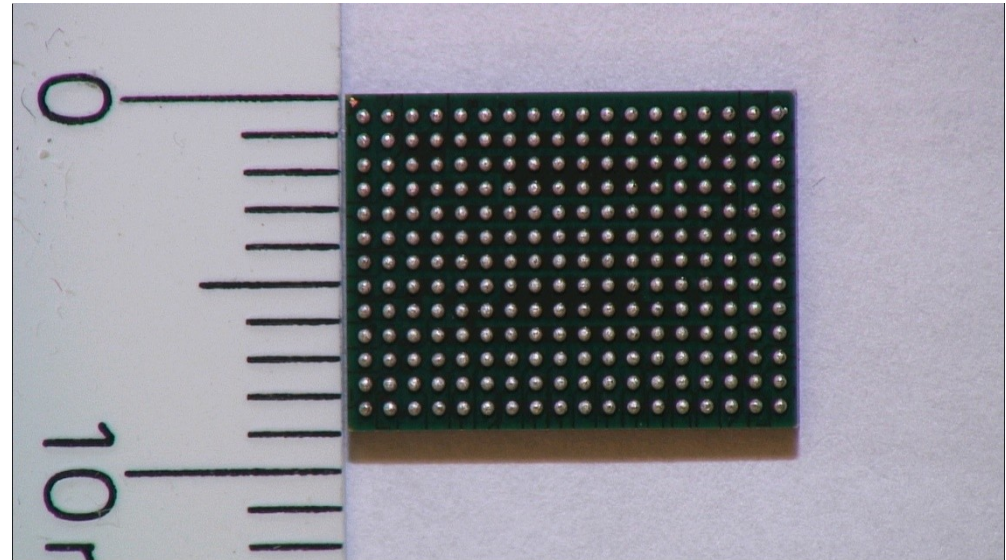
The packaged SALTRO-16 chip

- We have obtained a preseries of 34 packaged substrates, from the French company, for testing their functionality. The dimensions of the chip are 12x9 mm².
- In addition we have got 40 empty capsules, which will be used for soldering tests onto the MCM-board.
- The available number of dies is 840, after having got an additional batch from CERN. All dies are now at the French company. The substrates for all 840 dies have been ordered

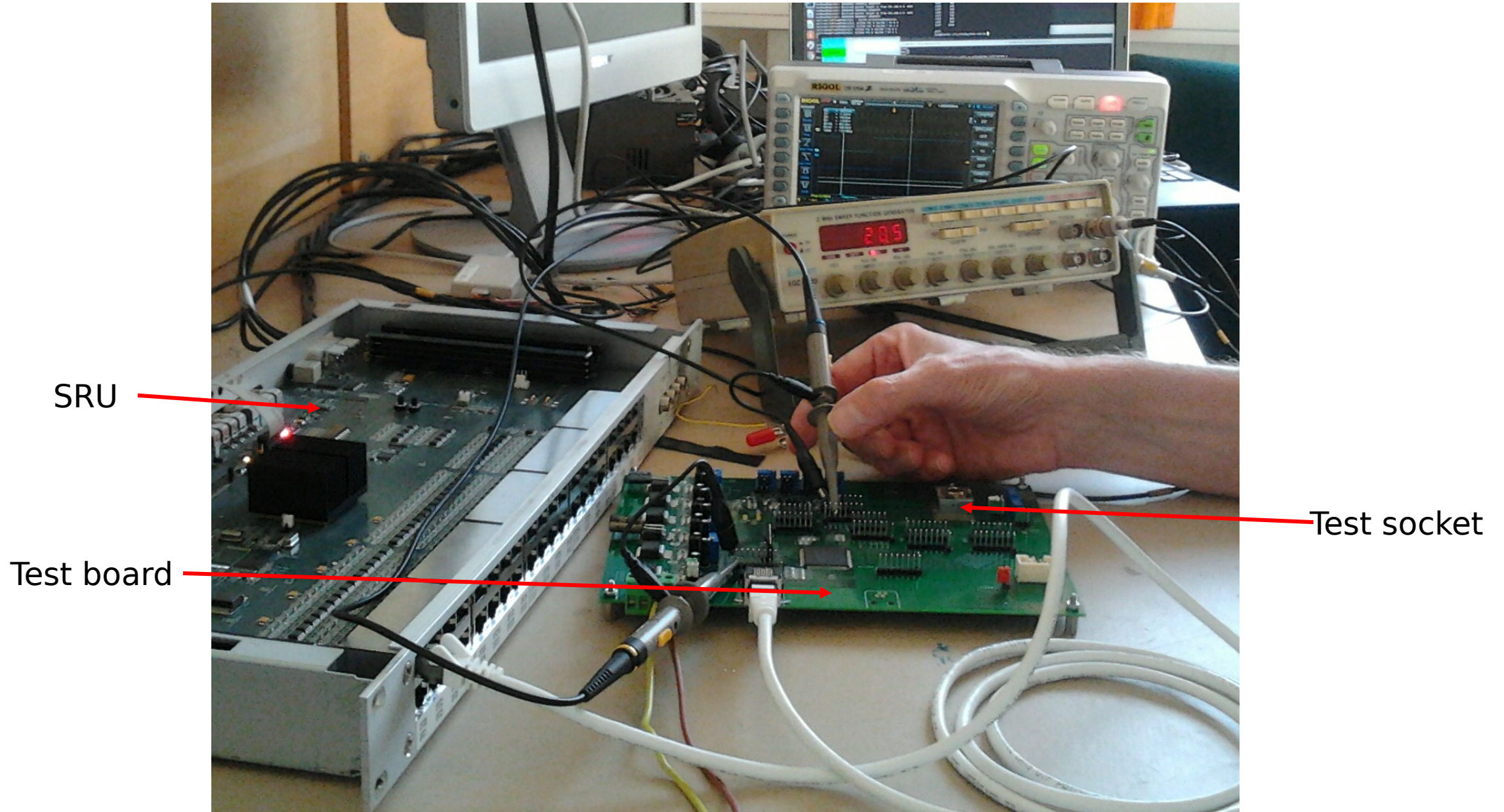
Top side



Bottom side

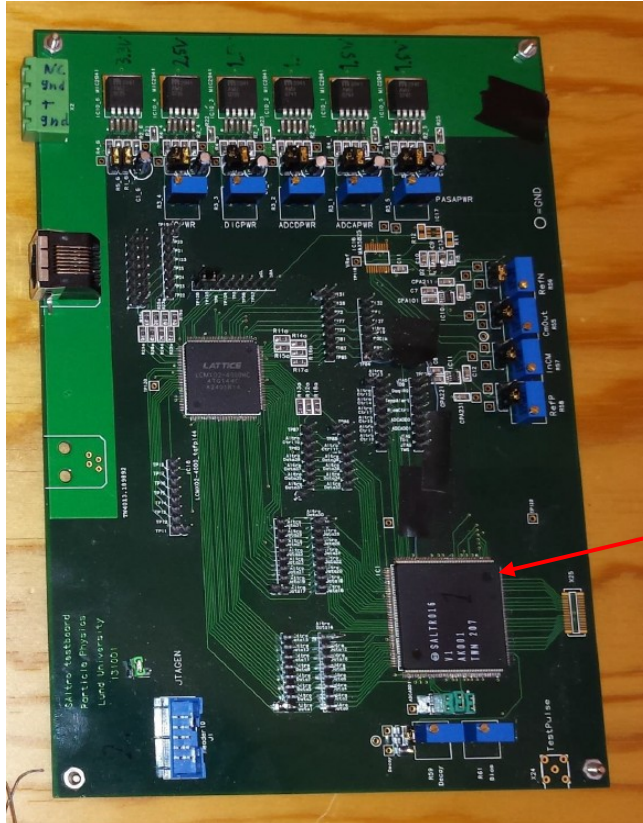


The presenttest set-up



Testing the test board

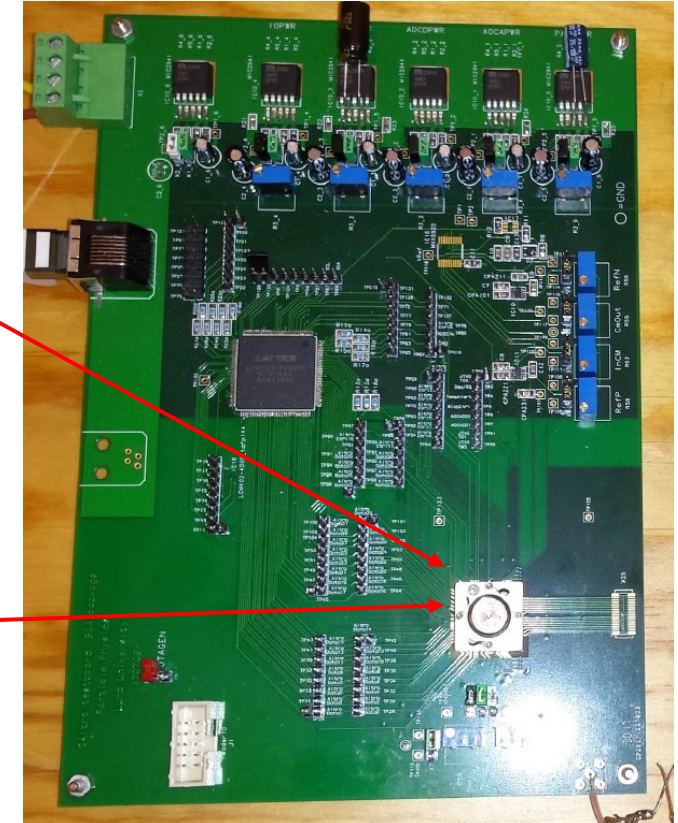
- In order to test the functionality of the test board it was equipped with a QFP-packaged chip, as used for tests at CERN.
- The chip that is mounted passed the CERN-tests.
- The tests in Lund gave results consistent with those from CERN \Rightarrow Indication that the test board is ok.
- On an identical board a test socket was mounted for tests of the BGA-packaged chips.



Area of by-pass capacitors
for the supply voltages
(bottom side)

Chip in QFP-package

Test socket



We have made a first preliminar test of all 34 chips to find out whether they are working or whether there are some problems. The results are shown in the table below.

Nr of chips	Test result
20	Passed the test
6	High-Low ADC-values for one channels per chip (see plot)
3	Bit problems for one channel per chip (see plot)
1	Short between power and ground
4	Don't work; no signals out

We are presently investigating what causes the problems. For the non-working chips we need an X-ray investigation.

34 chips x 16 channels/chip \Rightarrow 544 channels in total.

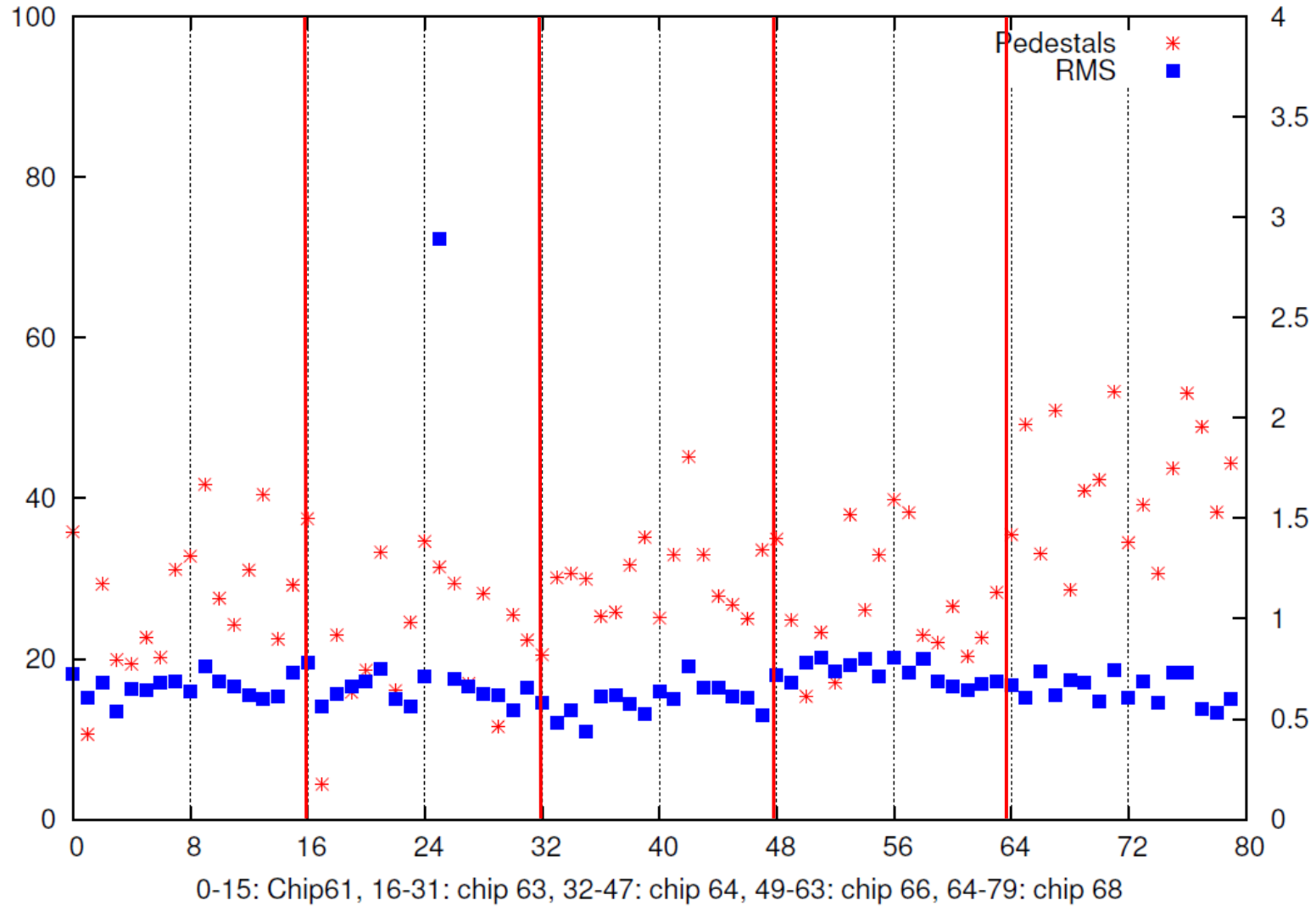
Number of channels with problems 9.

Number of dead channels $5 \times 16 = 80$.

Percentage of good channels 84%.

If we assume that 4 dead chips are the expected waste from untested dies we get 95 % good channels.

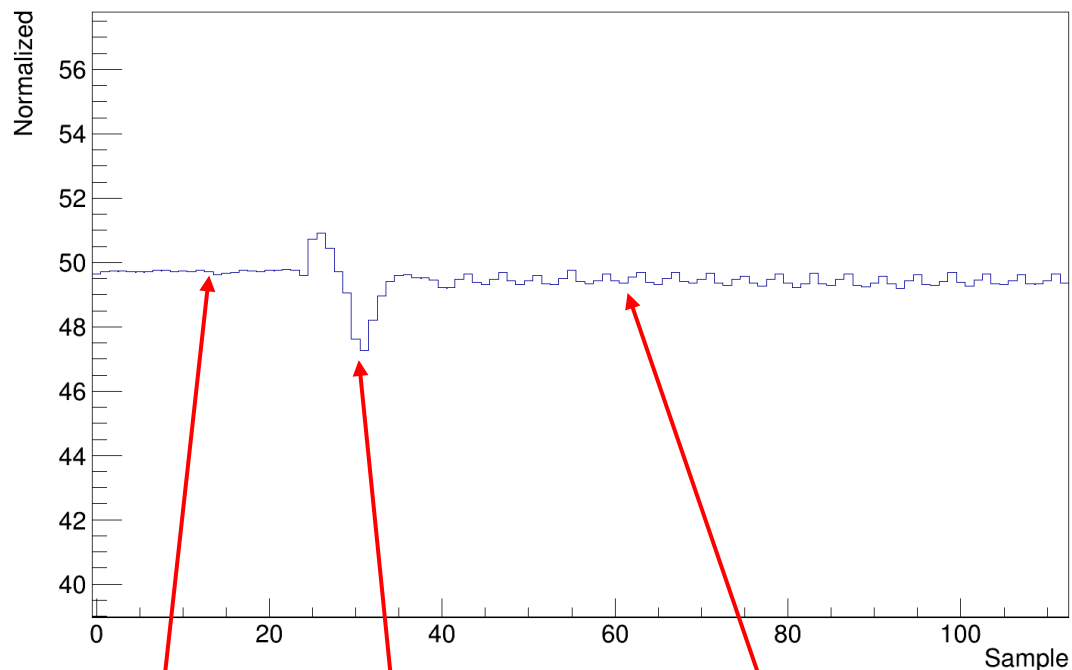
Pedestals (left y-scale) and rms (right y-scale) for 5 chips
(gain=12.5,shaping=120,decay=0.5V)



The average RMS noise is around 0.7 ADC channels \Rightarrow equivalent number of electrons \approx 350

Pedestal

Norm samples run 19879 ch 1 entries 200



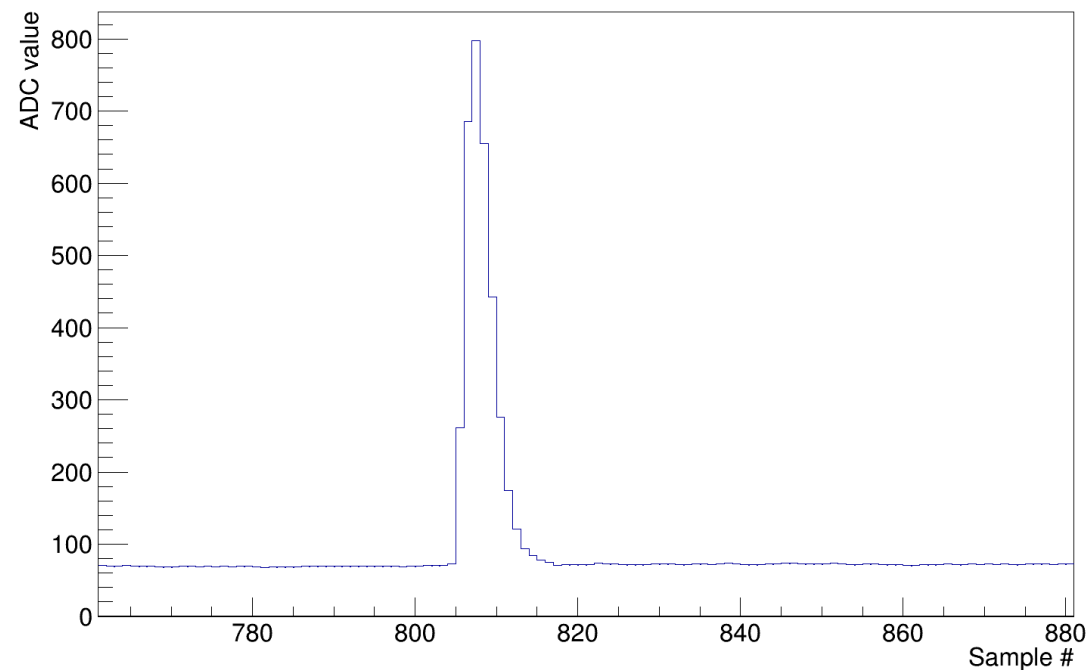
Pedestal
before trigger

Trigger

Pedestal after trigger
Pattern caused by the
sampling clock

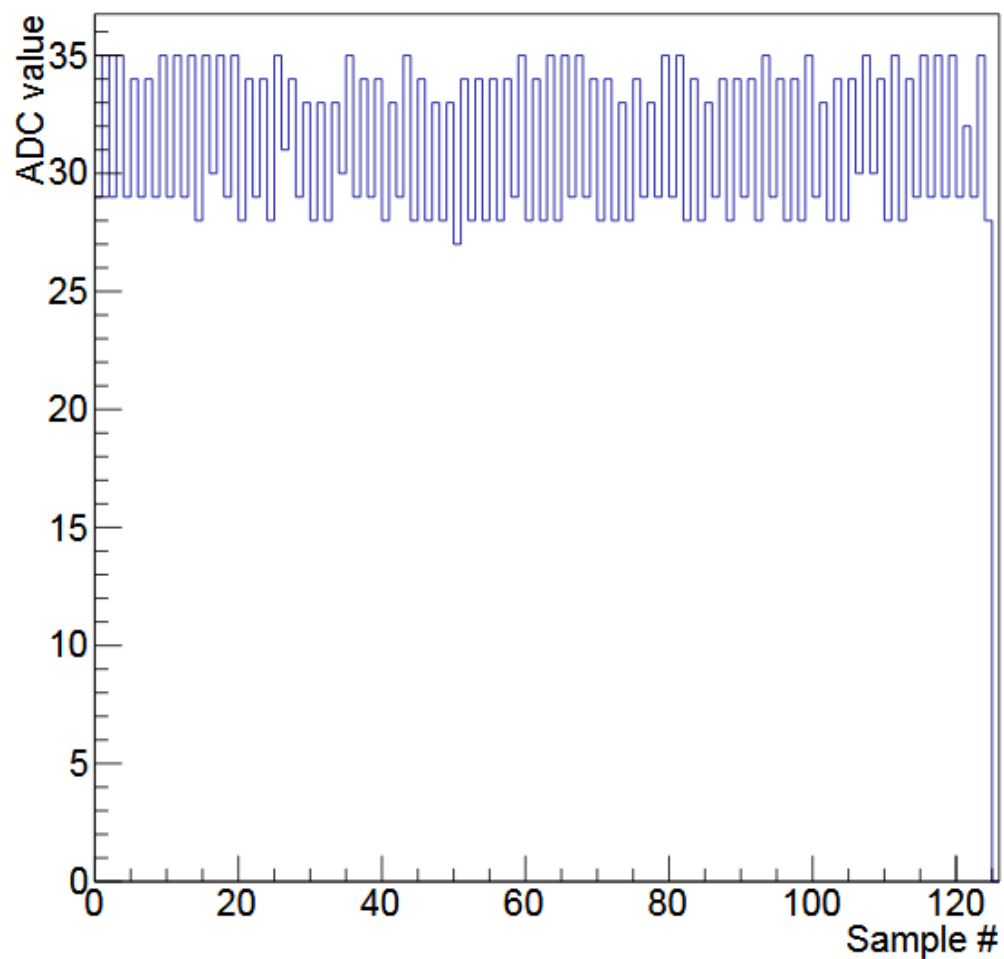
Signal

Run 19777 Event 2 Channel_14



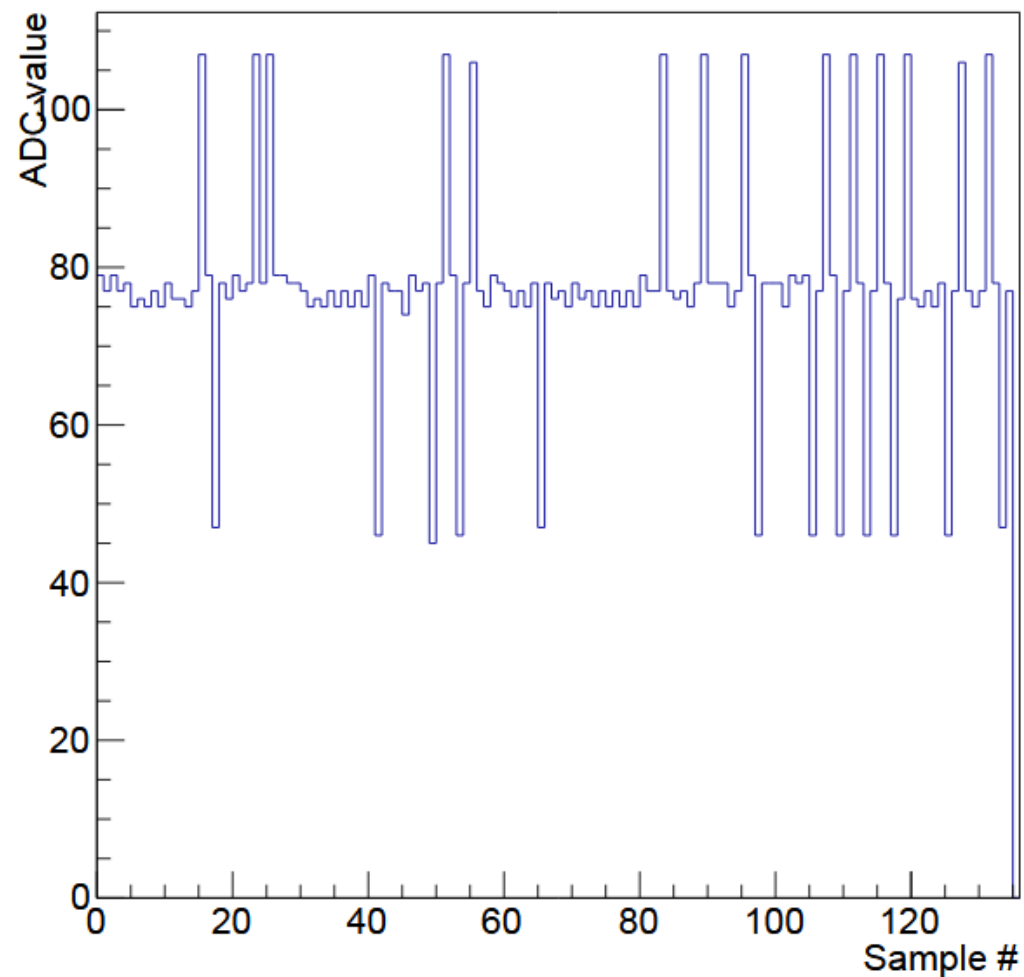
The 'high-low' problem

Run 20088 Event 1 Channel_9



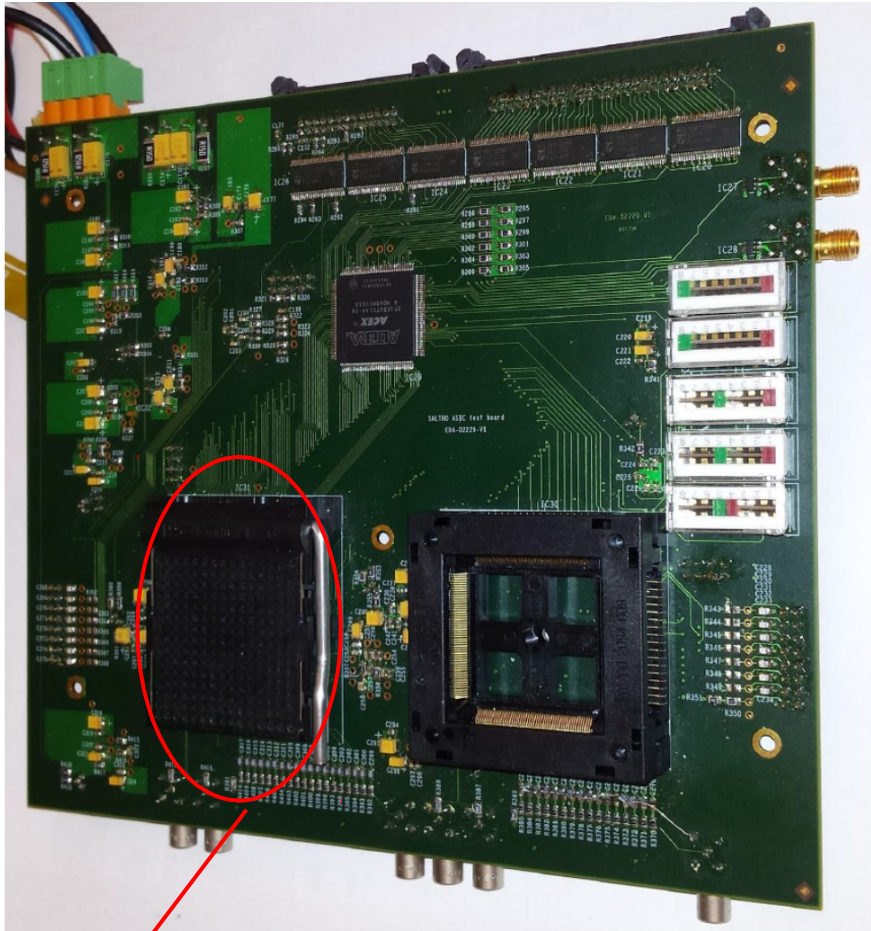
The 'bit'-problem

Run 20448 Event 1 Channel_14

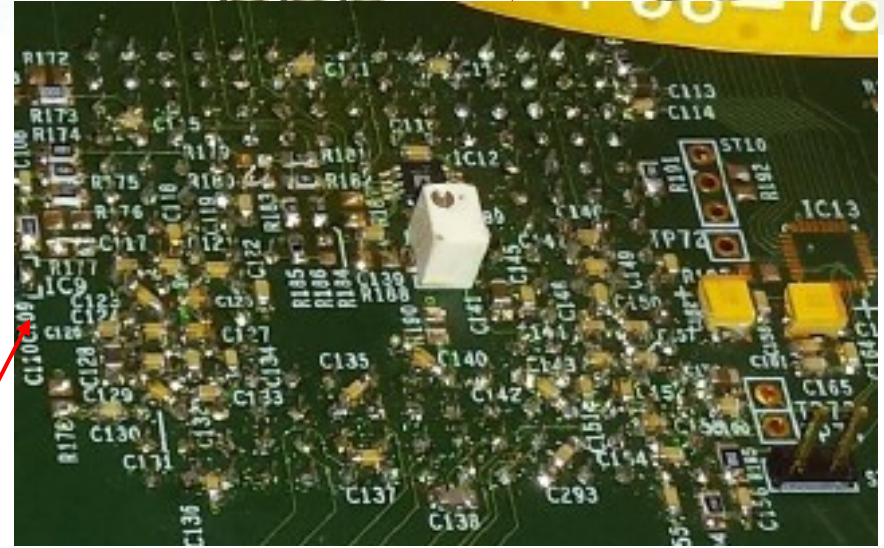
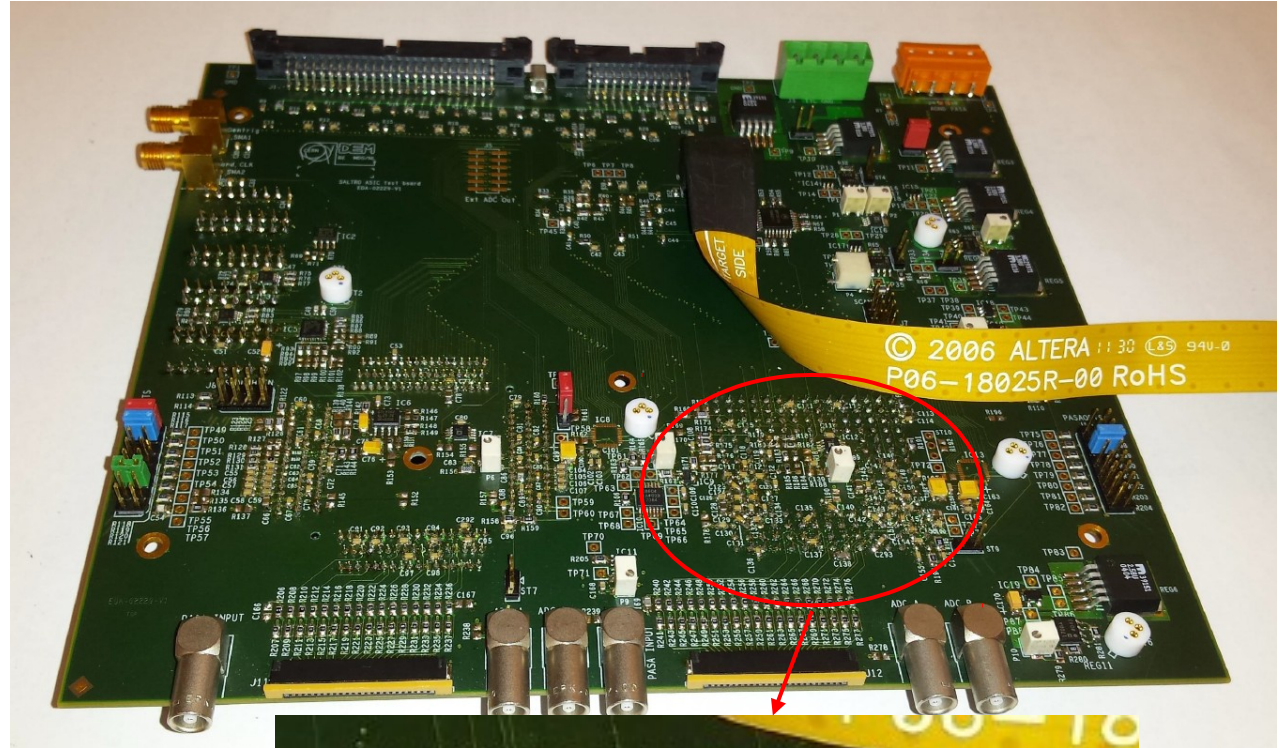


CERN Test Board

Top side



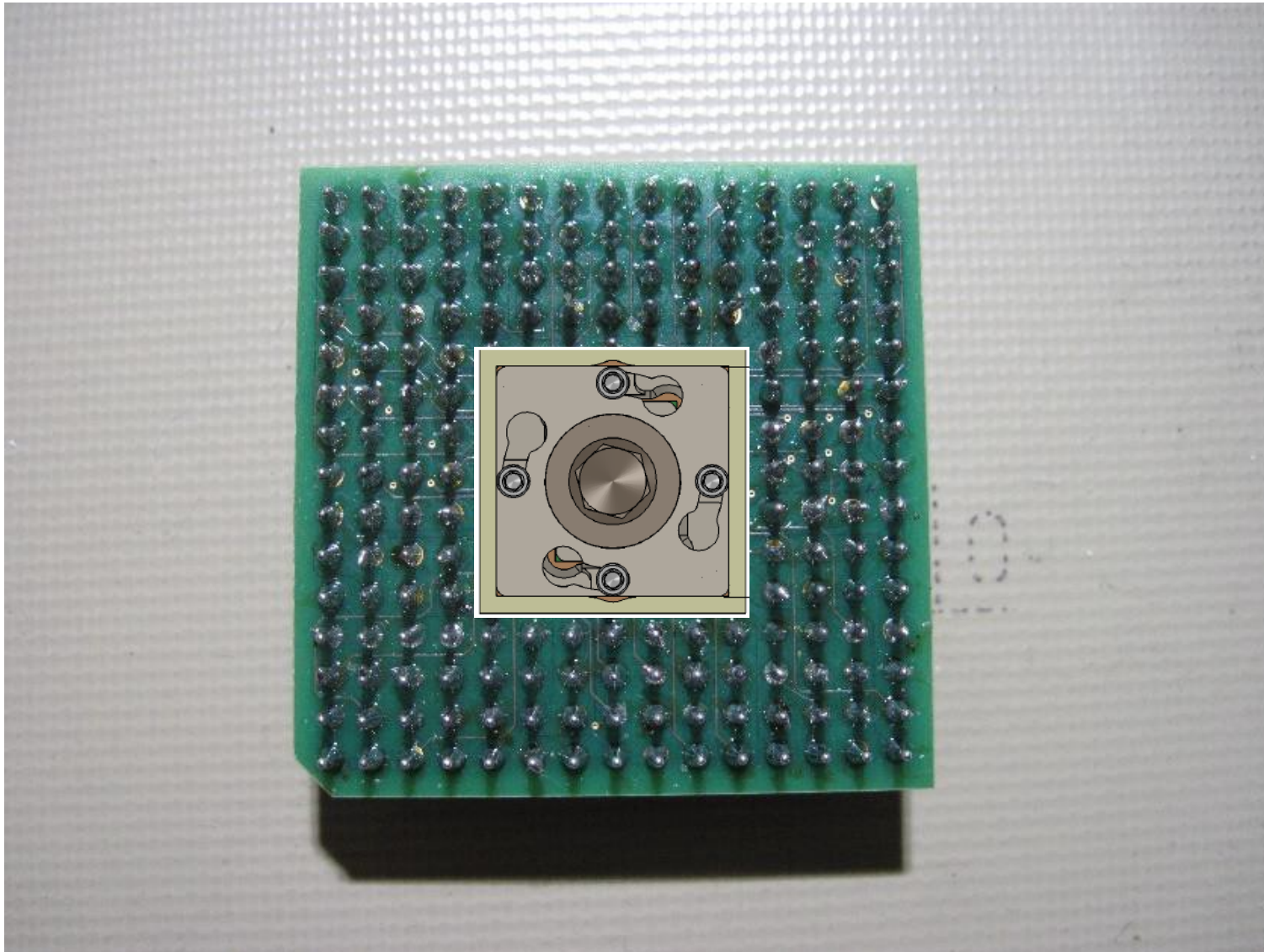
Bottom side



PGA-socket
Here an adaport board with a test socket will be plugged in

Area of by-pass capacitors to suppress the pick-up noise

The adaptor board



Summary

A contract has been signed with a French company for packaging our SALTRO16-chips.

The first pre-series of 34 chips has been delivered.

The first preliminar tests have been performed. Some problems have been discovered and are presently being investigated.

After successful tests: The full production will start.

The modifications of the MCM-board will be done.

Soldering tests of the empty packages onto the MCM-board will be performed.