Tile Detector

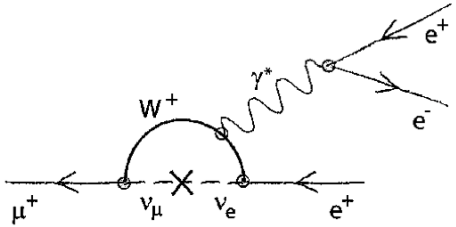
Mainz
March 8, 2018

Yonathan Munwes on behalf of the Tile Detector group

Introduction – signal

- Charged LFV $\mu^+ \rightarrow e^+e^-e^+$
- SM Branching ratio $\mathbf{<10^{-54}}$

  -> unobservable!



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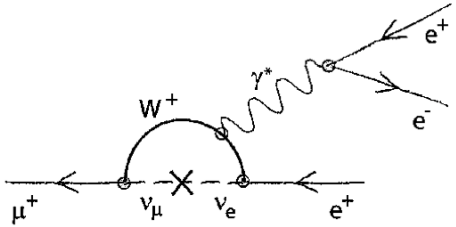
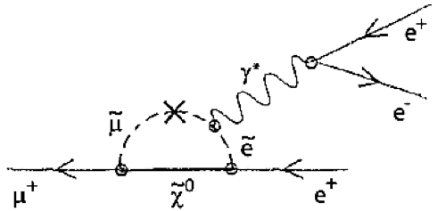
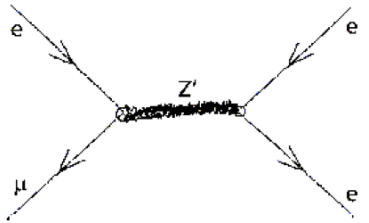
- Enhanced in (BR>1×10^{-16}):
  - Grand unified models
  - Super symmetry
  - Left-right symmetric models
  - Extended Higgs sector
  - Extra dimensions (Kaluza-Klein tower)
  - …





Loop diagram



Tree level

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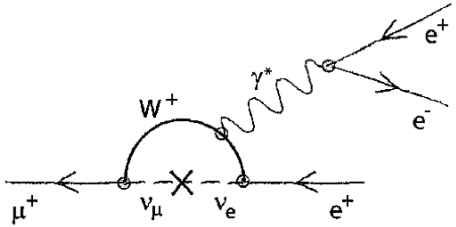

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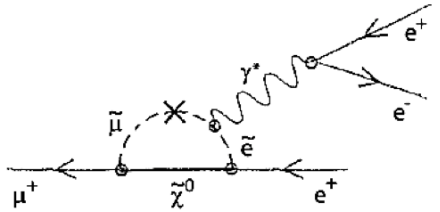

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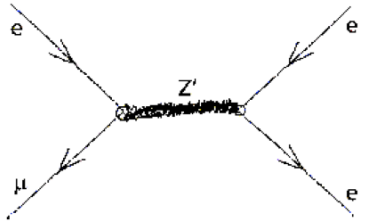
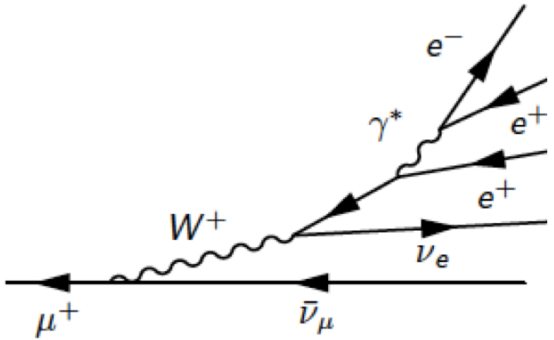


Tree level

- The current best limit >1×10^{-12} (SINDRUM 1988)
- Mu3e experiment aims for BR~ 10^{-16}

Background sources – internal conversion (irreducible)

- Internal conversion in SM 3.4×10^{-5}

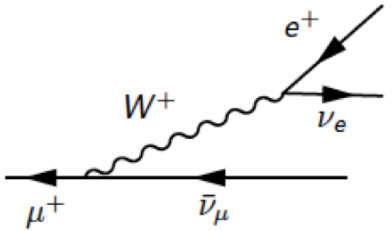


Missing energy

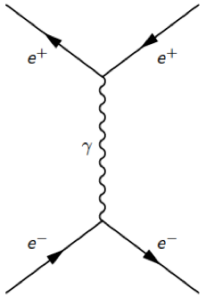
- Only distinguishing by missing momentum carried by neutrinos
- Need excellent momentum resolution!

Background sources – accidental background

- Michel decay (SM 99.997%) – generating e^+



- Bhabha scattering
  (e+ scattering with e in the target)



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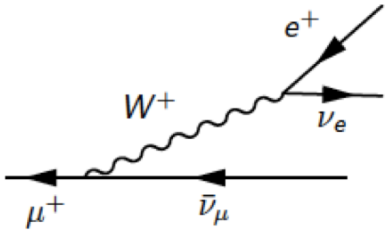

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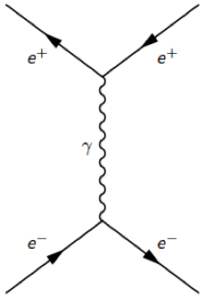

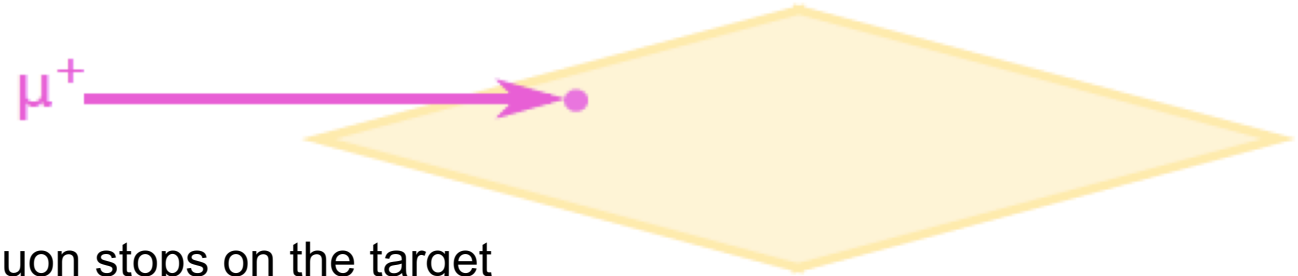

Positive muon stops on the target

Background sources – accidental background

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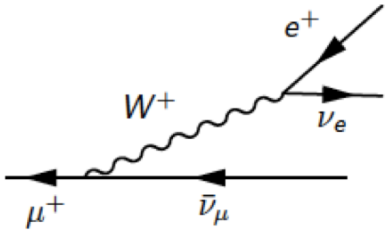

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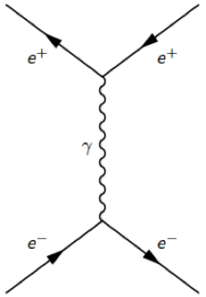

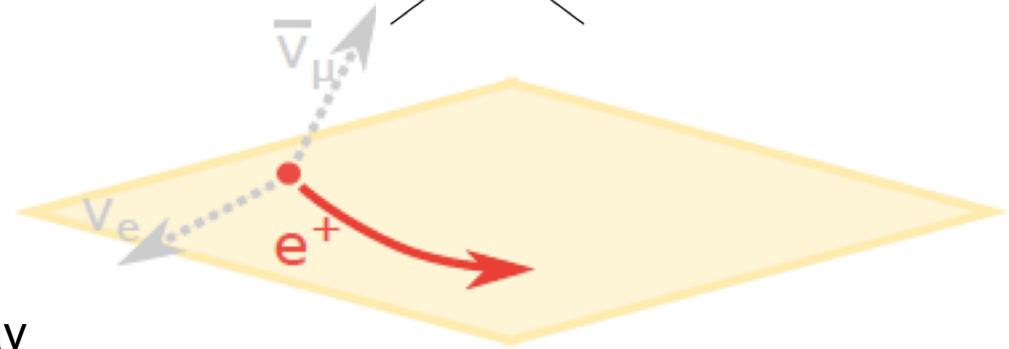

... Makes a Michel decay

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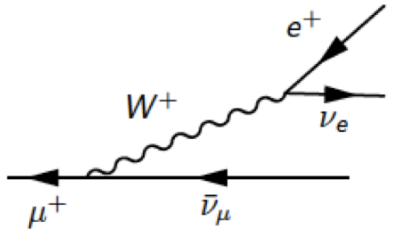

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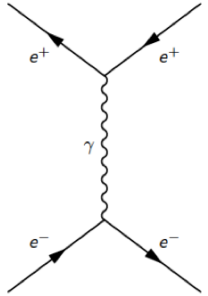

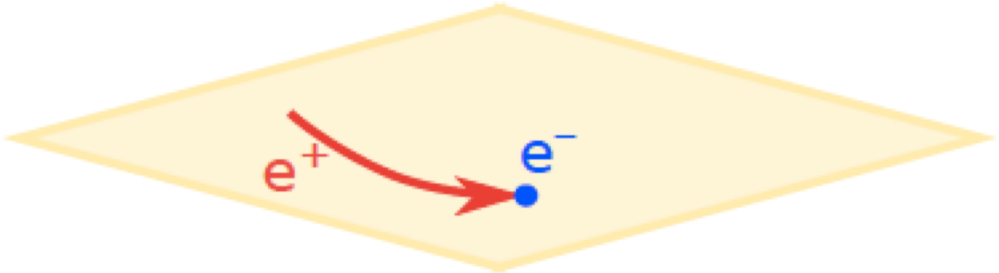

Positron hits an electron...

Background sources – accidental background

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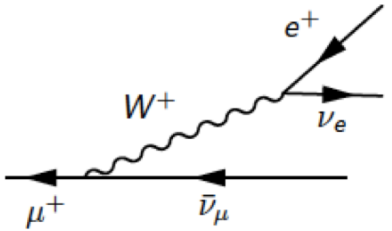

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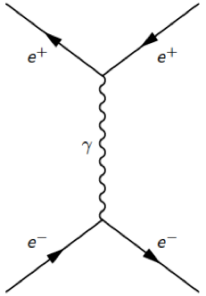
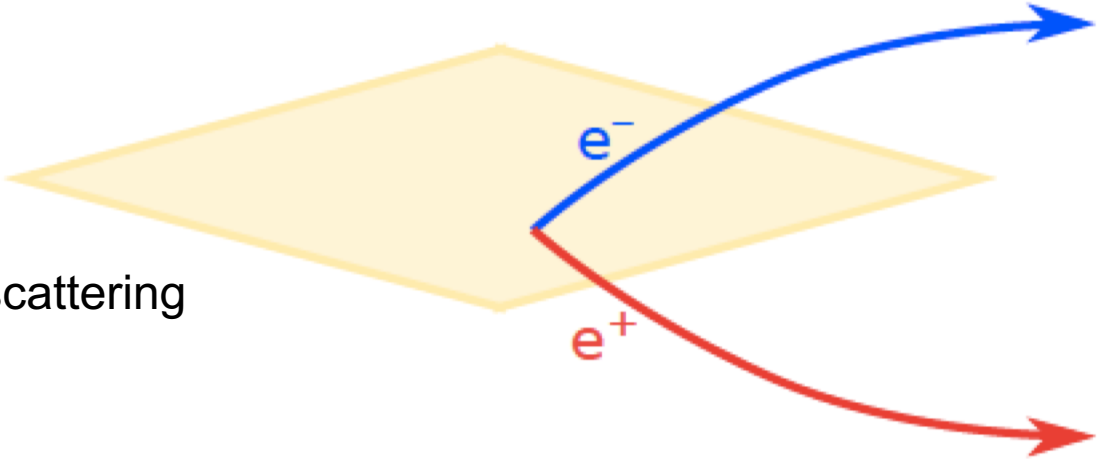


... Undergoing Bhabha scattering



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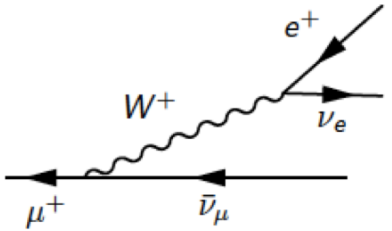

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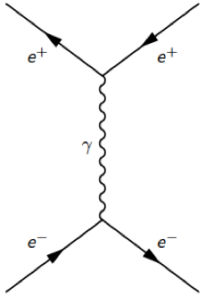

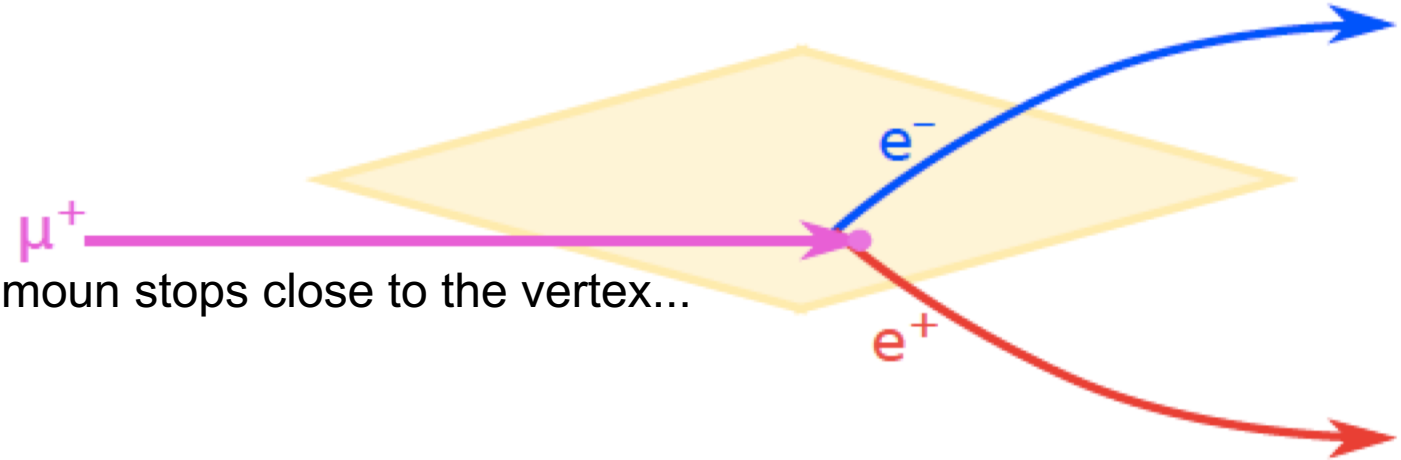

If another moun stops close to the vertex...

Background sources – accidental background

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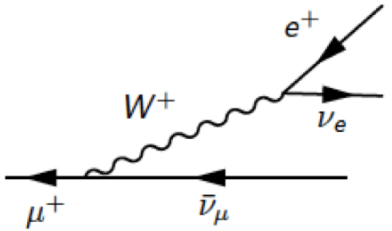

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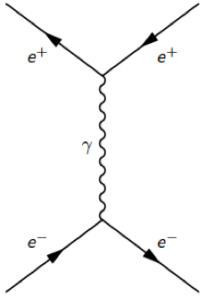

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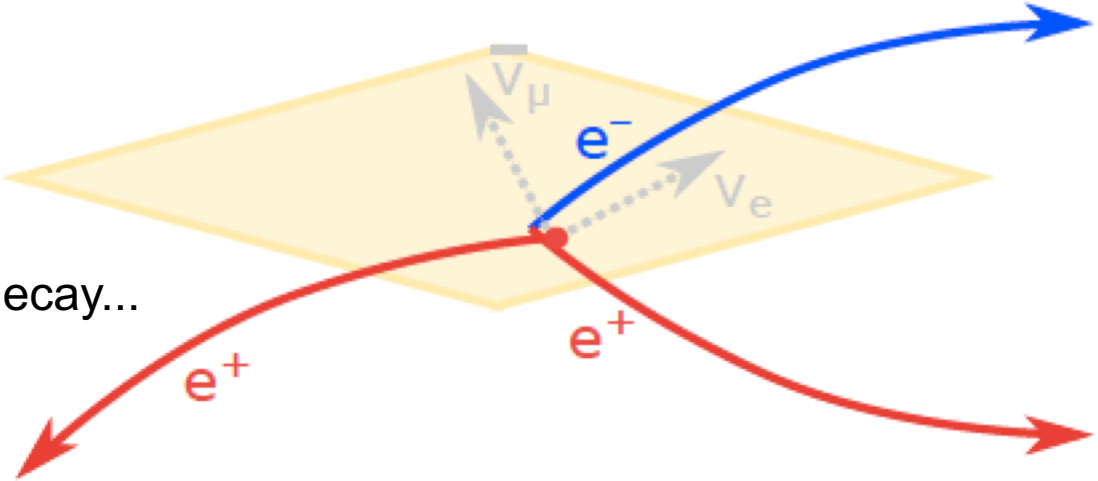

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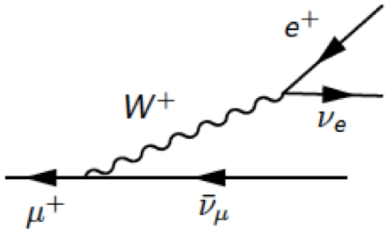

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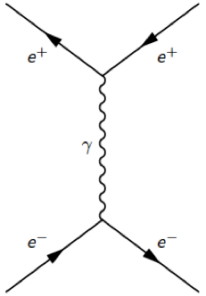
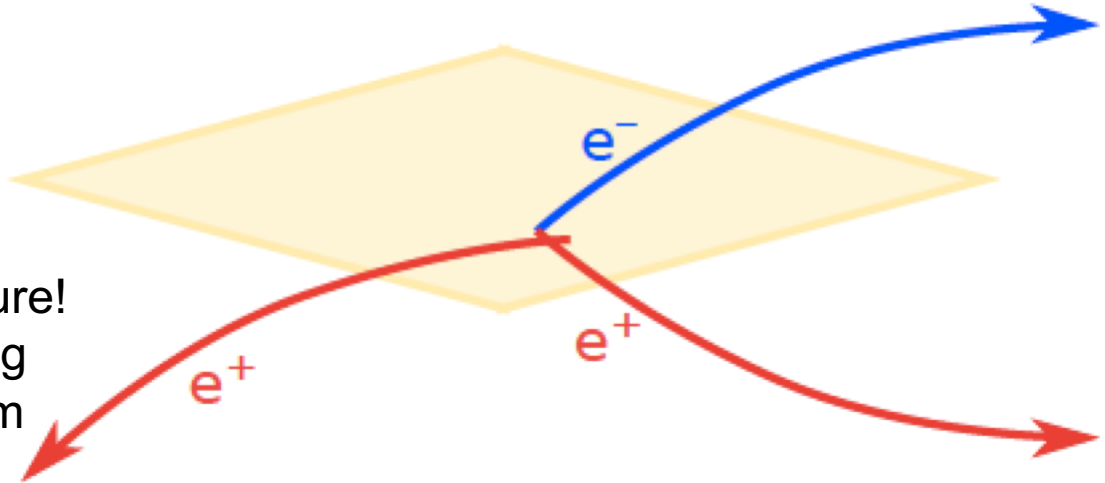
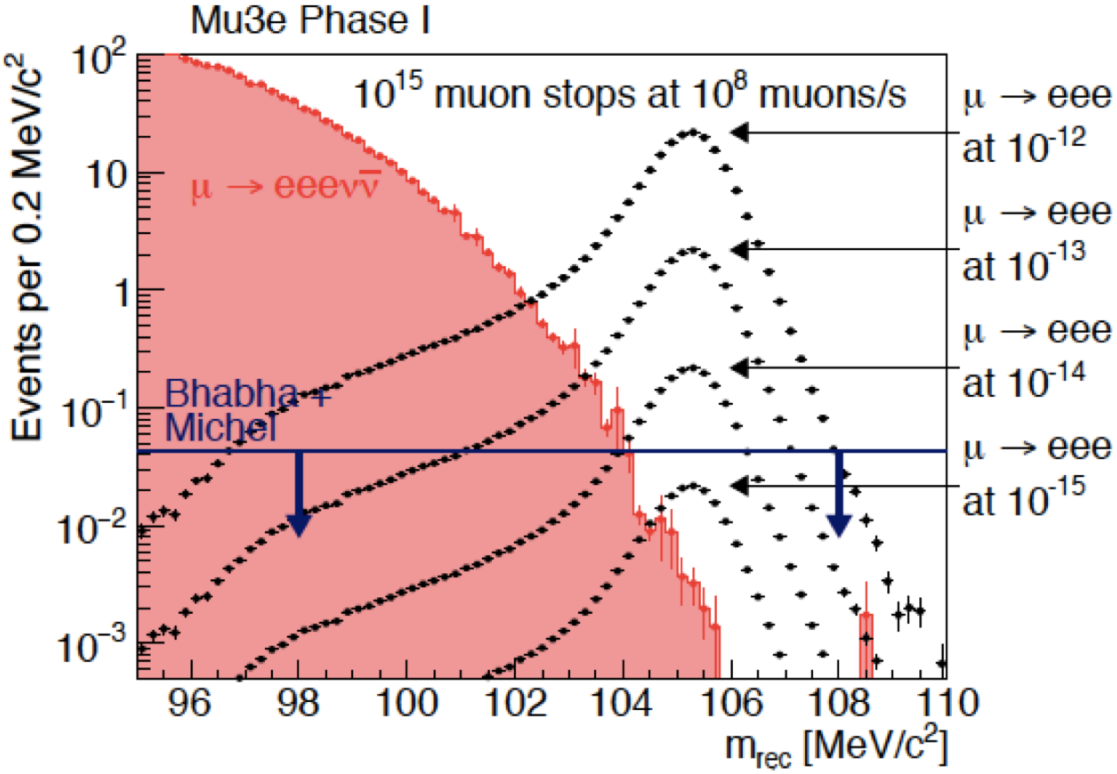




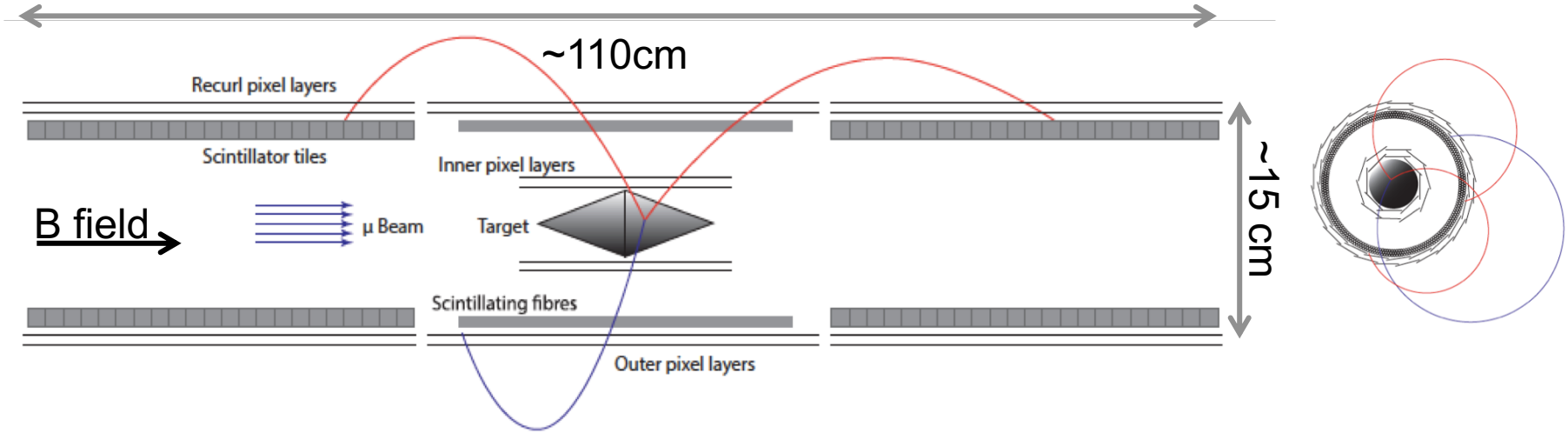
We got the basic signature!

- Need very good timing
- vertex and momentum resolution

Mass reconstruction



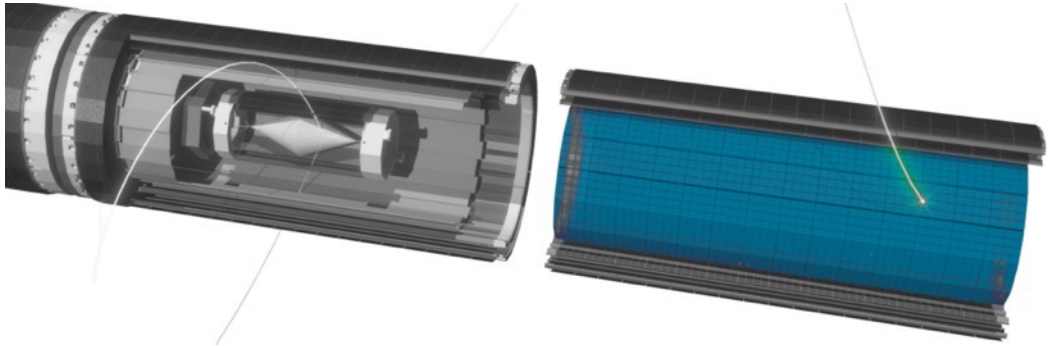
The Mu3e experiment – phase I



Key requirements:

- High muon stopping rate ($O(10^8$ muons/s))
- Vertex resolution ~200 μm
- Momentum resolution ~ 0.5 MeV
- Require low material budget
- Fiber time resolution < 500 ps (accidental background suppression)
- Tile time resolution < 100 ps (coincidence and event separation)

The Tile detector



Requirements

- Detection efficiency close to 100%
- Time resolution better than 100 ps
- Maximum hit rate up to 60 kHz/channel
- Enough energy resolution for time walk correction

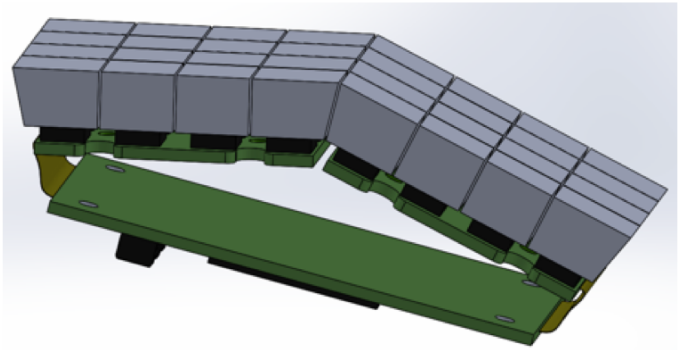
Background suppression factor

Tracker hits	Fibers	Tiles	Both
≧ 4	35	5.3	72
≧ 6	44	5.3	102

Detector overview

Submodule

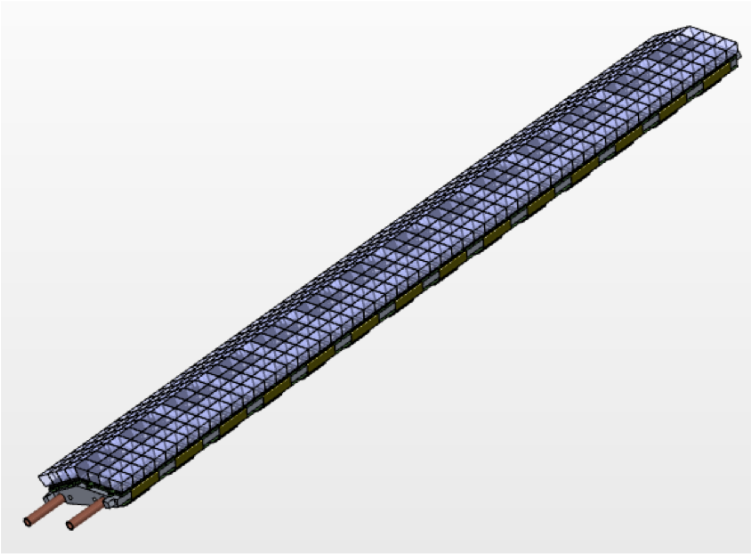
- 32 channel
- 3x3 mm^2 SiPMs
- FEBA – flex printed PCB
- MuTrig ASIC in BGA package
- Scintillator tiles Ej-228 ~6.5x6.5x5 mm^3 , two type (center and edge)
- ESR reflected foil, individual tile wrapping

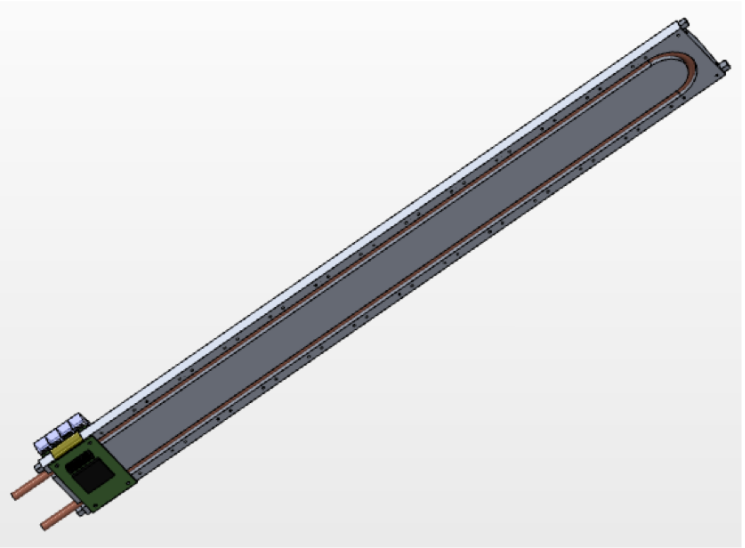


Detector overview

Moudule

- 14 submodule mounted on the cooling structure
- Water cooling
- 448 channels





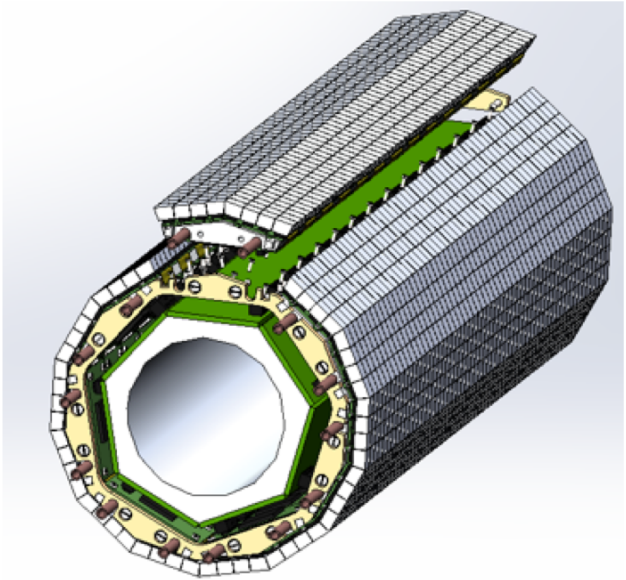
Detector overview

Recurl station

- 7 modules mounted on end rings
- Total length 36.8 cm
- 3136 channels

Full detector phase I

- 2 recurl station – total of 6272 channels

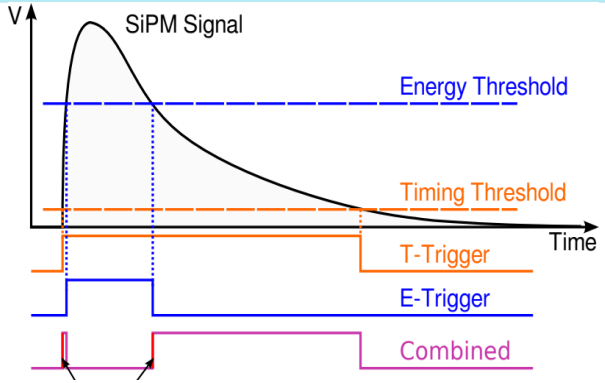


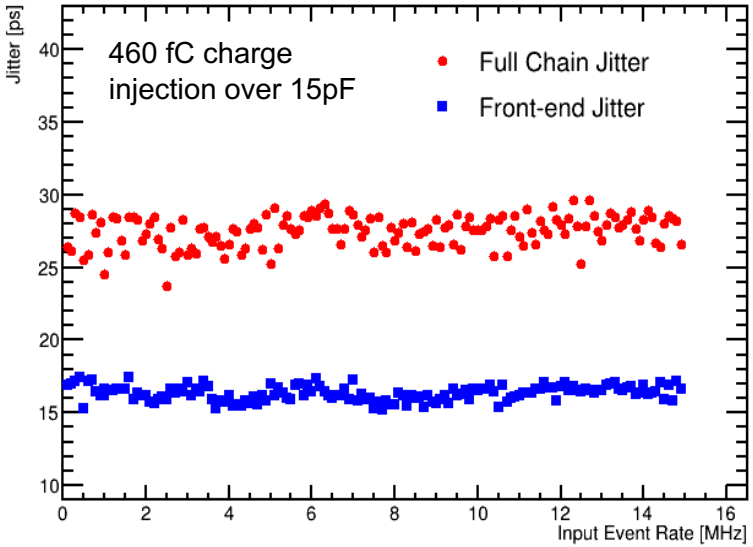
ASIC development

- 32 channels muTrig ASIC - developed in KIP HD (same front end of STiC 3.1)
- Gigabit serial data link (1.25 Gbps)

Two readout option:

- 48 bit/event (Tile detector):
  - both time and energy info
  - Event Rate limit: 20.24 MHz (632 kHz/ch)
- 27 bit/event (SciFi detector):
  - time info. + 1 bit energy info.
  - Event rate limit: 35MHz (1.1MHz/channel)





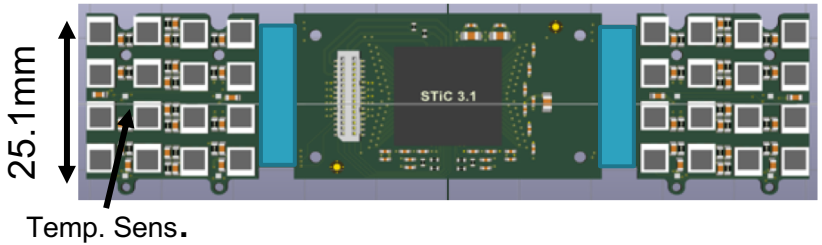
Technical prototype

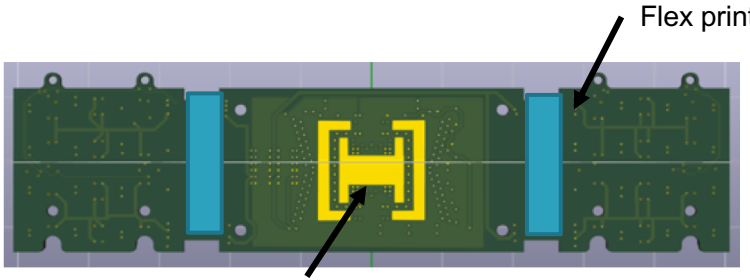
Goals

- Produce a module as close to design as possible
- Test mechanical support
- ASiC integration
- Cooling tests
- Learn and develop tools for assembly
- Develop test benches for detector characterization and quality control
- Measure detector performance
- Finalize detector design

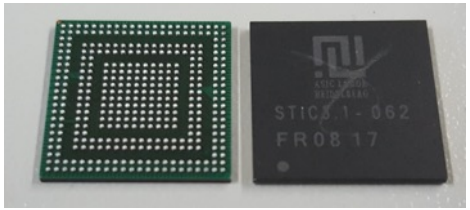
Front-end board

- Develop and produce the front-end board in the summer 2017
- Using the STiC 3.1 packaged ASIC (not MuTrig)
- Hamamatsu SiPMs S13360-3050PE



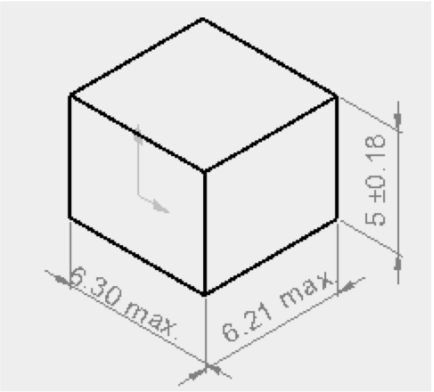


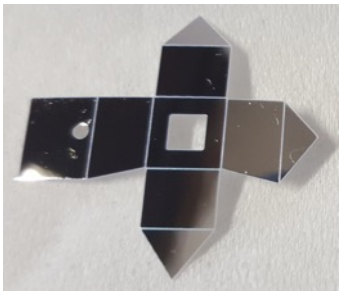
Test board for the packaged ASICs

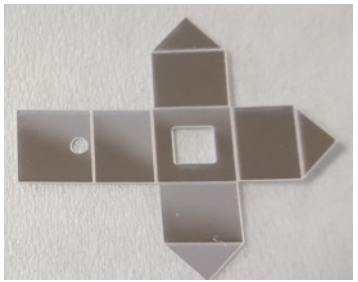


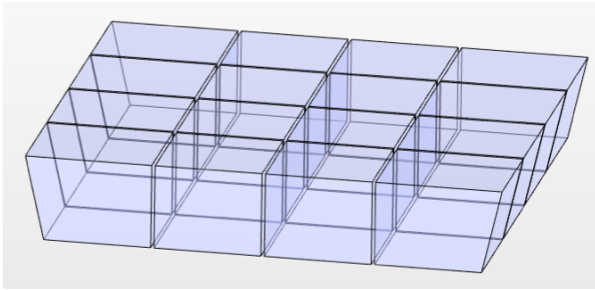
Tile individual wrapping

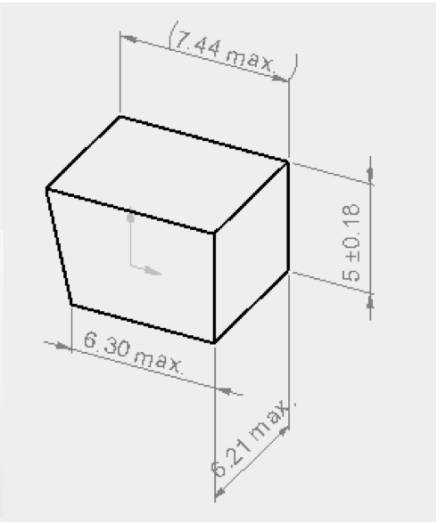
- Two type of tiles, Ej-228
- ESR 3M reflective foil
- The foil Foil design to maximize reflection
- Production in house using laser cutter
- Additional hole for monitoring the glue (might remove)
- The foil as a cover from the top and bottom





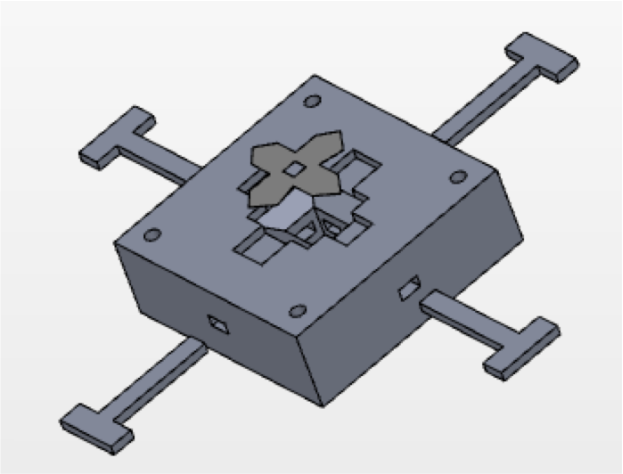


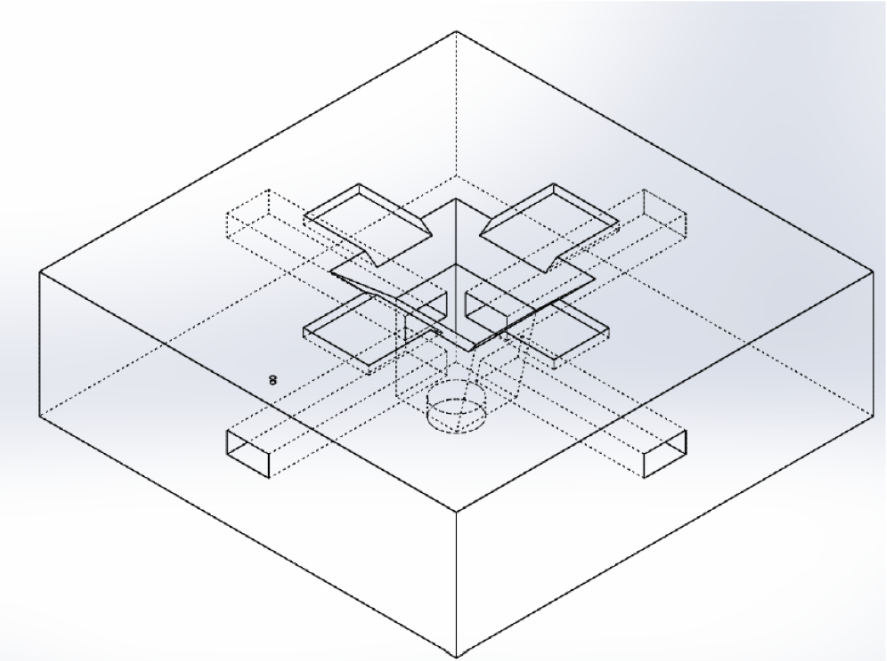




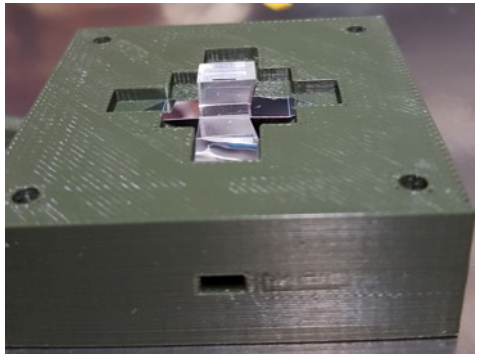
Wrapping tools

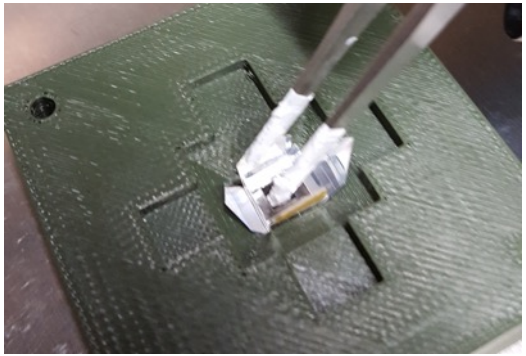
- Design 2 types of tools for different tile shapes
- 3D printed prototypes
- Will modified design for production

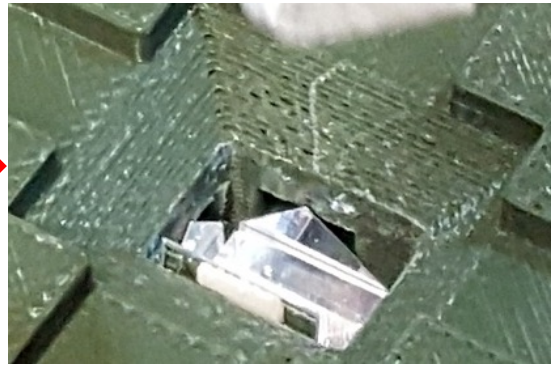


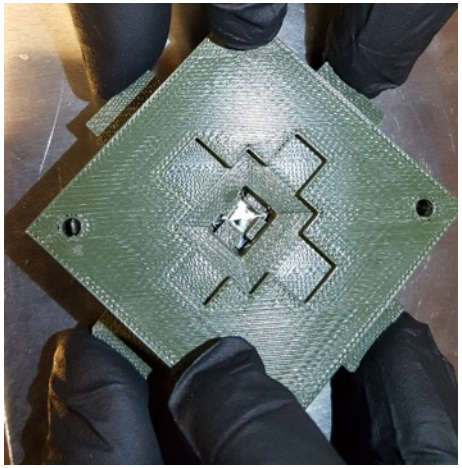


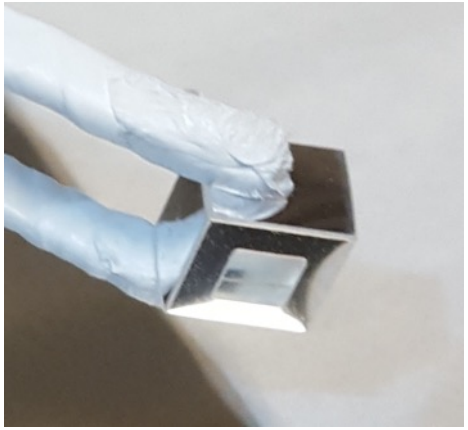
Tile wrapping procedure



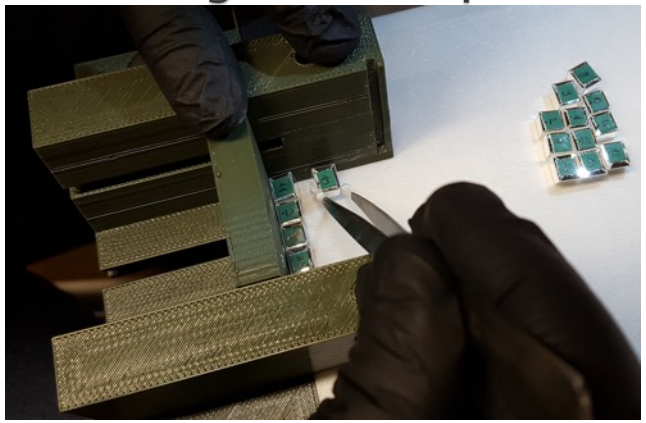


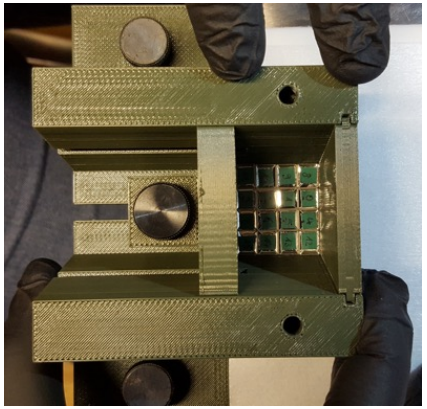


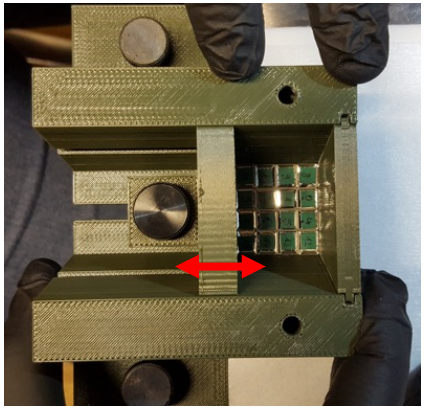


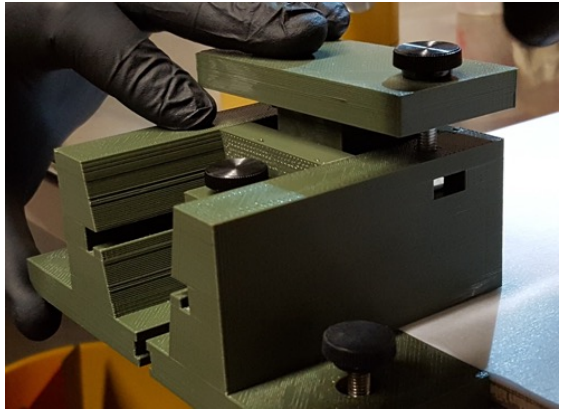


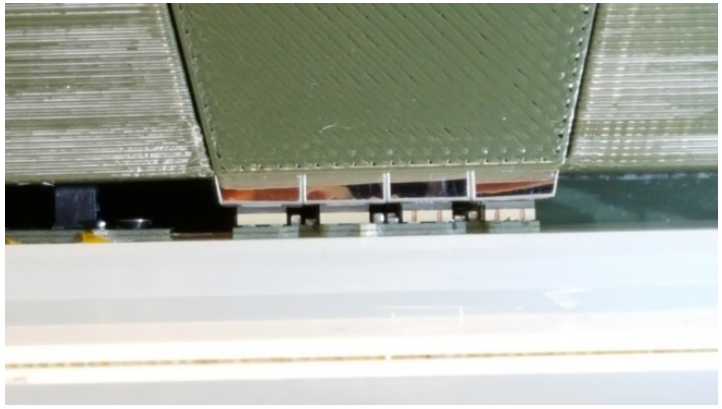
Gluing tool and procedure



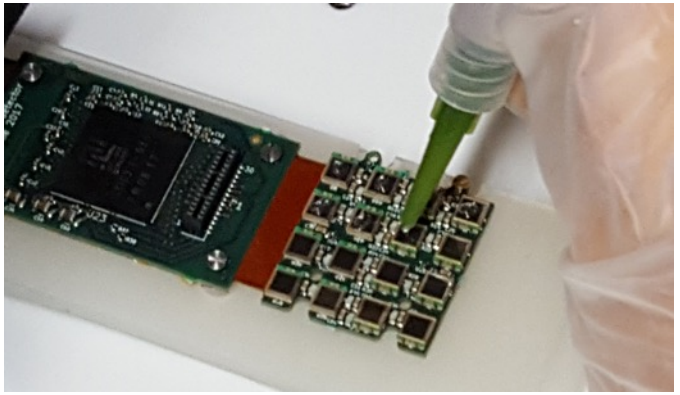


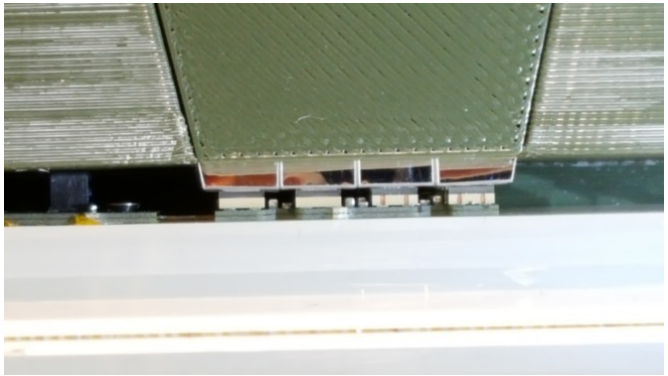


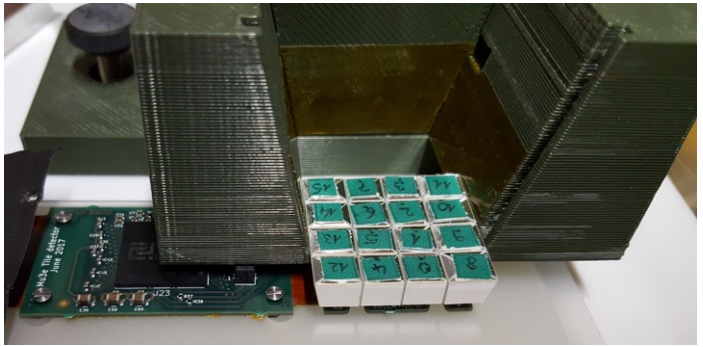




Gluing tool and procedure

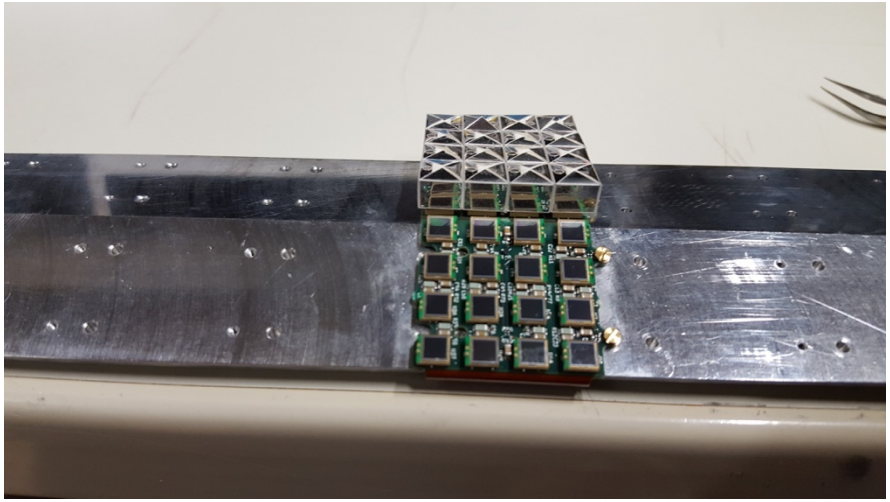






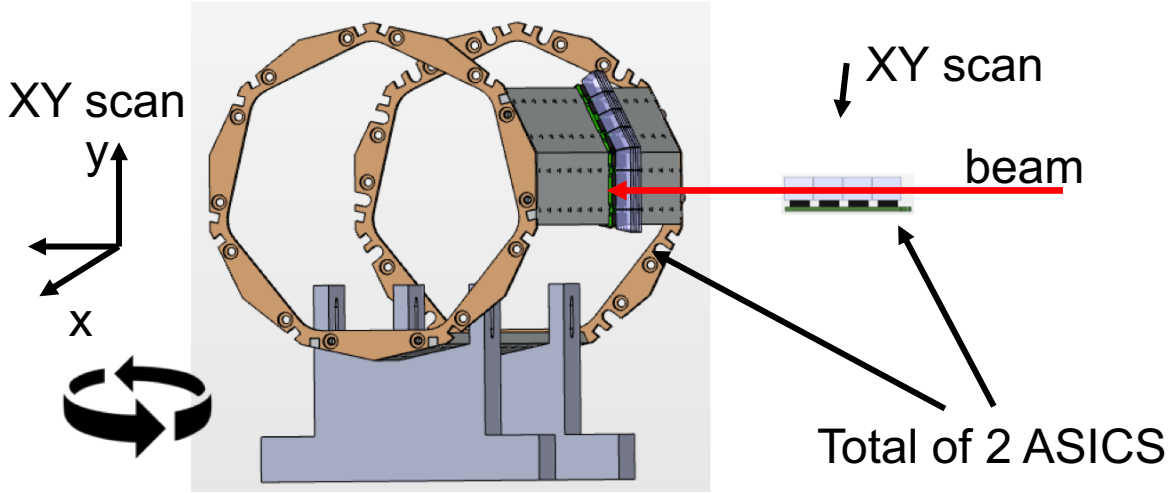
Assembly steps

- ASIC test before equipping the PCB
- SiPM diode test before soldering
- DCR test of submodule with fully equipped board
- Wrapping of Tiles (each day for 4 submodule, single module ~1h)
- Gluing 4 submodule in parallel
- QA test in the lab



Test beam setup

- Two weeks ago at DESY
- Trigger – submodule parallel to beam (passes 4 tiles)
- DUT – perpendicular to beam with the option for rotation



Test beam setup

- Two weeks ago at DESY
- Trigger – submodule parallel to beam (passes 4 tiles)
- DUT – perpendicular to beam with the option for rotation

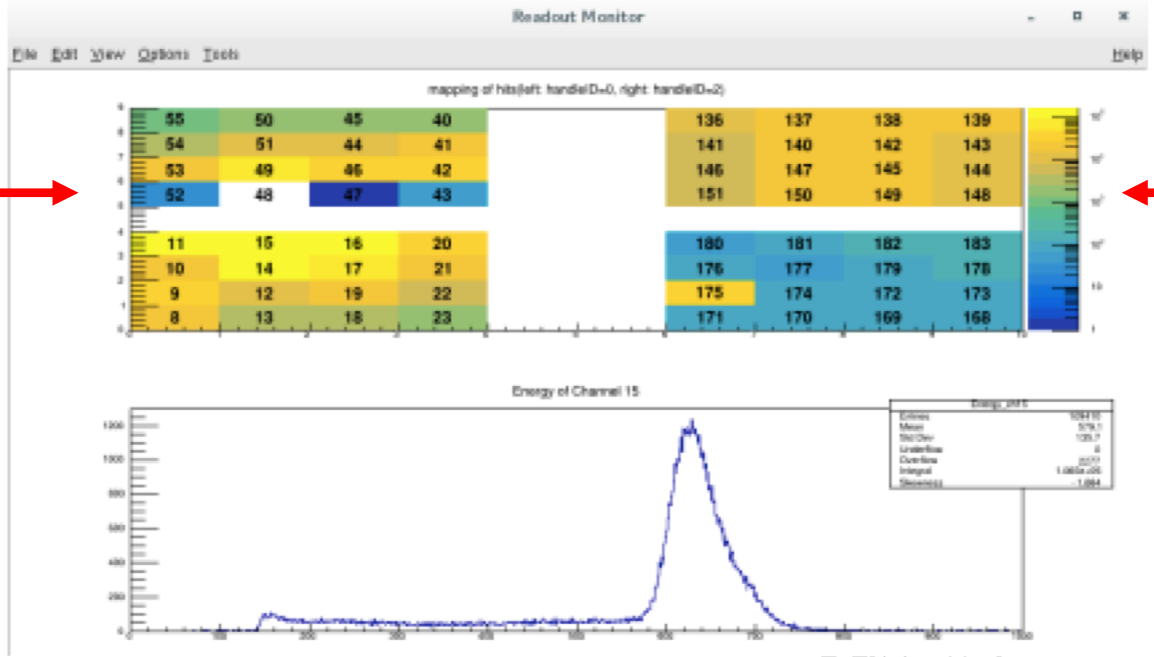
DUT
(one row
without tiles)

Trigger

Detector performance

- View from the online monitor

DUT



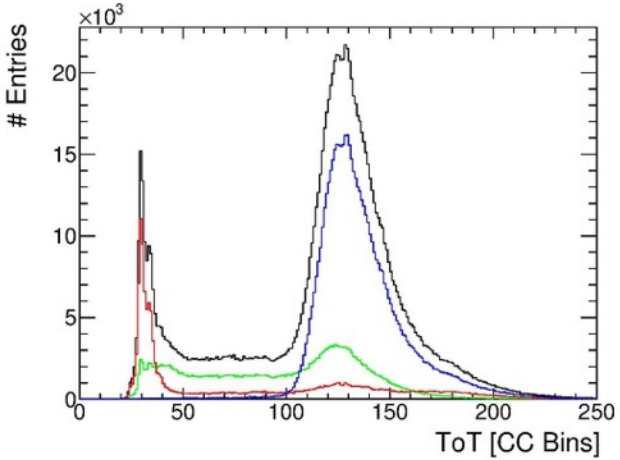
Trigger

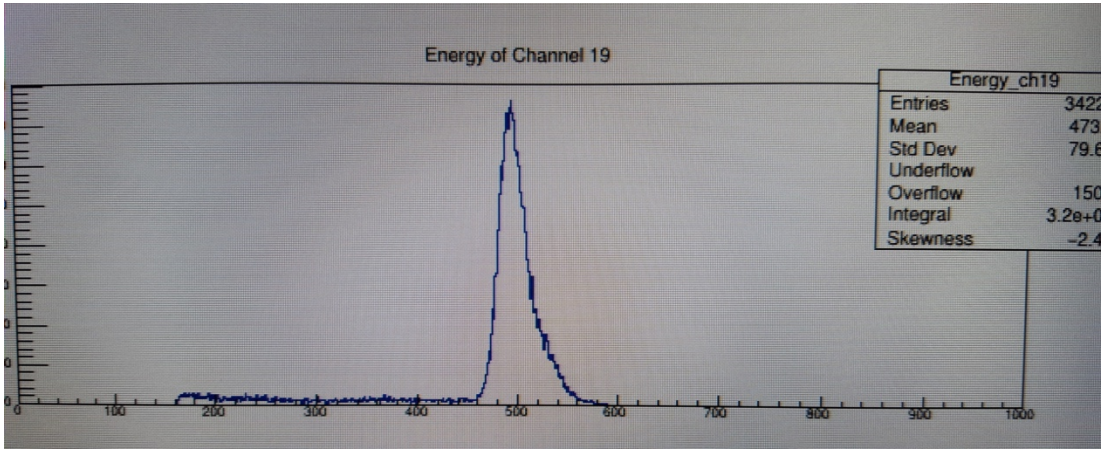
ToT spectrum

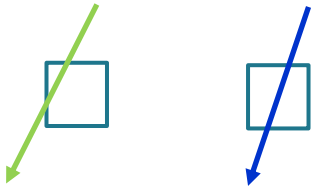
- ToT spectrum looks promising!
- Low crosstalk -> wrapping concept works!

11	15	16	20
10	14	17	21
9	12	19	22
8	13	18	23

Old prototype

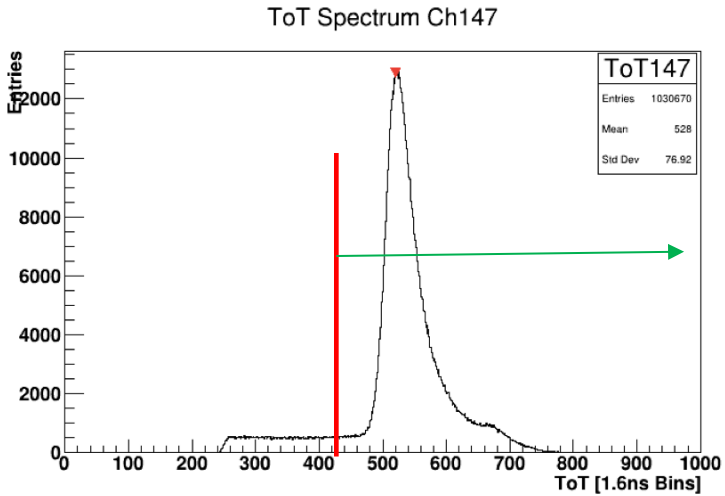






Trigger timing

- ASIC not optimize, only T-threshold scan
- Same HV for all channel
- Low energy cuts only (μ-3σ) and no time walk correction



Trigger timing

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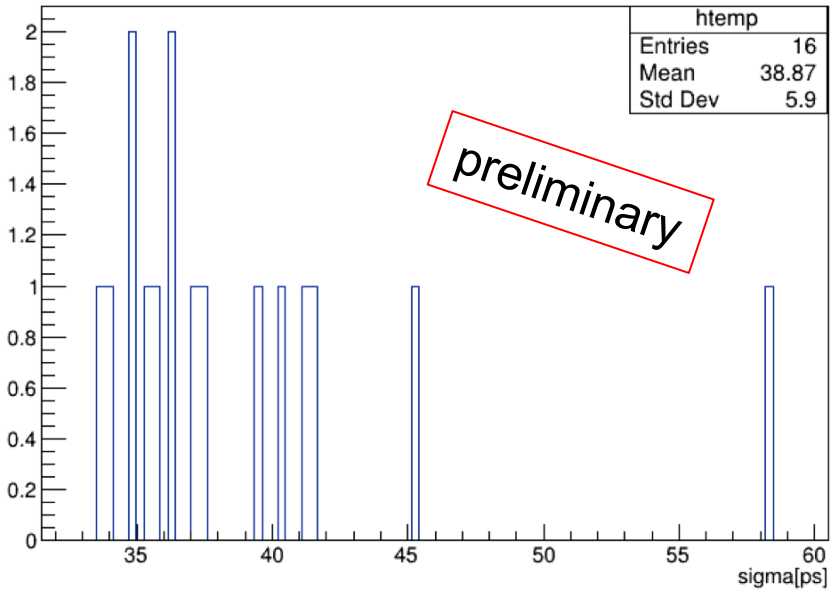
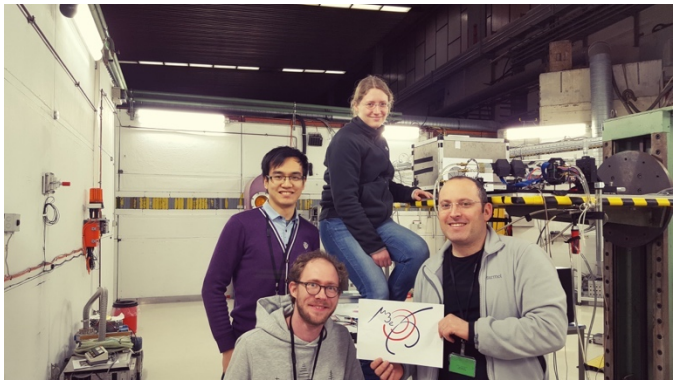


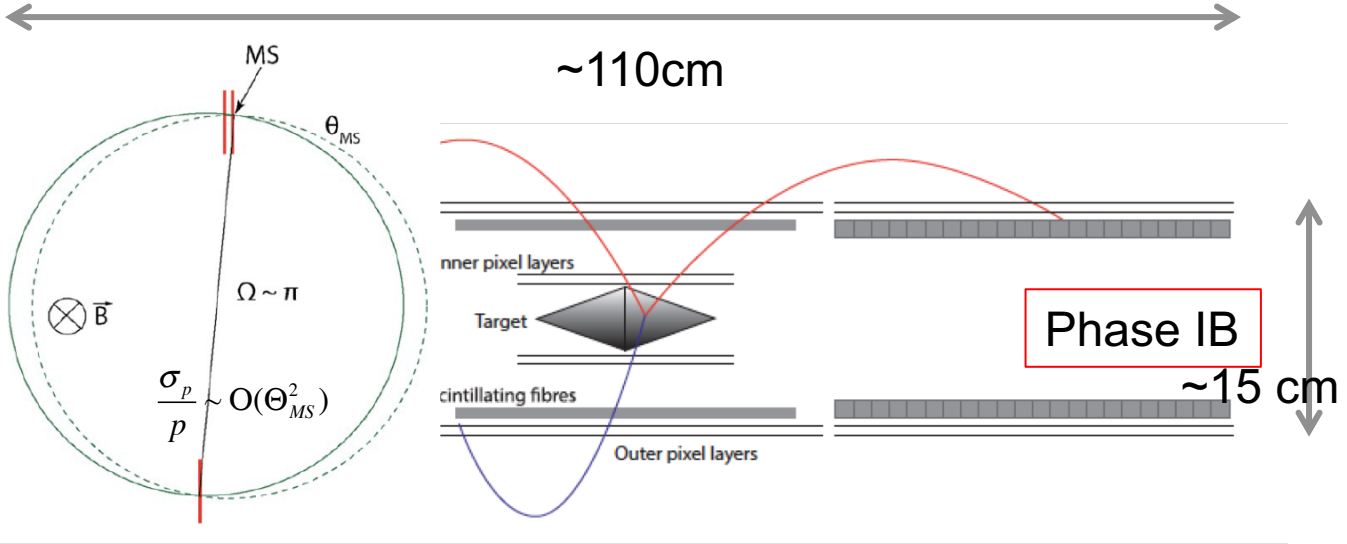
Outlook

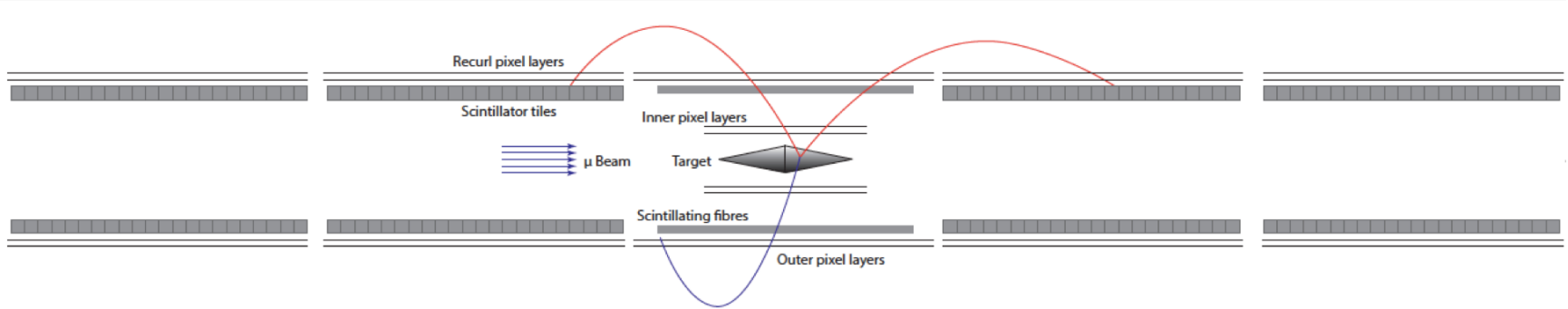
- Technical prototype with 96 channel was built
- Assembly tools were design and tested
- Assembly procedure will be finalize soon
- First results looks promising
- Next step - system readout integration
- Aim for vertical slice test by the end of the year (combine 3 detector system)



BK slides

Detector concept



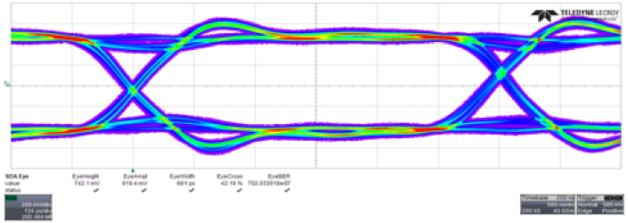


Phase II

- PSI - **Muon beam >10^9 muons/s**
- Helium atmosphere
- 1 T B-field
- Target double hollow cone

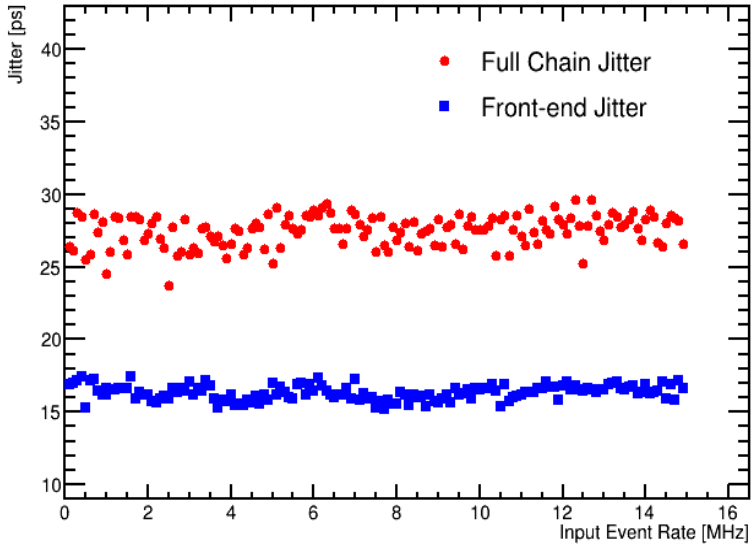
MuTrig characterization

- Customized LVDS TX: Opened eye diagram with 8b/10b encoded RPBS data pattern @ 1.25 Gbps
- Bit Error Rate (BER) upper limit of O(10^{-15}) for bit rate up to 1.9 Gbps.



Two readout option:

- 48 bit/event (Tile detector):
  - both time and energy info
  - Event Rate limit: 20.24 MHz (632 kHz/ch)
- 27 bit/event (SciFi detector):
  - time info. + 1 bit energy info.
  - Event rate limit: 35MHz (1.1MHz/channel)



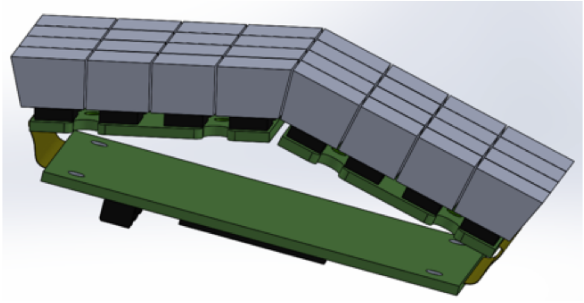
Jitter measurement:

- 460 fC charge injection over 15pF, input signal frequency up to 15MHz
- Use on-chip TDC for time stamp digitization

Detector overview

Submodule

- In total 32 channel
- 3x3 mm^2 SiPMs
- FEBA – flex printed PCB
- MuTrig ASIC in BGA package
- Scintillator tiles Ej-228
  ~6.5x6.5x5 mm^3 , two type (center and edge)
- ESR reflected foil, individual tile wrapping

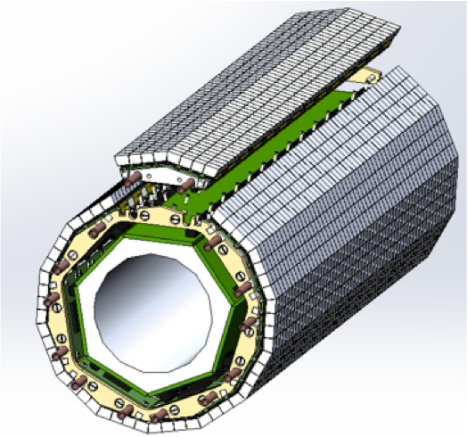


Moudule

- 14 submodule mounted on the cooling structure
- Water cooling
- 448 channels

Recurl station

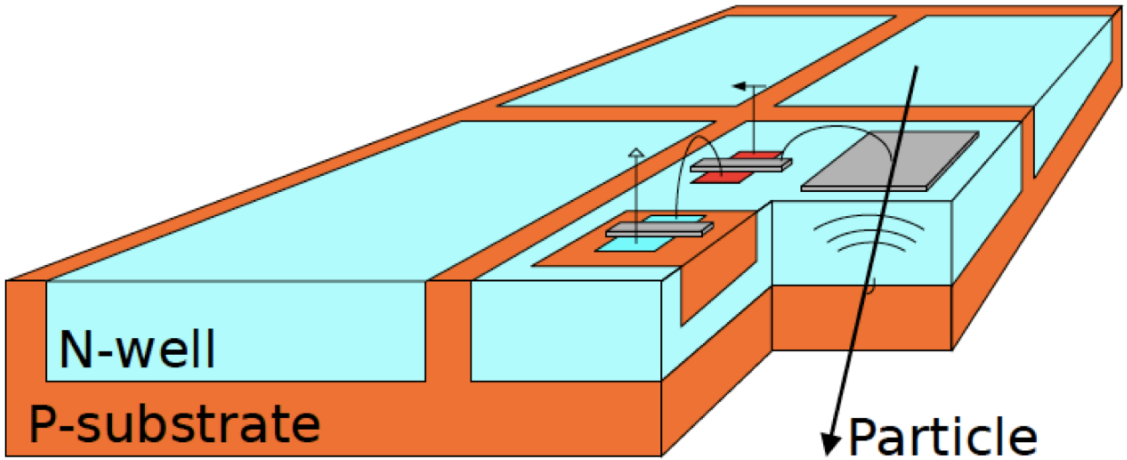
- 7 modules mounted on end rings
- Total length 36.8 cm
- 3136 channels



Full detector phase I

- 2 recurl station – total of 6272 channels

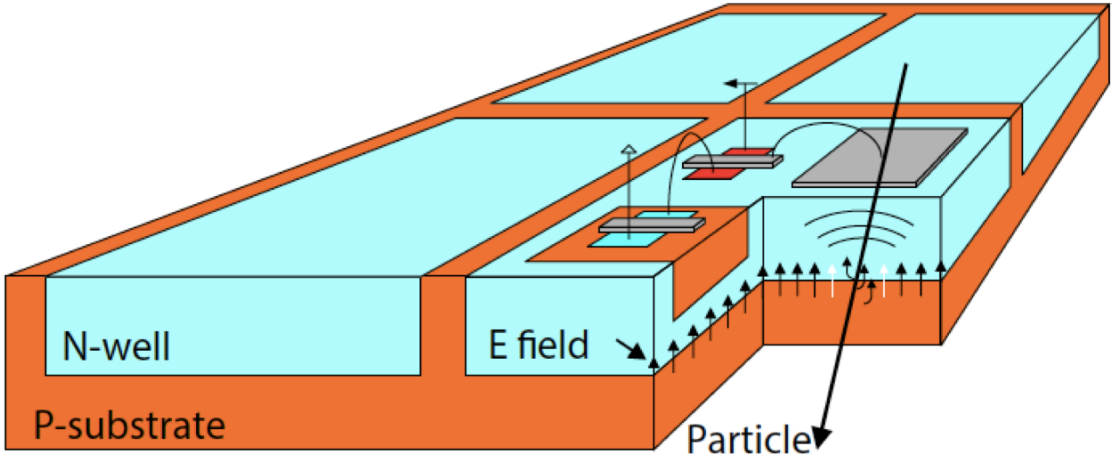
Pixel sensor



Ivan Perić, Nucl.Instrum.Meth. A582 (2007) 876-885

- Analog pixel electronics floats on sensor diode: **monolithic design**

Pixel sensor

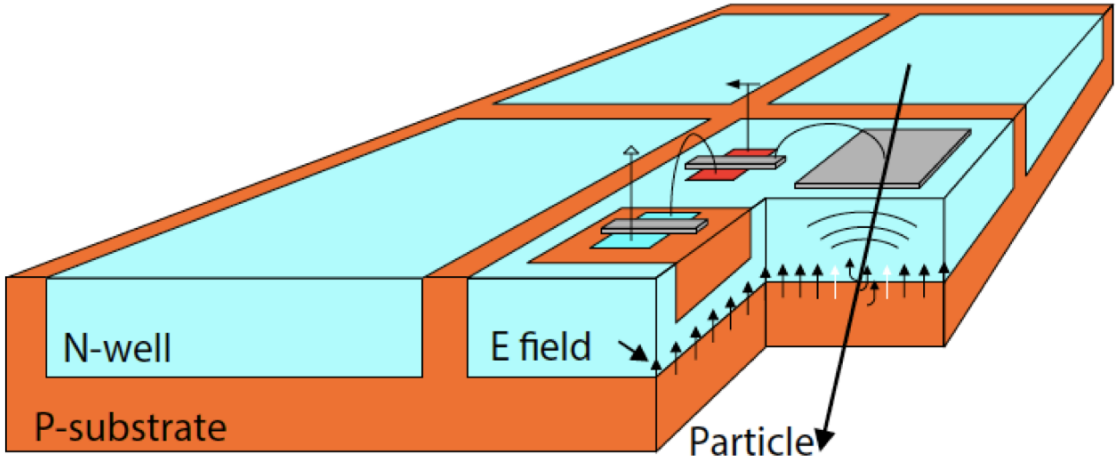


Ivan Perić, Nucl.Instrum.Meth. A582 (2007) 876-885

- Analog pixel electronics floats on sensor diode: **monolithic design**
- Industry standard HV CMOS process allows for E-field across diode ⇒ **depletion zone** of about 15 µm

20 / 60

Pixel sensor

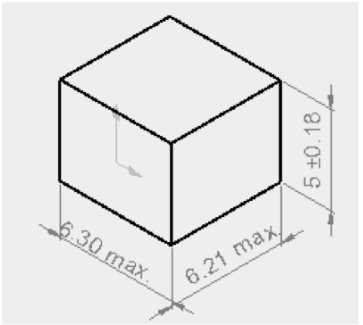


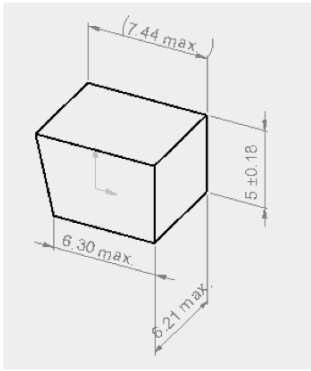
Ivan Perić, Nucl.Instrum.Meth. A582 (2007) 876-885

The MuPix chip is such a **depleted MAPS**, thinned to 50 µm $\approx$ 0.05% x/X_0

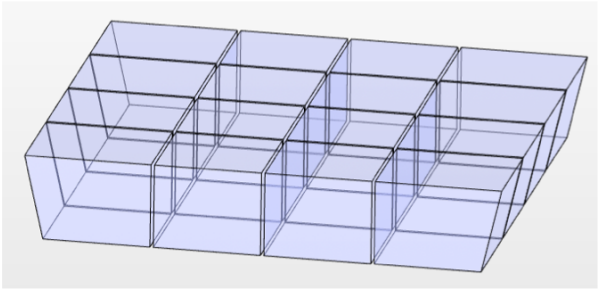
Scintillator tiles

- Using Ej-228
- Two type of tiles:
  - Central tiles- rectangle shape (6.3x6.2x5.0mm^3)
  - Edge tiles – trapezoidal shape (same base, top 7.44x6.2x5.0mm^3)



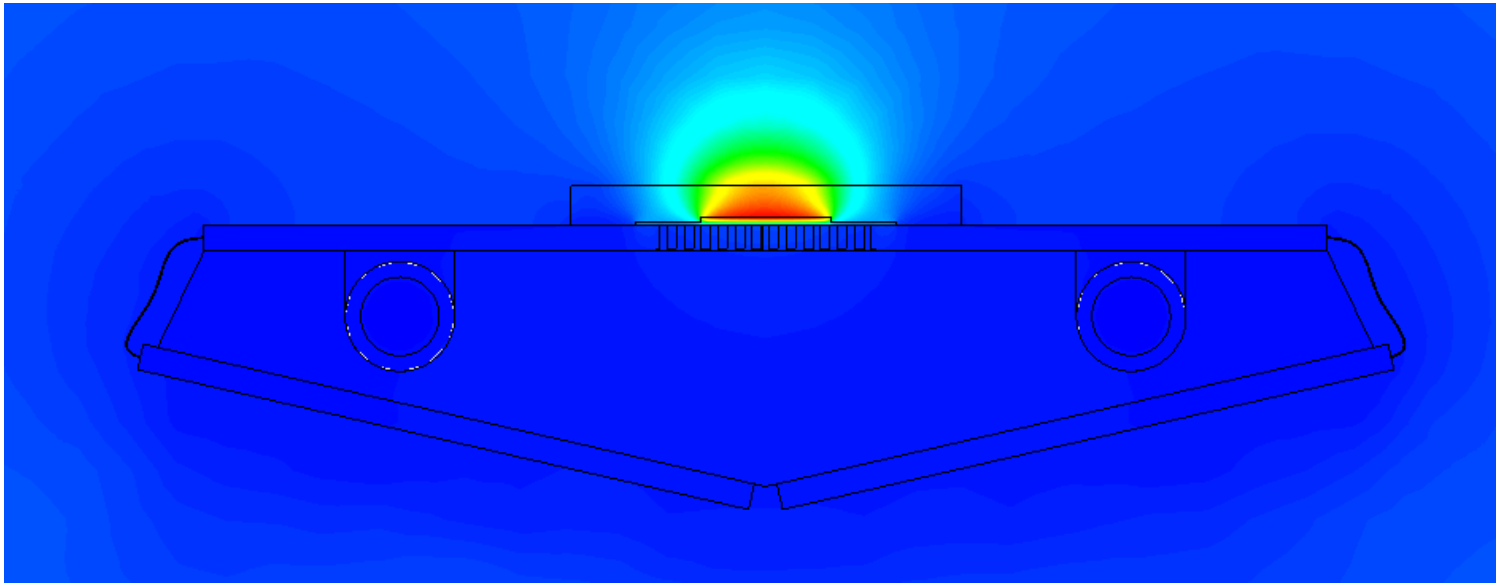


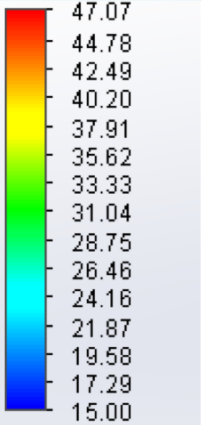
Properties	Value
Scintillation Efficiency (photons/1 MeV e$^-$)	10,200
Wavelength of Maximum Emission (nm)	391
Rise Time (ns)	0.5
Decay Time (ns)	1.4
Refractive Index	1.58
Coefficient of Linear Expansion	7.8 x 10^{-5} below 67°C
Light Output vs. Temperature Softening point	At 60°C, L.O. = 95% of that at 20°C No change from -60°C to 20°C 75°C
Temperature Range	-20°C to 60°C



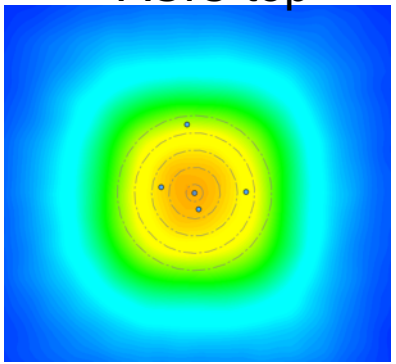
The technical prototype: Cooling studies

Example results for highest power consumption:



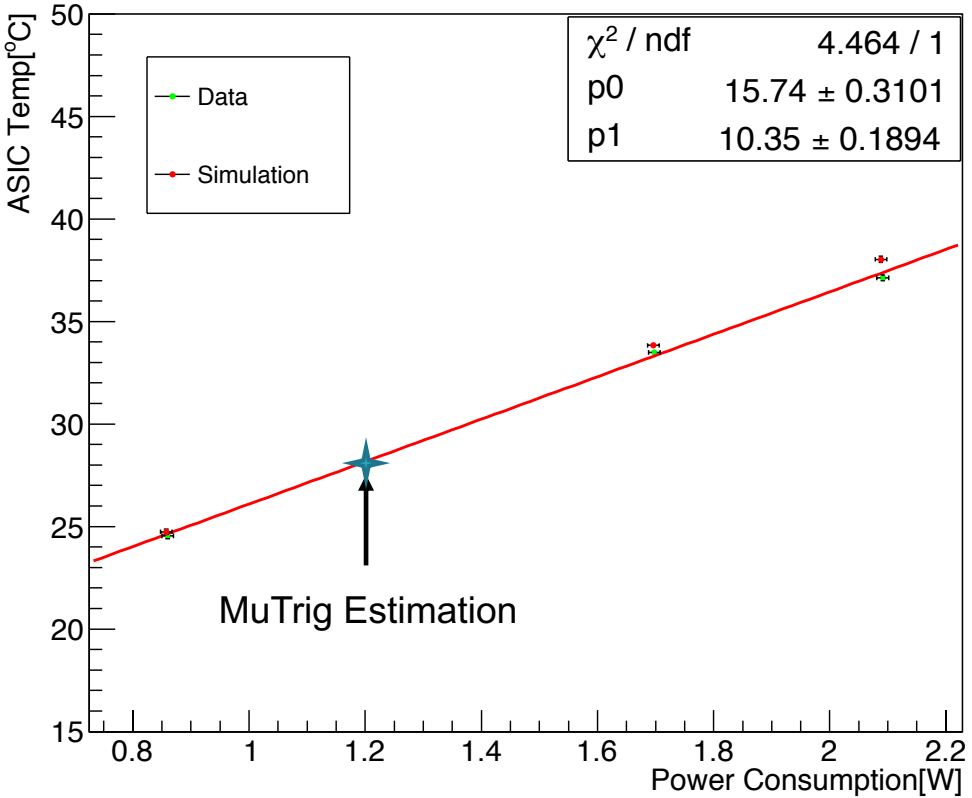


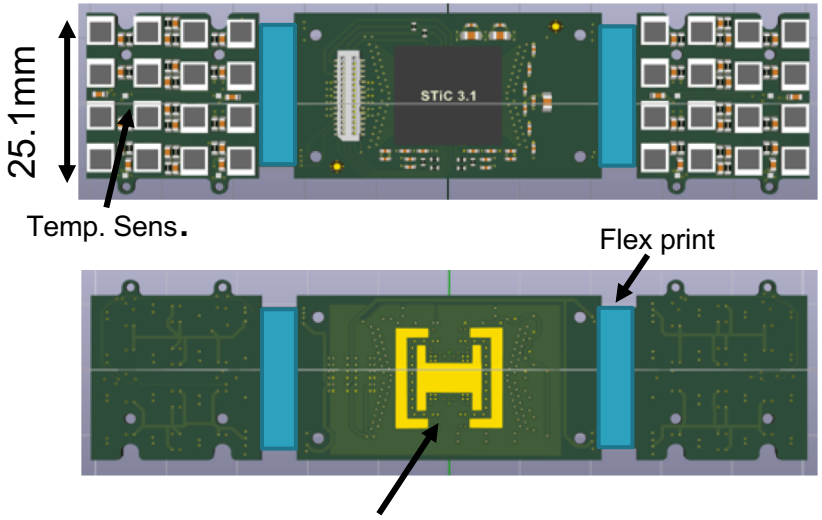
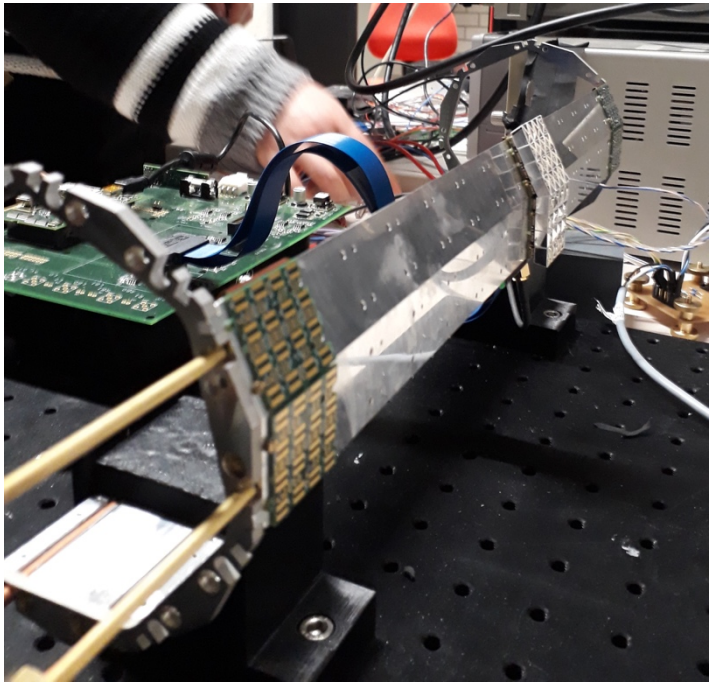
ASIC top



The technical prototype: Cooling studies

- Repeat at different power consumption of the ASIC
- Very good agreement to data (<1°C
- Small systematic error (Integration area of the temp. sensor is too small)
- Next step full module (ongoing)



Front-end board

- Develop and produce the front-end board in the summer 2017
- Using the STiC 3.1 packaged ASIC (not MuTrig)
- Hamamatsu SiPMs S13360-3050PE