PHC Star: RECFEB

FKPPL

News from FEV COB

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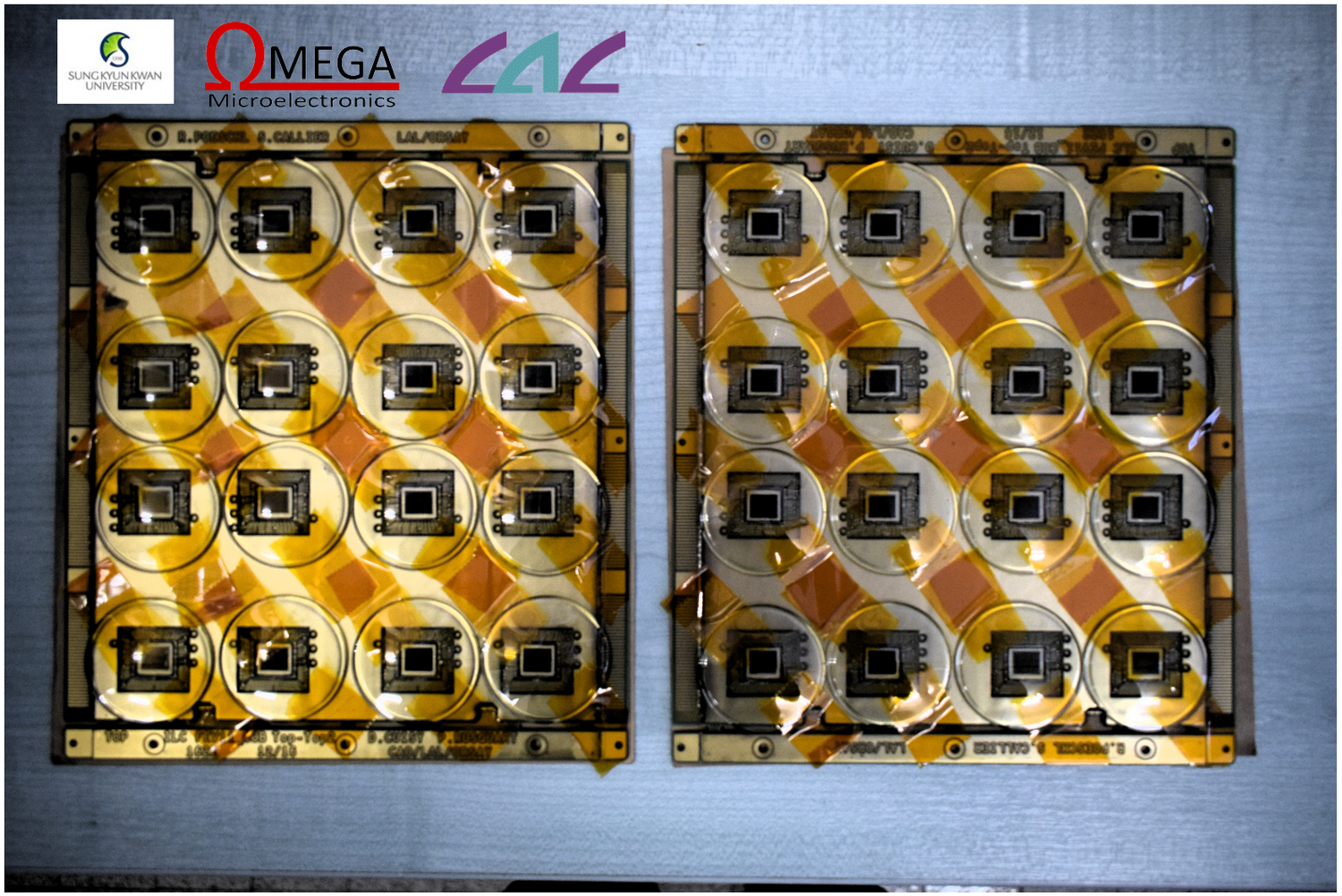
... on behalf of

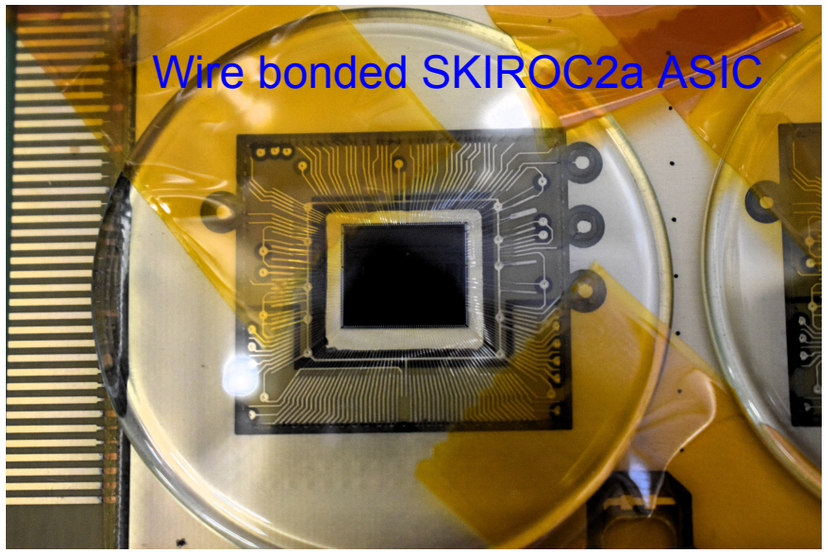
CALICE Meeting Mainz/Germany – March 2018

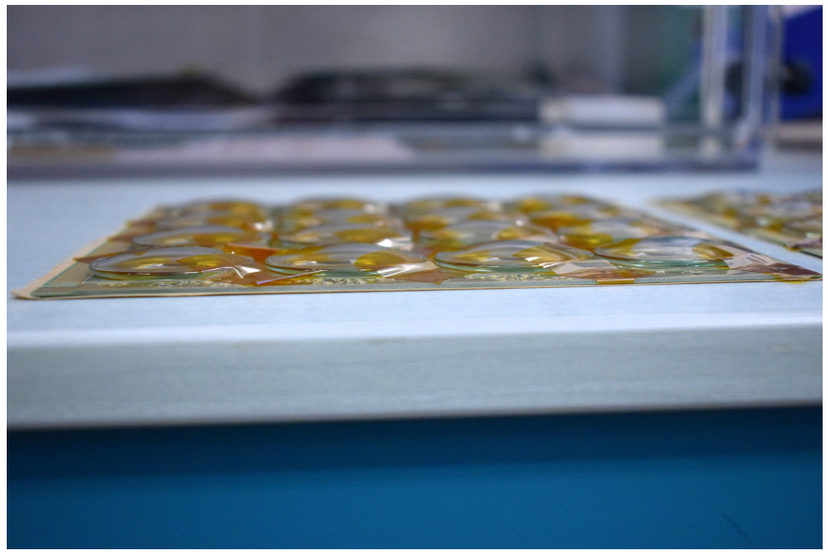
FEV11_COB available

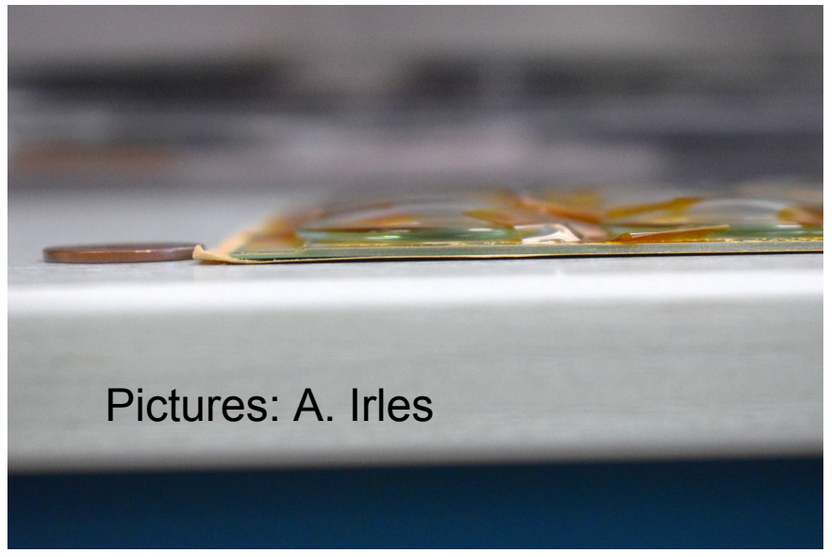


- 10 PCBs ready since beginning of December 2017 (SKKU/EOS)
- 4 PCBs delivered to LAL in January 2018
- 2 PCBs bonded at CERN at beginning of February 2018
  - Excellent service at CERN
  - Contact with P2IO Platform CAP
- First COB Version that should be equipped with Si Wafers

Impressions FEV11_COB







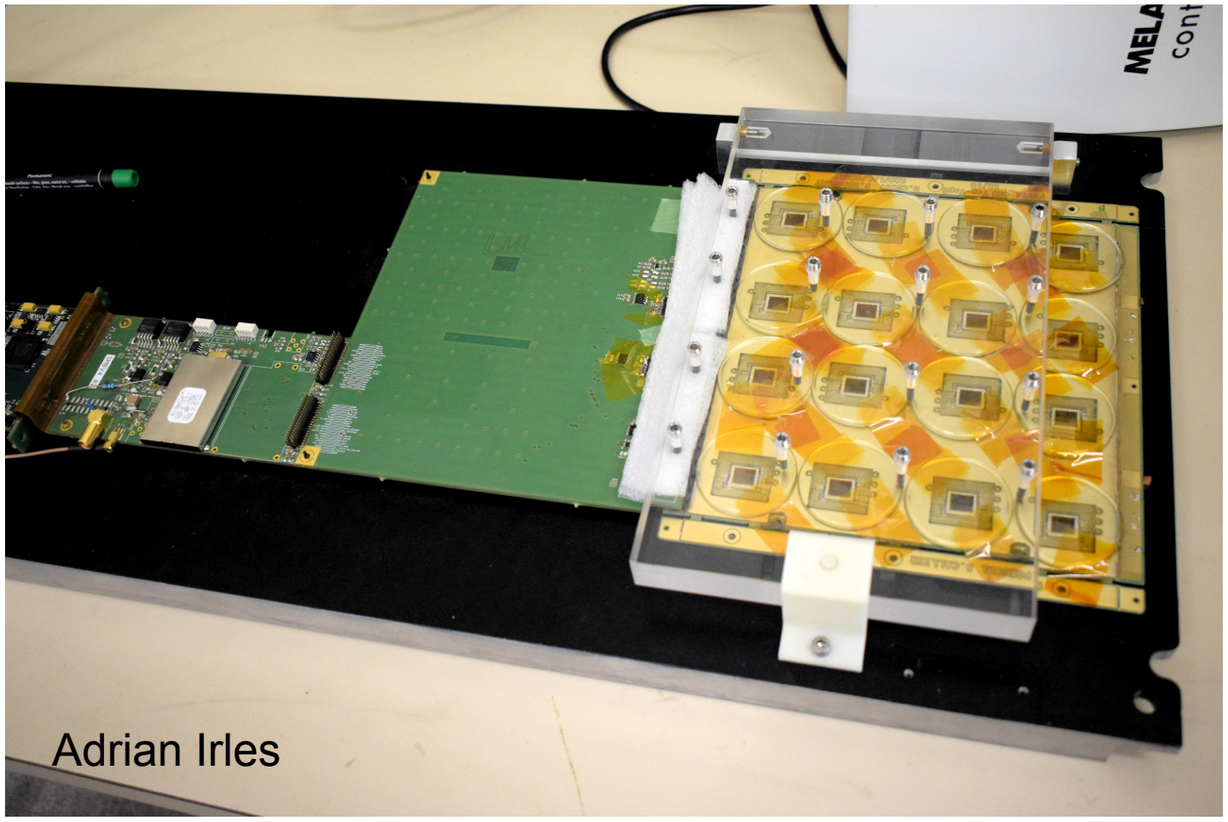
- Looks like a masterpiece, height 1.2mm (for a 9 layer board!!!)
- Planarity within specs for 4 out of 5 boards
  - (including mechanical prototypes from last autumn)
  - -> See next slide for examples of measurements
  - Question with planarity seems to be solved
- Boards well rectangular
- Towards debugging of boards

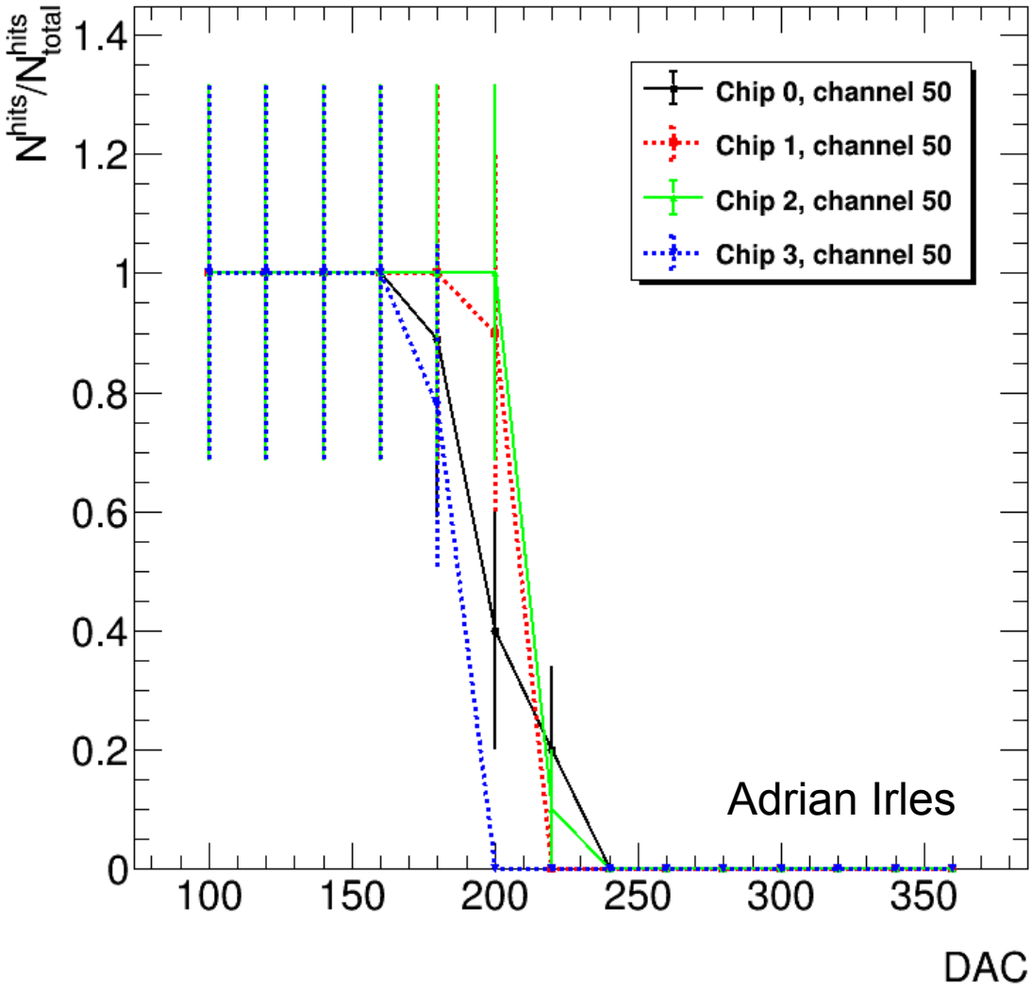
Metrology FEV11_COB

No.	Line No	Element / Tolerance	Pnt. / Ref.	X-Coord. / X-Angle / Nominal	Y-Coord. / Y-Angle / Up/Lo	Z-Coord. / Z-Angle / Actual	Diameter / Dist./Ang. / Dev./Error	Variance
				planeité				
1	49	PLAN			0.300	0.390	0.390	0.090
		Planéité						|--->>
				largeur exterieur				
2	51	Point		180.000	0.200	179.899	-0.101	
		Position X			-0.200			--****-----
				longueur interieur entre ouverture				
3	53	Point		180.000	0.200	180.245	0.245	0.045
		Position Y			-0.200			-----+--->>

No.	Line No	Element / Tolerance	Pnt. / Ref.	X-Coord. / X-Angle / Nominal	Y-Coord. / Y-Angle / Up/Lo	Z-Coord. / Z-Angle / Actual	Diameter / Dist./Ang. / Dev./Error	Variance
				planeité				
1	49	PLAN			0.300	0.299	0.299	
		Planéité						******
				largeur exterieur				
2	51	Point		180.000	0.200	179.863	-0.137	
		Position X			-0.200			--****-----
				longueur interieur entre ouverture				
3	53	Point		180.000	0.200	180.154	0.154	
		Position Y			-0.200			-----*****-

First tests and S-Curves





- Both boards are configurable!!!
- Can extract S-Curves
  - Btw. First signals with integrated SKIROC2a
- Still issues in communication with boards, corrupted data streams (both directions)
- Need a few more debugging sessions with experts before serious test series can start
- No real showstopper observed and decision on next steps (e.g. equipment with wafers) in April

Summary and conclusions

- New version of FEV11_COB available to be equipped with Si wafers for validation of technology
  (Reminder still the only PCB design that could cope with current ILD constraints)

- **Issue of planarity solved**

- Excellent collaboration wirh SKKU and EOS Company (both South-Korea)

- First tests on test bench show no show stopper but still a way to go before serious testing
  - e.g Corrupted data streams
  - Debugging will resume after CALICE Meeting (Callier, Cornat, Irles, Jeglot)

- To be equipped with Si wafers for validation of technology

Backup

Power-Pulsing:
New ultra-flat Capacitors!

We propose to use new ultra-flat capacitors to distribute over the ASUs, this will permit:

Peak current reduction: especially through the connectors

No more voltage drop along the slab

Homogeneous peak power dissipation during power pulsing.

We go from the 400 mF capacitor/ 12A (peak Current) for the whole SLAB to 140 mF / 1.2 A per ASU.

Reminder of power consumption values :

- DVVD (3.3V) 11 mA / Chip, Total 300 mA
- AVDD (3.3V) / Chip : 77 mA during ACQ, 20 mA during Conversion, 0.01 mA idle

- Distributing the capacitors along the slab permits reducing current between ASUs with a factor ~50-100.
- The current peak is local.
- The current delivered for charge reloading of the capacitors will be limited at the extremity of the Slab