Performance study of SKIROC2 & 2A

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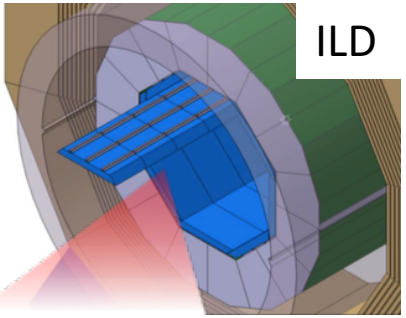
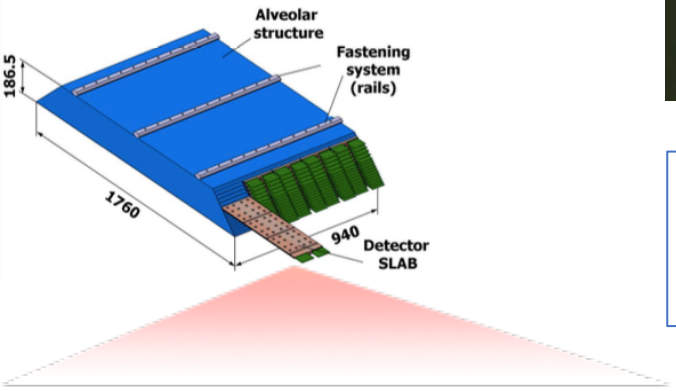
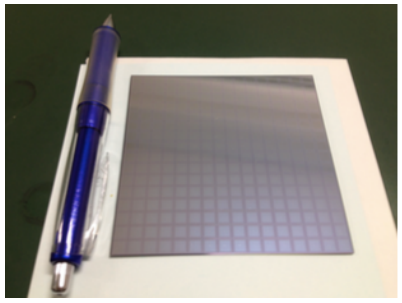
Introduction



ILD Si-W ECAL :Segmented for precise measurement

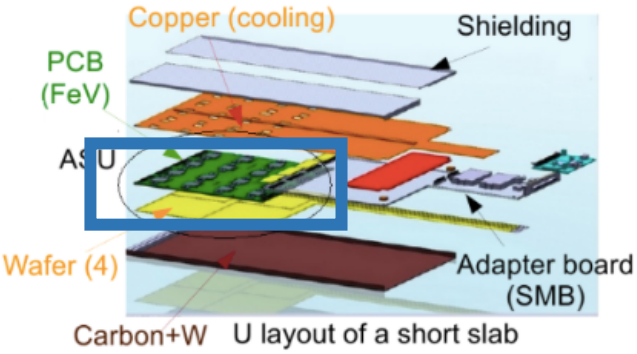




size	10 × 10 cm^2
cell size	5.5 × 5.5 mm^2
# of cell	16 × 16 = 256

Number of channel : 10^8

64 ch / ASIC → Number of readout ASIC : 10^6



U layout of a short slab

Before mounting ASICs to readout PCB, we need to check them …

to remove bad chips
to rank chips

We have to make an automatic measurement system for checking chips

SKIROC2/2A

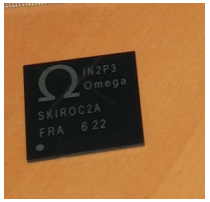
SKIROC2 specification

- ASIC for ILD ECAL
- 64 ch / chip
- Self trigger
- 15 analog memories / ch
- 12-bit ADC
  (Gain= 1 or 10)
- **Power pulsing**

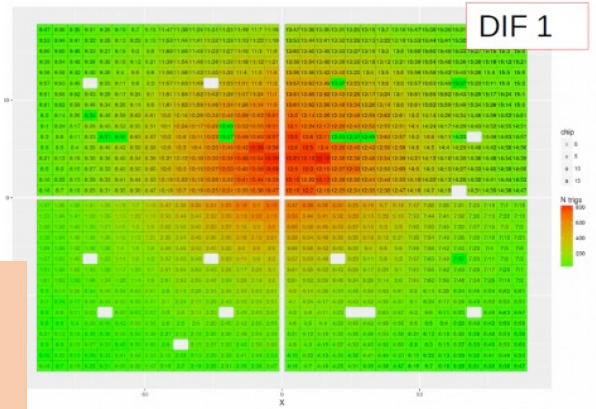
Some problems in beamtest

SKIROC2A improvement

- Trigger adjustment of Individual channels
- TDC
- Reduce noise
- Auto gain selection
- External trigger etc..



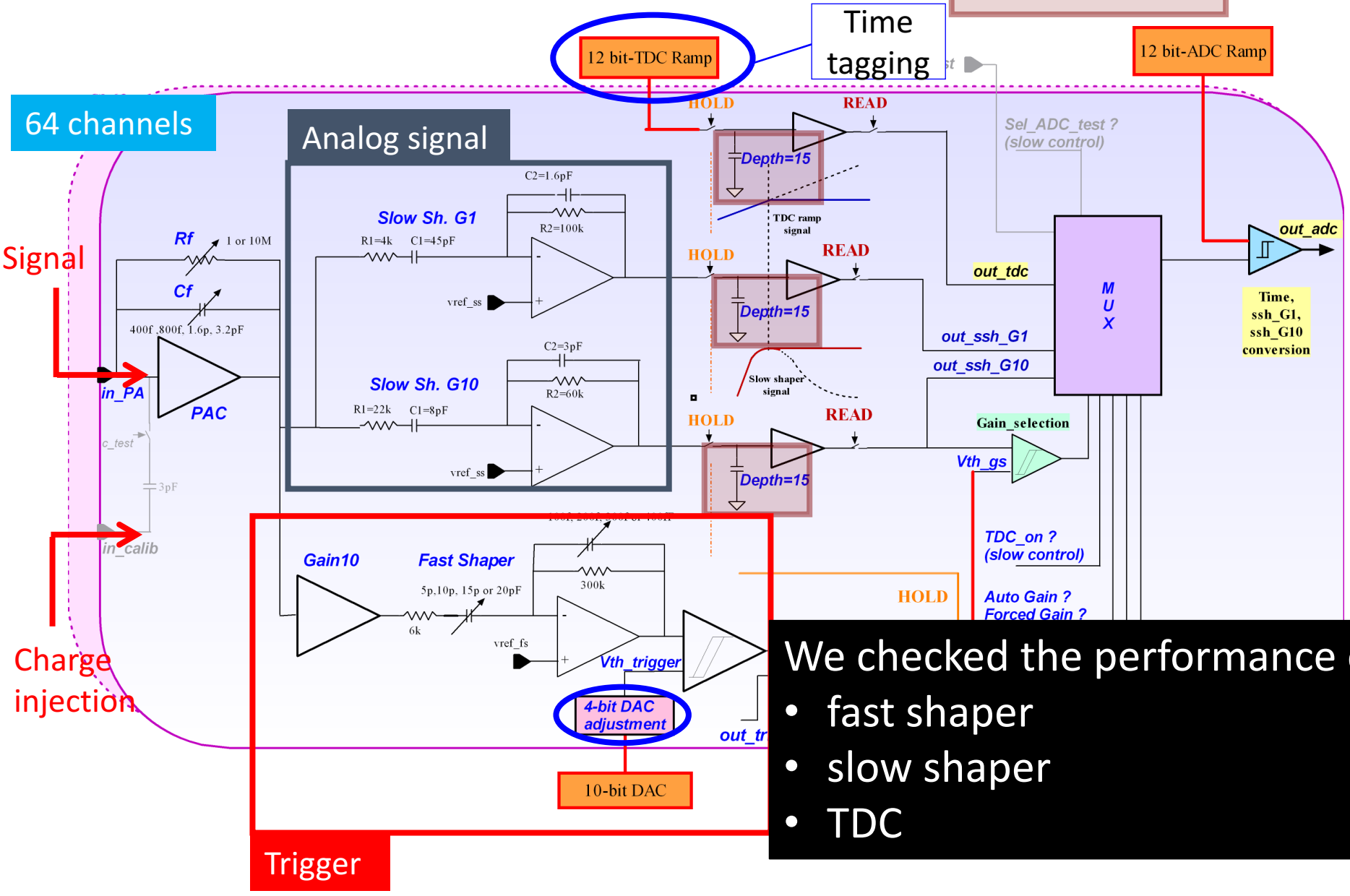
- ECAL technological prototype is developed
- In beam test, the prototype got the beam parameters and shown the feasibility



1. Trigger threshold : Dynamic range of threshold control on each channel is too small
2. Noisy channels : Noisy channels must be switched off
3. TDC
4. Retriggering
5. Empty event

SKIROC Analog part

15 cells Analog memories

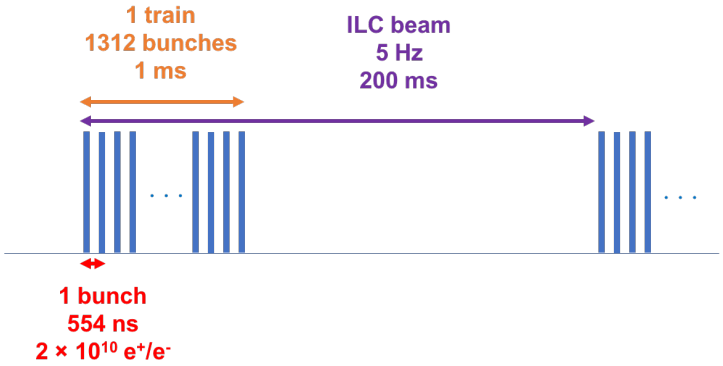


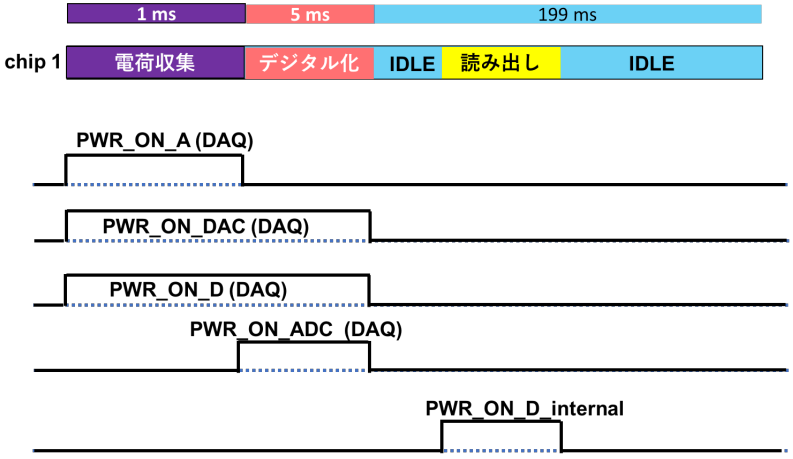
We checked the performance of

- fast shaper
- slow shaper
- TDC

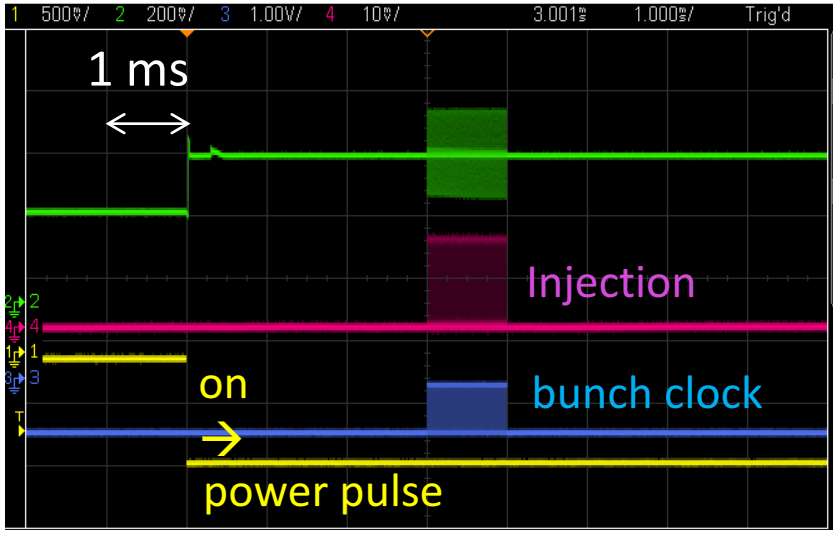
Power pulsing

Power control function of SKIROC2&2A which synchronized for ILC beam bunch





Enable to reduce the power & heat



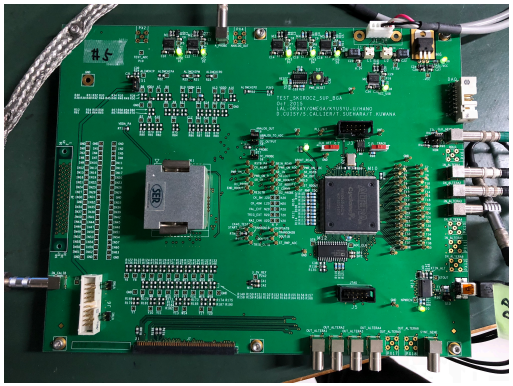
Only analog part is power-pulsed

BGA Testboard

- Two types

Socket version
(Merit) Easy to change chips
(Demerit) Sometimes connection goes loose

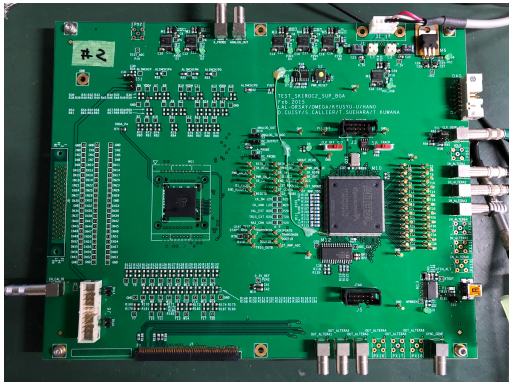
Soldered version
(Merit) Good connection
(Demerit) difficult to change chips



Testboard#5

New version

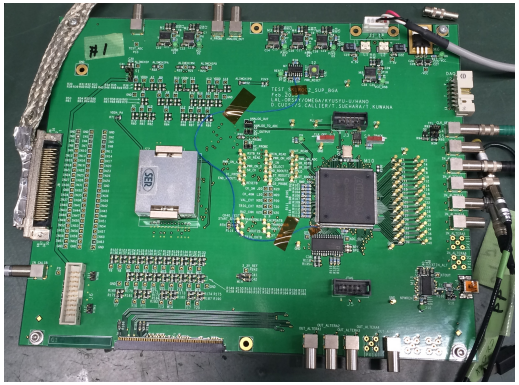
Add 1000 μF ×2 capacitors



Testboard#2

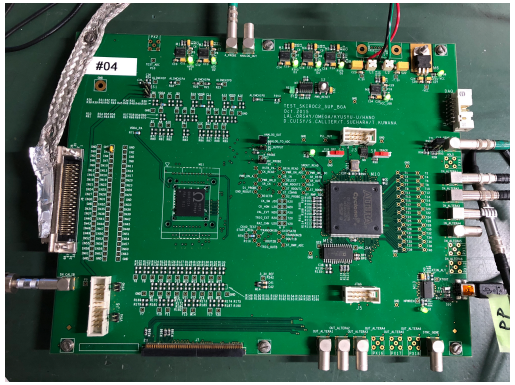
SKIROC2

Old version



Testboard#1

Old version



Testboard#4

SKIROC2A

New version

Performance study of SKIROC2 & 2A

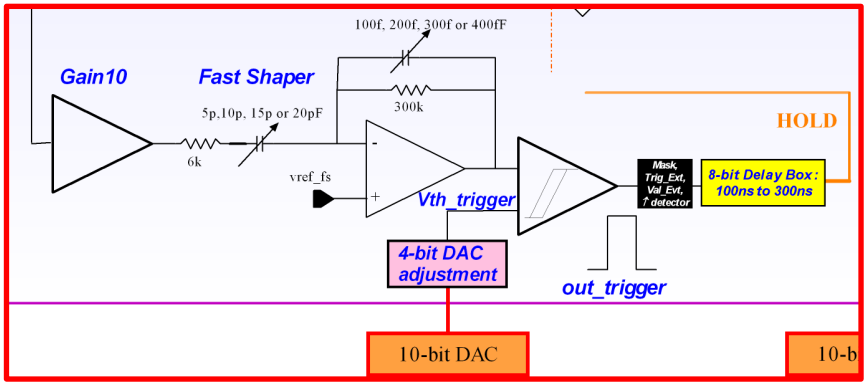
Common settings	feedback capacitance	compensation capacitance	Injection period
	1.2 pF	1 pF	500 kHz (1/10BX)

Fast shaper

- Trigger line
- Trigger threshold adjustment :

Individual channel: 4-bit DAC

Global :10-bit DAC



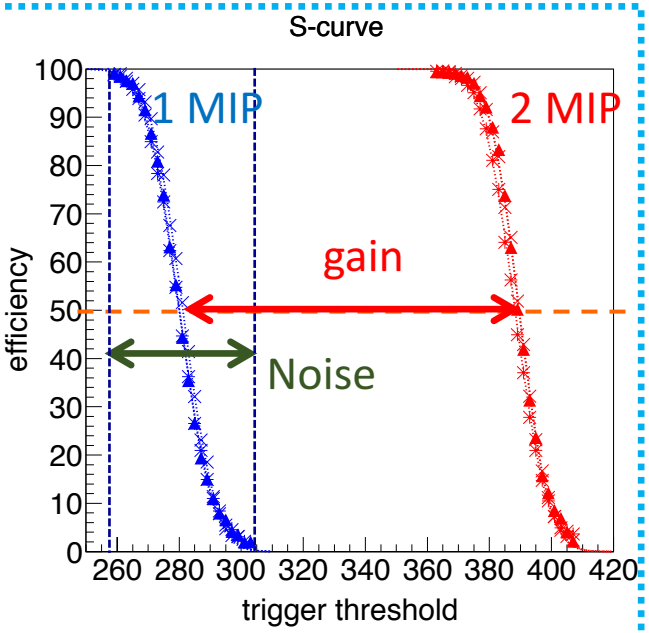
- **S-curve : Performance of fast shaper**

(Right figure) horizontal axis: trigger threshold
vertical axis: trigger efficiency

Gain: the difference between 1 & 2 MIPs
@ 50% efficiency

Noise : the width of fitted error function

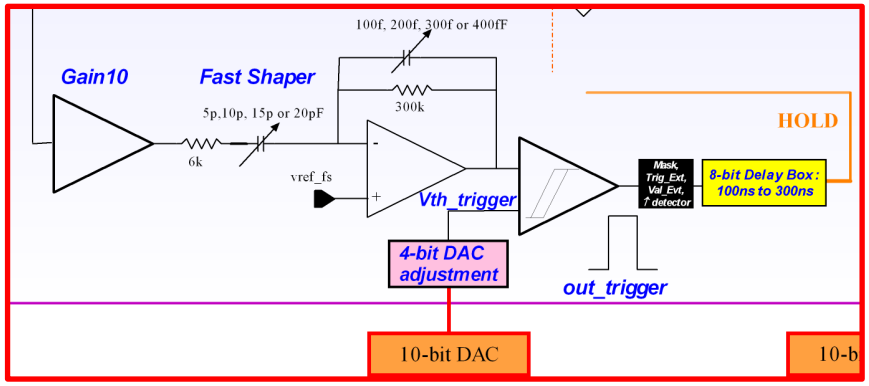
S/N ratio = Gain / Noise



Dynamic range of 4-bit DAC

Individual channel: 4-bit DAC

- 0-15 DAC
- Dynamic range:
  Global DAC / 15 4-bit DAC



If dynamic range > threshold variation over 64 channels
→ threshold correction can be done

The dynamic range is ...
(SKIROC2) too small
(SKIROC2A) wider than SKIROC2

We checked & compared
- threshold variation over 64 channels
- the dynamic range of 4-bit DAC

in SKIROC2 & 2A

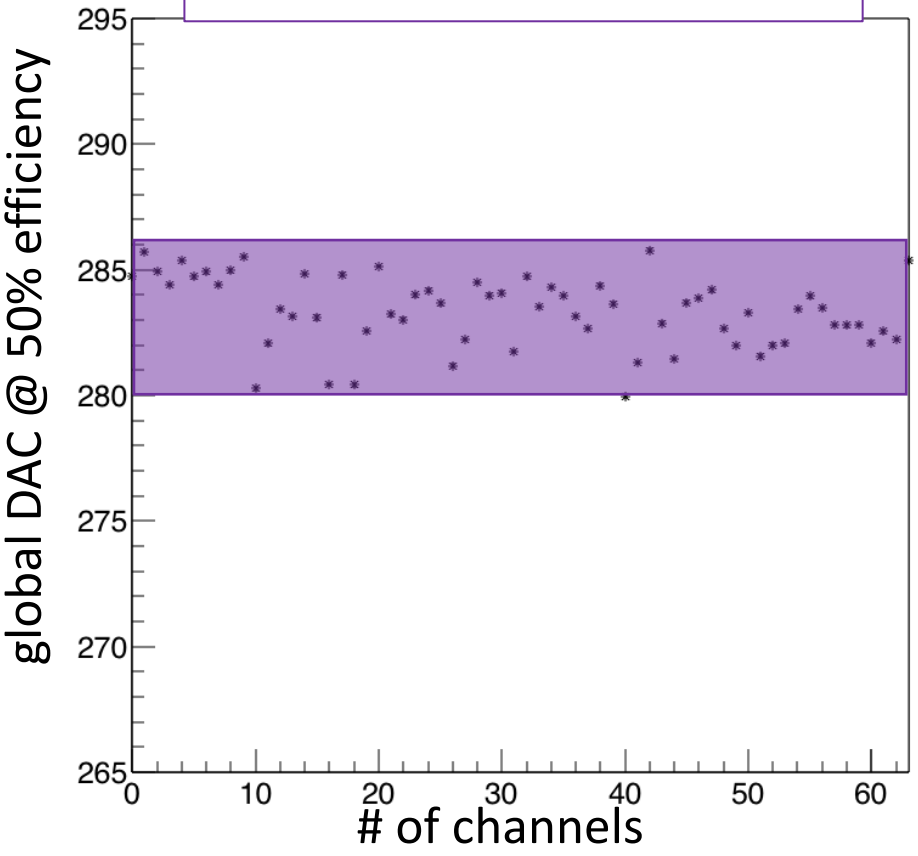
Injection		10-bit DAC trigger threshold		4-bit DAC trigger threshold
channel	charge [MIP]	SKIROC2	SKIROC2A	0 – 15 (one by one)
ch.0 - 63 (ch by ch)	1	280	300	

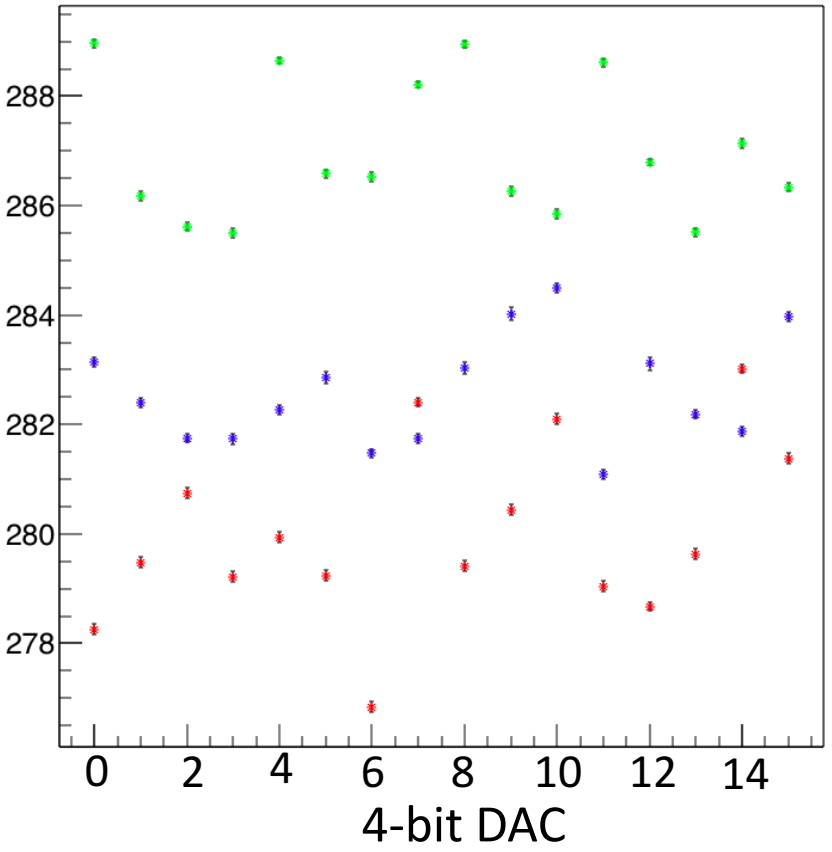
Dynamic range of 4-bit DAC

ch.0 ch.30 ch.60

Dynamic range:
No correlation / 15 4-bit DAC

Variation over 64 ch: 6 DAC





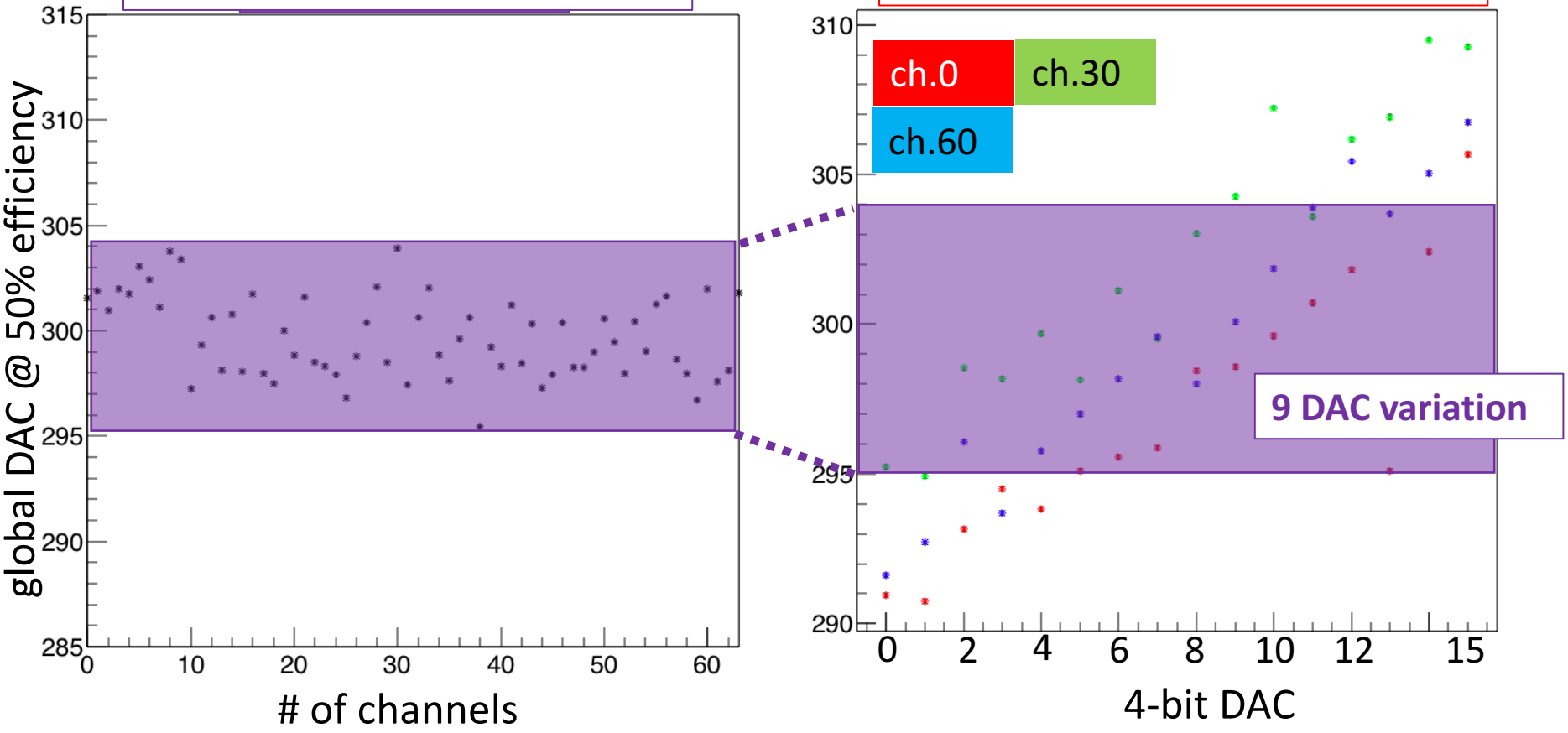
＜SKIROC2＞ No correlation

→Correction by 4-bit DAC is not possible

Dynamic range of 4-bit DAC

Variation over 64 ch: 9 DAC

Dynamic range:
15 global DAC / 15 4-bit DAC



< SKIROC2A > Variation < Dynamic range

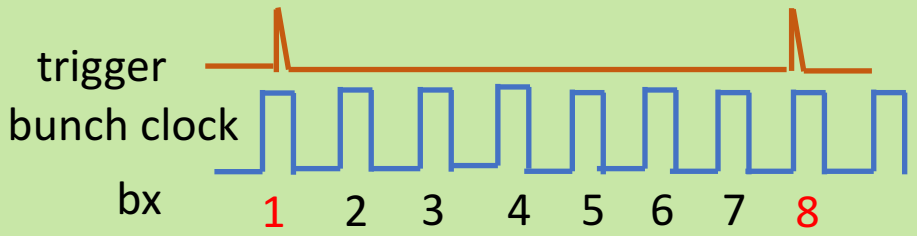
→Correction by 4-bit DAC is possible

Fast shaper

Injection		10-bit DAC trigger threshold	
channel	charge [MIP]	1 MIP	2 MIP
ch.0-63 (ch by ch)	1 and 2	250-340 (at 4 interval)	360-450 (at 4 interval)

bx = 9,10,11
: count hit and event
bx > 11 : count event only
→Trigger efficiency
= hit / event @ each channel

- bunch crossing ID (bx) : Stored bunch clock index when an event is triggered



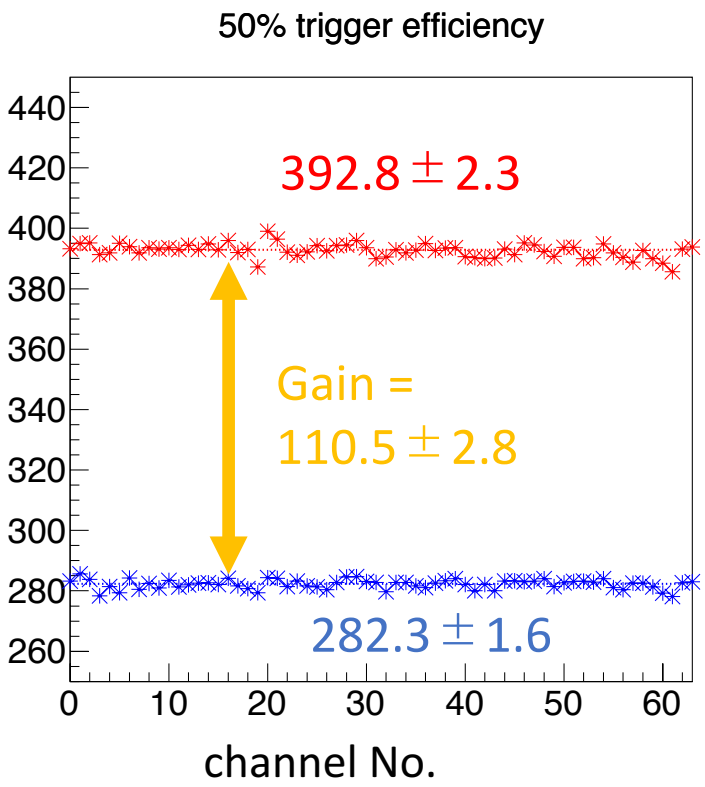
<Procedure>
1. (Testboard#5) Set a SKIROC2 or 2A to the socket
2. Run the automatic acquisition
    1. Set the injection charge
        2. Set one injection channel
            3. Set the threshold
                4. Run the automatic system
            5. Change the threshold & do 4. again
        6. Change the injection channel & do 4.-5. again
    7. Change the injection charge & do 4.-6. again

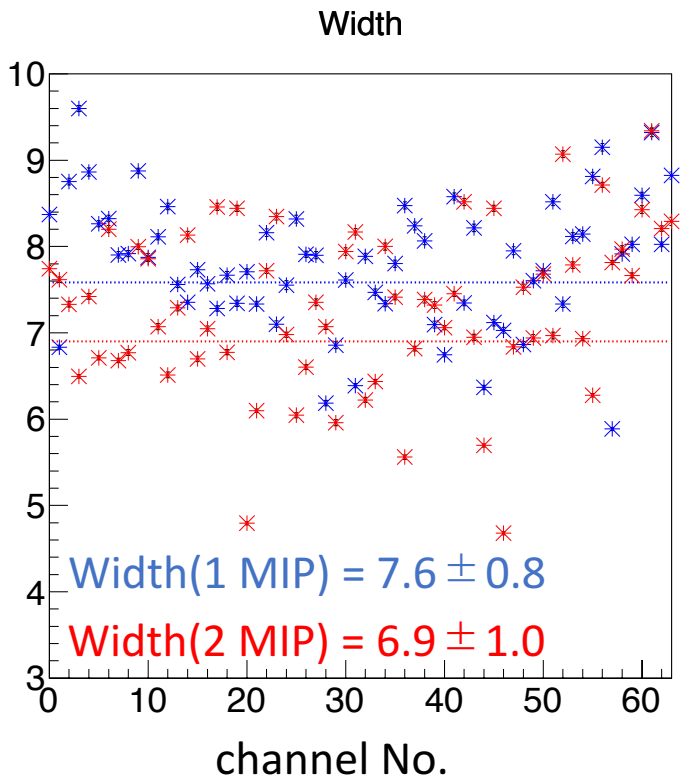
<The automatic acquisition system>
1. Reset the FPGA parameters by Labview script
2. Write new parameters
3. Check the written parameters
4. Do data acquisition

Fast shaper

- Testboard#5 (socket version), SKIROC2A chip1

*: 1 MIP
*: 2MIP



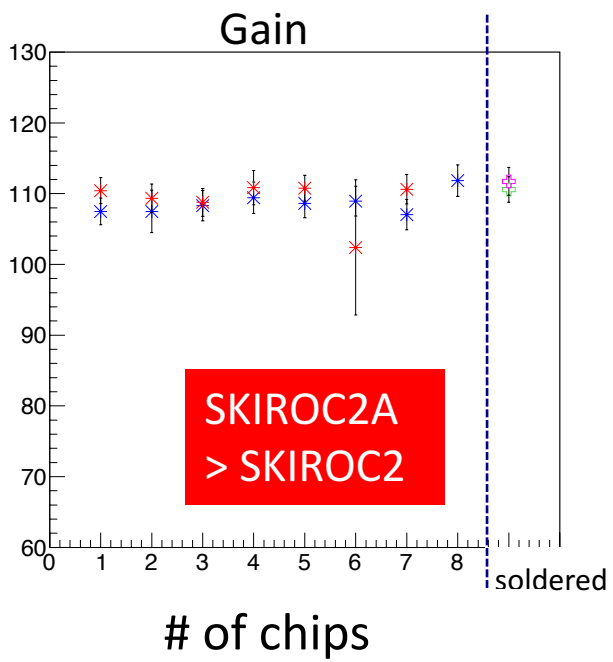


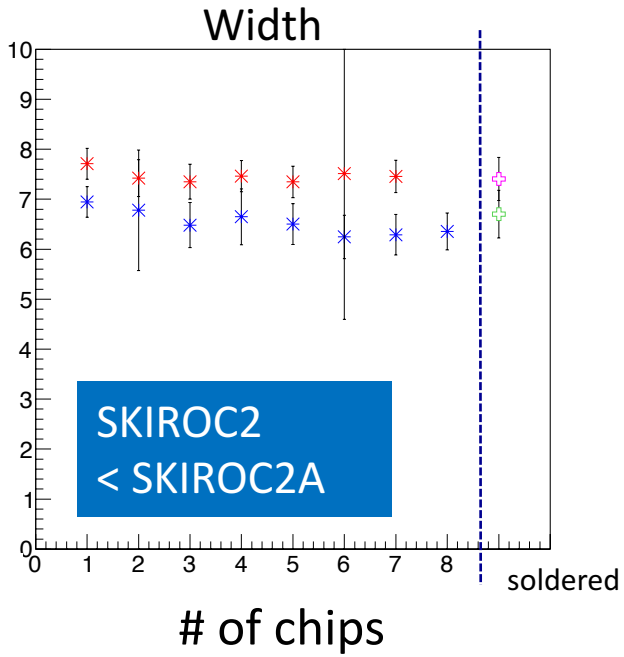
SKIROC2A chip1	Fitted mean	Channel variation (sigma)
Gain	110.5	2.8
Width (1 MIP)	7.6	0.8
S/N	14.6	1.5

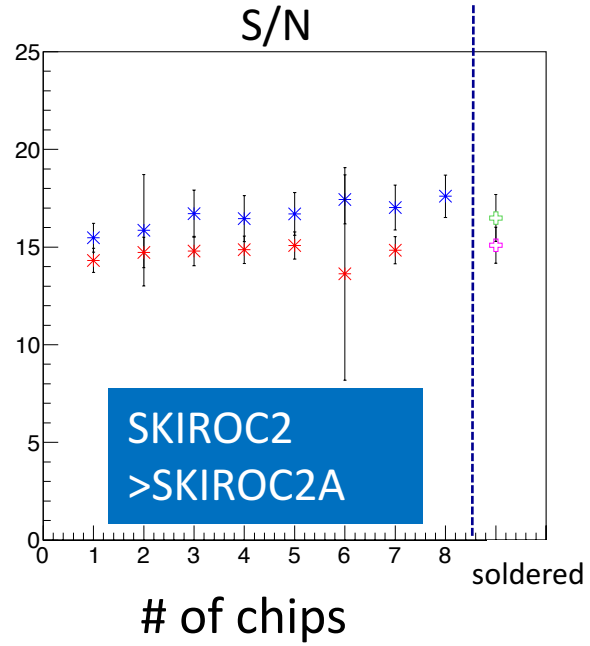
Fast shaper

- Testboard#5 (socket version)
  Testboard#2, #4 (soldered version)
- At Testboard#5,
  8 SKIROC2 chips and 8 SKIROC2A chips are measured.

Testboard#5
*: SKIROC2
*:SKIROC2A
✚:Testboard#2, SKIROC2
✚:Testboard#4, SKIROC2A







Some channel cannot be measured due to the socket got loose @ Testboard#5, chip6

All results of both SKIROC2 and 2A chips are in acceptable range.
We can use the automatic measurement system for checking chips .

Slow shaper

Injection		10-bit DAC trigger threshold		acquisition event
channel	charge [MIP]	SKIROC2	SKIROC2A	
ch.0-63 (ch by ch)	1 and 2	260	280	500

Gain (/ MIP) = (ADC between 1 MIP & 2 MIP)

Width of pedestal : ADC without charge injection @ 1 MIP

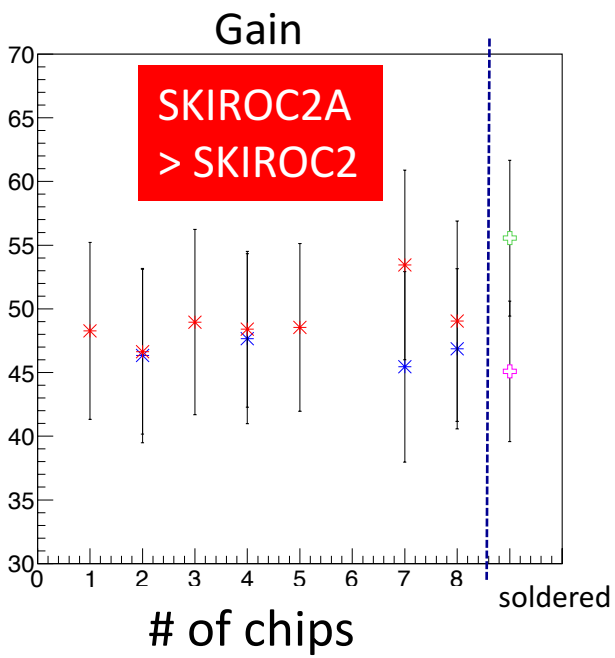
<Procedure>

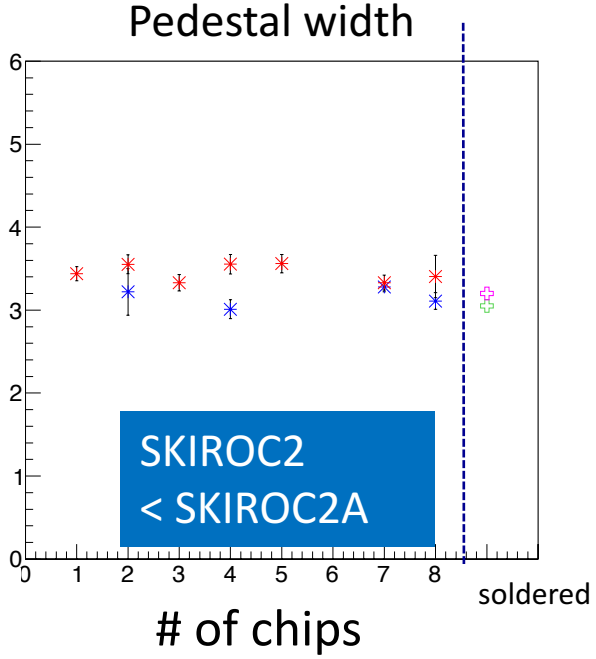
1. (Testboard#5) Set a SKIROC2 or 2A to the socket
2. Run the automatic acquisition
    1. Set the injection charge
        2. Set one injection channel
            3. Run the automatic system
        4. Change the injection channel & do 3. again
    5. Change the injection charge & do 3.-4. again

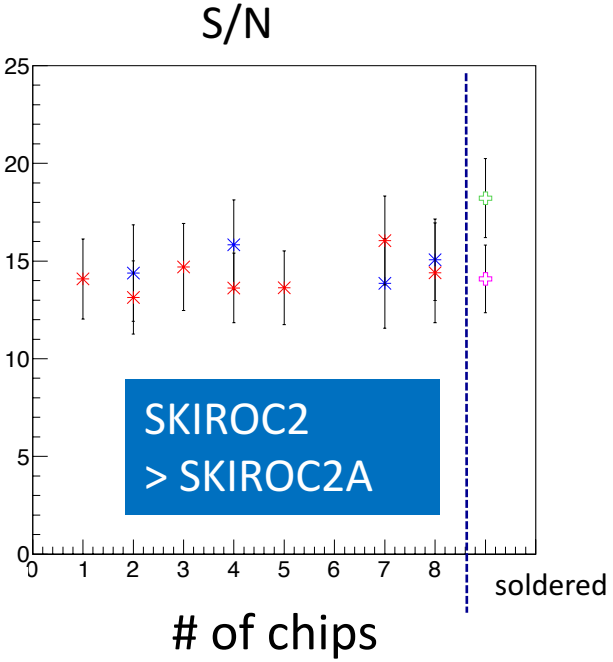
Slow shaper

- Testboard#5 (socket version)
  Testboard#2, #4 (soldered version)
- At Testboard#5,
  4 SKIROC2 chips and 7 SKIROC2A chips are measured.

Testboard#5
*: SKIROC2
*:SKIROC2A
✚:Testboard#2, SKIROC2
✚:Testboard#4, SKIROC2A



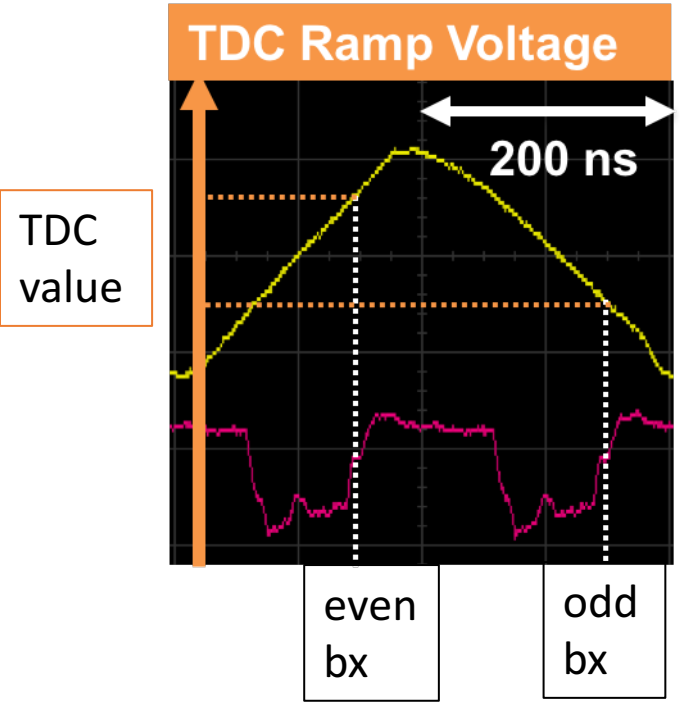




All results of both SKIROC2 and 2A chips are in acceptable range.

TDC

Test signal		10-bit DAC trigger threshold		TDC ramp	Clock delay value [ns]
input	charge [MIP]	SKIROC2	SKIROC2A	internal	0 – 200 (at 8 interval)
ch.10	5	350	350		

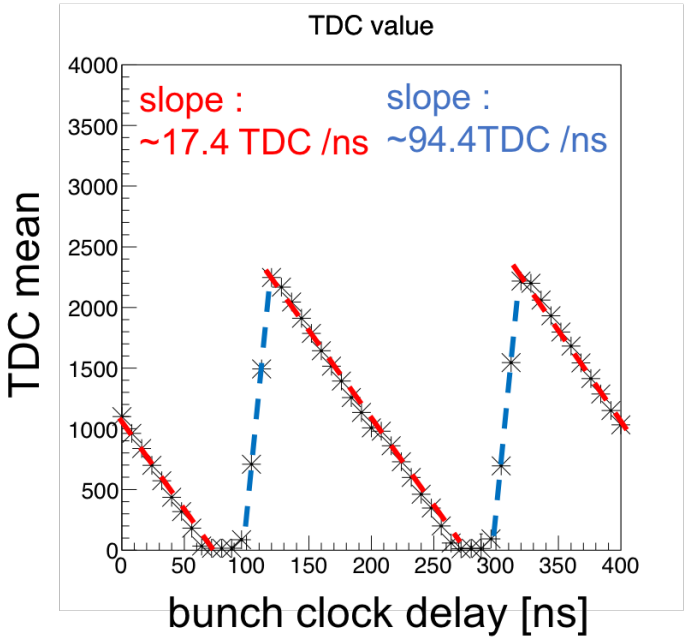


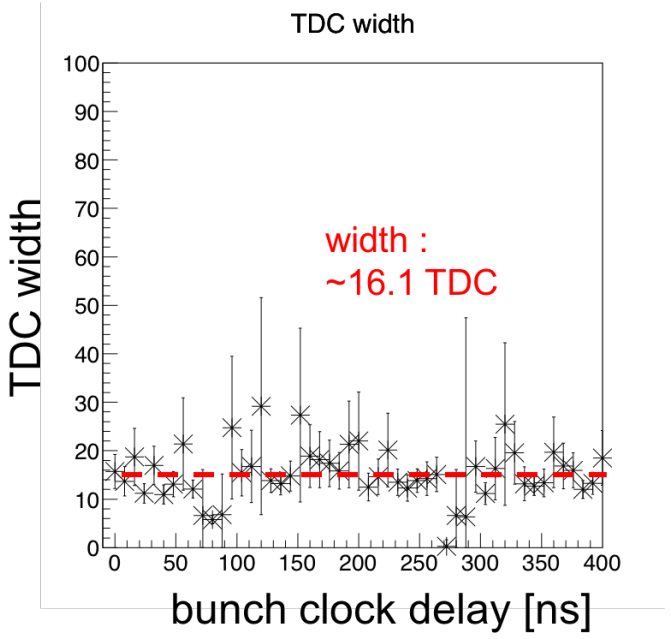
<Procedure>
1. Set a delay from slow clock to injection
2. Do data acquisition
3. Change the delay value & do 2. again

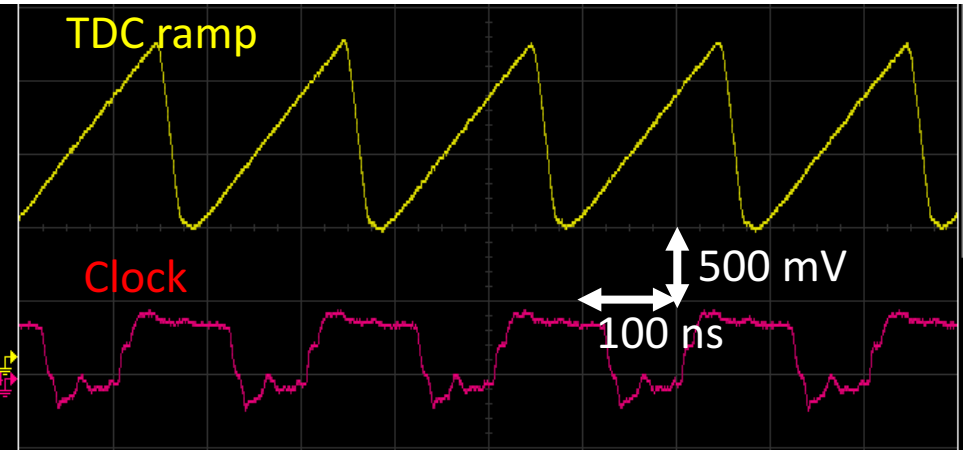
<Analysis>
1. Get both TDC value at even bx & odd bx from one acquisition data
2. Plot the TDC value against the clock delay value
3. Get the slope of TDC plot

TDC

<SKIROC2>







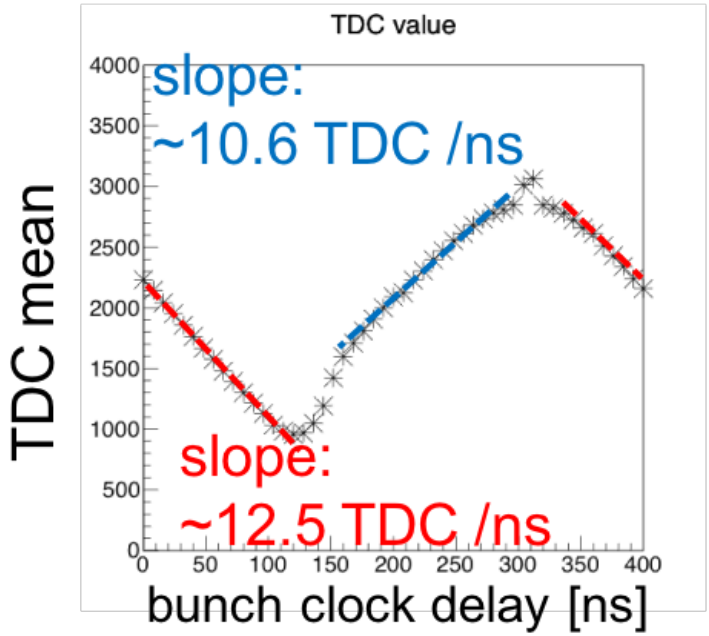
The period is in 1 bx

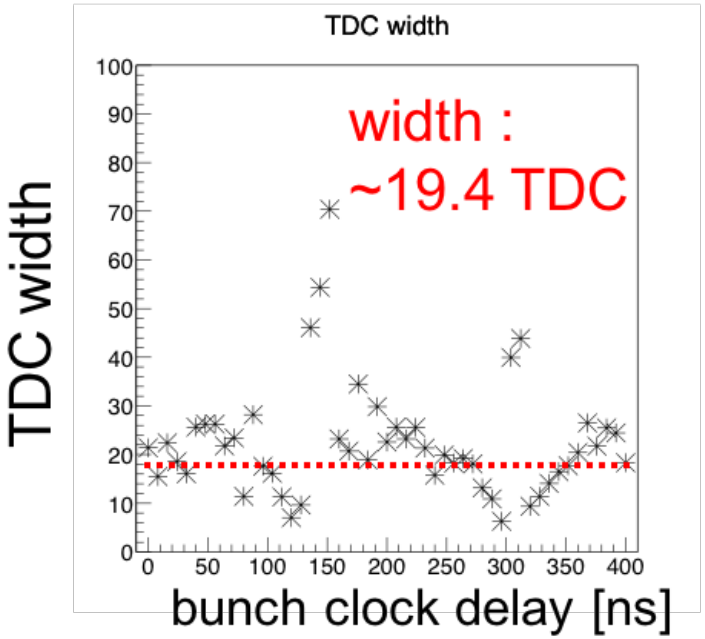
→ We cannot distinguish blue or red

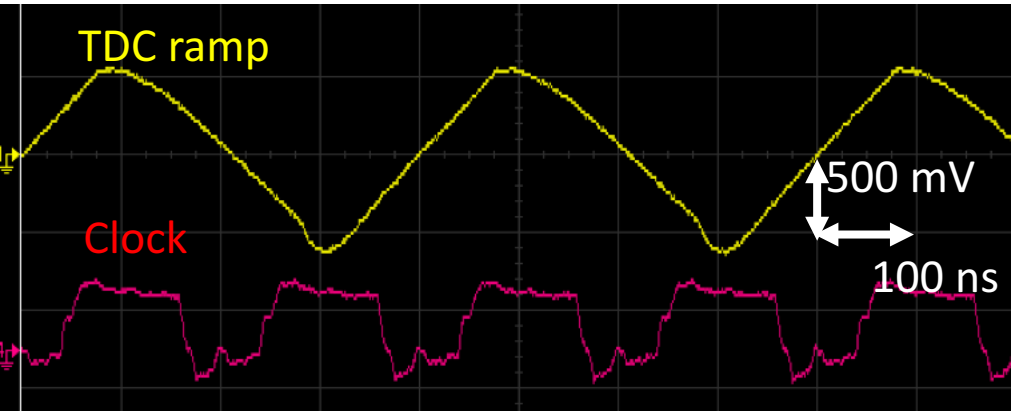
The time resolution is less than 1 ns.

TDC

<SKIROC2A>







The period is in 2 bx

→ We can distinguish blue or red

The time resolution is about 1.7 ns.

Summary

- We checked the performance of SKIROC2/2A
- For fast shaper & slow shaper, both SKIROC2 & 2A have good performance.
- For TDC, SKIROC2 has good performance at specific timing.
- For TDC, SKIROC2A has good performance.
- The automatic measurement system is usable.

Plan

- We make the slab prototype → check the performance in the testbeam

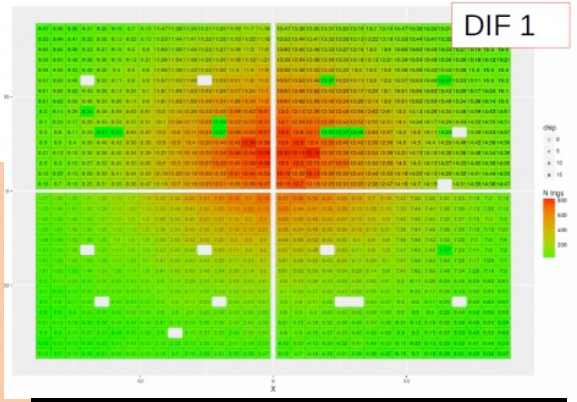
Backup

ECAL技術的プロトタイプと問題

- ILC ECALの技術的プロトタイプのビーム照射試験が行われている

  読み出しASICとしてSKIROC2を利用

- しかし、SKIROC2に関する問題が発生

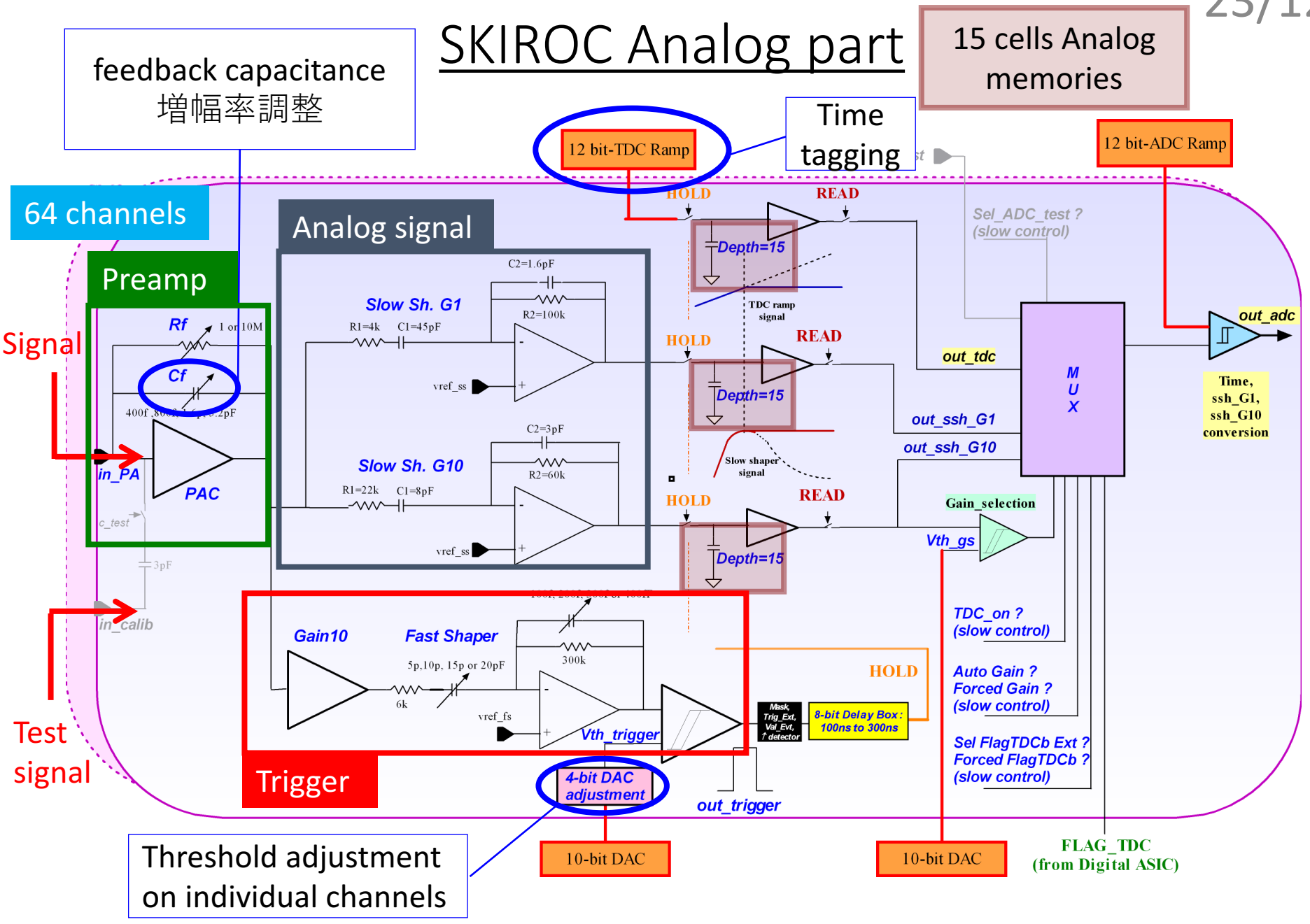


SPS test beam, Nov. 2015

1. Trigger threshold
2. Noisy channels
3. TDC
4. Retriggering発生：
   イベント発生直後に大量のトリガーが発行される現象
5. Empty event発生：
   イベント発生後、トリガーがない空データが収集される現象

→SKIROC2Aで改善された

SKIROC Analog part



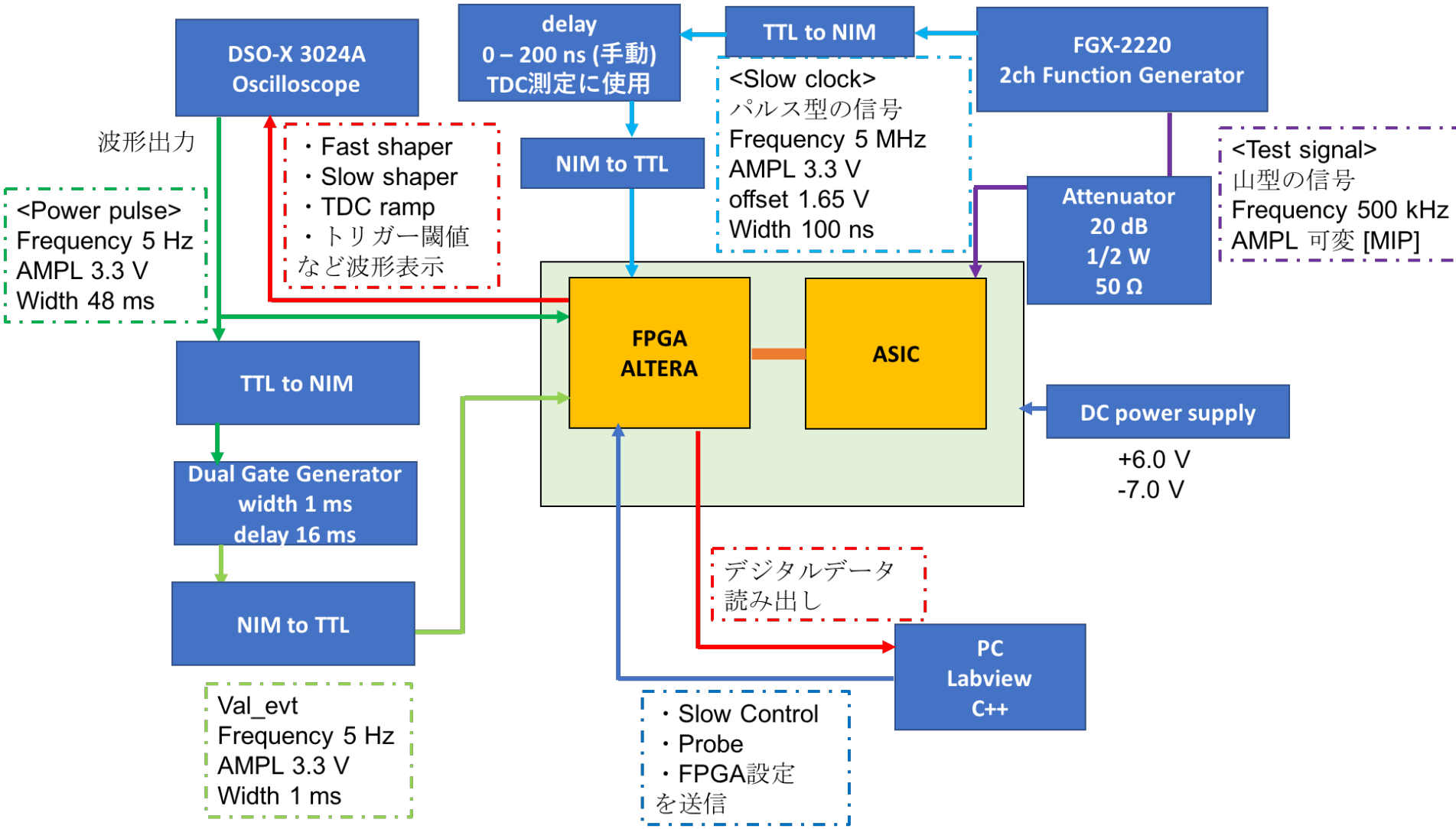
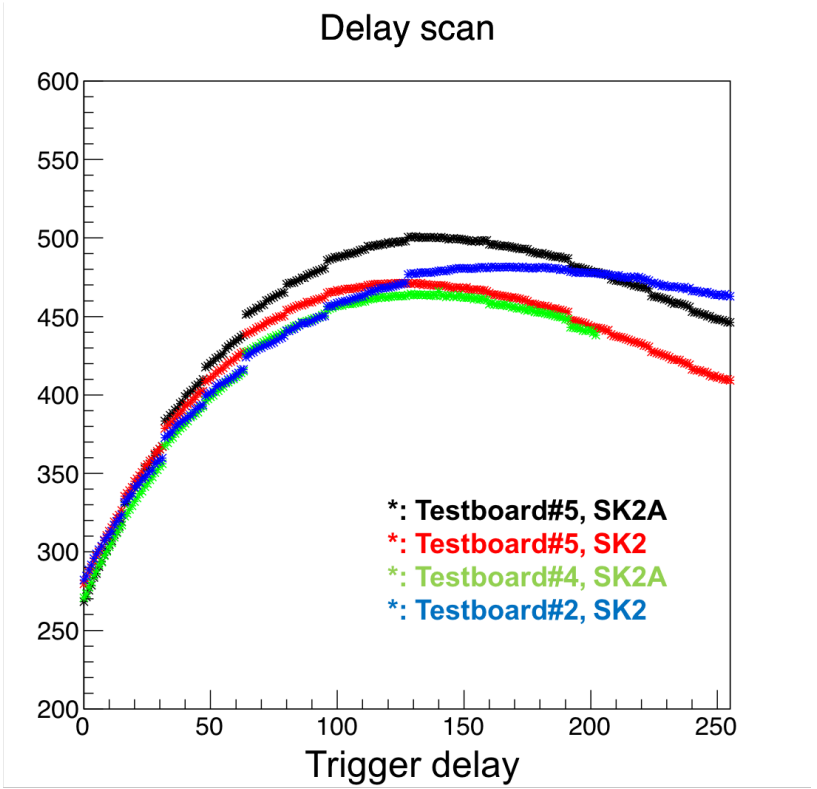

DSO-X 3024A
Oscilloscope
delay
0 – 200 ns (手動)
TDC測定に使用
TTL to NIM
FGX-2220
2ch Function Generator
波形出力
・Fast shaper
・Slow shaper
・TDC ramp
・トリガー閾値
など波形表示
NIM to TTL
<Slow clock>
パルス型の信号
Frequency 5 MHz
AMPL 3.3 V
offset 1.65 V
Width 100 ns
<Test signal>
山型の信号
Frequency 500 kHz
AMPL 可変 [MIP]
<Power pulse>
Frequency 5 Hz
AMPL 3.3 V
Width 48 ms
Attenuator
20 dB
1/2 W
50 Ω
FPGA
ALTERA
ASIC
TTL to NIM
DC power supply
+6.0 V
-7.0 V
Dual Gate Generator
width 1 ms
delay 16 ms
デジタルデータ
読み出し
NIM to TTL
PC
Labview
C++
Val_evt
Frequency 5 Hz
AMPL 3.3 V
Width 1 ms
・Slow Control
・Probe
・FPGA設定
を送信

表 5.1　SKIROC トリガー遅延の最適値 (Testboard#2,5)

Testboard	SKIROC	delay
#5	2 （チップ 1）	128
#5	2A （チップ 1）	139
#2	2 （チップ 1）	168
#4	2A （チップ 1）	134



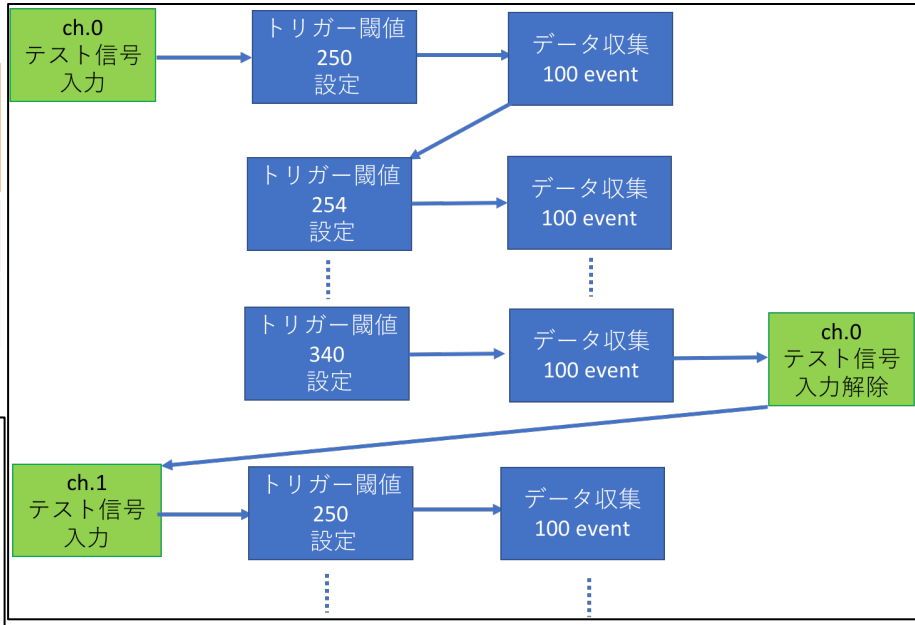
Automatic measurement system

Fixed

Trigger delay	feedback capacitance	compensation capacitance	4-bit DAC trigger threshold
Depend on testboards/chips	1.2 pF	1 pF	All channel：8

Variable

Test signal 1 MIP = 4.1 fC		10-bit DAC trigger threshold	
input	charge	1 MIP	2 MIP
ch.0-63	1 MIP,2 MIP	250-340	360-450



Process:

1. Set the injection charge
2. Select the injection channel
3. Set the threshold
4. Acquire 100 event
5. Change the threshold

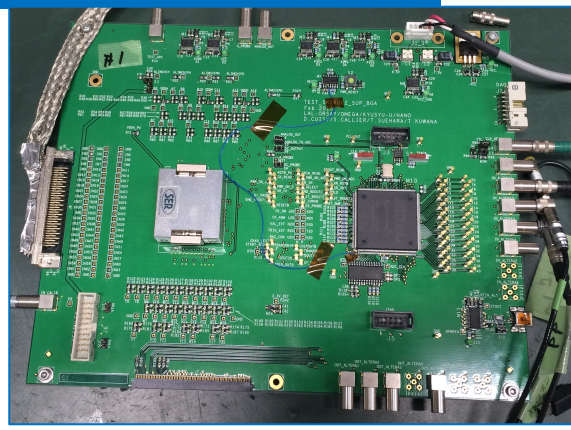
…

Semi-automatic measurement of 89 chips

Trigger delay	feedback capacitance	compensation capacitance	4-bit DAC adjustment
139	1.2 pF	1 pF	Disabled

	Form	Frequency	Amplitude	width
Test signal	Ramp	50 kHz		
Clock	Pulse	5 MHz	3.3 V	100 ns
Power pulse	Pulse	5 Hz	3.3 V	40 ms
val_evt	Pulse	5 Hz	3.3 V	1 ms

Used Testboard#1



<Semi-automatic measurement system>

1. Reset the FPGA parameters by Labview script
2. Write new parameters
3. Check the written parameters
4. Do data acquisition