KLauS: Updates on HBU Integration

KIP, Heidelberg University

Wei Shen

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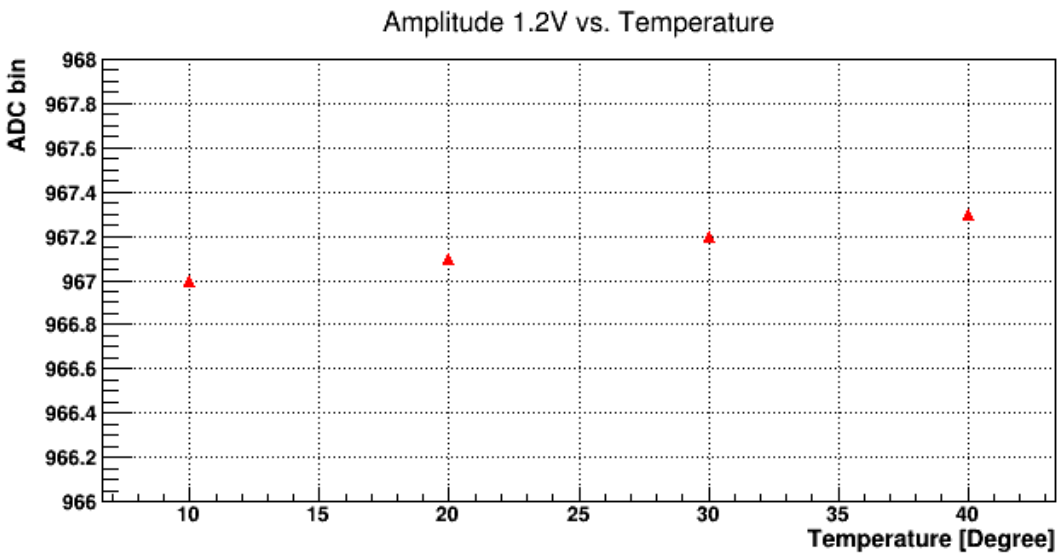
Overview

- Status of the KLauS ASIC
  - Temperature measurements
  - Timing measurements
  - The next KLauS version 6
- Status of the KLauS HBU integration

ADC @ different temperature

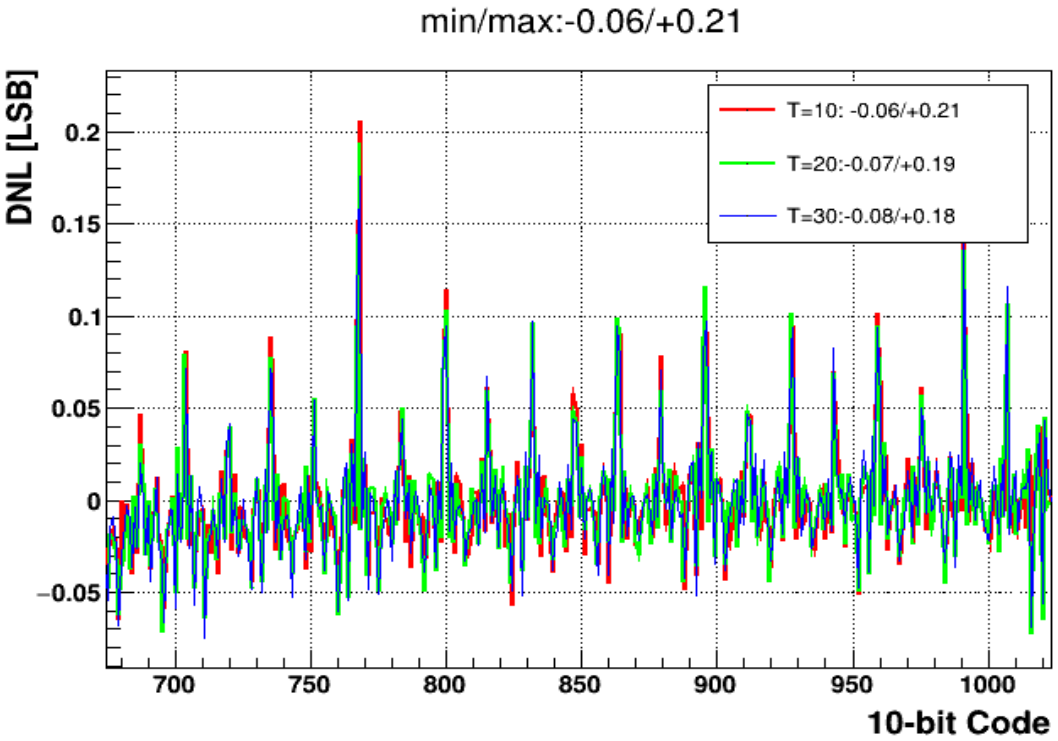
- AD conversion @ fixed DC input



No big changes in ADC alone.

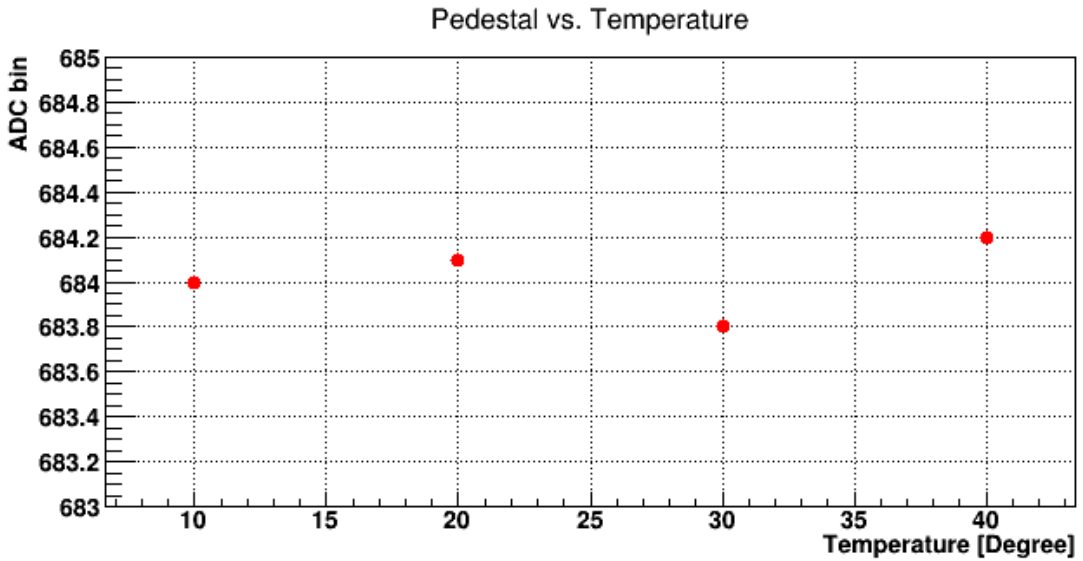
Expected: performance determined by the mismatches between capacitors.

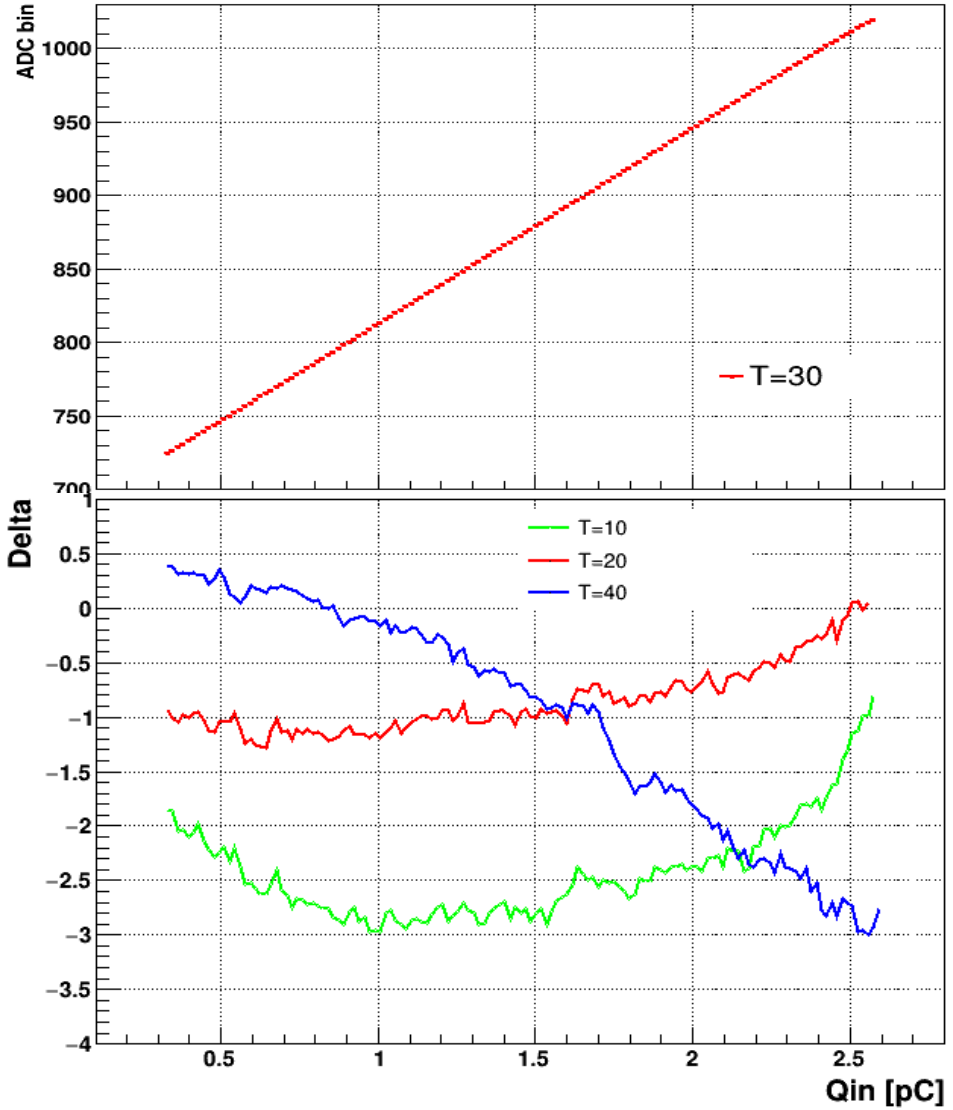
- Differential Non-Linearity (ROI)



Fullchain charge injection @ different temperature

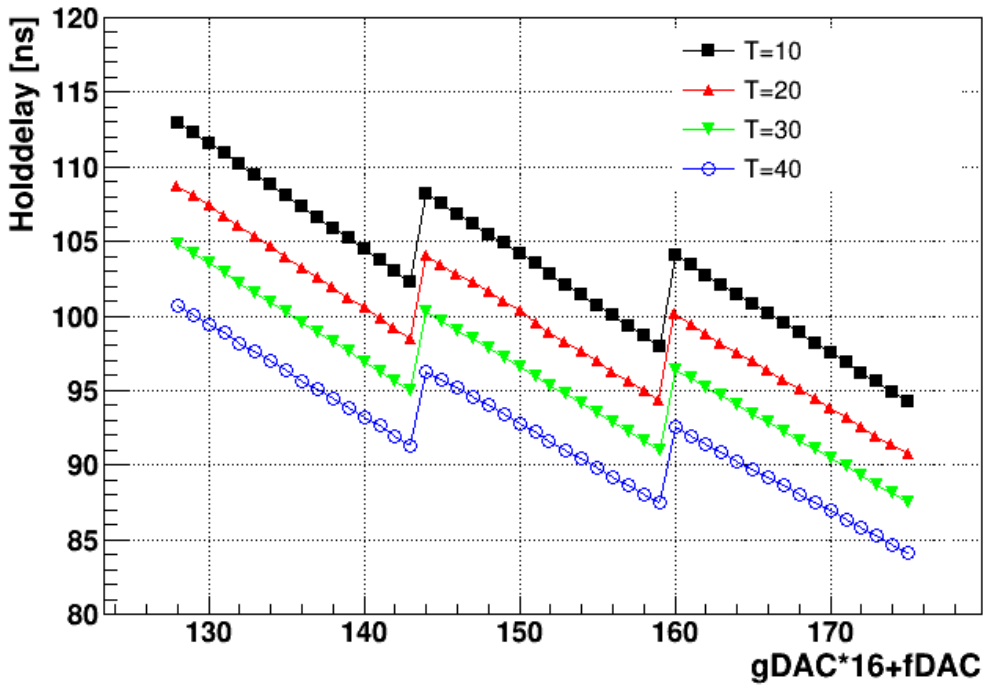
- **Input SiPM bias**: doesn‘t change
- **Front-end Pedestal**: no big change
- **Charge injection**:
  - For the working range 20-40°C, delta < 3 bin, within 1% FSR.

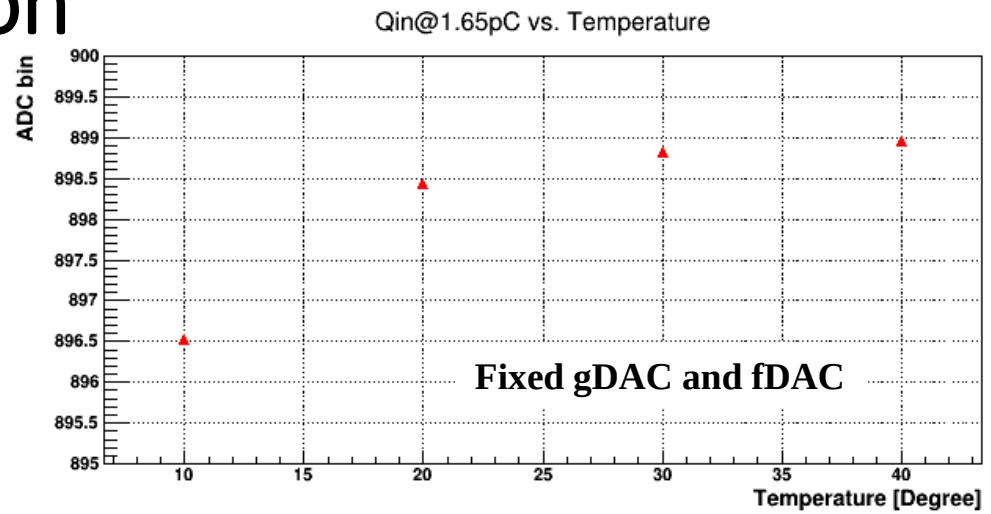


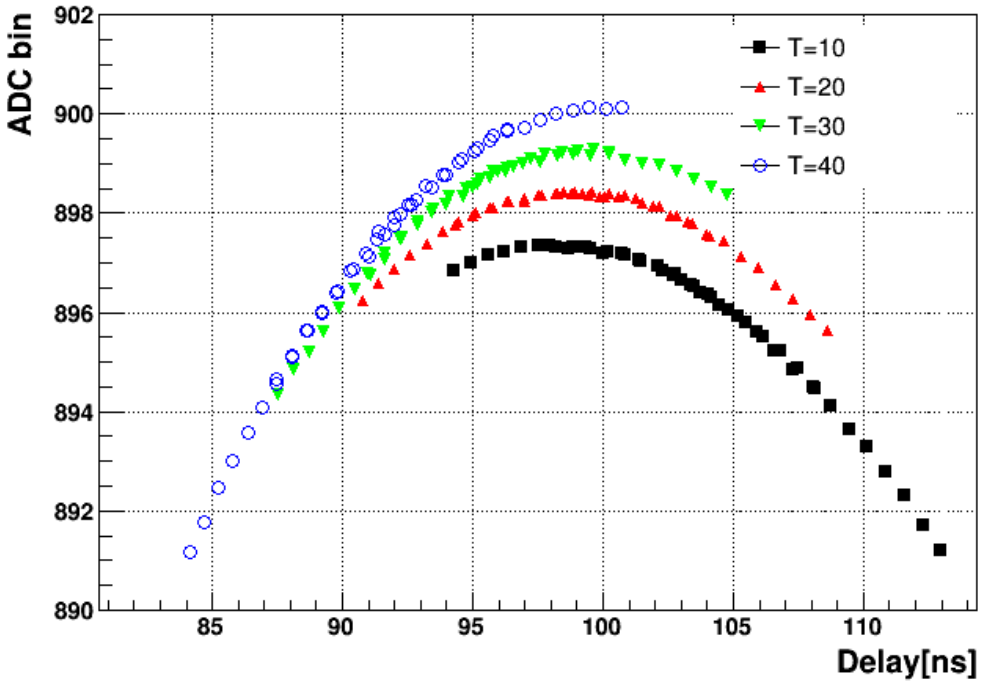


Fullchain @ fixed charge injection

- Close look at fixed charge injection with pulse reconstruction
  - Hold-delay contributes: 0.4ns/°C
  - Peak time no changes, but peak height changes around 1bin/°C

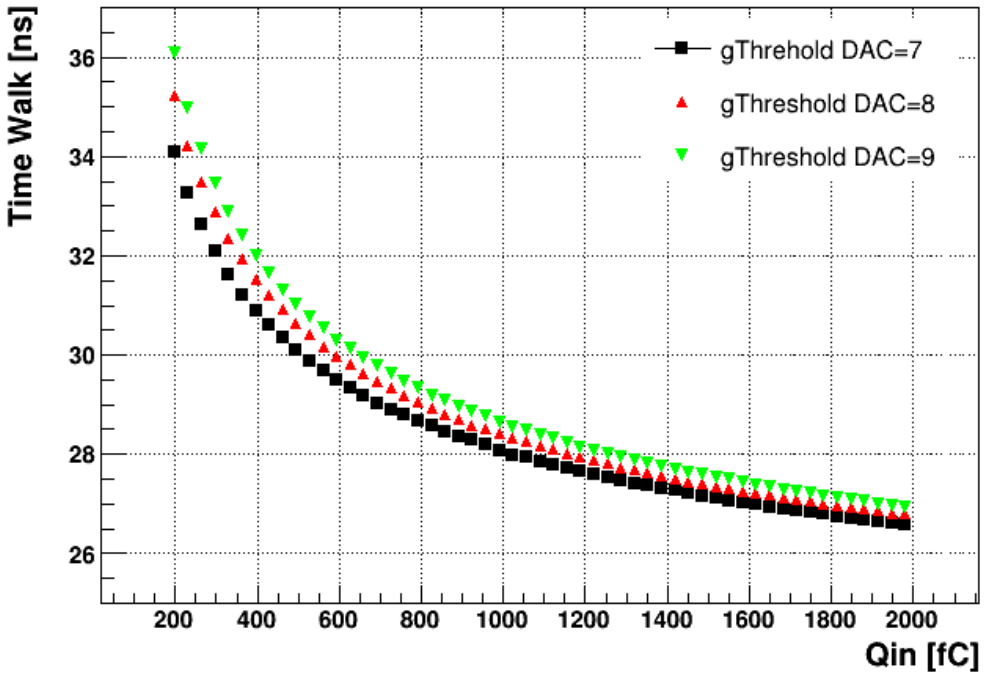


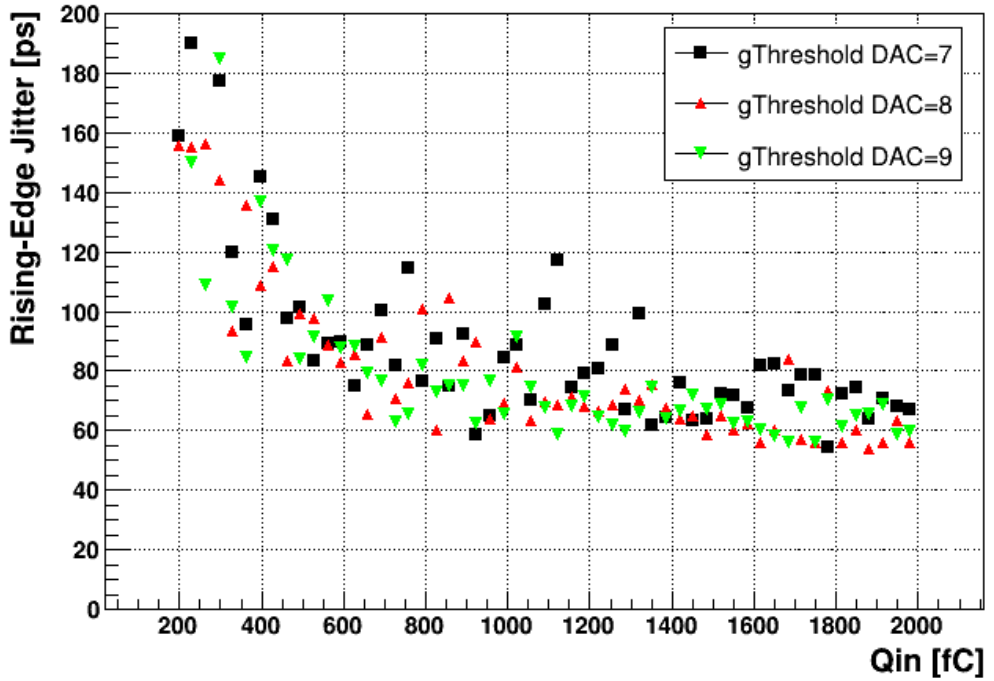




Timing measurements

- Time walk and rising edge jitter of the front-end trigger signal
- Jitter around 50-100ps(σ) for the front-end
  - ➢ No reason to pursue a TDC with binsize smaller than 180ps($50 \times \sqrt{12}$)





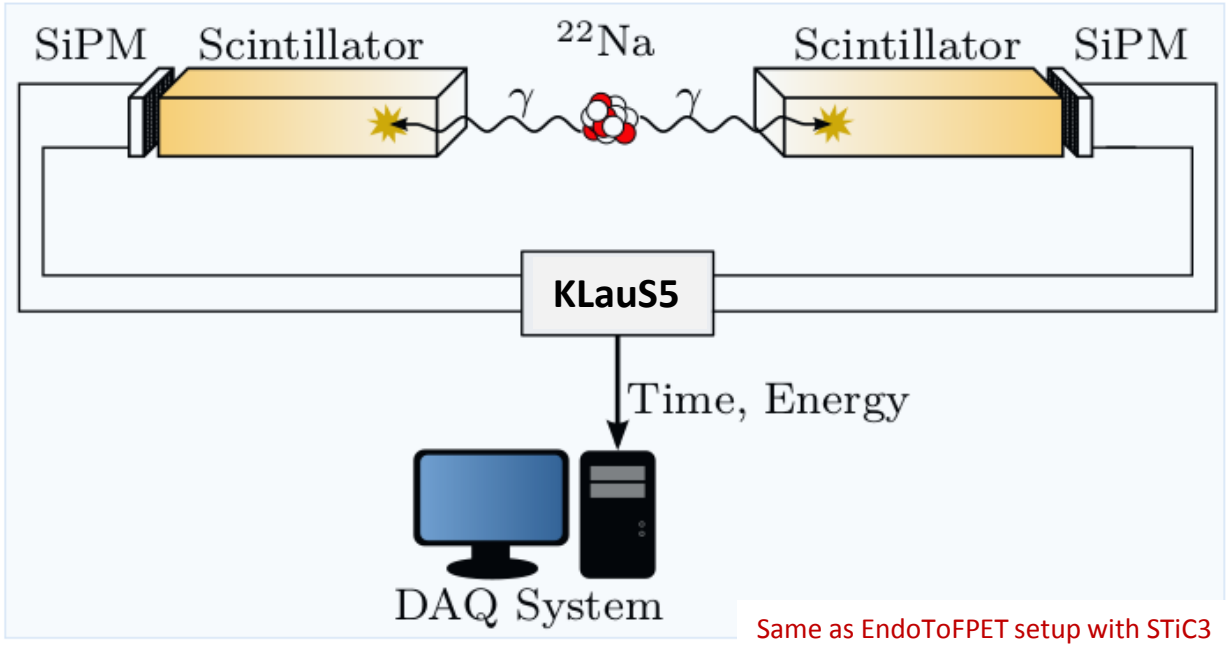
CTR Measurement Setup

Scintillator: LYSO:Ce, $3.1 \times 3.1 \times 15mm^2$

Hamamatsu MPPC S12643-050CN(X)

Temperature: 15℃

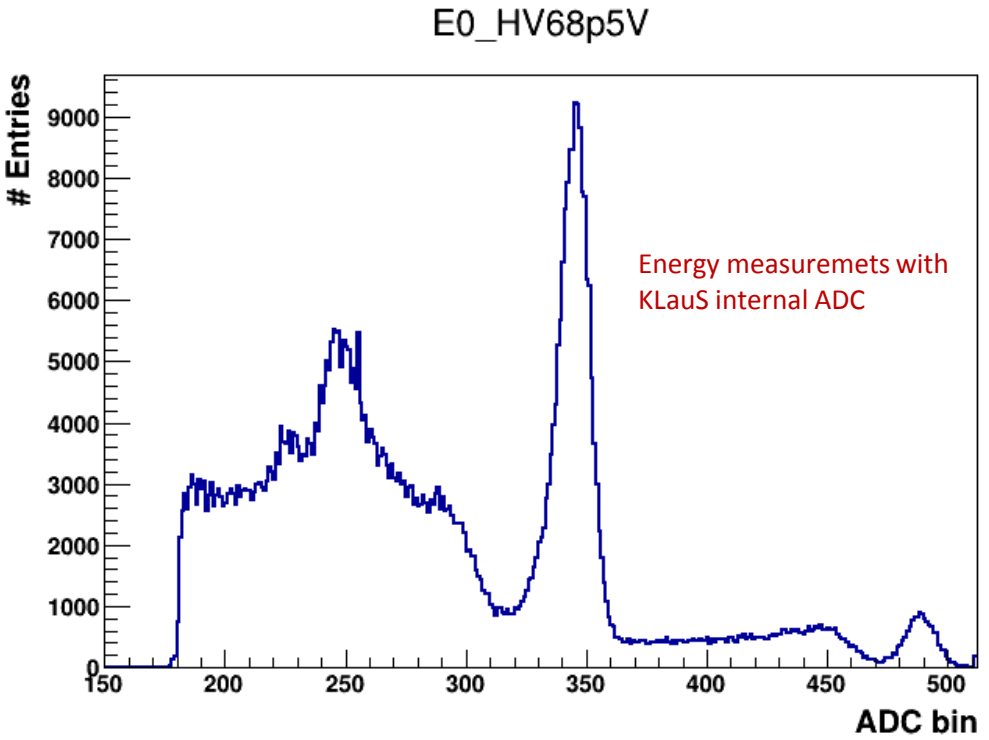
Two ASIC used. Scope to get the amplitude/timing information



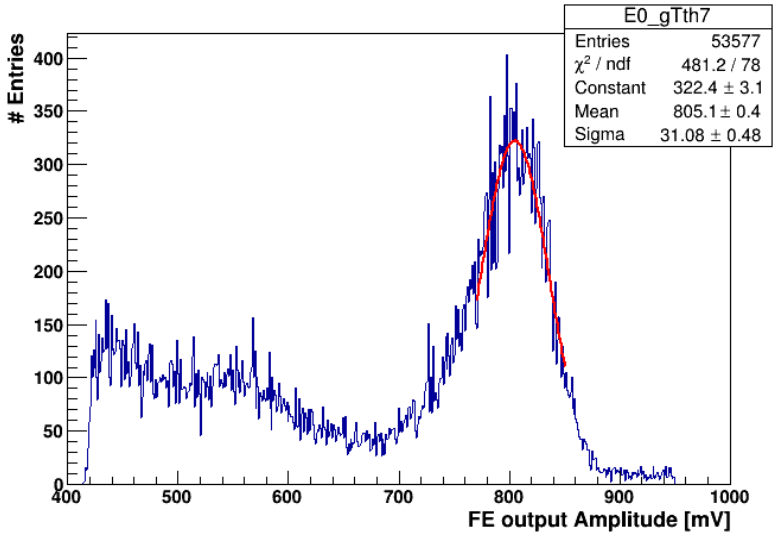
Same as EndoToFPET setup with STiC3

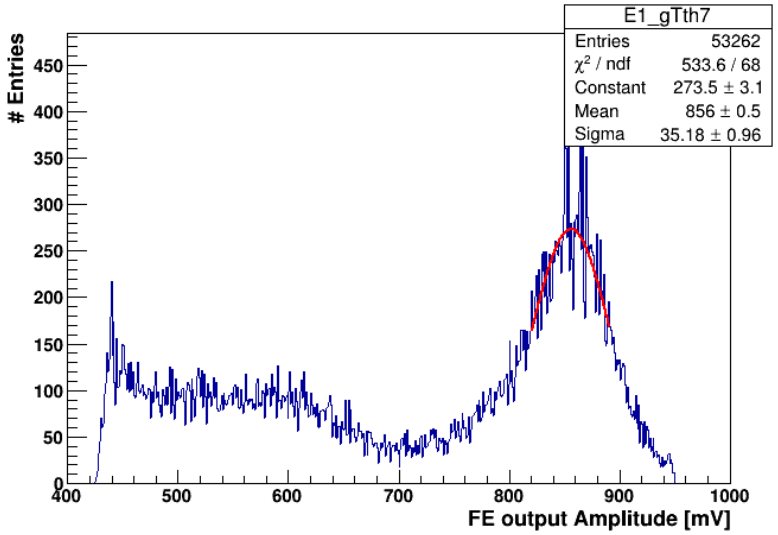
Energy resolution: 11.5%

Two peaks (511keV, 1275keV) are used to do the calibration



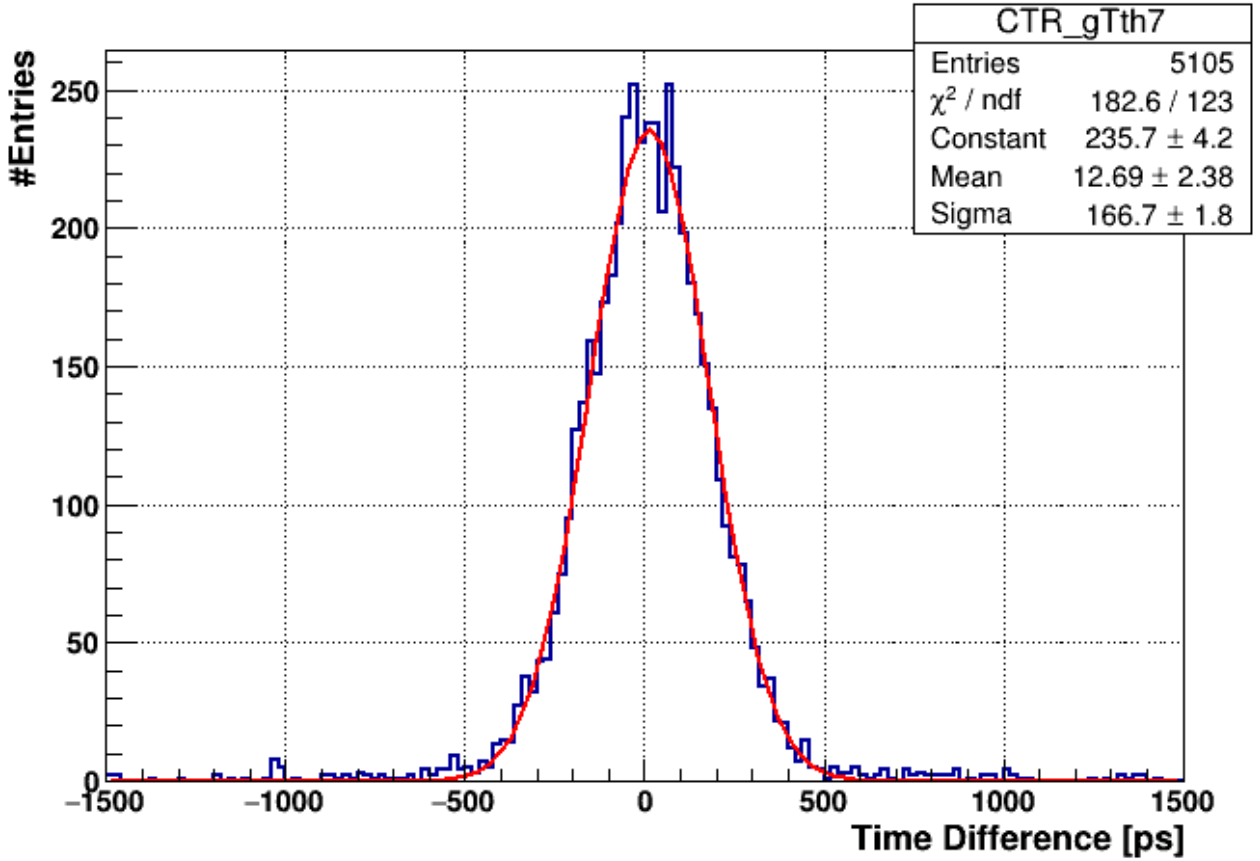
Coincidence Timing Resolution





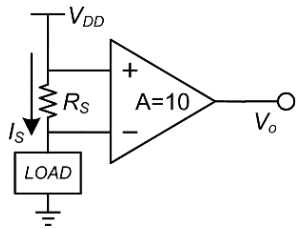
Results (no needs to apply time-walk correction):

- **393ps (FWHM)** with energy cut of $\pm\sigma$
- 423ps (FWHM) with energy cut of $\pm 2\sigma$



TDC Design Considerations: power constraints

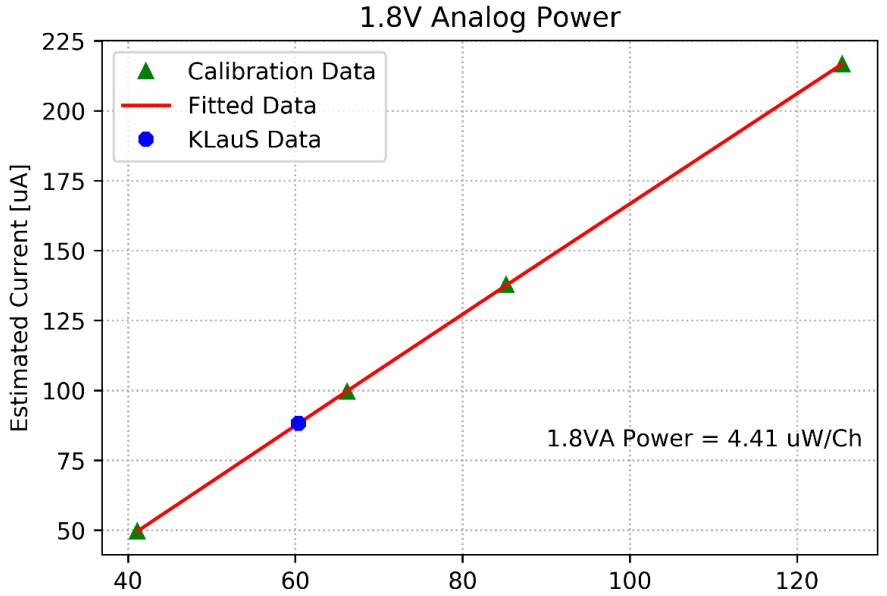
- **Re-measure** the power consumption under *acquisition-off state*
  - Same setup as before
  - Setup calibrated: resistor, gain, offset
  - Exclude power from other active components

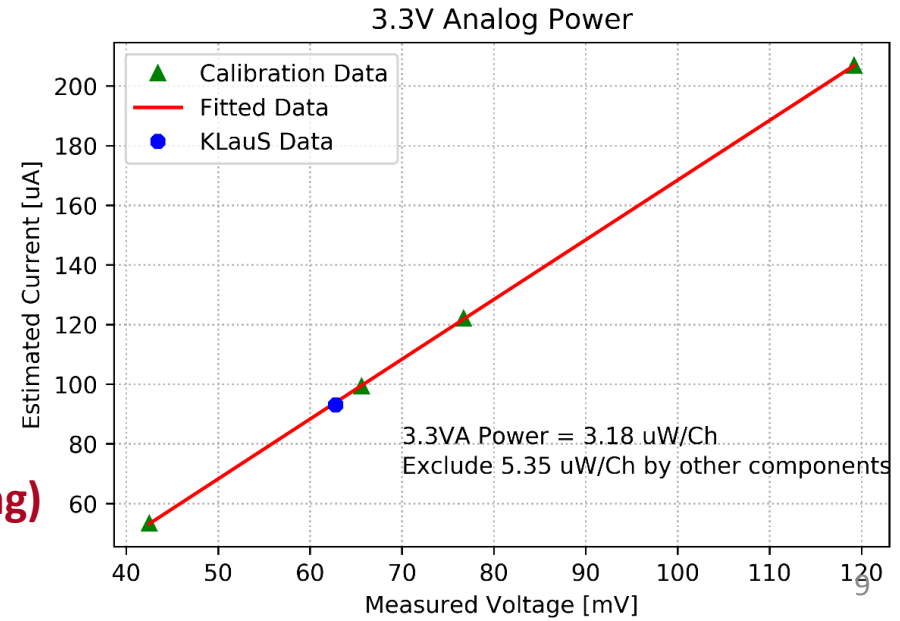


- **Results:**
  - Same for results under acquisition-on state
    - **2.5 mW/Ch** (VA3.3 → 0.93, VA1.8 → 1.53)
  - New results for acquisition-off state

Name	Simulation	Measurement
3.3 V VA	3.78	3.18
1.8 V VA	3.63	4.41

  - Power-consumption under 0.5% PP duty-cycle:
    - **20 uW/Ch** (for analog power only)
    - **5 uW/Ch budget left for TDC and digital parts (challenging)**





KLauS6 Design Status

- **TDC Design Specfications:**
  - Bin-size: 200ps(depending on the actual power consumption)
  - Time range: 16ms for test-beam mode (1.6ms for ILC mode)
  - Fast lock time: < 10us (smaller than the front-end settling time)
  - Power consumption: < 18mW (for all channels, scaled to 2.5uW/Ch with 0.5% duty cycle)

- **Design Implementations:**
  - Data structure: BXID + CC(16bits, 1.6ms) + FC(7bits, 25ns)
  - Byte number of hit data 5 bytes unchanged; T0 channel stores the BXID
  - Discard the T0 channel data if no event hit
  - TDC strucutre: PLL-based TDC, PLL clock multiply factor of 4, slightly different from STiC

- **The KLauS6 will be submitted at Q1 2019**

Updates on the HBU integration

- KLauS5 packaging
  - 52 naked chips will be sent and expect get 47 chips back
  - Purchase Order from DESY received by Novapack
  - Expected submit the substrate order before the end of this month (guess it‘s delayed)
  - Expected get the packaged chip by the end of Oct.

- Test-board for the packaged chip
  - Design on-going, expected ready by the end of Oct.

- HBU integration
  - HBU_HD Schematic design already finished by Mathias. Waiting for the PCB layout design.....
  - Also POWER board finished
  - Firmware and software design will start once we get the HBU board ready