New Results on the 36-channel KLauS ASIC

Z. Yuan, K. Briggl, H. Chen, Y. Munwes,
W. Shen, V. Stankova, H.-C. Schulz-Coulon

Kirchhoff Institute of Physics, University Heidelberg
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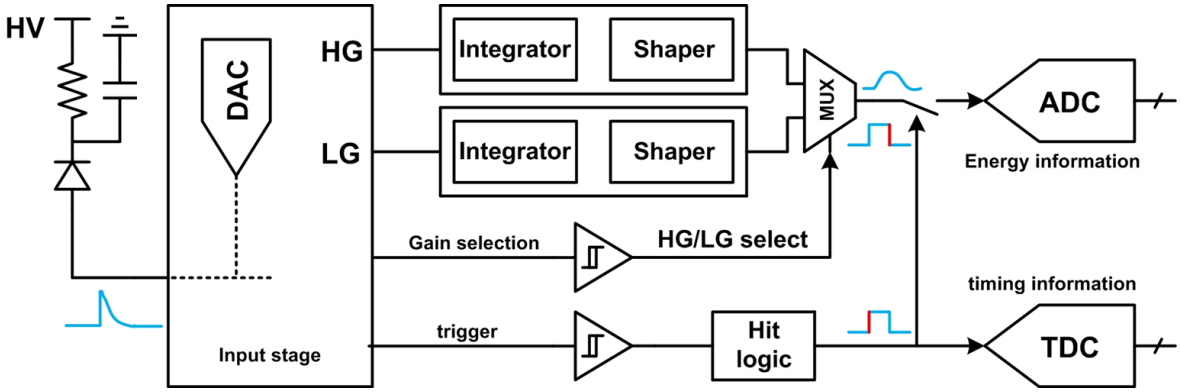
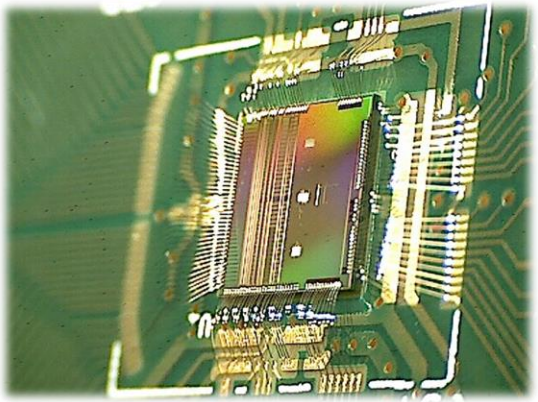
- Results of the 36-channel ASIC
  - Front-end
  - ADC
  - Full-chain linearity
  - Detector measurements
- Summary

KLauS chip and test setup





KLauS5

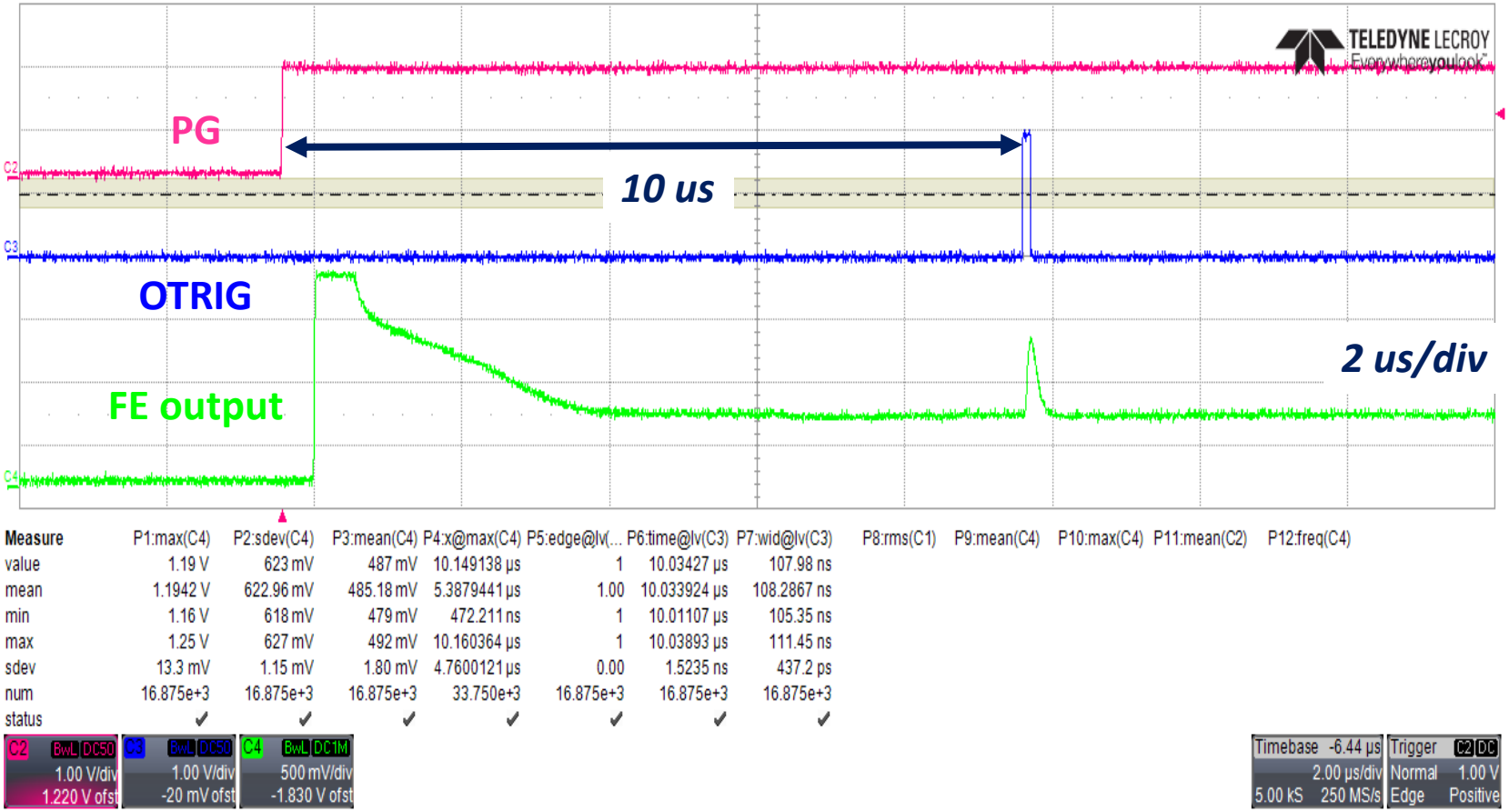
Received in Nov. 2017
Test started 2 weeks ago

Setup same as KLaus4:

- **Raspberry Pi**
- **Interface board**
- **Testboard**

I2C for data-taking

Scope waveforms



Measure	P1:max(C4)	P2:sdev(C4)	P3:mean(C4)	P4:x@max(C4)	P5:edge@lv(...	P6:time@lv(C3)	P7:wid@lv(C3)	P8:rms(C1)	P9:mean(C4)	P10:max(C4)	P11:mean(C2)	P12:freq(C4)
value	1.19 V	623 mV	487 mV	10.149138 µs	1	10.03427 µs	107.98 ns					
mean	1.1942 V	622.96 mV	485.18 mV	5.3879441 µs	1.00	10.033924 µs	108.2867 ns					
min	1.16 V	618 mV	479 mV	472.211 ns	1	10.01107 µs	105.35 ns					
max	1.25 V	627 mV	492 mV	10.160364 µs	1	10.03893 µs	111.45 ns					
sdev	13.3 mV	1.15 mV	1.80 mV	4.7600121 µs	0.00	1.5235 ns	437.2 ps					
num	16.875e+3	16.875e+3	16.875e+3	33.750e+3	16.875e+3	16.875e+3	16.875e+3					
status	✔	✔	✔	✔	✔	✔	✔					

C2 BwL DC50 1.00 V/div 1.220 V ofst | C3 BwL DC50 1.00 V/div -20 mV ofst | C4 BwL DC1M 500 mV/div -1.830 V ofst

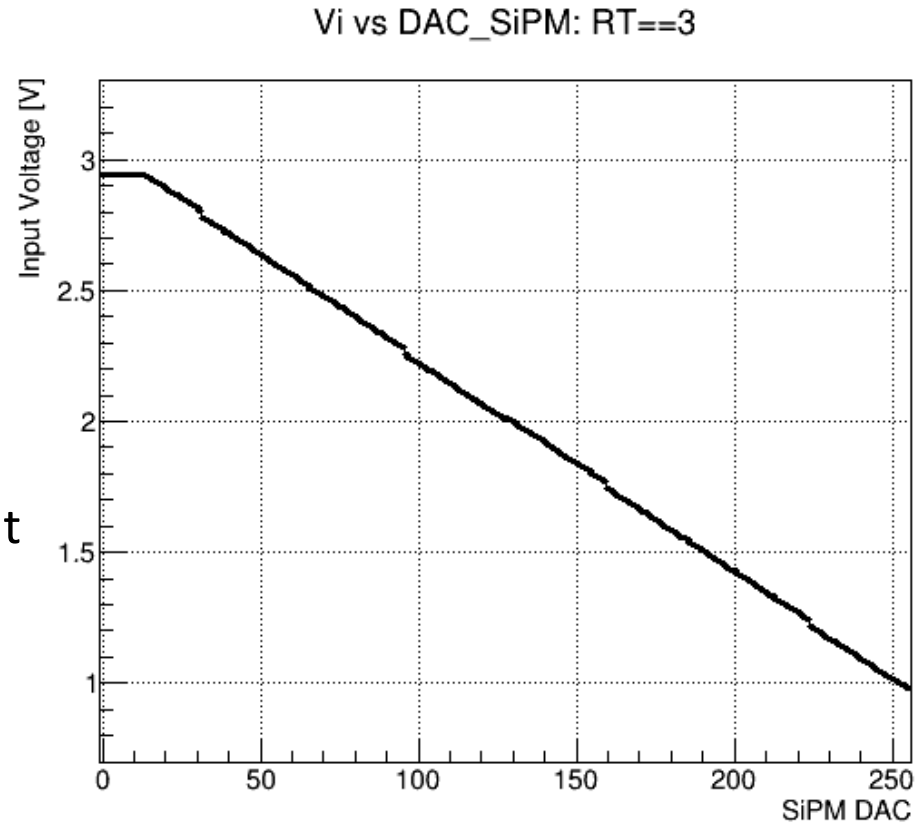
Timebase -6.44 µs 2.00 µs/div 5.00 kS 250 MS/s | Trigger C2 DC Normal 1.00 V Edge Positive

SiPM bias voltage tuning

- 8-bit DAC to tune the SiPM Bias voltage

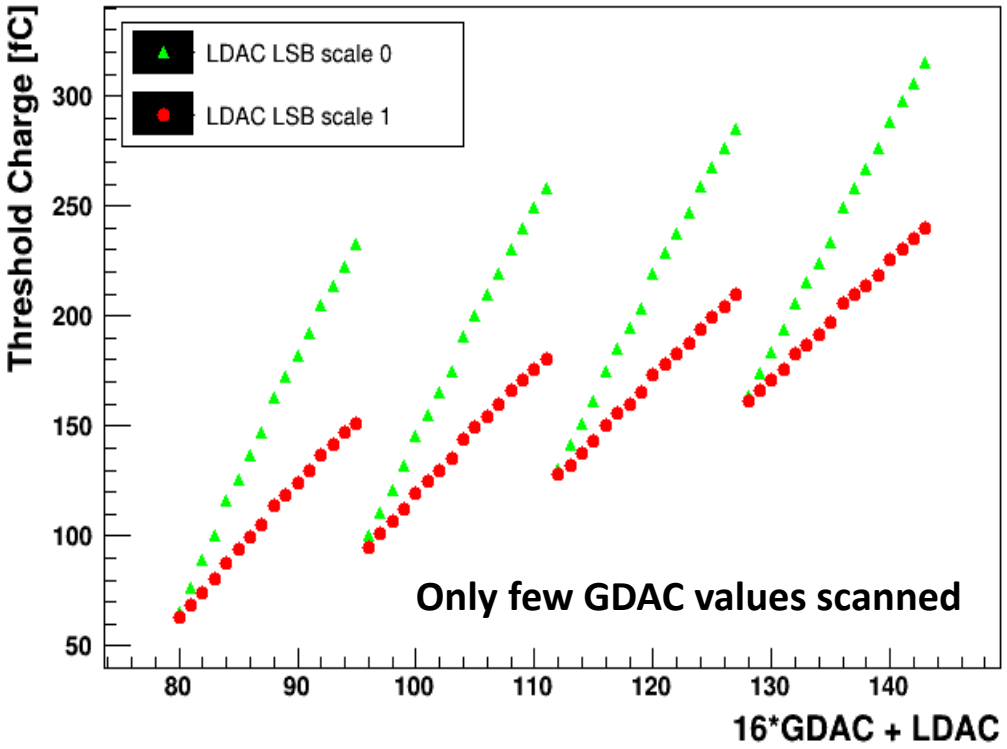
2V tuning range as expected

Negeligible impact on the FE output
Pedestal value



Trigger comparator

- Generate trigger signal for time-stamping and digitization
- Set the threshold to the same pixel levels



Two DACs to adjust the threshold:

- **Global 6-bit DAC**:
  - Coarse setting, ~25fC/LSB
- **Local 4-bit DAC** per channel:
  - Fine tuning
  - ~ 6 fC/LSB (trig scale=1)
  - ~11 fC/LSB (trig scale=0)

Dispersion among channels/chips (uniformity) can be tuned by this two DACs

ADC in 10-bit mode

- Linearity measurements --- sweep DC voltage
  - Range: 1.62V ⇦ parasitics in the MSB array

DNL:

Differential Non-Lineairty

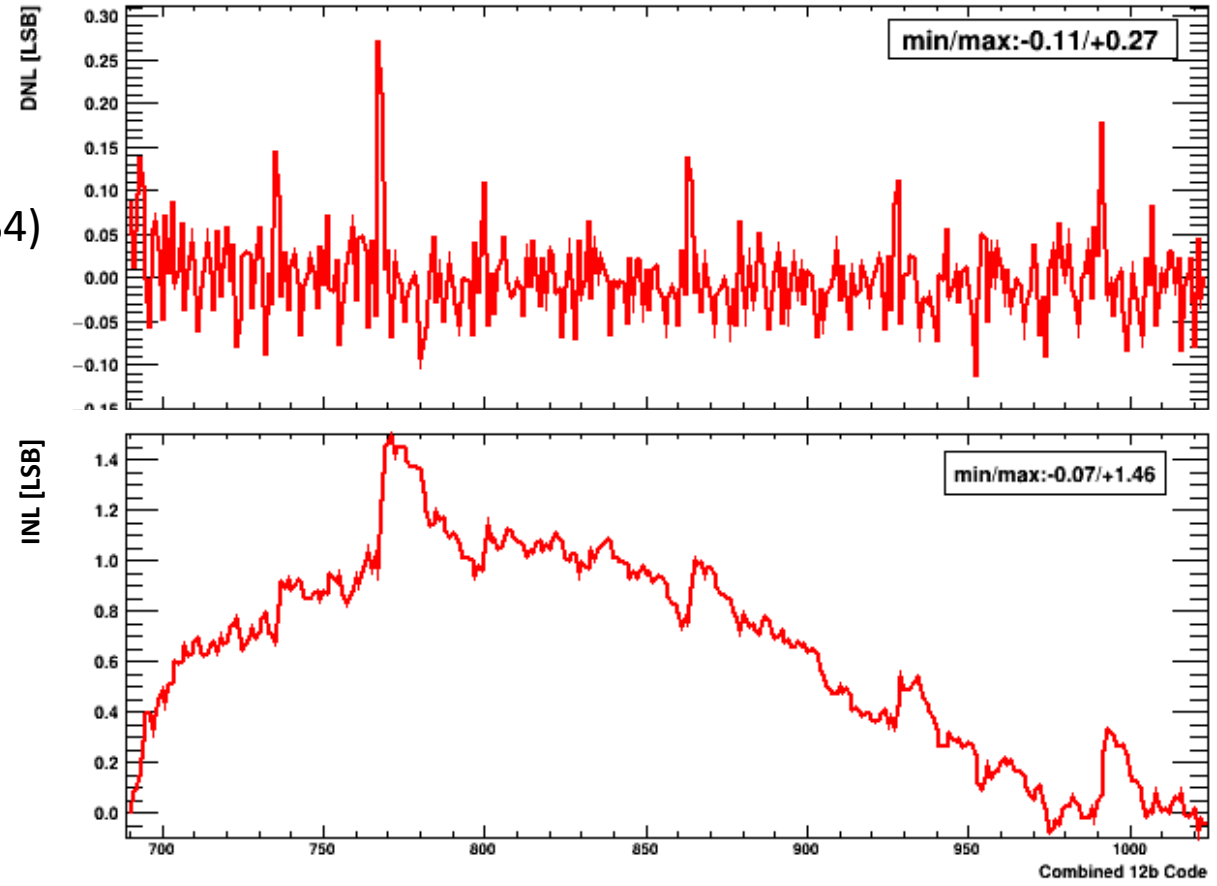
- -0.11/+0.27 LSB
- -0.52/+0.14 LSB (KLauS4)

INL:

Integral Non-Lineairty

- -0.07/+1.46 LSB

  Within 1% FSR



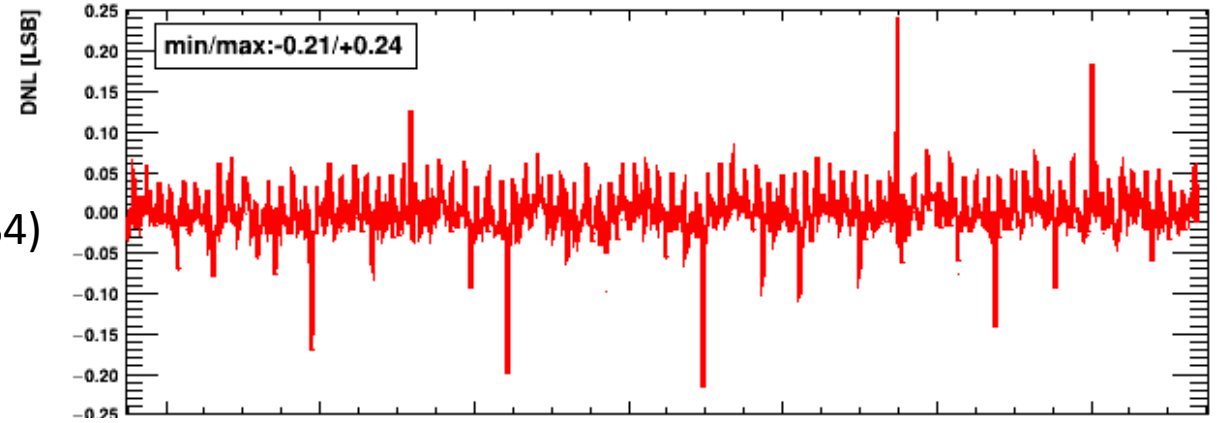
ADC in 12-bit mode

- Linearity measurements --- sweep DC voltage
  - Range: 1.62V ⇦ parasitics in the MSB array

DNL:

Differential Non-Lineairty

- -0.21/+0.24 LSB
- -0.44/+0.36 LSB (KLauS4)

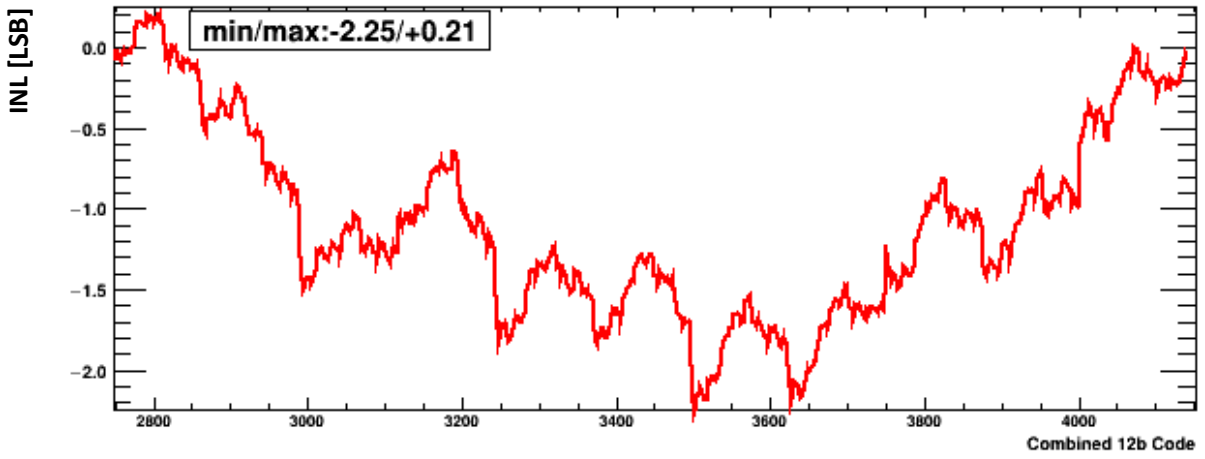


INL:

Integral Non-Lineairty

- -2.25/+0.21 LSB

  Within 1% FSR



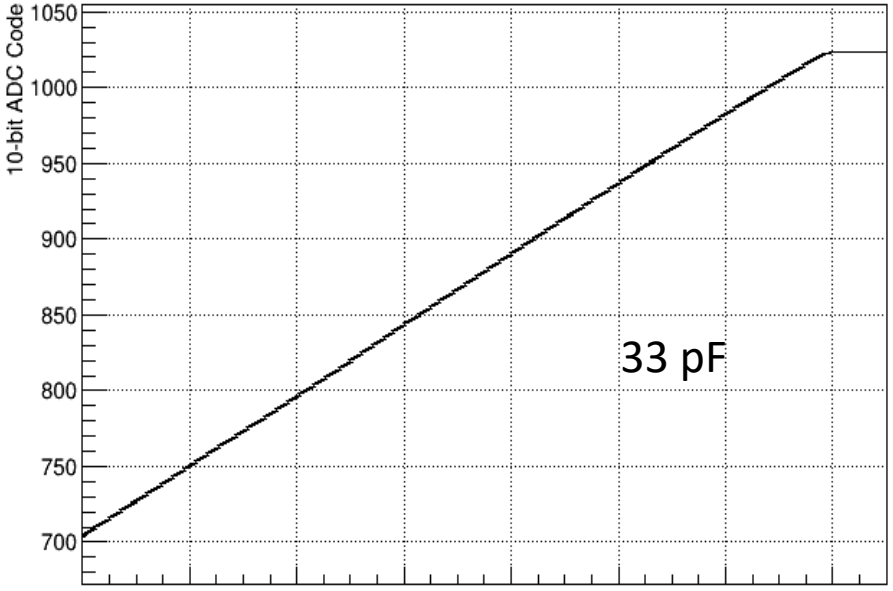
Charge measurements

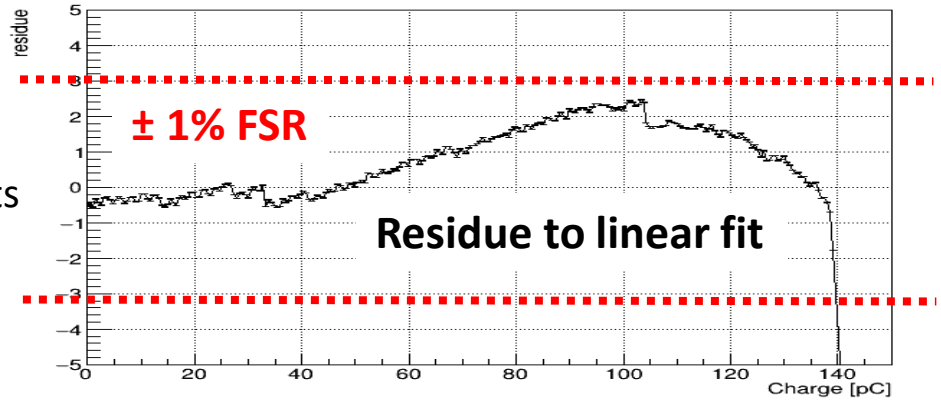
	Parameters	KLauS4	KLauS5*
HG	DR [pC]	2.3	2.4
	ENC [fC]	4.5	4.6
	Gain [mV/fC]	0.425	0.365
MG	DR [pC]	15.1	15.5
	ENC [fC]	15.3	16.6
	Gain [mV/fC]	70.5e-3	58.6e-3
LG	DR [pC]	131	140
	ENC [fC]	56	70.5
	Gain [mV/fC]	7.8e-3	6.95e-3

* non-conclusive, needs detailed measurements

- No degradation in ENC & DR

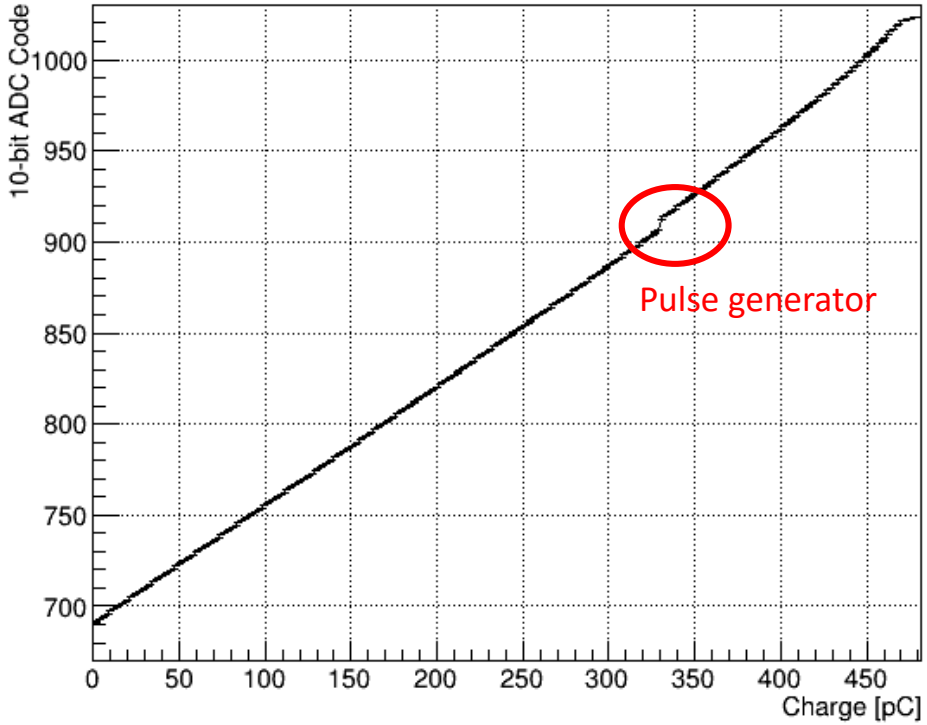
10-bit ADC Code ~ Input charge





Ultra low gain branch

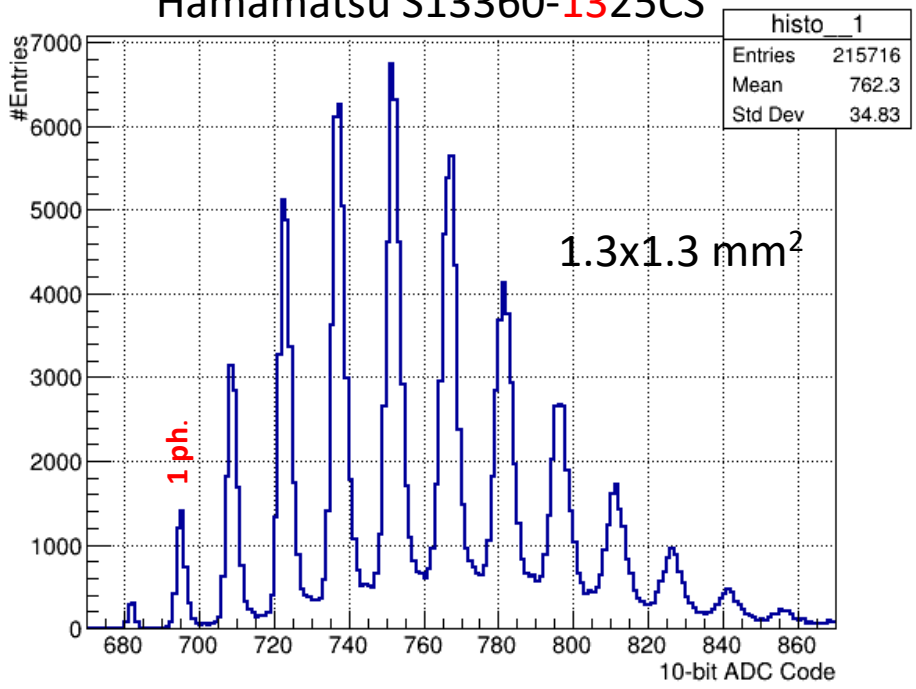
- High dynamic range for large device (e.g. 3x3 mm^2 device)
  - Around 460pC



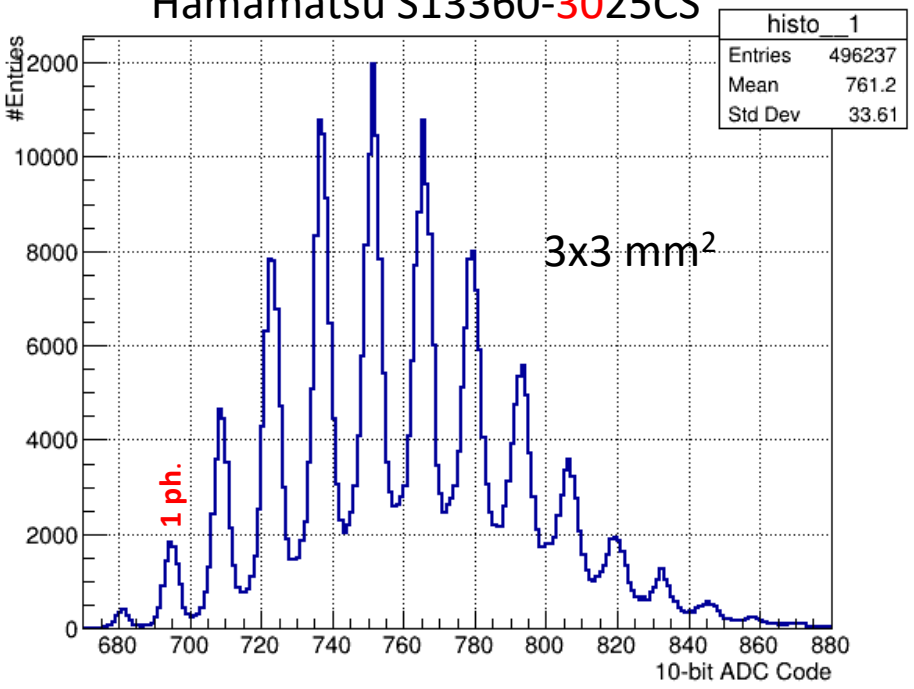
Single photo spectra

- Hamamatsu 25µm pitch devices
  - 25°C, nominal voltage, Gain: 7.0 x 10e5 e./ph.
  - **HG branch,10-bit ADC**, External trigger

Hamamatsu S13360-1325CS

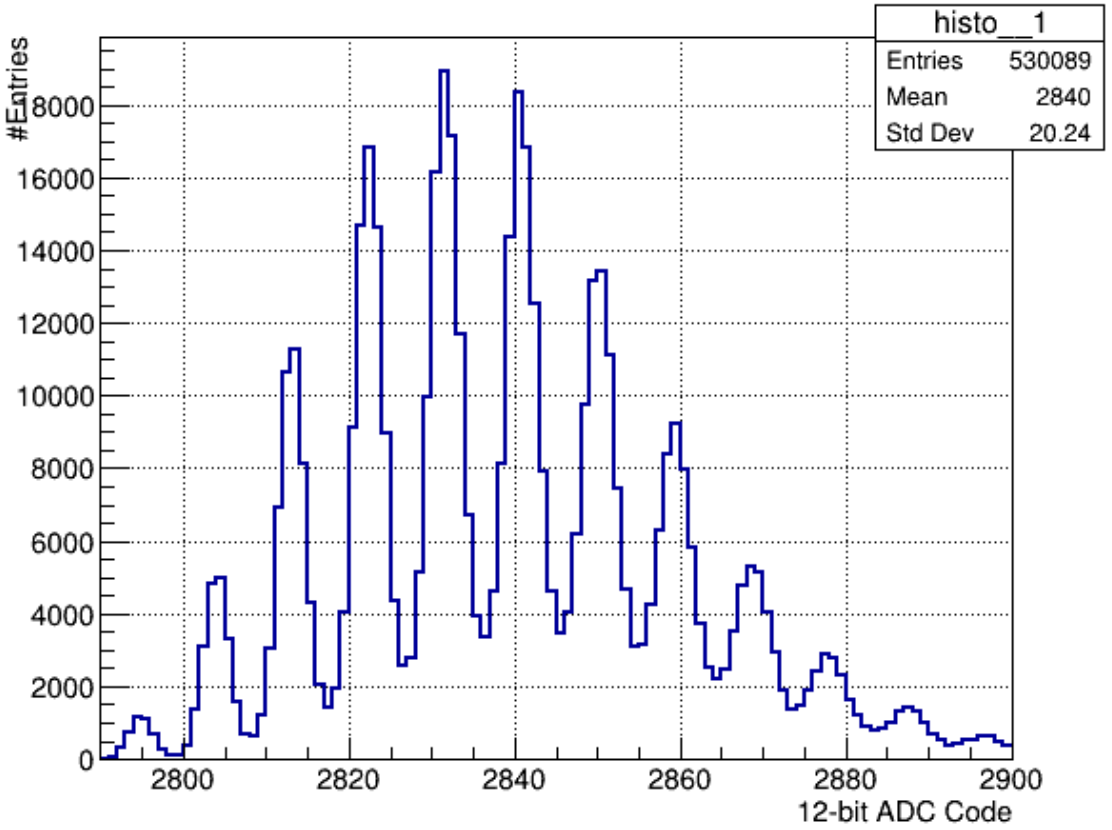


Hamamatsu S13360-3025CS



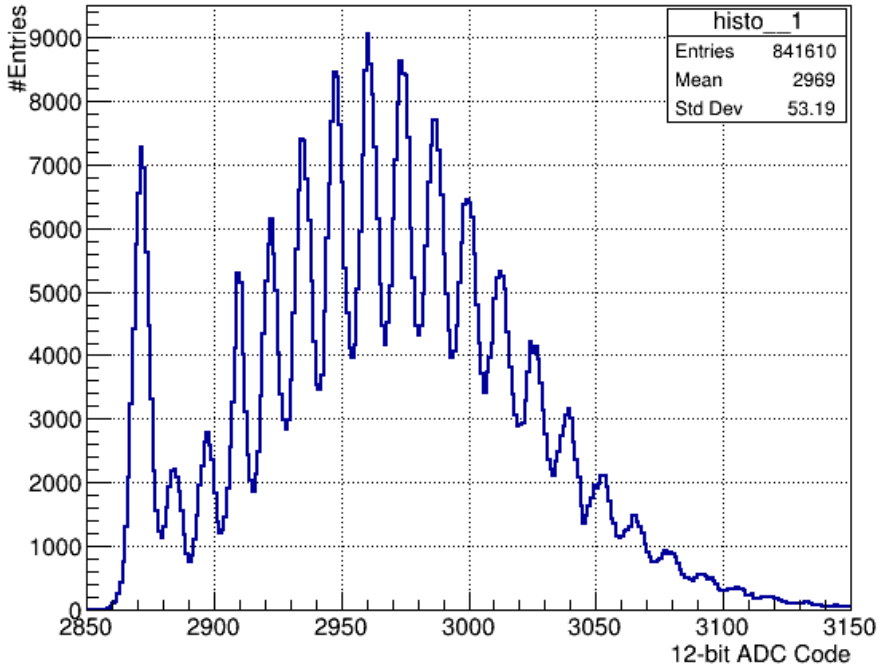
Single photo spectra

- Hamamatsu S13360-1325CS
  - 25°C, nominal voltage, Gain: 7.0 x 10e5 e./ph.
  - **MG branch,12-bit ADC**

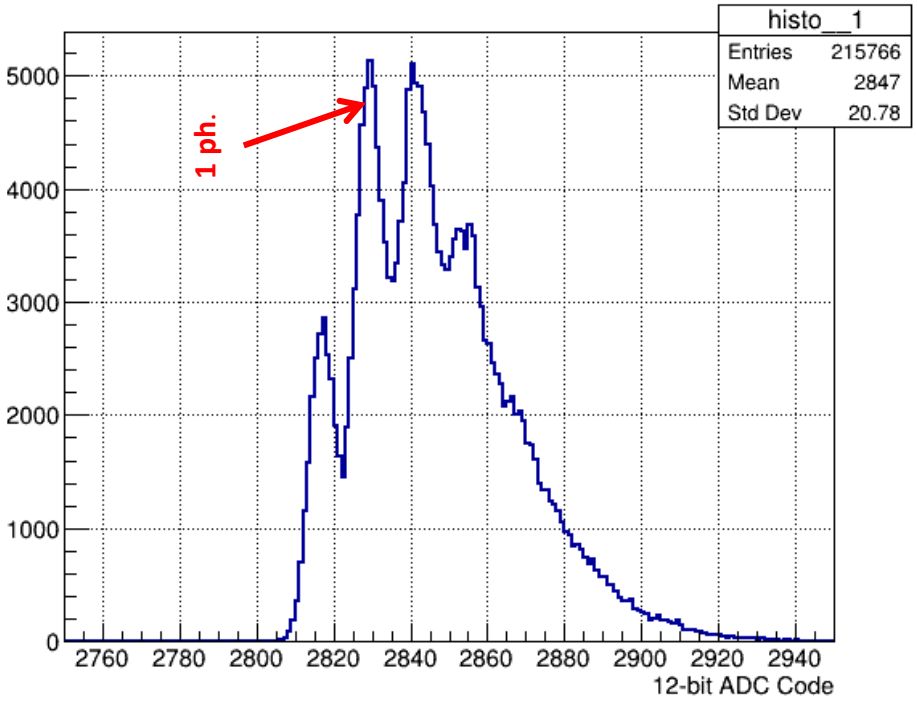


Single photo spectra

- Hamamatsu S12571-010C
  - 25°C, nominal voltage
  - Gain: ~ 1.35 x 10e5
  - HG branch,12-bit ADC
  - Internal trigger



- FBK 7.5um device
  - 10°C, ~ 5V Excess bias
  - Gain: ~ 1.4 x 10e5
  - HG branch, 12-bit ADC
  - External trigger



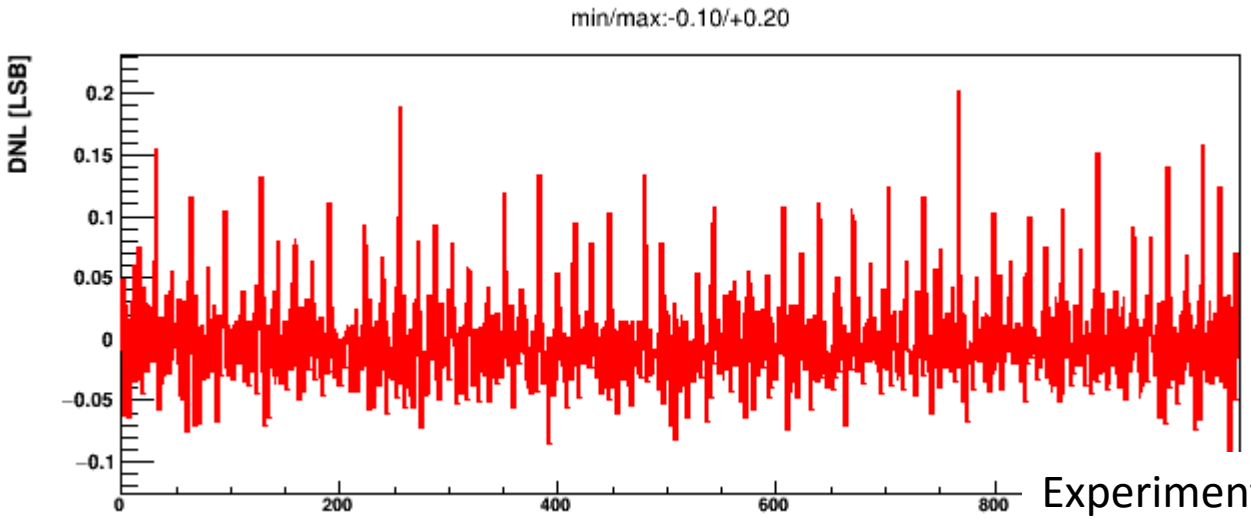
Conclusion and plan

- The 36-channel KLauS5 works excellent
  - No functionality failure, no performance degradation found
  - Bugs fixed

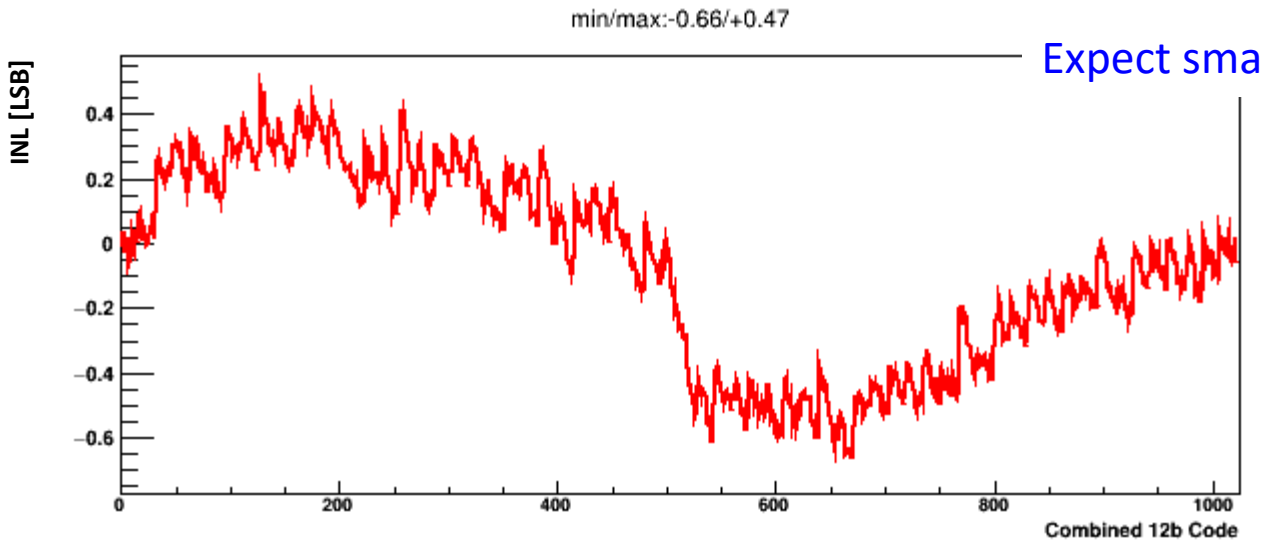
- Future characterization plan:
  - Power consumption
  - Performance under power-pulsing
  - Uniformity among channels/chips

- Packaging for HBUs...

ADC in 10-bit mode – full range linearity



Experimental setup is not optimized.



Expect smaller INL