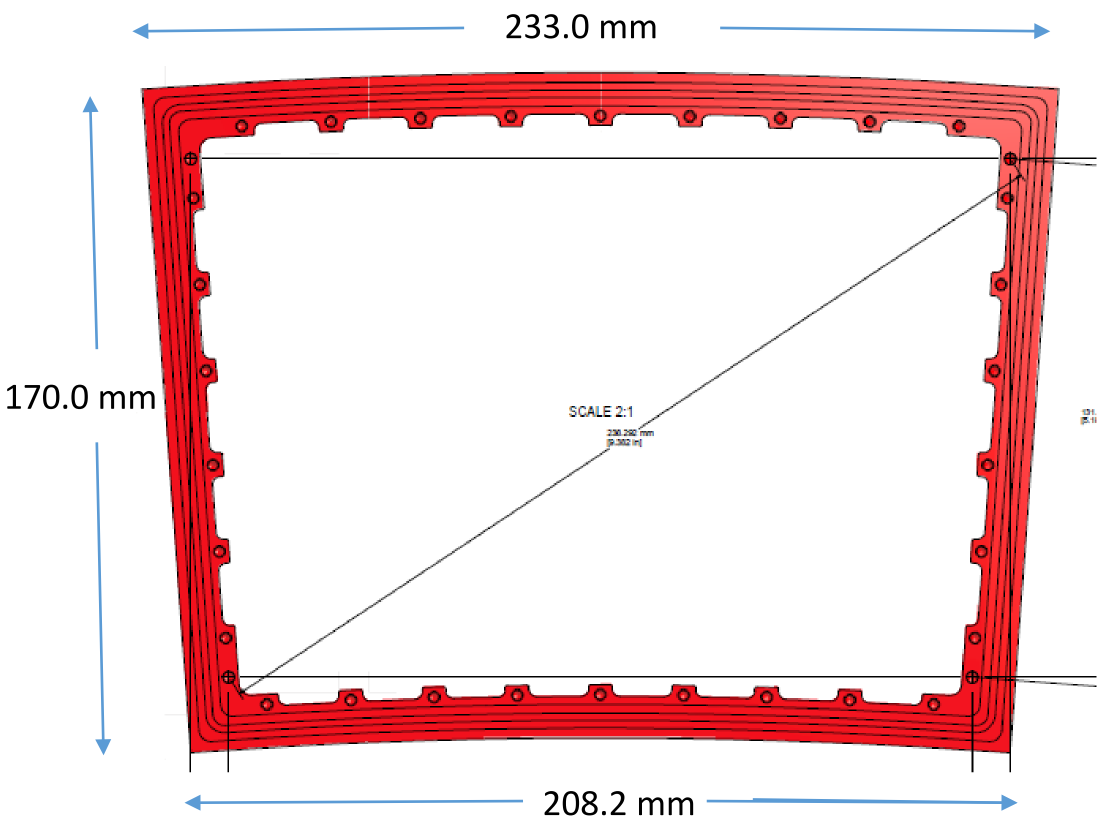
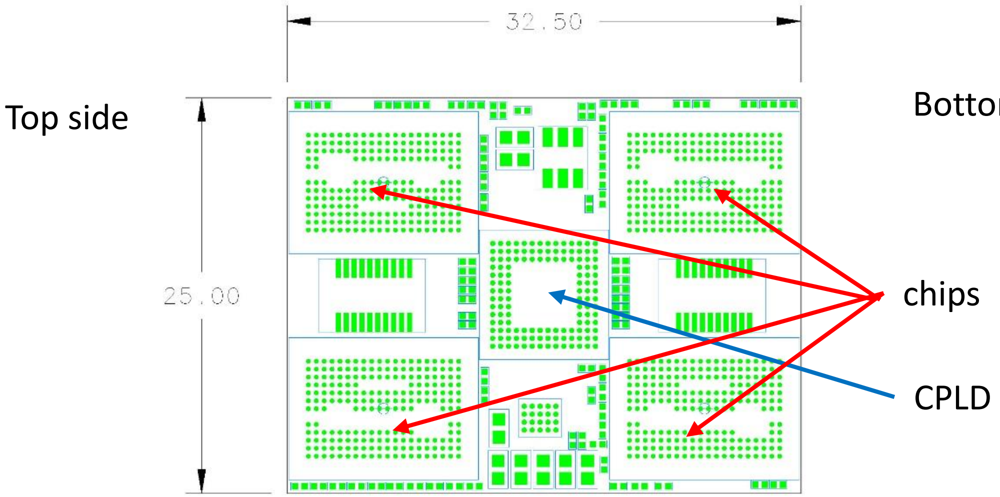
Our system

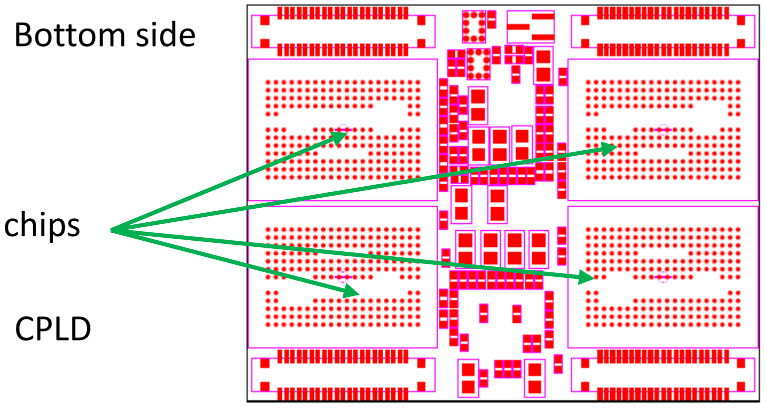
The TPC endcaps are subdivided into wedge shaped readout modules.



Each module contains 5 x 5 Multichip modules (MCM), each of which has a size of 32.5 x 25 mm^2.

Each MCM-board contains 8 carrier boards with SALTRO16 -chips, 4 on the top surface and 4 on the bottom surface. In addition a CPLD is placed on the top side





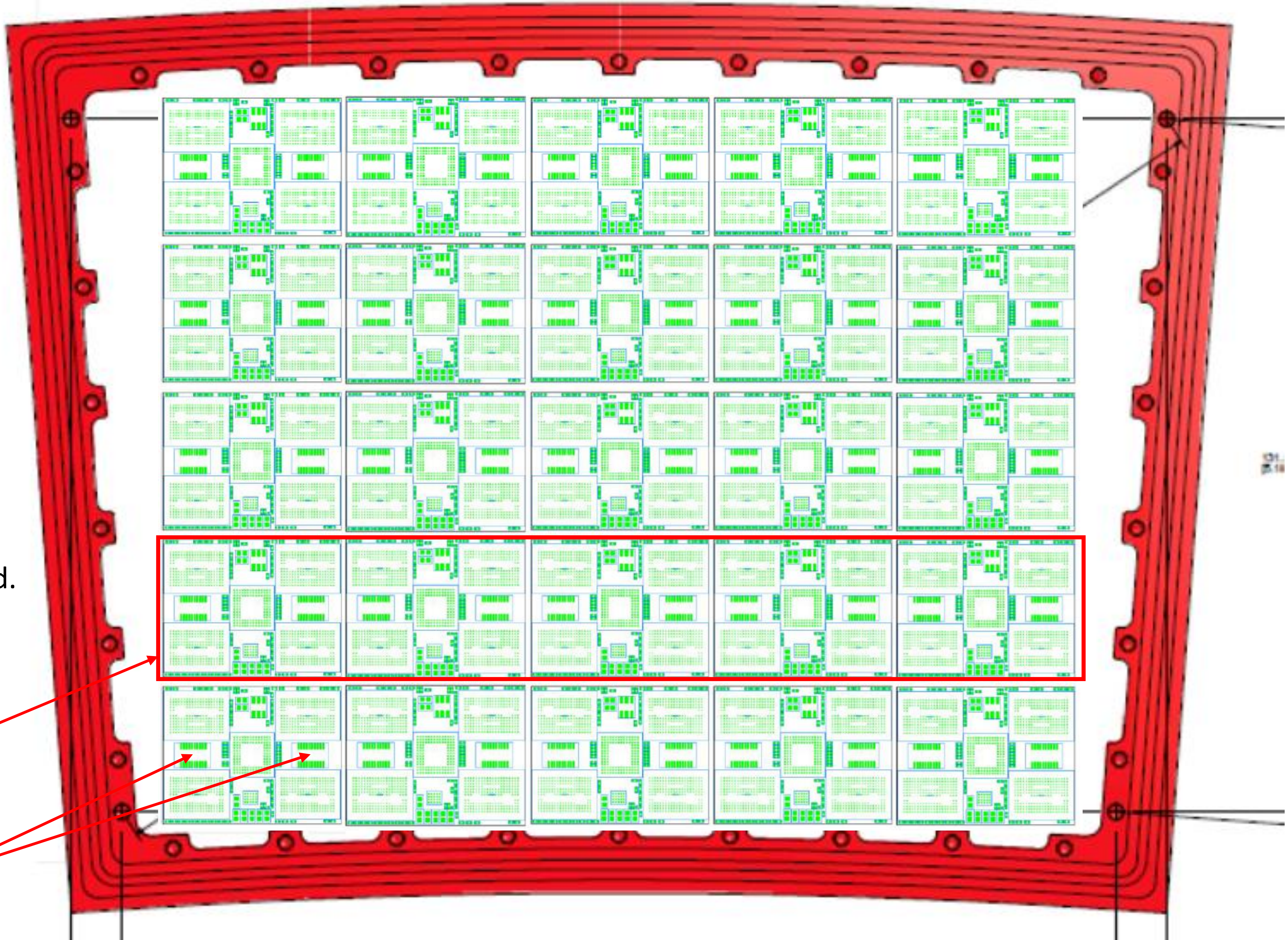
The carrier boards with the SALTRO16-chips

The size of the carrier board is 8.9 x 12 mm^2.
The chip itself is 8.7 x 6.2 mm^2.
The carrier boards are covered with a thin epoxy glob to protect the ASIC and the bondwires.
The flatness of the glob is < 0.2 mm.
The cooling system should have as good thermal contact with the carrier boards as possible. Would it be possible to use an elastic thermal interface.

The MCM-boards are organized in 5 ladders, where each ladder contains 5 MCM boards. The length of a ladder is 166.5 mm and the height is 25 mm.

The total area to be cooled Is 166.5 x 129 mm^2.

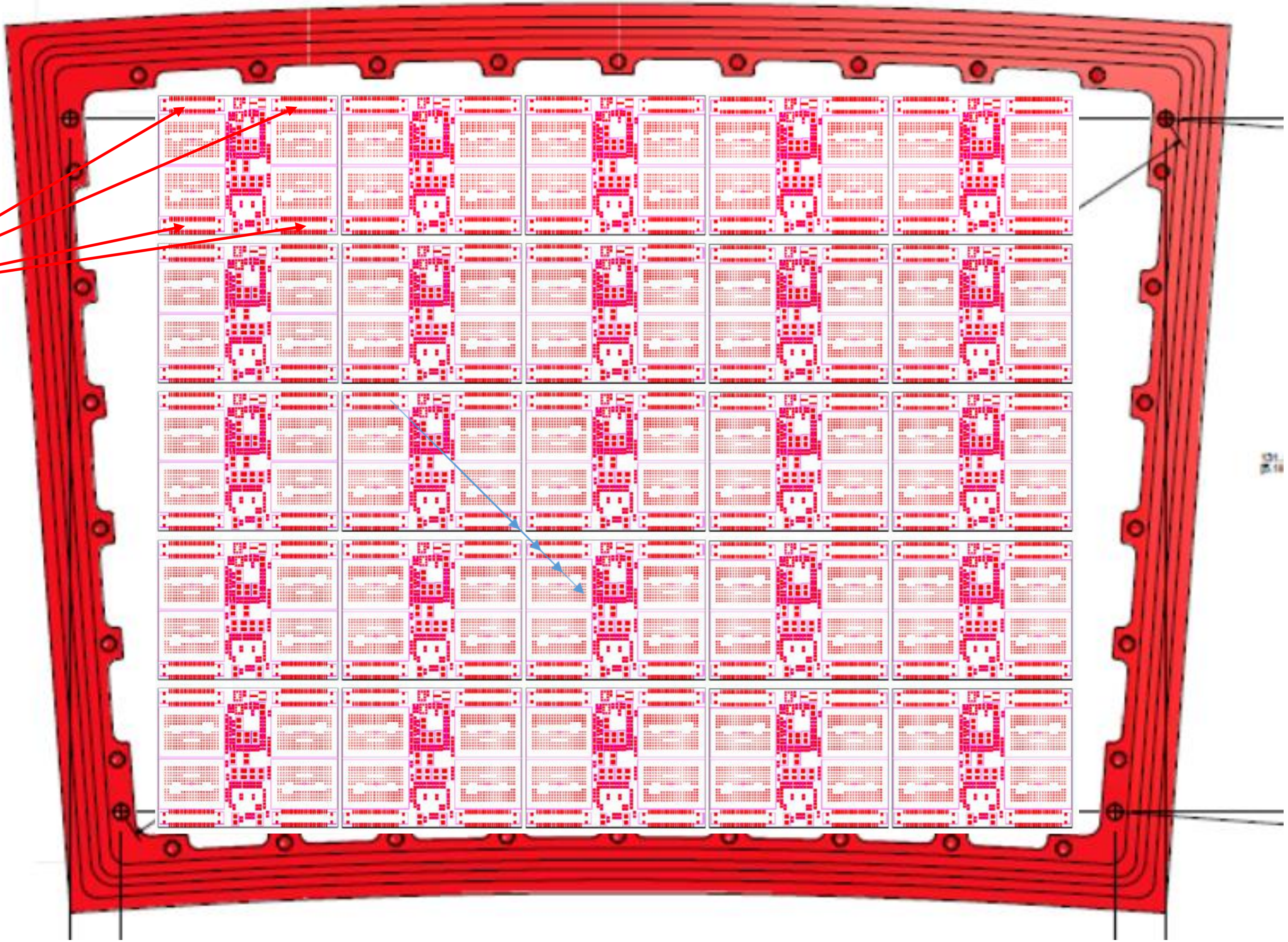
There has to be cut-outs for the connectors in the cooling system. On the top side there are two connectors per MCM-board. The connectors for one MCM-board are indicated in the figure.



Bottom side

Connectors

On the bottom side there are four connector per MCM-board, which connect the MCM-boards to the padplane



Power consumption (continuos operation):

- Per chip: 757 mW

CPLD: 175 mW (can not be power pulsed)

- *Per MCM-board:*

top side: 4 chips x 757 mW + 175 mW (CPLD) = 3203 mW

bottom side : 4 chips x 757 mW = 3028 mW

- *Per ladder:*

Top ladder: 5 x 3203 mW ≈ 16 W

Bottom ladder: 5 x 3018 ≈ 15 W

Power consumption (power pulsing operation)

Test beam: 5 ms beam at 10 Hz

- Per chip = 9.2 + 10 Hz x 5 ms x 0.654 mJ = 42 mW
- *Per MCM-board:*

top side: 4 x 42 mW + 175 mW = 343 mW

bottom side: 4 x 42 mW = 168 mW

- *Per ladder:*

Top side: 5 x 343 mW ≈ 1.7 W

Botton side: 5 x 168 mW ≈ 0.8 W

Requirements on cooling:

- Operating temperature: 25-30° C
- Temperature stability/gradient: <± 1° C
- The temperature stability should mainly be space, such that the temperture gradient along the ladder should be kept within the requirements.
- The variation in time is expected to be slow and we will monitor the gas temperature at various positions to control this variation.

Material budget

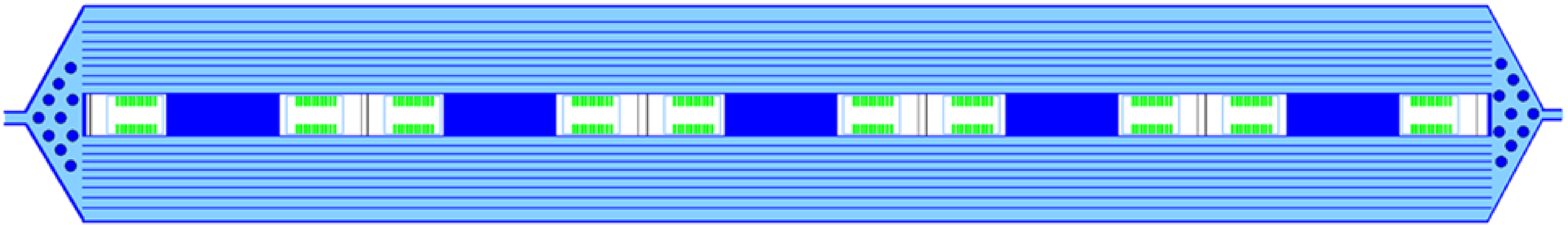
- The target for the material budget of the end cap is that X/X_o should be below 0.25.
- The GEMs and the pad plane are estimated to have $X/X_o \approx 0.08$.
- The electronic boards are estimated to have $X/Xo \approx 0.03$.

$\Rightarrow \Sigma X/Xo \approx 0.11$

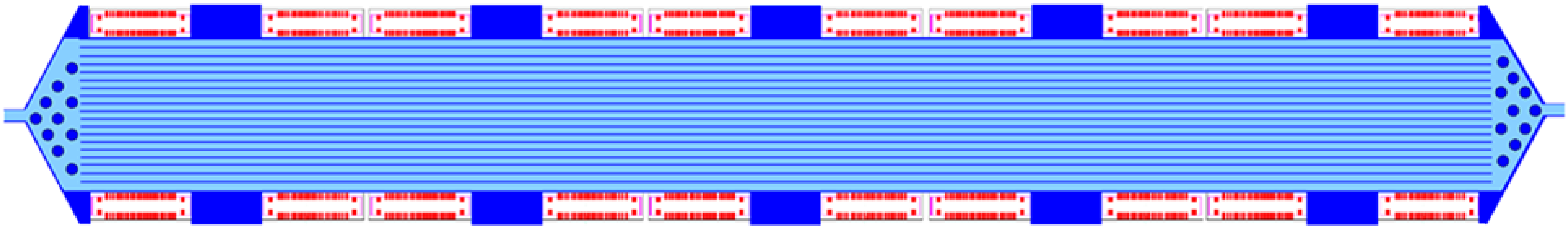
These numbers are however very rough estimates

We propose to start a test with a 'one-ladder' prototype. Such a prototype system is illustrated below.

Top side



Bottom side



What we want to know:

- What is the optimal design of the in- and outlet to get a homogeneous flow (cooling) over the full surface?
- The dimensions and pitch of the cooling grooves in order to keep the temperature gradunt over the full length within the requirements?
- What material is preferred? On the top side the CPLD is not covere by cooling grooves ⇒ needs material with good thermal conductivity?

At an operational temperature of around 25-30°, and the temperature stability probably less than$\pm$ 1°.
According to the diagram this corresponds to an uncertainty of 0.003 cm/μs in the drift velocity, which corresonds to a relative uncerttatinty in the drift velocity of around 0.0004%.
$\Rightarrow$ A spatial uncertainty of 800 μm for 2 m drift length, which exceeds the required accuracy of less than 500 μm over the full drift length.
It has to be tested in a mock-up system how much of the temperature variation in the electronics that is tranfered to the drift gas.