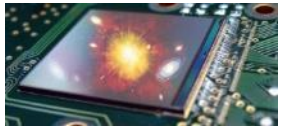
PICSEL



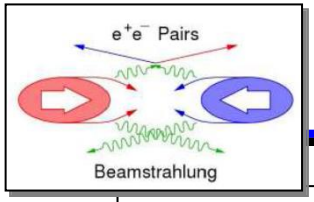
On-going Development of CMOS Pixel Sensors (CPS) and Emerging Fast Timing Perspectives

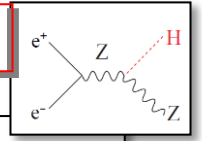
On behalf of IPHC-Strasbourg PICSEL group

- CPS on going developments
  - ⇨ MIMOSIS for CBM-MVD experiment
  - ⇨ Road to ILD-VXD
  - ⇨ ILC: Power consumption and data flux
- Long term & fast timing perspectives

Reminder: ILC VXD requirements

$$\sigma_b < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m.$$



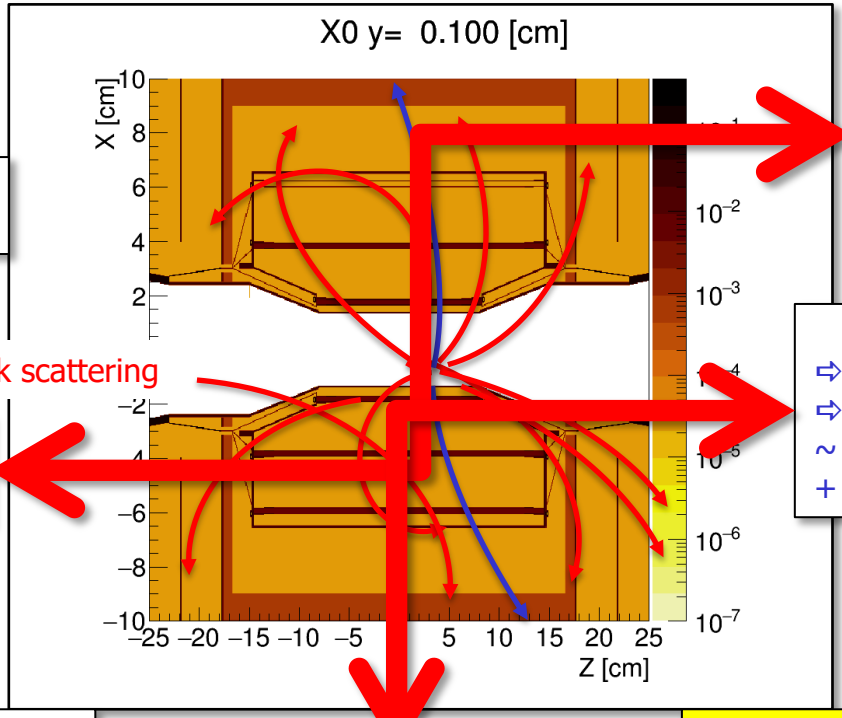


Physics
- ⇨ Flavour tagging
- ⇨ Low pT tracks

Beam background

Physics (<Hz/cm²)

Beam background (~ 5 hits/BX/cm² on layer 0)



Vertex reconstruction
- ⇨ granularity
- ⇨ Pitch ~17 um
- ⇨ (σ_{sp} ~3 um)

Radiation hardness
O(100kRad/an) & O(10^{11})neq/an

Rad.Tol. devices

Back scattering

Material Budget
- ⇨ ~ 0.15% X_0 / layer
- ⇨ < 1% X_0 for the whole VTX
- ~ 900 μm Si
- + ~0.14% X_0 for the beam pipe

Read-out speed
O(1-10 μs)

Power consumption
~< 50mW/cm²

Fast read-out & low Power architectures

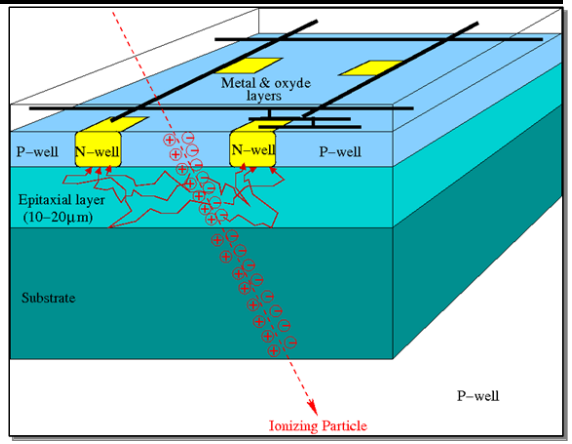
Cooling
Stiffness / Alignment

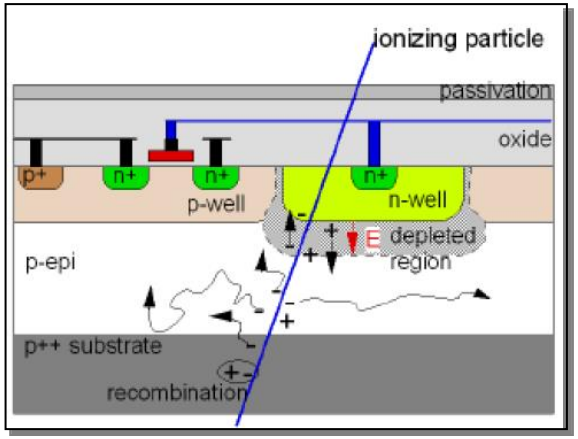
Low material detectors & supports structures

Challenge : meet the requirements all together

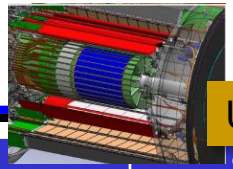
CMOS pixel sensor (CPS) for charged particle detection

- Main features
  - Monolithic, p-type Si
    - Signal created in low doped thin epitaxial layer ~10-30 μm
  - Thermal diffusion of e-
    - Limited depleted region
  - Charge collection: N-Well diodes
    - Charge sharing ⇨ resolution
  - Continuous charge collection
    - No dead time
- Main advantages
  - Granularity
    - Pixel pitch down to 10 x 10 μm^2 ⇨spatial resolution down to ~ 1 μm)
  - Material budget
    - ⇨ whole sensor routinely thinned down to 50 μm
  - Signal processing integrated in the sensor
  - Flexible running conditions
    - From ≤ 0°C up to 30-40°C if necessary
    - Low power dissipation (~ 100 mW/cm^2) ⇨ material budget
    - Radiation tolerance: > MRad and O(10^{13} n_{eq}) ⇨f(T,pitch)
  - Industrial mass production
    - Advantages on costs, yields, fast evolution of the technology,
    - Possible frequent submissions
- Main limitations
  - Industry adresses applications far from HEP experiments concerns
    - Different optimisations on the parameters on the technologies
  - Recently: new accessible processes:
    - Smaller feature size, adapted epitaxial layer
    - Open the door for new applications

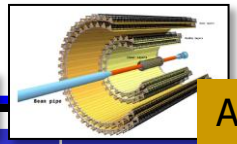




Evolving CPS



ULTIMATE



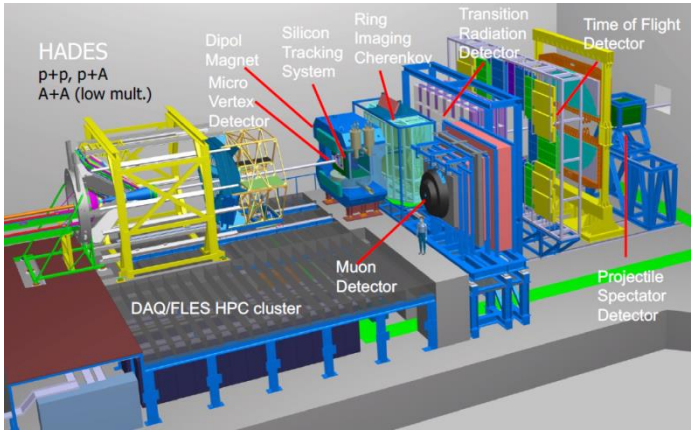
ALPIDE

MIMOSIS

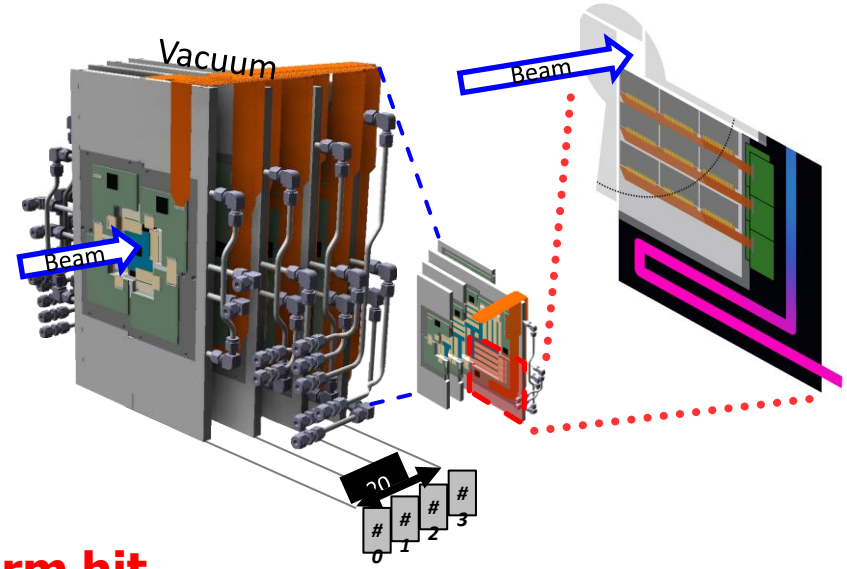
PSIRA proposal

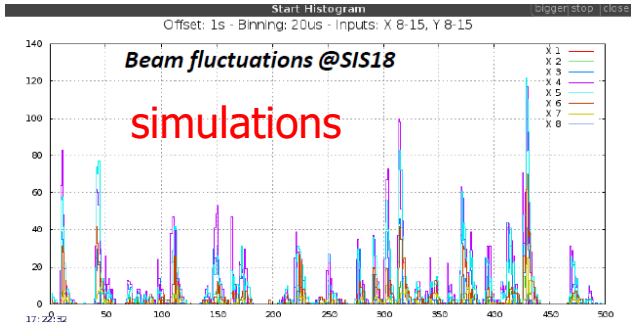
	STAR-PXL	ALICE-ITS	CBM-MVD	ILD-VXD
Data taking	2014-2016	>2021-2022	>2021	>2030
Technology	AMS-opto 0.35 μm	**0.18 μm**	0.18 μm	0.18 μm (conservative) < 0.18 μm ?
	4M	HR, V_{bias} ~-6V Deep P-well	HR, Deep P-well	?
Architecture	Rolling shutter + sparsification + binary output	**Asynchronous r.o.** **In pixel discri.**	Asynchronous r.o. In pixel discri.	Asynchronous r.o. (conservative)
Pitch (μm^2) / Sp. Res.	20.7 x 20.7 / 3.7	27 x 29 / 5	22 x 33 / <5	~ 22 / ~ 4
Time resolution (μs)	~185	**5-10**	5	**1 – 4**
Data Flow		~10^6 part/cm²/s Peak data rate ~ 0.9 Gbits/s	peak hit rate @ 7 x 10^5 /mm²/s **>2 Gbits/s output** **(20 inside chip)**	~375 Gbits/s (instantaneous) ~1166Mbits / s (average)
Radiation	O(50 kRad)/year	2x10^{12} n_{eq}/cm² 300 kRad	3x10^{13} n_{eq}/cm²/yr & 3 MRad/yr	O(100 kRad)/year & O(1x10^{11} n_{eq}(1MeV)) /yr
Power (mW/cm²)	< 150 mW/cm²	**< 35 mW/cm²**	< 200 mW/cm²	~ 50-100 mW/cm²
Surface	2 layers, 400 sensors, 360x10^6 pixels 0.15 m²	7 layers, 25x10^3 sensors **> 10 m²**	4 stations Fixed target	3 double layers 10^3 sensors (4cm²) 10^9 pixels ~0.33 m²
Mat. Budget	~ 0.39 % X_0 (1st layer)	~ 0.3% X_0 / layer		~ 0.15-0.2 % X_0 / layer
Remarks	1st CPS in colliding exp.	(with CERN)	Vacuum operation Elastic buffer	Evolving requirements

CBM-MVD



Joachim Stroth | 56th Winter Meeting on Nuclear Physics | Bormio (Italy)

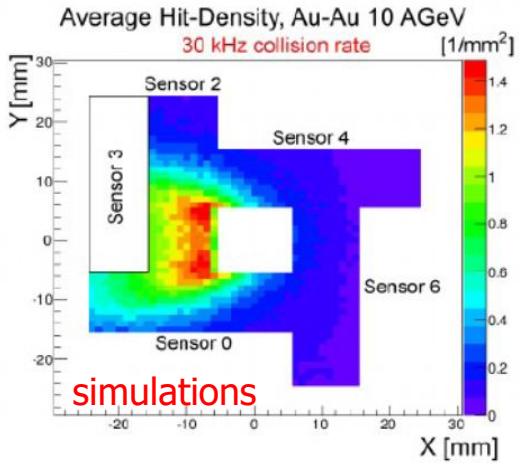


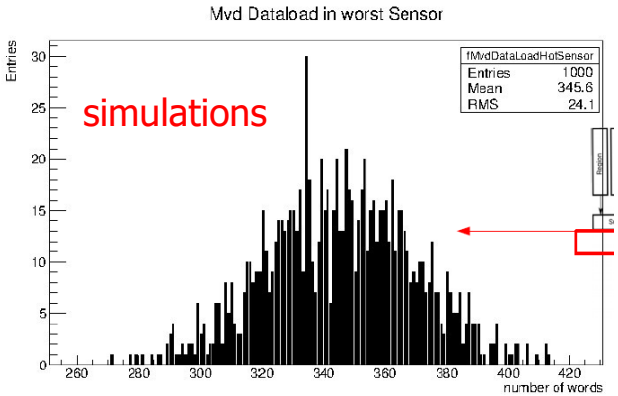


Michal Koziel| deutsche physikalische gesellschaft 2017| Münster (Germany)

Au/Au 10 AGeV 100kHz

Non uniform hit density in time and space



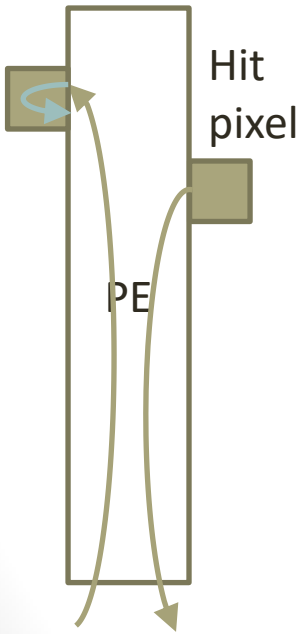


Data load distribution in most occupied sensor

(number of 16 bits words during 5 μs)

MIMOSIS architecture

Matrix dimension: 1024 (col.) x 504 (row)
Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
2 kind of pixels: AC and DC coupled
Priority encoder
Integration time: 5 µs



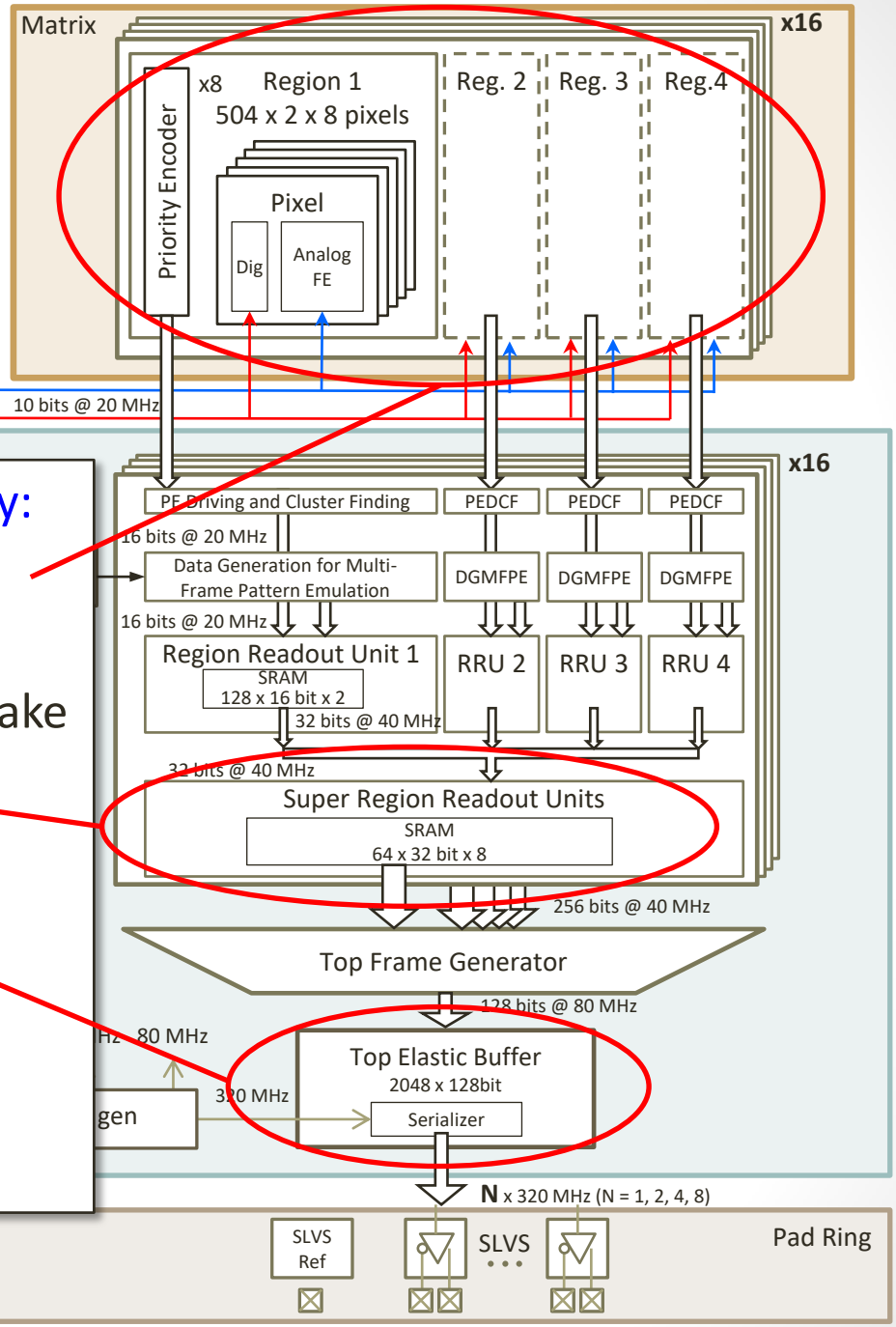
Matrix x16
x8 Region 1
504 x 2 x 8 pixels
Priority Encoder
Pixel
Dig
Analog FE
Reg. 2
Reg. 3
Reg.4

DACs
10 bits @ 20 MHz

Digital Periphery x16
PE Driving and Cluster Finding
PEDCF
16 bits @ 20 MHz
Multi-Frame Pattern Emulation
Data Generation for Multi-Frame Pattern Emulation
DGMFPE
16 bits @ 20 MHz
Region Readout Unit 1
SRAM 128 x 16 bit x 2
RRU 2
RRU 3
RRU 4
32 bits @ 40 MHz
Super Region Readout Units
SRAM 64 x 32 bit x 8
256 bits @ 40 MHz
Top Frame Generator
128 bits @ 80 MHz
Pixel Config Management
Registers
I2C
CMU Control Management Unit
Sequencer
20 MHz 40 MHz 80 MHz
CLK: 40 MHz
PLL
320 MHz
Clock gen
Top Elastic Buffer
2048 x 128bit
Serializer
N x 320 MHz (N = 1, 2, 4, 8)
Pad Ring
SLVS Ref
SLVS

MIMOSIS architecture

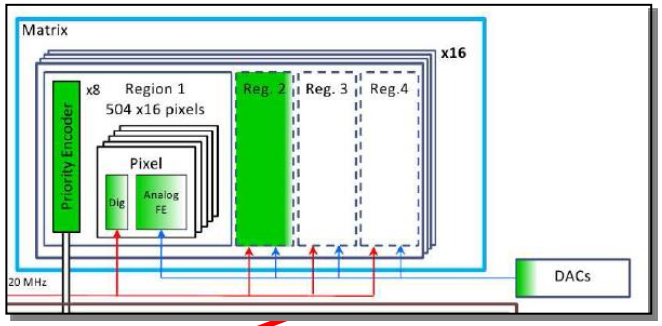
Matrix dimension: 1024 (col.) x 504 (row)
Pixel dimension: 26.88 µm (height) x 30.24 µm (width)
2 kind of pixels: AC and DC coupled
Integration time: 5 µs

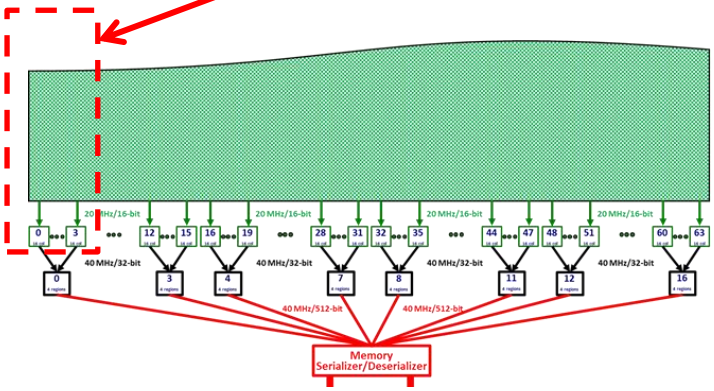


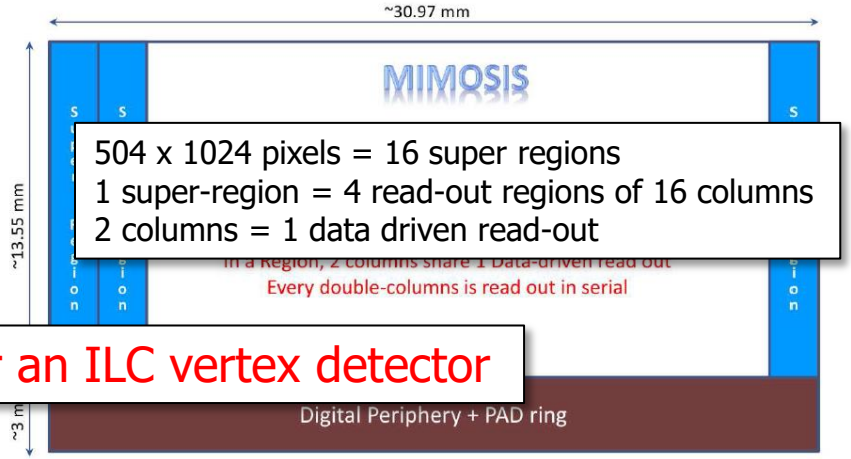
- To sustain high local hit density:
  - Pixel matrix divided into 64 regions
  - 4 regions are grouped to make a super region
- To absorb data fluctuation:
  - 1 Elastic buffer can store 9 maximal frames
  - Write speed = 4 x read speed
  - Use quiet moment to read remaining data

MIMOSIS roadmap

- 4 prototypes:
- MIMOSIS-0: = 2 regions
  - Back from foundry
  - Test in progress (2018)
  - Test pixel Radiation hardness and priority encoder frequency
    - Radiation hardness design (SEU)
    - Testability
- MIMOSIS-1: 1st prototype of complete sensor
  - (end 2018)
- MIMOSIS-2:
  - (end 2019)
- MIMOSIS-3: final pre-production sensor
  - (~2020)



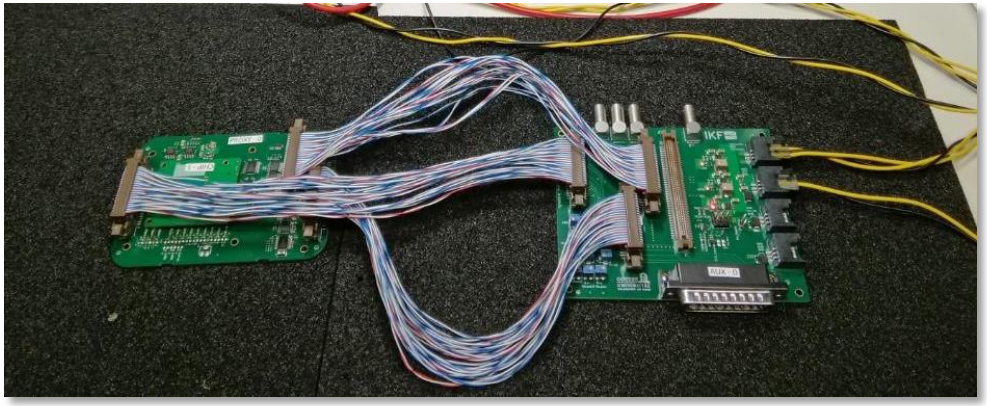




504 x 1024 pixels = 16 super regions
1 super-region = 4 read-out regions of 16 columns
2 columns = 1 data driven read-out

⇨ architecture adaptable to a fast sensor for an ILC vertex detector

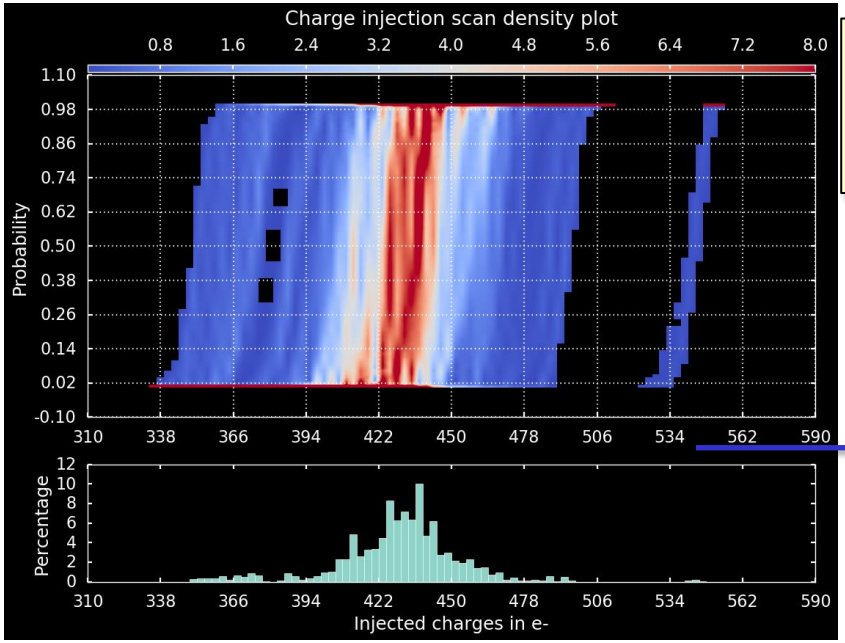
MIMOSIS-0: test setup



- Test setup developed by IKF (Frankfurt) with support of IPHC
  - PXI acquisition setup
  - Started in spring 2018
- Goals
  - Architecture validation
  - JTAG software validation
  - Measure pixel to pixel dispersion through charge injection at the pixel diode level

MIMOSIS-0 tests : Very Preliminary results

- Threshold scans with charge injection at the pixel diode level

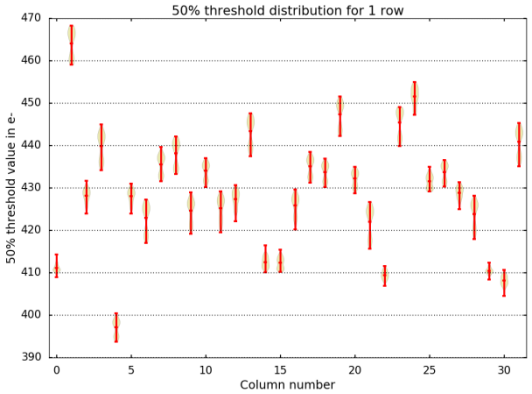


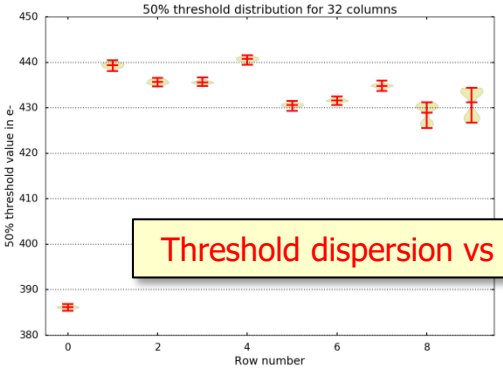
e^-

Pixel to pixel dispersion
~< O(15-20 e-)
(Very preliminary, not optimized yet)

Block	Test
JTAG registers	Write/read on all
DACs	Transfer function / Linearity
Sequencer	Working up to 70 MHz (nominal 20 MHz)
Priority encoder	Working at 20 MHz ➔ higher frequency planned
Pixel Masking and pulsing	OK
Charge injection scan on pixels	In progress
Analogue pixels test	Circuit edit (pad issue) in progress
Irradiation ionizing and non-ionizing	Planned soon

Threshold dispersion vs column ~<O(10 e-)



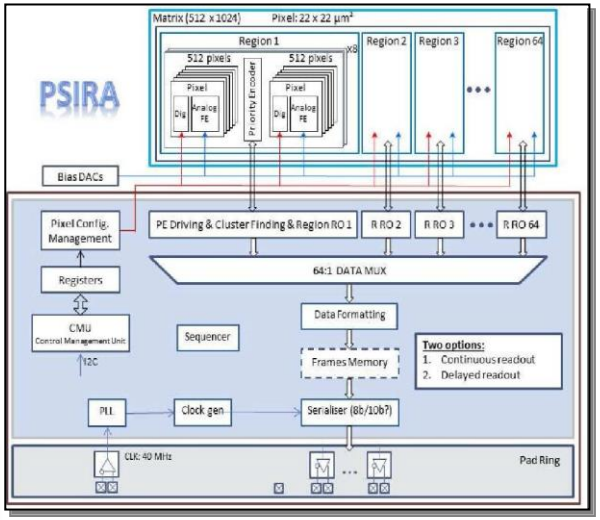


Threshold dispersion vs row~<O(5 e-)

Extension of MIMOSIS to ILC vertexing and tracking

- Conservative approach
  - Minimize changes w.r.t. MIMOSIS
    - Keep TJ 0.18 μm technology & a similar architecture
  - 2 sub-systems targeted
    - Vertex detector & Silicon inner trackers (SIT @ ILD)
  - Performances targeted
    - 22x22 μm^2 ~ 20% better spatial resolution (vertexing)
    - Read-out time: 2-4 μs (ILD-VXD) and 1 μs (ILD-SIT)
    - Faster = higher Power consumption

⇨ PSIRA



⇨ Finalize CPS ~2025

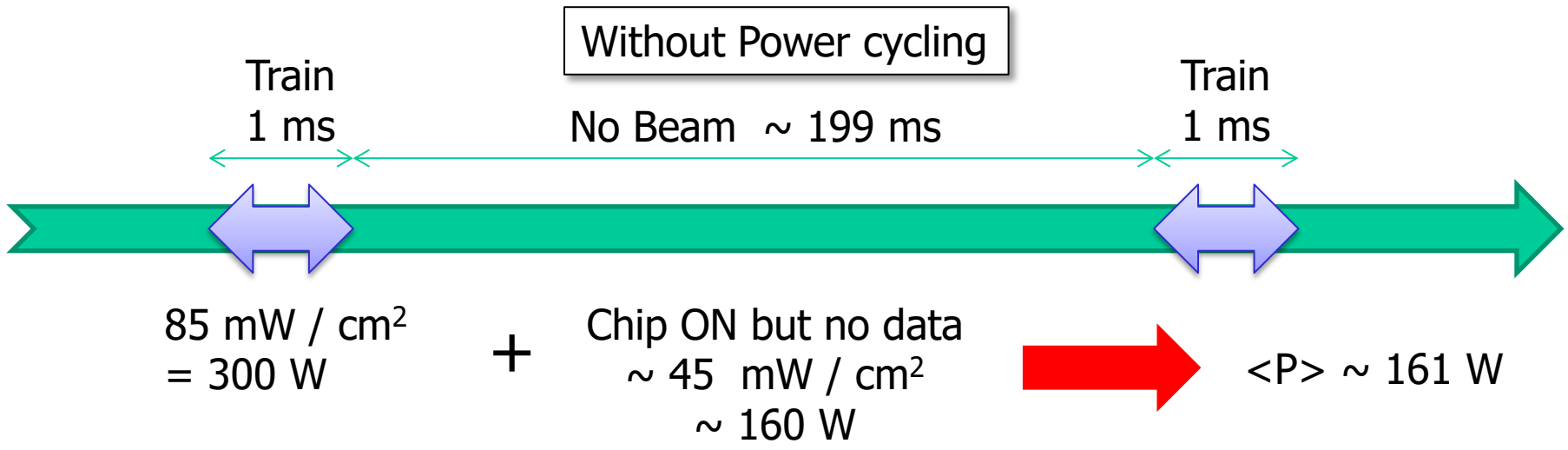
- Expected Performances
  - σ_{sp} ~4 μm ⇨Use double sided ⇨ σ_{sp} ~2.8 μm
  - Signal peaking time ~ 2 μs
  - Single pixel adress read-out = 50 ns
    - (with 20 MHz clock)
  - Sustainable occupancy (~5 pixels/hits)
    - ~ 4 hits/region/μs ~ 100 hits/cm^2/μs
  - Power (instantaneous)

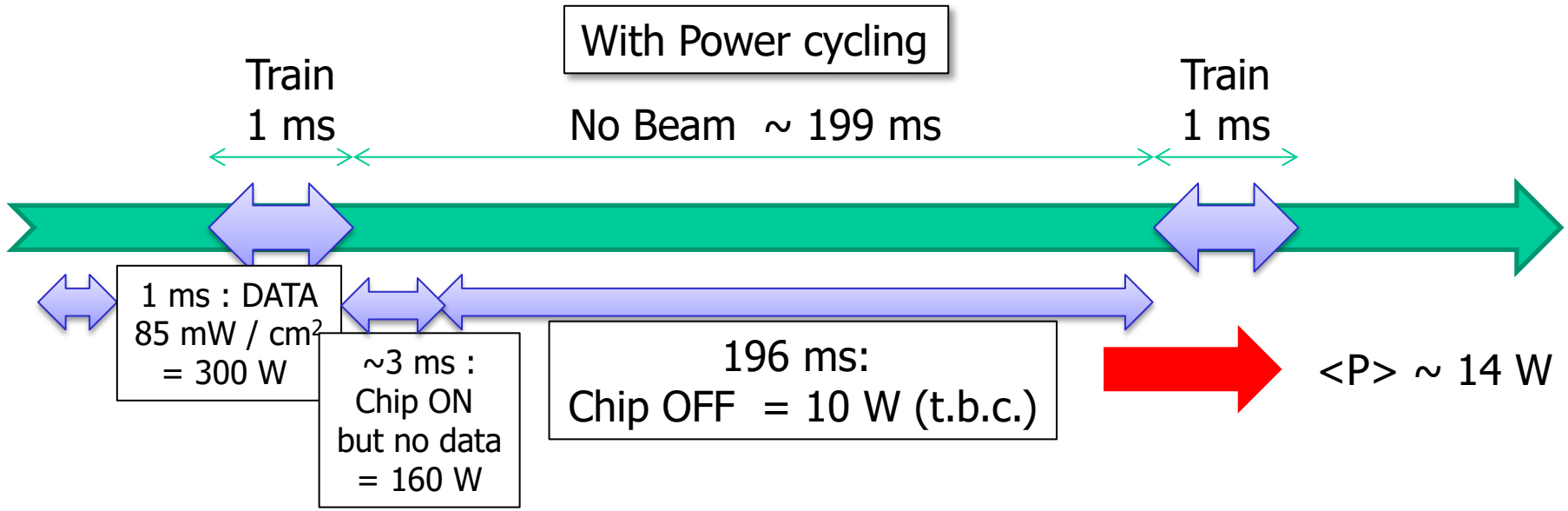
	Baseline	High occupancy	High read out speed	combined
Occupancy	DBD	DBD x 2	DBD	DBD x 2
Read out time	4 μs	4 μs	2 μs	2 μs
Power (mW/cm^2)	85	125	110	150

- Elementary read-out region:
  - 8 pairs of columns (512 rows)
  - Pitch 22 x 22 μm^2 ⇨ region ~ 4 mm^2
- Can one reach : Pitch ~ 18 x 18 μm (σ_{sp} ~ 3 μm) & r.o.time ~ 2-4 μs ?
  - Doable with smaller feature sizes

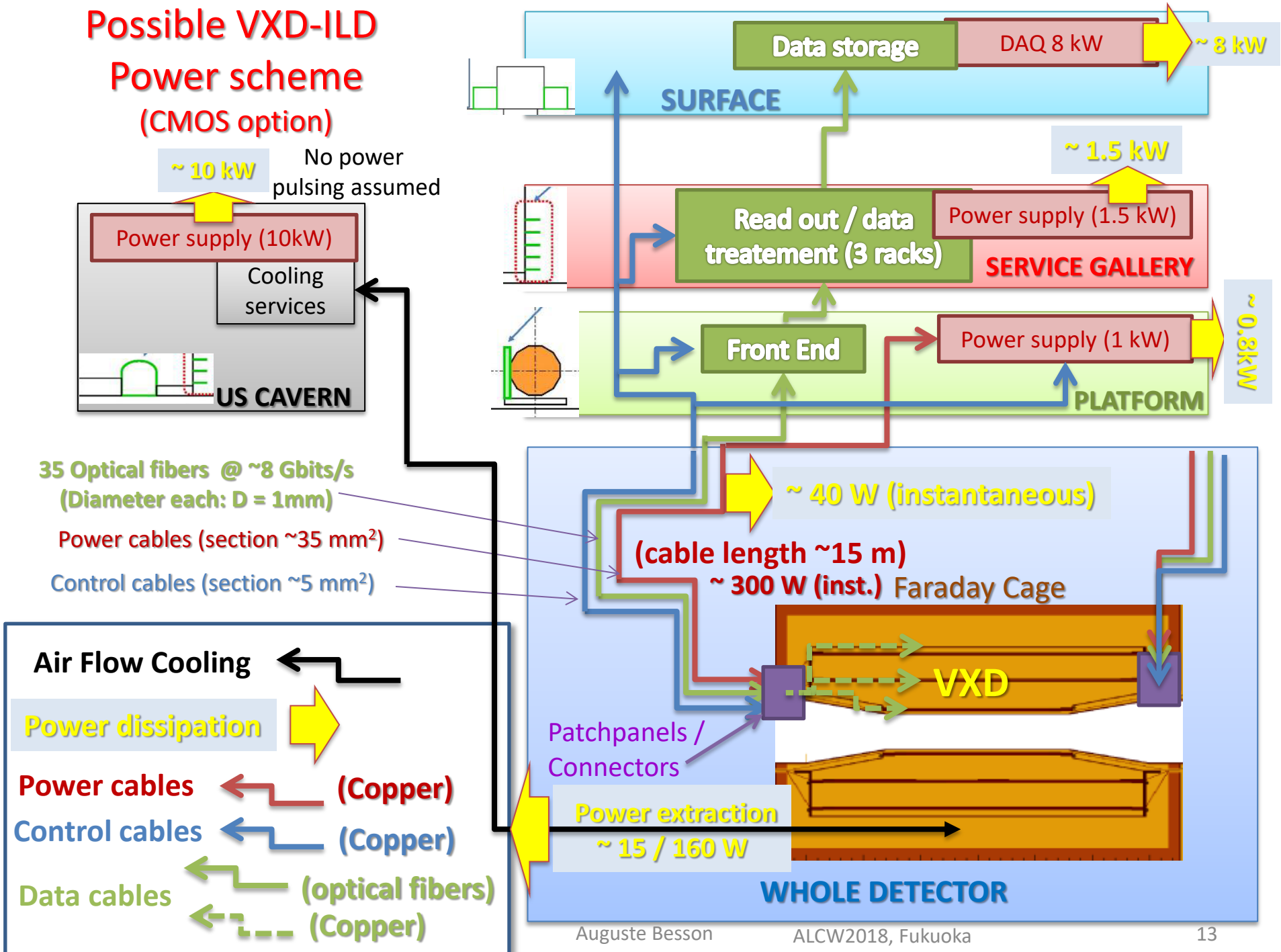
⇨ PSIRA architecture already reaching 4-8 BX read-out time
⇨ Power vs read-out speed compromise
⇨ Avoiding power pulsing possible ?

Power scheme





Possible VXD-ILD Power scheme (CMOS option)



VXD-ILD: Data flux

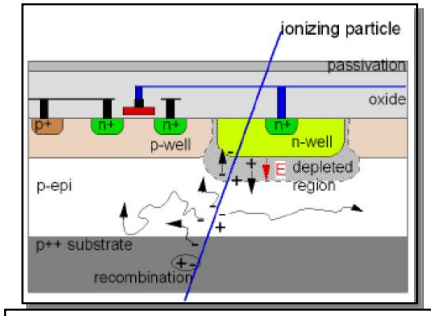
Layer	DBD occupancy (hits/cm²/BX)	Detector surface (mm²)	#hits/BX	#hits/read out	#hits/train	# hits/s	Data rate (Mbits/train)	Data rate (Mbits/s)	Data rate (Mbits/train) With safety factor of 3	Data rate (Mbits/s) With safety factor of 3
	@ √s = 500 GeV	Length x width x # ladders		assuming 4 µs i.e. 8 BX	Assuming 1312 bunches per train	Assuming 5 trains / s	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit	Assuming 16 bits/pixel & 5 pixels/hit & 10 bits header = 100 bits/hit
0	6.32 ± 1.76	125 x 11 x 10 = 13 750	870	7000	1140 K	5700 K	114	570	342	1710
1	4.00 ± 1.18	125 x 11 x 10 = 13 750	550	4400	720 K	3600 K	72	360	216	1080
2	0.25 ± 0.11	125 x 2 x 2.2 x 11 =60 500	150	1200	197 K	985 K	19.7	98.5	59.1	295.5
3	0.21 ± 0.09	125 x 2 x 2.2 x 11 =60 500	130	1040	171 K	855 K	17.1	85.5	51.3	256.5
4	0.04 ± 0.03	125 x 2 x 2.2 x 17 =99 000	40	320	52 K	260 K	5.2	26	15.6	78
5	0.04 ± 0.03	125 x 2 x 2.2 x 17 =99 000	40	320	52 K	260 K	5.2	26	15.6	78
TOTAL		346 100 mm² ~ 0.35 m²	1780	14280	2332 K	11660 K	233.2	1166	700	3500

- average raw data size (without or with safety factor on beam background included)
  - Average size per BX : ~0.18 Mbits / BX ⇨ 0.54 Mbits / BX (with safety factor of 3) ~375 Gbits/s (instantaneous)
  - Average size per event (~8 BX) : ~1.4 Mbits/ readout ⇨ 4.3 Mbits / readout (with safety factor of 3)
  - Average size per train : ~233 Mbits / train ⇨ 700 Mbits / train (with safety factor of 3)
  - Average size per second : ~1166Mbits / s ⇨ 3500 Mbits / s (with safety factor of 3)

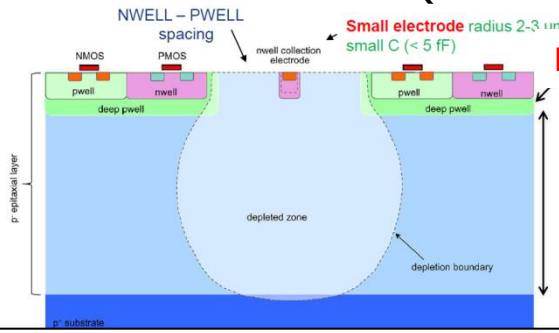
Long term & fast timing perspectives

Long term: CMOS is an evolving technology

Classical CMOS



State of the art (ALPIDE & MIMOSIS)

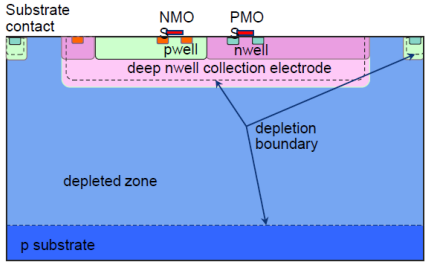


Deep P-well (PMOS)

Reverse bias (6V) increases depletion

High resistivity > 1kΩ.cm

HV-CMOS



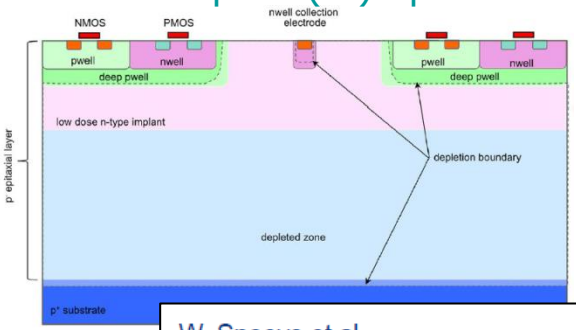
~100 V
High capa
High Power, large pixels
Full depletion
Radiation hardness
⇨ Not suited for ILC

Monolithic Pixel Developments - T. Kugathasan - ACES 2018 - CERN - 25/04/2018

- Explore smaller feature sizes 180 nm ⇨110 nm or even 65 nm.
  - Motivations
    - Smaller pixel dimensions & faster read-out
    - Reduced power consumption

⇨ Smaller feature size offers opportunities to get closer to ILC bunch tagging

- Emerging fast timing perspectives
  - New option (TJ) : planar n-implant



W. Snoeys et al.
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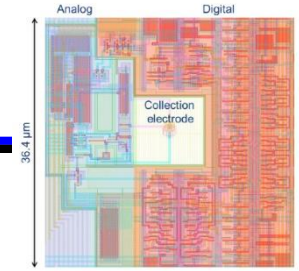
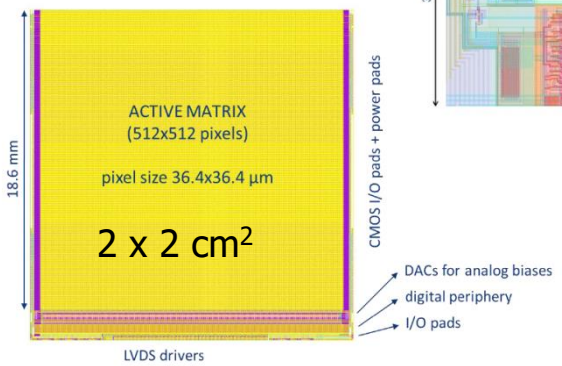
⇨ Explored by U.Bonn & CERN: MALTA (for ATLAS)

- Full depletion
- Low capacitance ⇨ low power

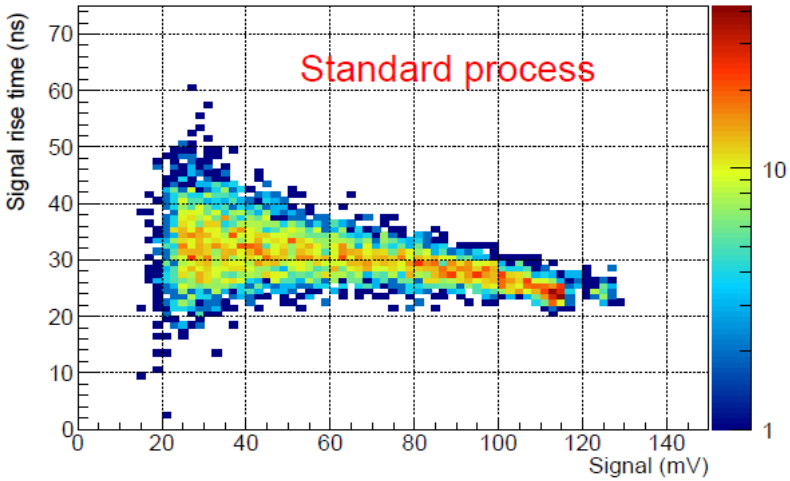
MALTA for ATLAS (CERN)

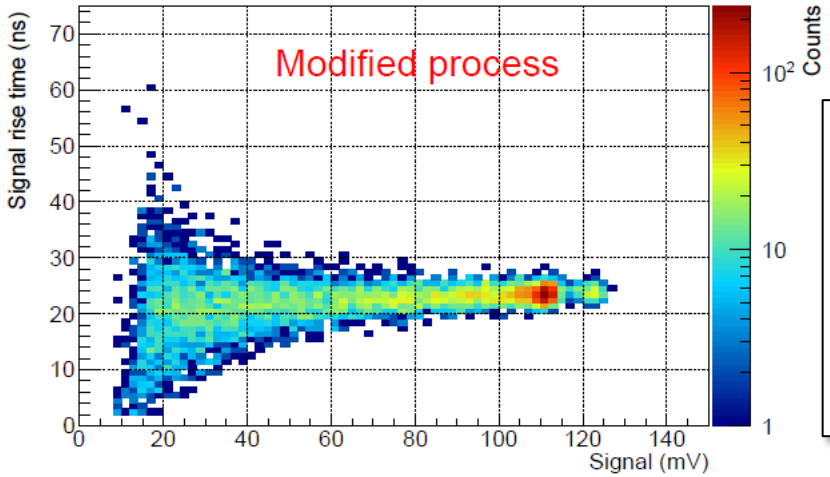


- MALTA Large scale demonstrator
  - Chip for ATLAS outer pixel layers
  - New architecture (novel asynchronous r.o.)
  - Timing ~25 ns
  - High hit rate capabilities (w.r.t. ALPIDE)
  - while preserving a moderate power consumption
    - Analog power dominates ~< 75 mW/cm^2 (with a pitch 36.4x36.4 μm^2)
    - ⇨ going to 22x22 μm^2 ⇨ factor ~3 in pixel density
    - Characterization in progress
    - Promising results



- ^{55}Fe tests:



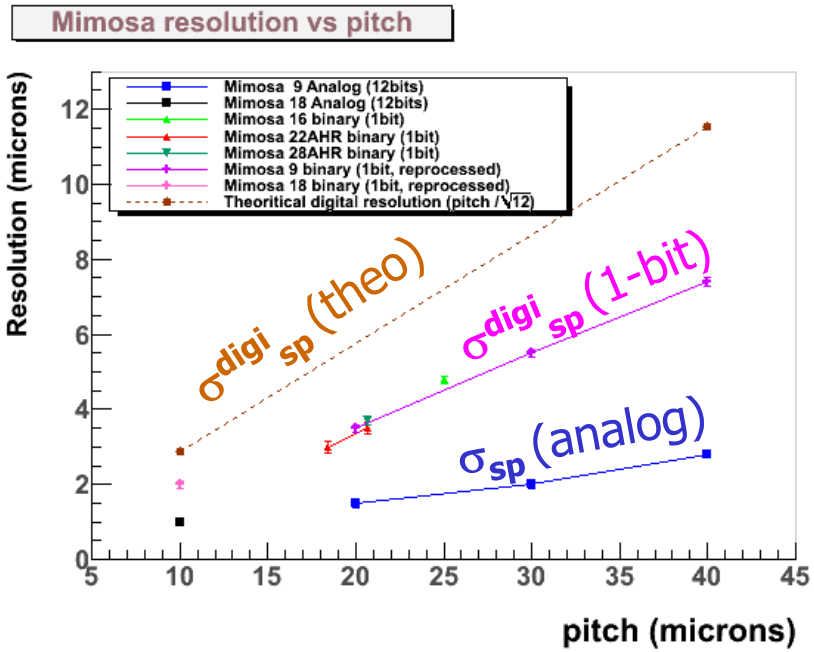


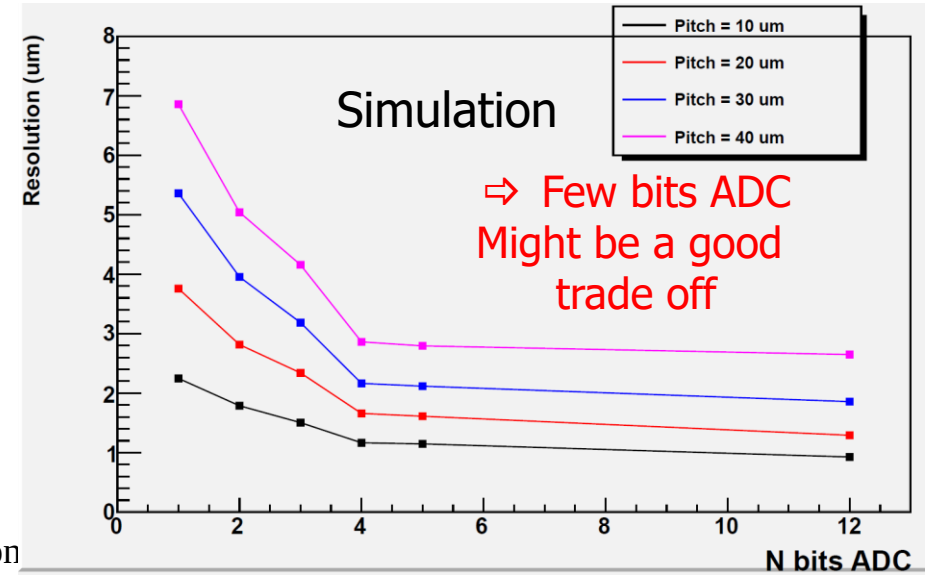
⇨Less charge sharing
⇨Uniform signal rising time

Charge collection Diffusion vs Drift

- Resolution governed by
  - Pitch
  - S/N & Collecting diode
    - Charge sharing
    - epi. thickness, resistivity, etc.
  - Signal encoding (binary or ADC)

- Drift reduces charge sharing
  - ⇨ Reduces cluster size
  - ⇨ degrades resolution
  - ⇨ Improve S/N in seed
  - ⇨ Better Radiation hardness
  - ⇨ Faster charge collection time (<10 ns)



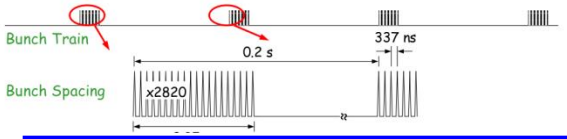


Summary

- State of the art architecture (MIMOSIS & ALPIDE)
  - offers already an attractive trade off in the parameter space for ILC
    - Pitch 22x22 μm ⇨ σ_{sp} ~4 μm ⇨Use double sided ⇨ σ_{sp} ~2.8 μm
    - Read-out time ~ 2-4 μs
    - Power ~< 50 mW/cm^2 without Power pulsing
  - MIMOSIS-0 tests has begun

- CPS are entering into the below μs read out time era
  - Continuous technology progress
    - Smaller feature sizes, deep implant, etc.
    - Imaging industry ⇨ cost effective
  - R&D and new design ideas coming from LHC, etc.
    - MALTA could be a breakthrough: Fast and low power cons.
- However
  - Optimization for each application mandatory
  - Integration is still the ugly duckling of VXD R&D.

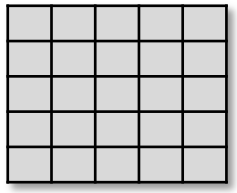
Back-up



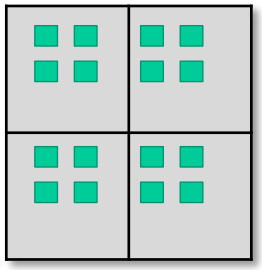
Read-out strategies vs resolution/occupancy

Read-out between trains

~5 μm

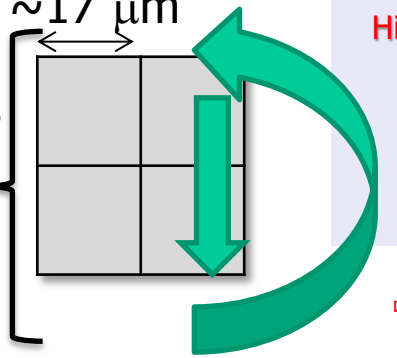


>25-30 μm



Continuous read-out during train

~17 μm

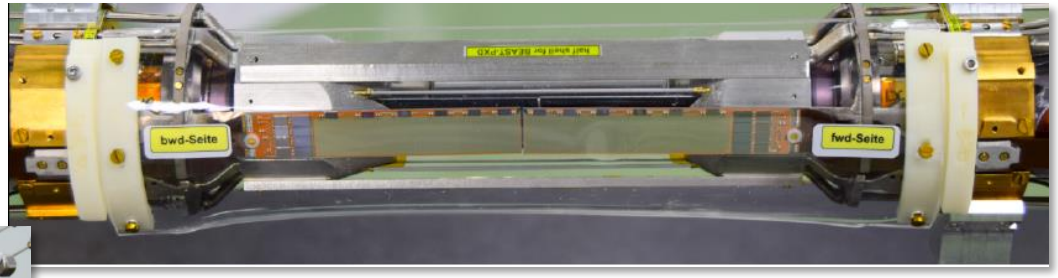


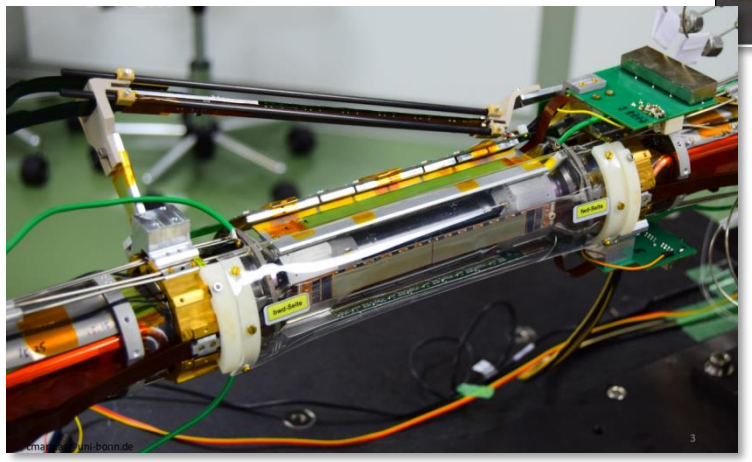
Power	Time resolution	Spatial resolution	Advantages	Caveats
Fine pixels (e.g. FPCCD)				
Low	1 complete train	~ 1 μm	Spatial Resolution Hit separation Beam background tagging capabilities ? (cluster shapes)	⇨x16 #pixels to read-out in 200ms ⇨No time stamping ⇨Occupancy issues ?
In pixel circuitry to store hits with time stamping (e.g. chronopixels, SOI)				
Low	Single or few bunches (>~ 0.5 μs)	>~ 5 μm	Hit time stamping Well suited to outer layers	⇨BX time stamping storage in conflict with granularity
Continuous read-out during train (e.g. DEPFET, CMOS): rolling shutter or priority encoding.				
High	Few to 10s bunches (5-50 μs)	~ 3 μm	Time & spatial resolution compromise	Power cycling mandatory ? ⇨F(Lorentz) ~ 10^5 grams ⇨Distribute 100s Amps shortly before train ⇨heat cycles the ladders.

⇨ Figures may evolve significantly with R&D and access to new technologies
e.g. feature size ⇨Power, read-out speed, granularity, etc.
⇨Different options / room for mixed strategies ?
e.g. double sided ladders: 1-fast / 1-precise

BEAST (beam commissioning)

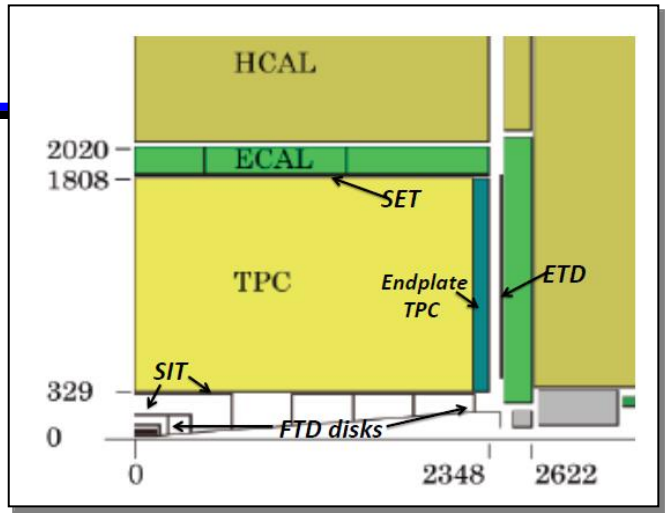
- Motivation
  - Machine commissionning and beam parameters optimization
  - Check rad. safety for VXD
- Beast II installed in the VXD volume
  - 4 PXD Modules DEPFET
  - PLUME ladders
  - Other radiation monitors



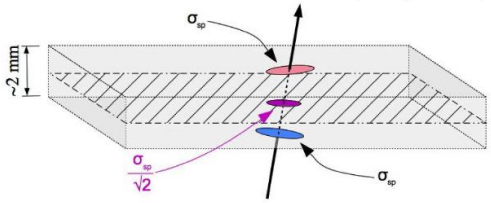


First collisions: March 2018 (until June/July 2018, int. lumi. ~ 20 fb^{-1})

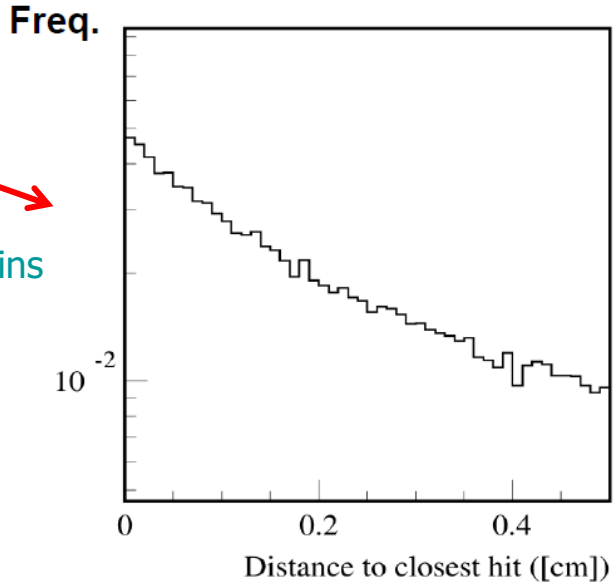
PSIRA for Pixelated SIT



- Concept
  - 2 double-sided layers
    - Improved spatial resolution & track seeding
  - Baseline:
    - $\sigma_{R\phi,Z}$ = 5 μm
    - Δt = 1 μs



- Expected occupancies
  - Beam background ~10^{-2} hits/cm^2/μs
    - Negligible impact on r.o. time
  - Physics hits
    - e.g.: If 5 hits/region/μs ⇨ ~ 750 ns to read it.
    - This actually governs the minimal read-out time !
    - Monte-Carlo input needed
  - Data stored in buffers on the chip and transfered inbetween trains



- Accelerating read-out speed ? (below 1μs)
  - At the expense of Power consumption
    - Needs shrinking peaking time 2μs ⇨ ~300 ns
    - x 5 Power consumption (8 mW/cm^2 ⇨ 40mW/cm^2)
- Potential improvements
  - Clock freq. 20 MHz ⇨ 40 MHz ⇨ 25ns pixel read-out
  - Priority encoder architecture

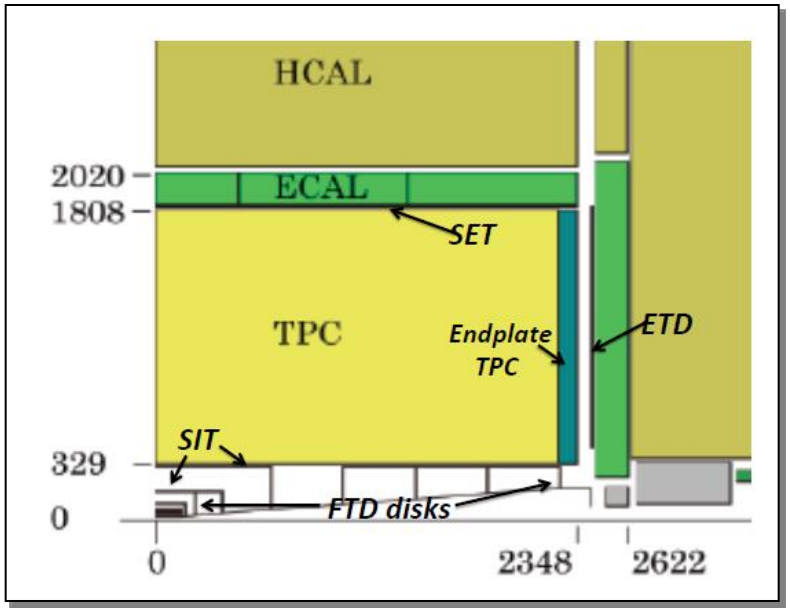
Typical occupancy rate (layer 1, with DBD rates)

Pixel pitch	σ_{sp}	Read-out Time / time resolution	Assumed average cluster multiplicity	Lumi Mode (bunch Per train)	BX time spacing	√s	Assumed Expected Background	Expected background with safety factor 5	Occupancy	remarks
(μmxμm)	μm	(μs)	# pixels	B/train	ns	GeV	#hits/cm²/BX		w.o./w safety	
17x17	~3	50	5	Baseline (1312)	554	500	6	30	$8x10^{-3}$ / $4x10^{-2}$	DBD
17x17	~3	50	5	Upgrade (2625)	**366**	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Lumi upgrade
17x17	~3	50	5	1312	554	**250**	3	15	$4x10^{-3}$ / $2x10^{-2}$	250 GeV
17x17	~3	50	5	2500	366	**1000**	10	50	$2x10^{-2}$ / $1x10^{-1}$	1 TeV
17x17	~3	**25**	5	Baseline (1312)	554	500	6	30	$4x10^{-3}$ / $2x10^{-2}$	DBD X 2 faster
22 x 22	**~4**	4	5	Baseline (1312)	554	500	6	30	$1.5x10^{-3}$ / $8x10^{-3}$	Async. Read-out
25 x 25	**~5**	**1BX**	**3**	Baseline (1312)	554	500	6	30	$1x10^{-4}$ / $5x10^{-4}$	Bunch stamping
5 x 5	**~1**	**1 train**	**6**	Baseline (1312)	554	500	6	30	$1x10^{-2}$ / $6x10^{-2}$	Fine pixel BB tagging

$$\text{Occupancy} = (\#\text{hits/cm}^2\text{/BX}) \times \langle\text{mult}\rangle \times (\text{pitch})^2 \times (\text{r.o.time}) / (\text{BXtime}) \times \text{safety}$$

5 part/cm²/BX ⇨17x17 μm² pitch, cluster mult. ~5, 50 μs read-out time @ 0.5TeV on Layer 1 ⇨ ~ 1 %

ILD dimensions



Barrel system						
System	R(in)	R(out)	z /mm	comments		
VTX	16	60	125	3 double layers	Silicon pixel sensors,	
				layer 1: $\sigma < 3\mu m$	layer 2: $\sigma < 6\mu m$	layer 3-6 $\sigma < 4\mu m$
Silicon						
- SIT	153	300	644	2 silicon strip layers	$\sigma = 7\mu m$	
- SET	1811		2300	2 silicon strip layers	$\sigma = 7\mu m$	
- TPC	330	1808	2350	MPGD readout	$1 \times 6\text{mm}^2$ pads	$\sigma = 60\mu m$ at zero drift
ECAL	1843	2028	2350	W absorber	SIECAL	30 Silicon sensor layers, 5×5 mm^2 cells
					EcECAL	30 Scintillator layers, 5×45 mm^2 strips
HCAL	2058	3410	2350	Fe absorber	AHCAL	48 Scintillator layers, 3×3cm^2 cells
					SDHCAL	48 Gas RPC layers, 1×1 cm^2 cells
Coil	3440	4400	3950	3.5 T field	2λ	
Muon	4450	7755	280	14 scintillator layers		

SIT characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
153	368	0.910	R: σ=7.0,	307.7 (153.8)	0.65
300	644	0.902	z: σ=50.0	σ=80.0	0.65

SET characteristics (current baseline = false double-sided Si microstrips)					
Geometry			Characteristics		Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	Time [ns]	RL[%]
1811	2350	0.789	R: σ=7.0,	307.7 (153.8)	0.65

ETD characteristics (current baseline = single-sided Si micro-strips, same as SET ones)				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
419.3-1822.7	2420	0.985-0.799	x:σ=7.0	0.65

FTD characteristics (design baseline: pixels for two inner disks, microst				
Geometry			Characteristics	Material
R[mm]	Z[mm]	cosθ	Resolution R-ϕ[μm]	RL[%]
39-164	220	0.985-0.802		0.25-0.5
49.6-164	371.3	0.991-0.914	σ=3-6	0.25-0.5
70.1-308	644.9	0.994-0.902		0.65
100.3-309	1046.1	0.994-0.959		0.65
130.4-309	1447.3	0.995-0.998	σ=7.0	0.65
160.5-309	1848.5	0.996-0.986		0.65
190.5-309	2250	0.996-0.990		0.65

Power details

Sensitive Surface (mm²)		412
Hit rate (MHz/cm²)		10
Integration time (µs)	<10	
Pixels/cluster		2,3

ALPIDE Power consumption	mW	
Analogue pixels		22
Bias		3,2
Priority Encorders		3
Digital periphery		45,7
PLL		18,5
Serializer		30,6
LVDS		18,8
Other+		10,2
Total		152
Power consumption mW/cm²		36,9

Sensitive Surface (mm²)	253,8	Pixel: 22 x 22 µm²
Hit rate (MHz/cm²)	10,0	?
Integration time (µs)	**4**	
Pixels/cluster	5	

PSIRA Power consumption	mW		
Analogue pixels		35	faster readout time
Bias		3,2	
Priority Encorders		3	50 ns/pixel
Digital periphery		45,7	
PLL		18,5	
Serializer		61,2	x2 speed
LVDS		37,6	x2 pads
Other+		10,2	
Total		214,4	
Power consumption mW/cm²		84,5	

Sensitive Surface (mm²)	253,8	Pixel: 22 x 22 µm²
Hit rate (MHz/cm²)	10,0	?
Integration time (µs)	**2**	
Pixels/cluster	5	

PSIRA Power consumption	mW		
Analogue pixels		50	faster readout time
Bias		3,2	
Priority Encorders		6	25 ns/pixel
Digital periphery		91,4	x 2 ?
PLL		18,5	
Serializer		61,2	x2 speed
LVDS		37,6	x2 pads
Other+		10,2	
Total		278,1	
Power consumption mW/cm²		109,6	