VTX

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For FPCCD Group

R&D This year

- Trying higher readout speed (Sato)
- CO2 cooling (Sugimoto)
- Interface document (Ishikawa)

Toward readout speed of 10Mpix/s

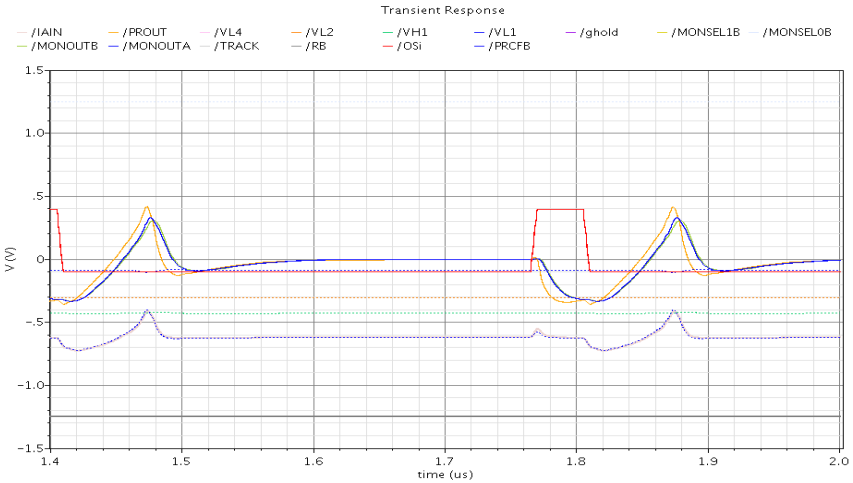
- FPCCD pixels should be read in between trains, 199msec. This corresponds to 100nsec/pixel or 10Mpix/s.
  - readout speed upto 2.5Mpix/s was performed for FPCCD+ASIC so far
  - Only with ASIC, 12.5Mpix/s was achieved.

- We found three problems in the FPCCD+ASIC combined test aiming for 10Mpix/sec operation.
  1. ASIC response to CCD reset feed-thourgh pulse
  2. Pedestal level rapidly rises
  3. Gain drop
- These should solved in the next production

1st problem and solution
ASIC bias shift to CCD reset feed-through

FPCCD reset feed-through pulse drives pre-amplifier in reset phase into some state. It takes time for pre-amplifier to return to normal bias. It works properly only below 2.5Mpix/sec

Simulation of pre-amplifier in reset phase reproduces the bias shift due to reset feedthrough pulse.



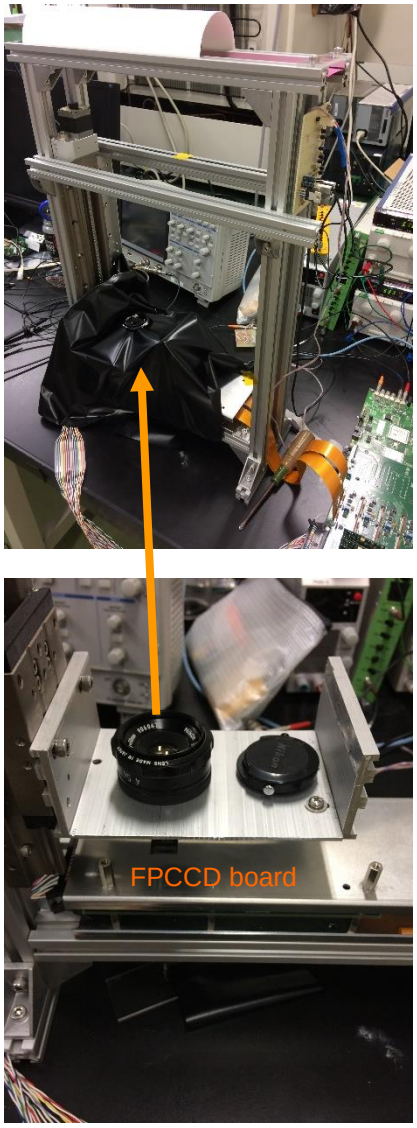
Counter reset pulse can be a temporally solution for the pre-amplifier behavior problem and proved by simulation with both 5M and 10Mpix/s cases.

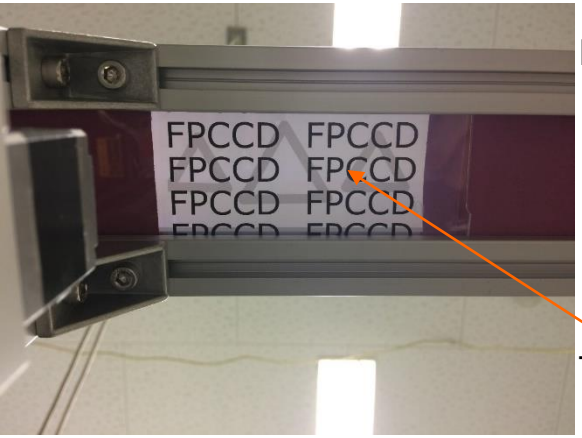
FPCCD measurement using photo image

1. Easy to debug DAQ system
2. Easy to test FPCCD + ASIC
3. Plan to upgrade for Large-CCD test and FPC ladder test

Scene of measuring.

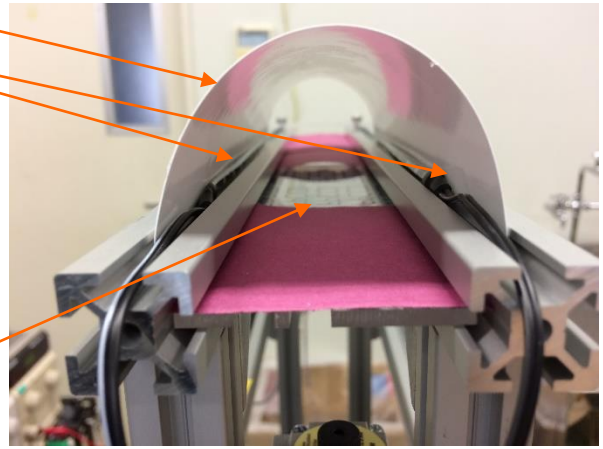
Outer black sheet revealed.





reflecter

LED array



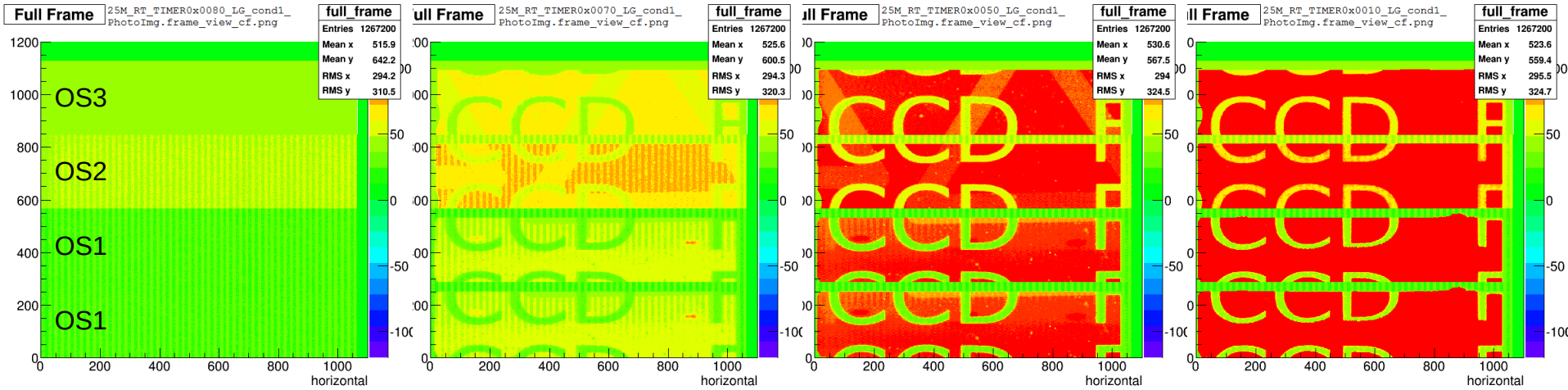
Test image

CCD output with different LED exposure time

OS3,OS2,OS1,OS1 (ASIC ch6,7,8,8) from top.

2.5M sampling/sec

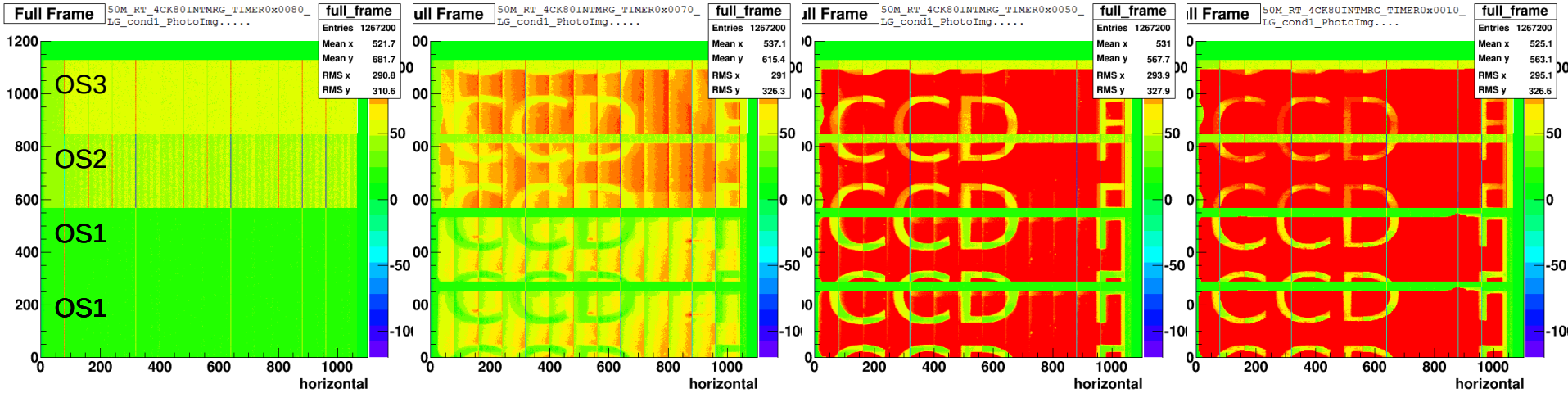
LOW gain LED 0msec 160msec 480msec 1120msec



5.0M sampling/sec

Vertical lines at every 80 pixels are caused by intermittent RG.

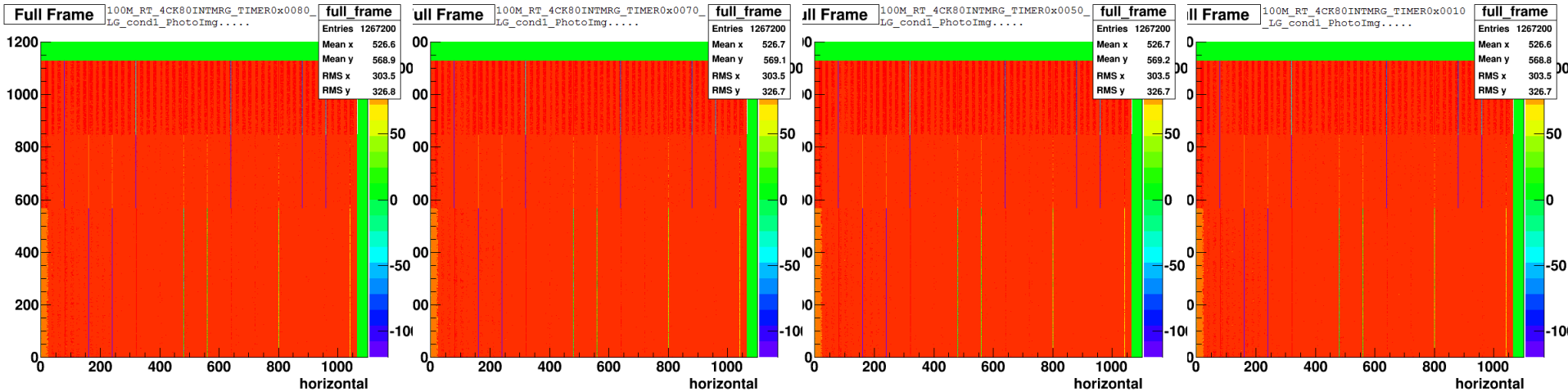
LOW gain LED 0msec 160msec 480msec 1120msec



2nd problem: Pedestal level rapidly rises

10.0M sampling/sec intermittent RG

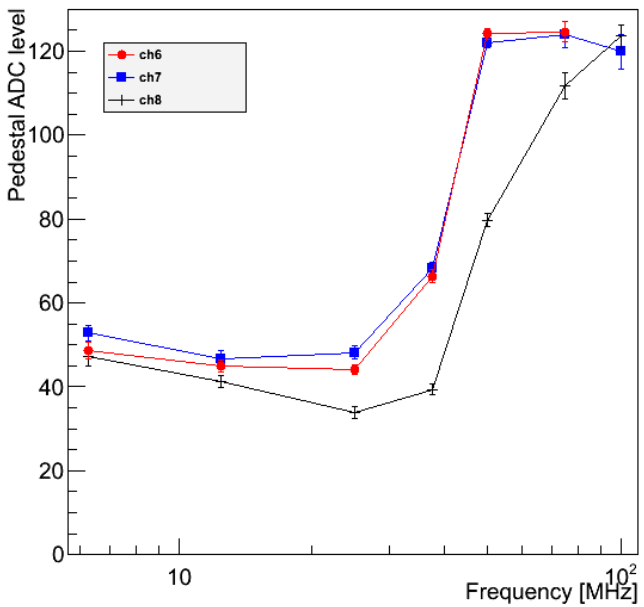
LOW gain LED 0msec 160msec 480msec 1120msec



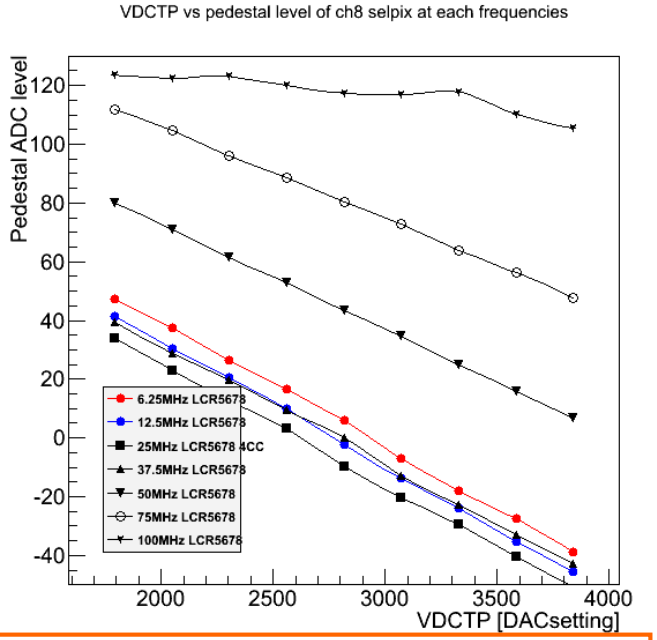
Pedestal level rapidly rises above 2.5Mpix/sec, and ADC overflows.

Reason: over/under shoot on OS signal (FPCCD output), caused by clock feed-through.

freq vs pedestal level of ch6,7,8

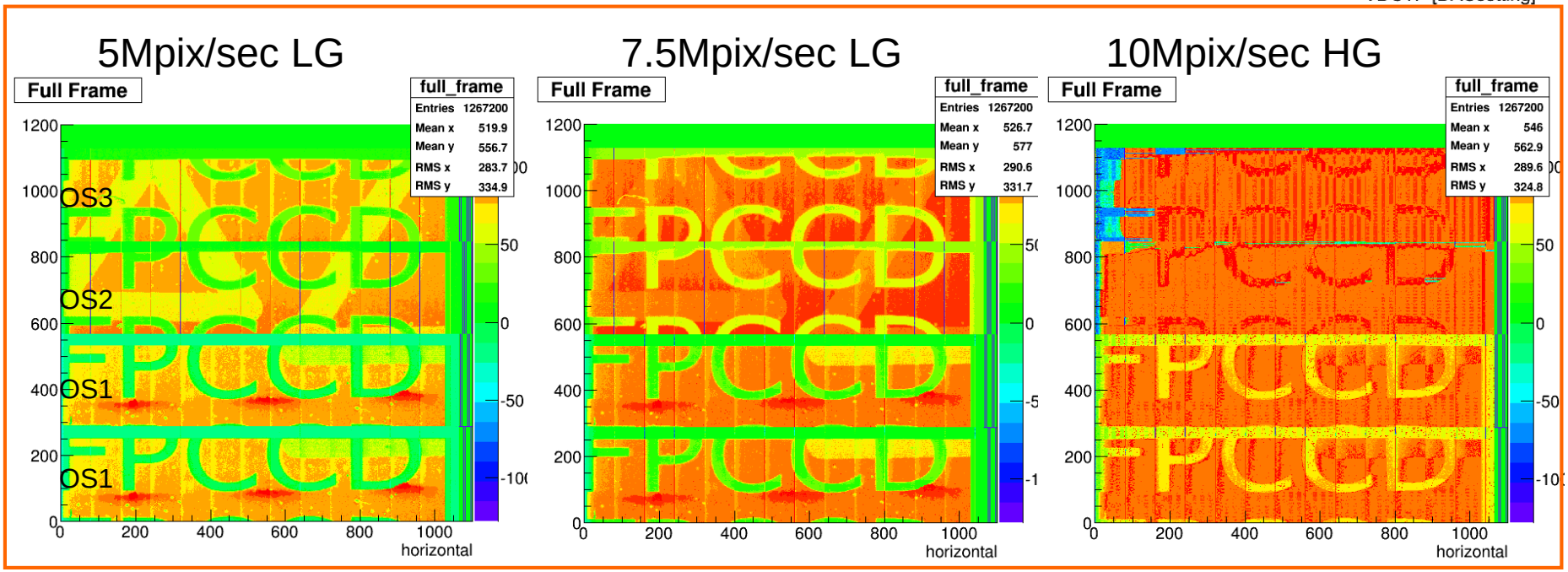


Temporal solution to avoid ADC overflow.

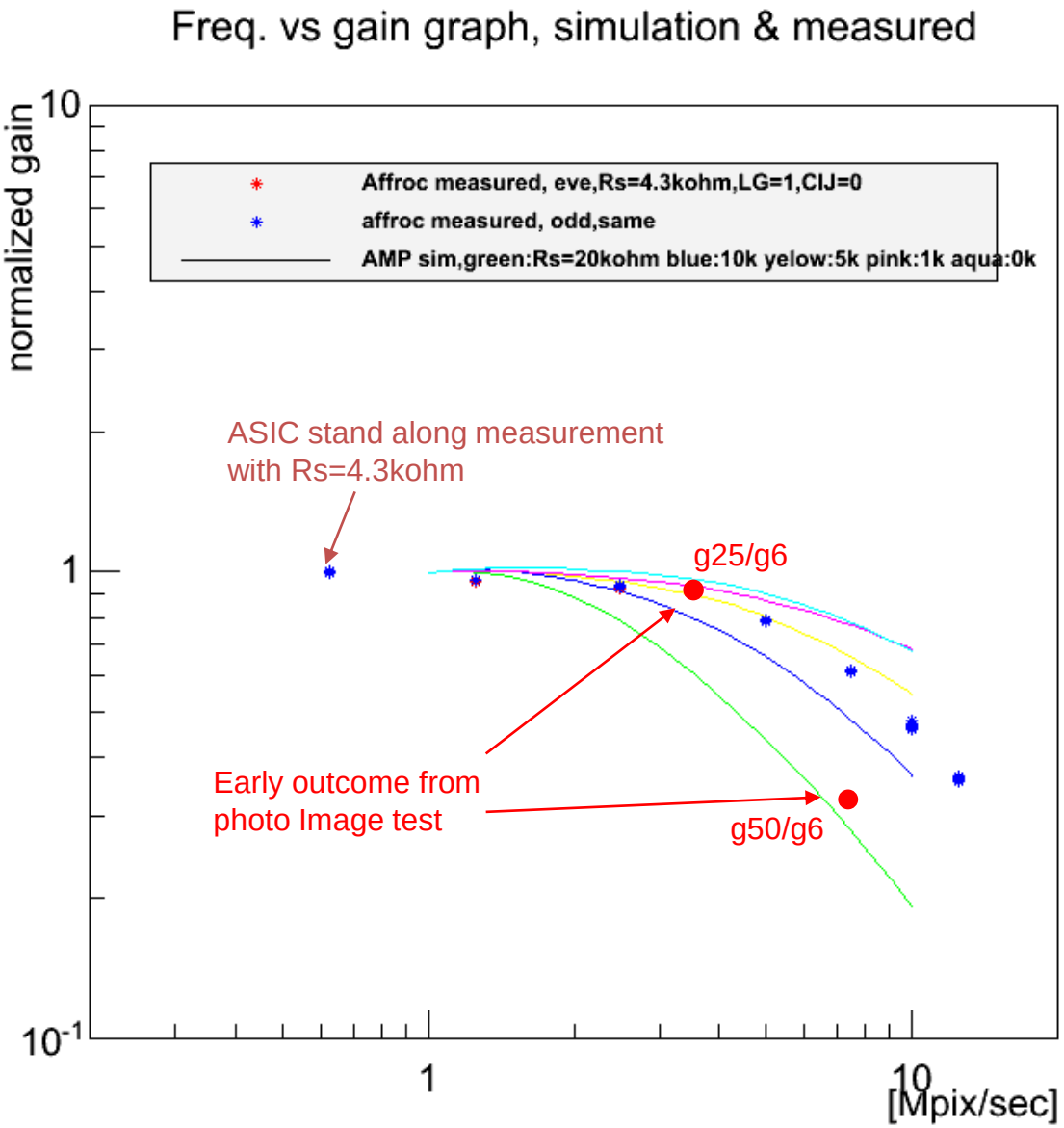


- decrease amplitude of SG (sum gate drive signal, one of CCD clocks).
- introduce counter signal through ASIC test pin
--- very effective, see the right graph.
- increase ADC reference voltage: VREF1/VREF2

Finally signal at 10Mpix/sec seen.



3rd problem : Gain drop



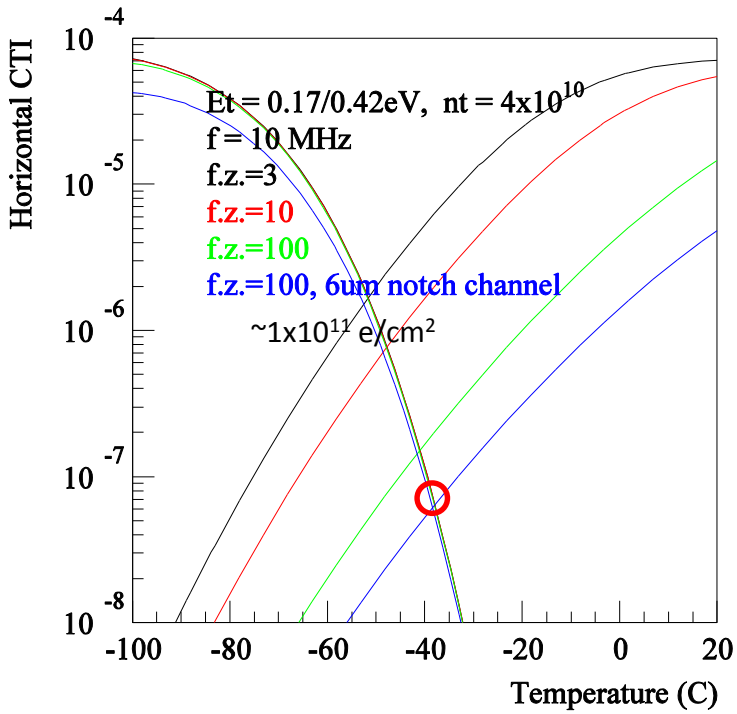
FPCCD output impedance is smaller than 2kohm, because of 2kohm pull down resister.

Early phase photo image test result shows more rapid gain drop than CR model circuit simulation result which agree to ASIC alone test result.

We are working on this problem.

Why we need CO2 cooling?

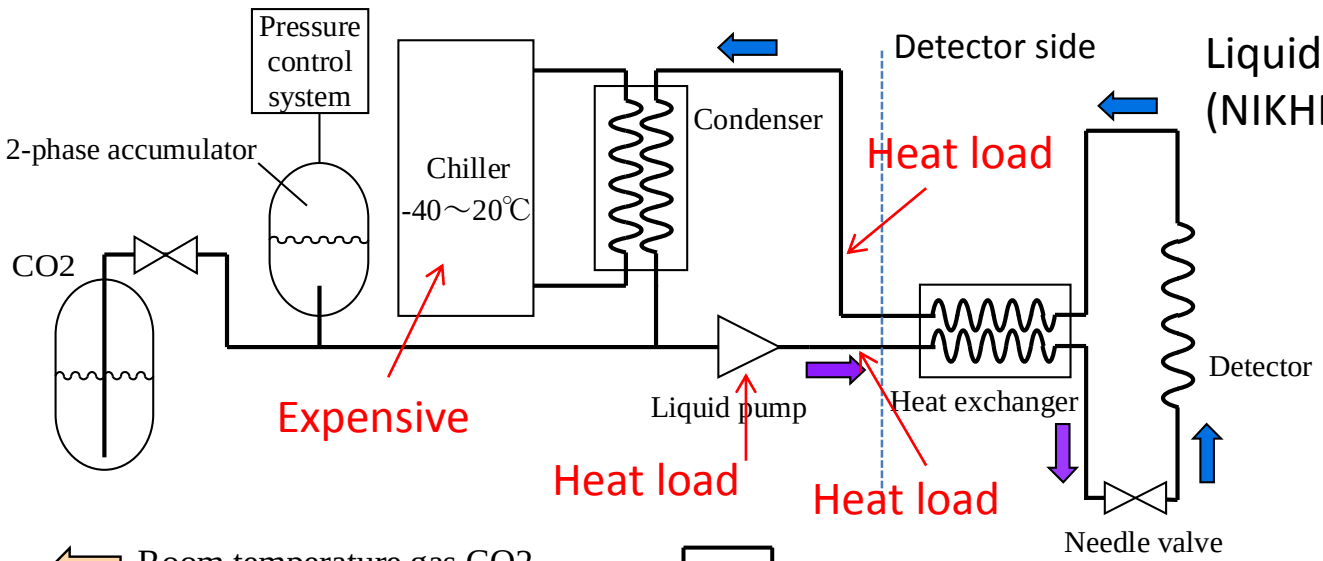
- Operation temperature
  - Charge Transfer Inefficiency (CTI) of FPCCD due to radiation damage is a function of temperature
  - A simple simulation of CTI based on Shockley-Read-Hall theory shows around −40℃ is optimal
  - Cooling at −40℃ is achievable by 2-phase CO2
  - 2-phase CO2 cooling gives constant temperature cooling with the cooling power of 300J/g

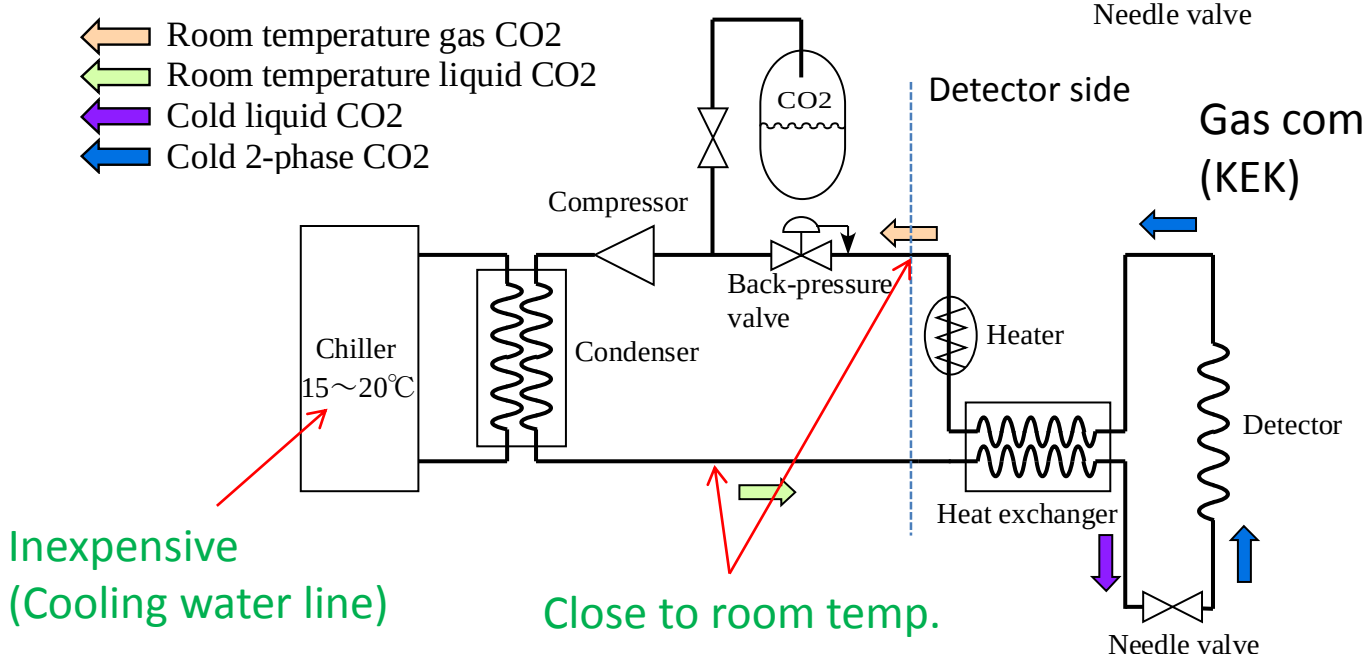


Why we need CO2 cooling?

- Material budget / dead region
  - Heat sources of FPCCD VTX locate mainly at both ends of ladders (on-chip amps and front-end ASICs)
  - Cooling by 2-phase CO2 at both ends of ladders seems an attractive solution
  - 2-phase CO2 can go through very thin cooling tube (OD 2mm or less) → Only 0.3%X_0 increase of material budget of the end-plate
  - Gas cooling requires much thicker tube → Dead space between FTD and beam pipe

Schematic diagram

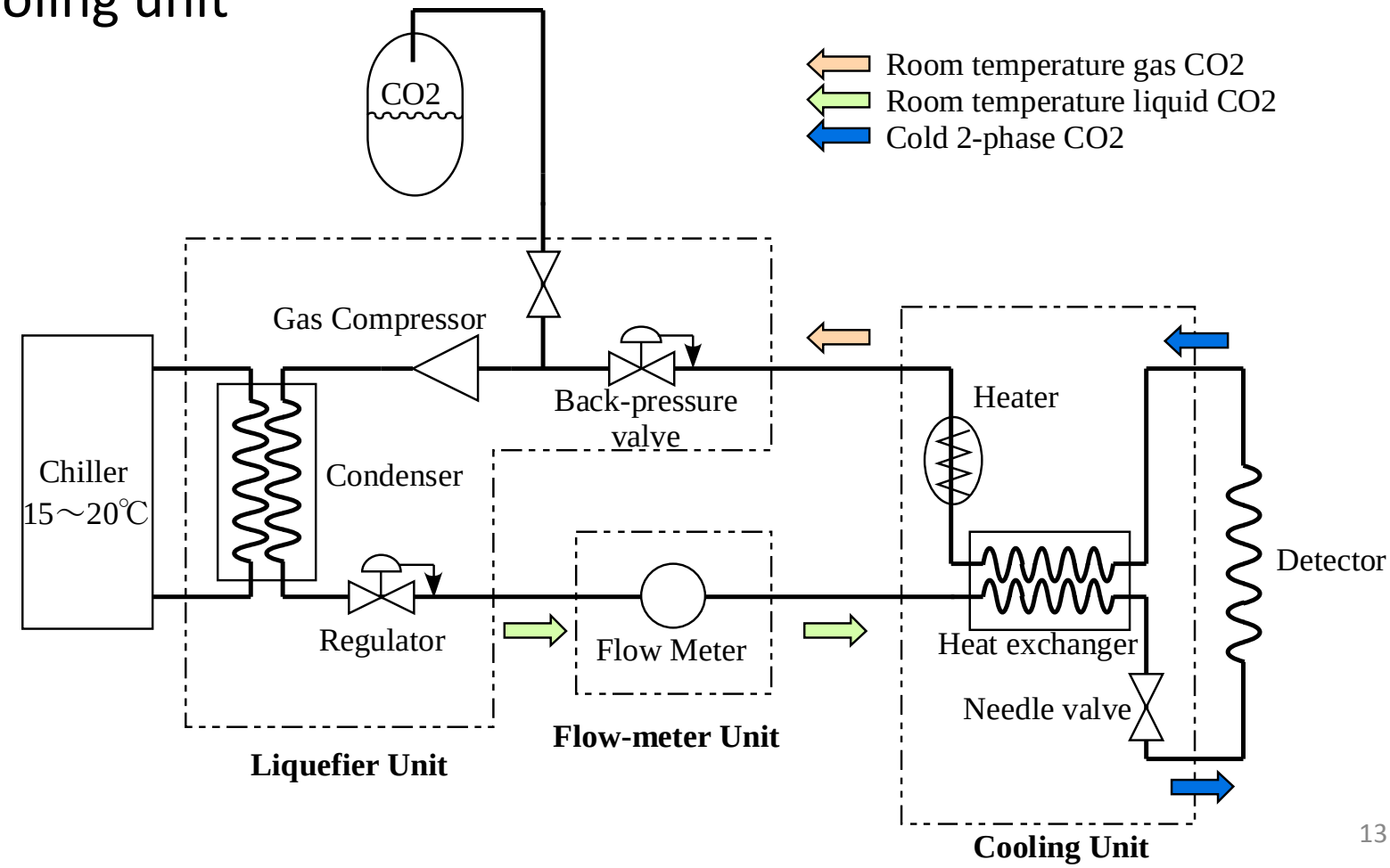




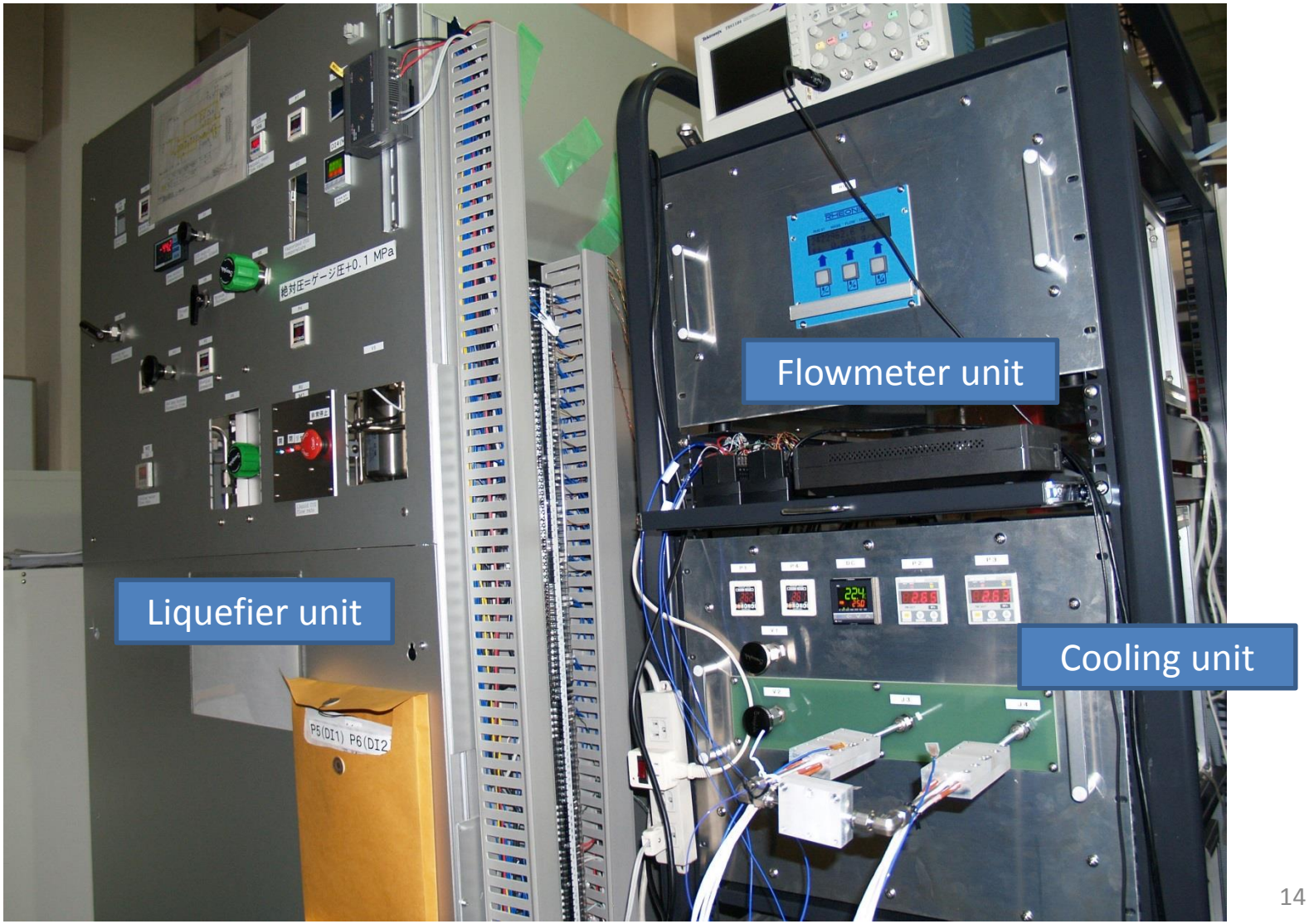
Cold CO2 only detector side!
No thermal insulator needed

Prototype

- Consists of 3 units; Liquefier unit, flowmeter unit, and cooling unit

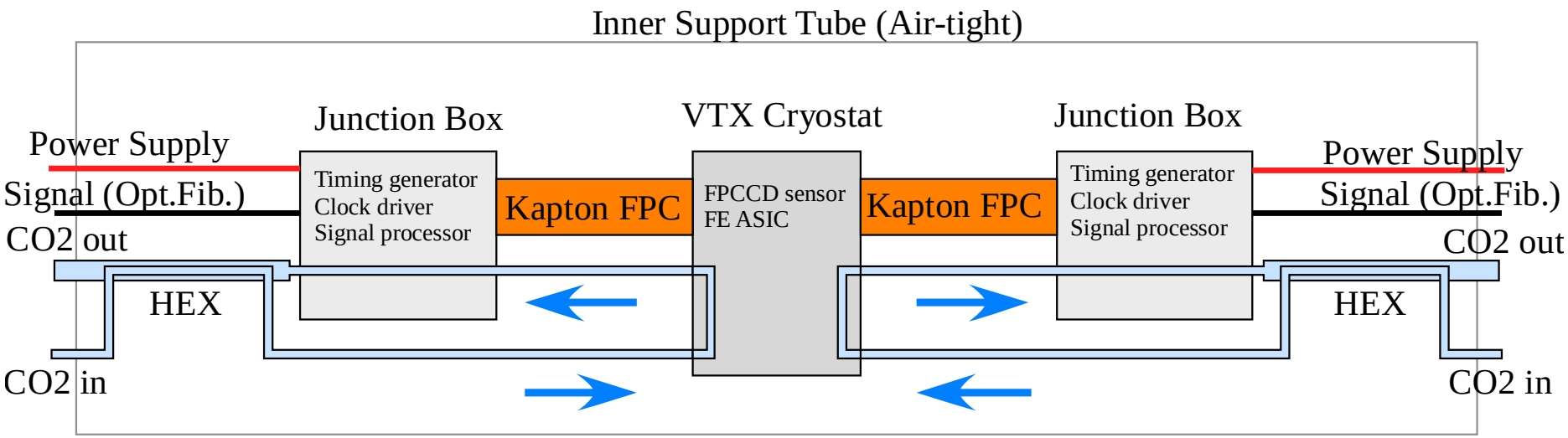


Prototype



Low-mass heat exchanger

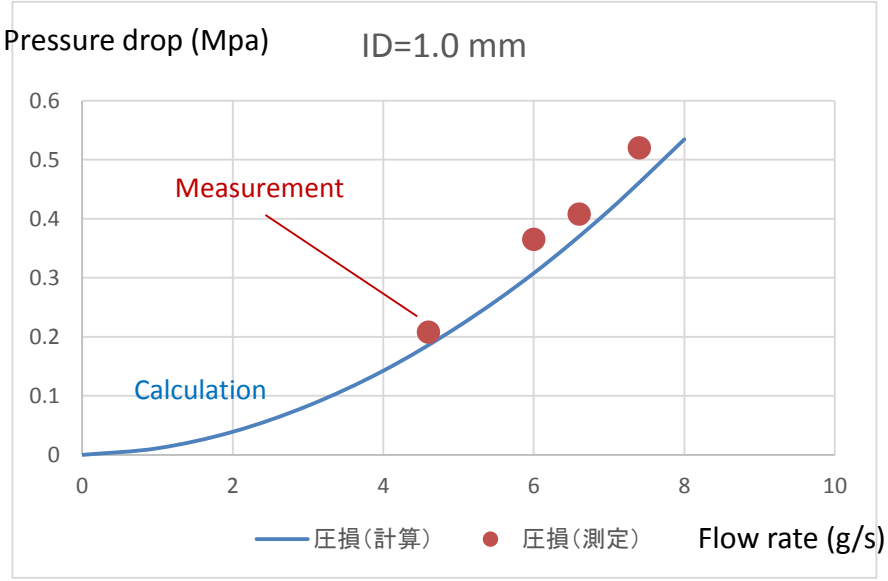
- Heat exchanger (HEX) will be placed inside the inner support tube filled with dry air
- Low mass HEX is indispensable
- R&D of double-layer tube HEX is on going
  - Inner thin tube works as a pressure reducer instead of a needle valve

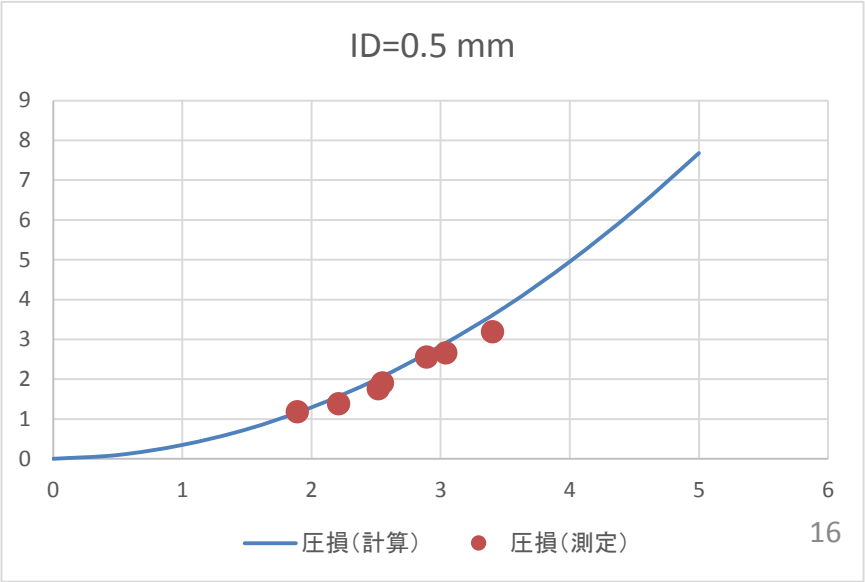


Low-mass heat exchanger

Nominal CO_2 flow rate for FPCCD cooling is 1g/side

- R&D items
  - Pressure drop
    - Pressure drop through several inner diameter tubes has been measured
    - Measured value was consistent with calculation
  - Heat exchange efficiency
    - Systematic study of heat exchange efficiency is planned in coming several weeks





Interface Document

- Since (at least) three technologies are proposed for ILD vertex detector, we should separate common issues and specific issues
- Common issue
  - Detector support including EMI shield and cryostat
- Specific issue
  - Cables
  - Location of Frontend electronics
  - Power consumption and Cooling (N_2, CO_2)
  - DAQ system and racks
- Version 1 for FPCCD is not available yet but in preparation

Serious Personpower Problem

- From this fiscal year, we do not have students working on FPCDD.
  - Currently, four Master students working on physics analysis and one is on pair monitor simulation in Yamamoto-lab
- Murai-kun moved to Belle (II), but he decided to quit from HEP. He will leave from our group in Mar 2019.
- Before that we should find other person to take over his study.
  - I am very busy for Belle II so I could not.

- Otherwise, FPCCD group can not finalize the R&D with reasonable timeline.

Summary

- 10Mpix/s Operation
  - Found three problems.
  - We should find much deeper understanding for the sources of the problems to develop new FPCCD and ASIC.
- CO2 cooling
  - Gas compressor based CO2 cooling is better
- Interface document
  - Version 1 in preparation

- Serious Personpower problem
  - No student working on FPCCD in Yamamoto-lab

backup