ReadOut ASICs for ILC Calorimeters

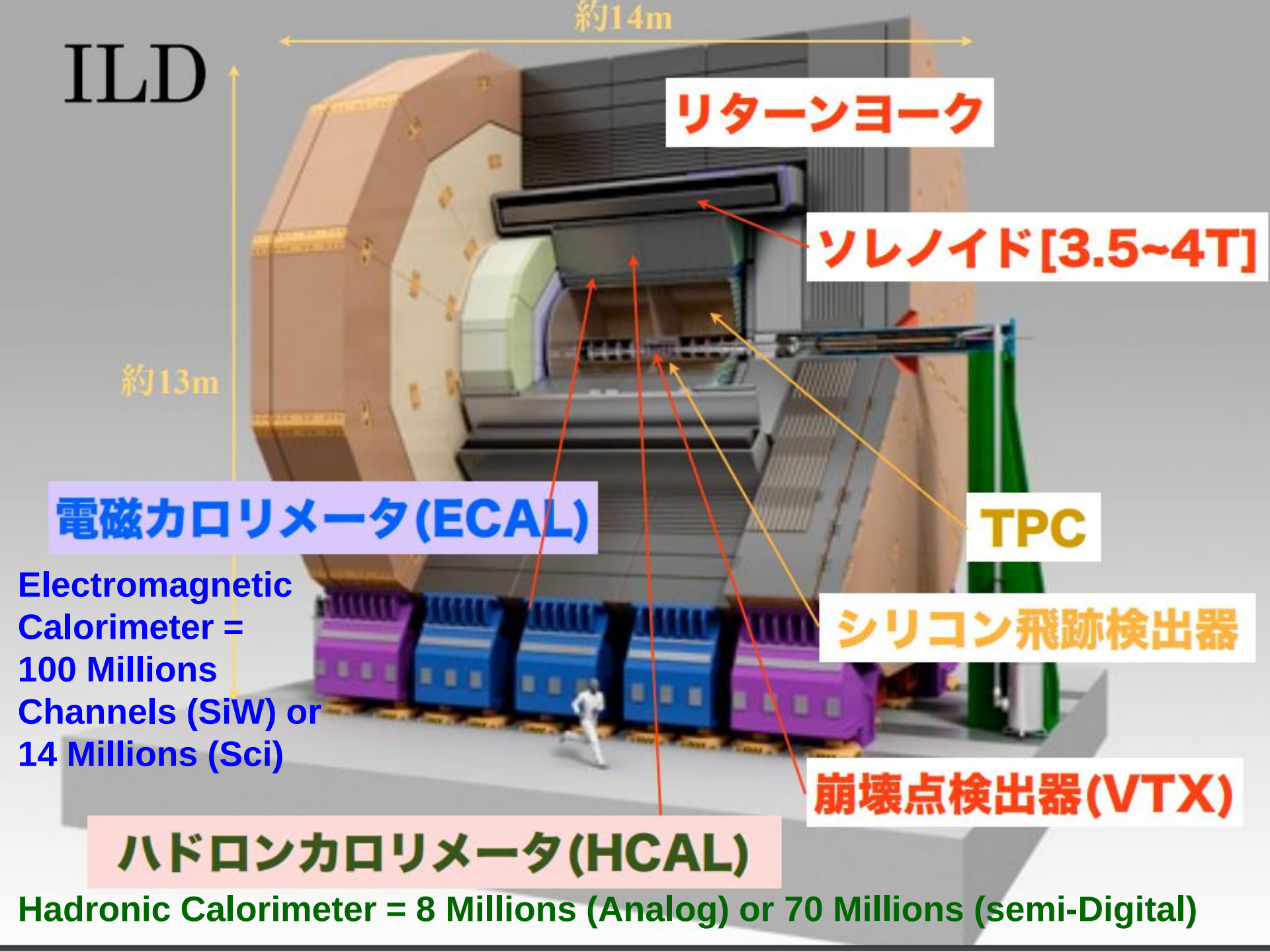
ILC PHYSICS AND DETECTOR MEETING 2018, KEK, つくば市

Stéphane Callier on behalf of OMEGA microelectronics group

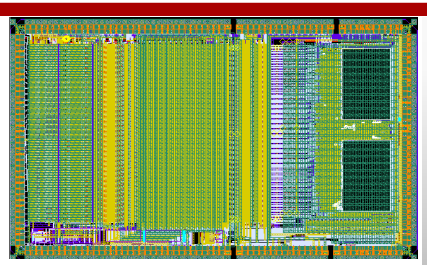
Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

20th March 2018

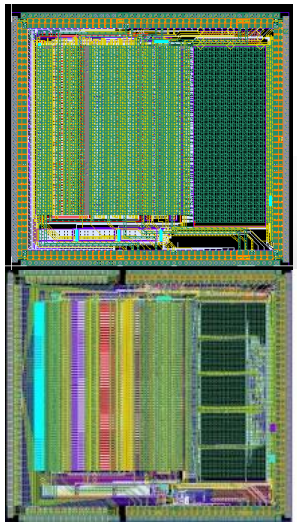
Organization for Micro-Electronics desiGn and Applications


ILD
約14m
約13m
リターンヨーク
ソレノイド[3.5~4T]
TPC
シリコン飛跡検出器
崩壊点検出器(VTX)
電磁カロリメータ(ECAL)
Electromagnetic Calorimeter = 100 Millions Channels (SiW) or 14 Millions (Sci)
ハドロンカロリメータ(HCAL)
Hadronic Calorimeter = 8 Millions (Analog) or 70 Millions (semi-Digital)

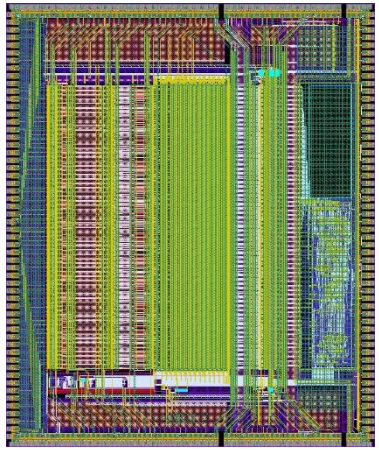
ROC chips for ILC prototypes



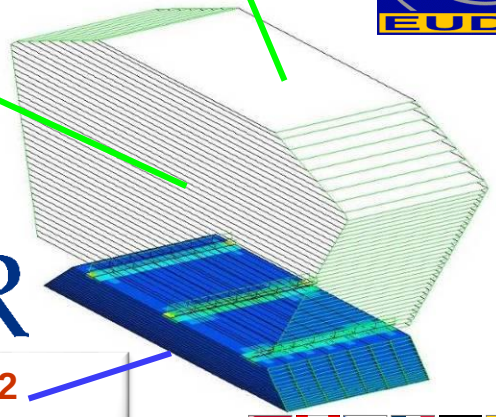
SPIROC2
Analog HCAL (AHCAL)
(SiPM)
36 ch. 32mm²
Jun07, Jun08, Mar10, Sept11
Feb15, Feb 16



HARDROC2/3 and MICROROC
Semi Digital HCAL (sDHCAL)
(RPC, µmegas or GEMs)
64 ch. 16mm²
Sept06, Jun08, Mar10, Feb14,
Feb15



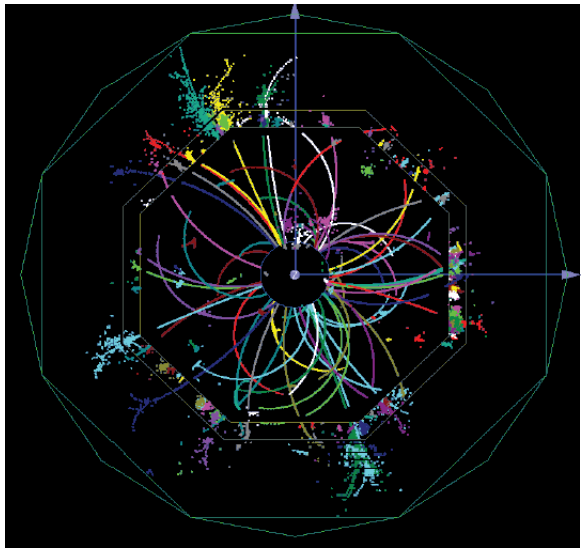
SKIROC2
ECAL
(Si PIN diode)
64 ch. 70mm²
Mar10, Feb16



ROC chips for **technological prototypes**: to study the feasibility of large scale, industrializable modules (Eudet/Aida funded)

Requirements for electronics

- Large dynamic range (15 bits)
- Auto-trigger on ½ MIP
- On chip zero suppress
  - (reduce data volume)
- **10^8 channels -> Integration**
- Front-end embedded in detector
- **Ultra-low power : 25µW/ch**



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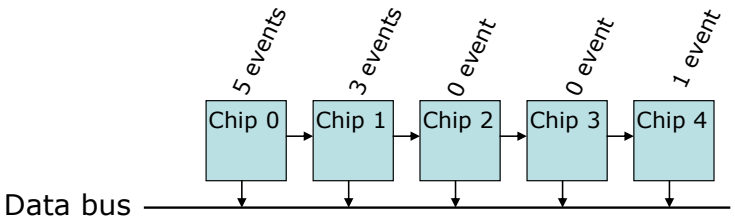
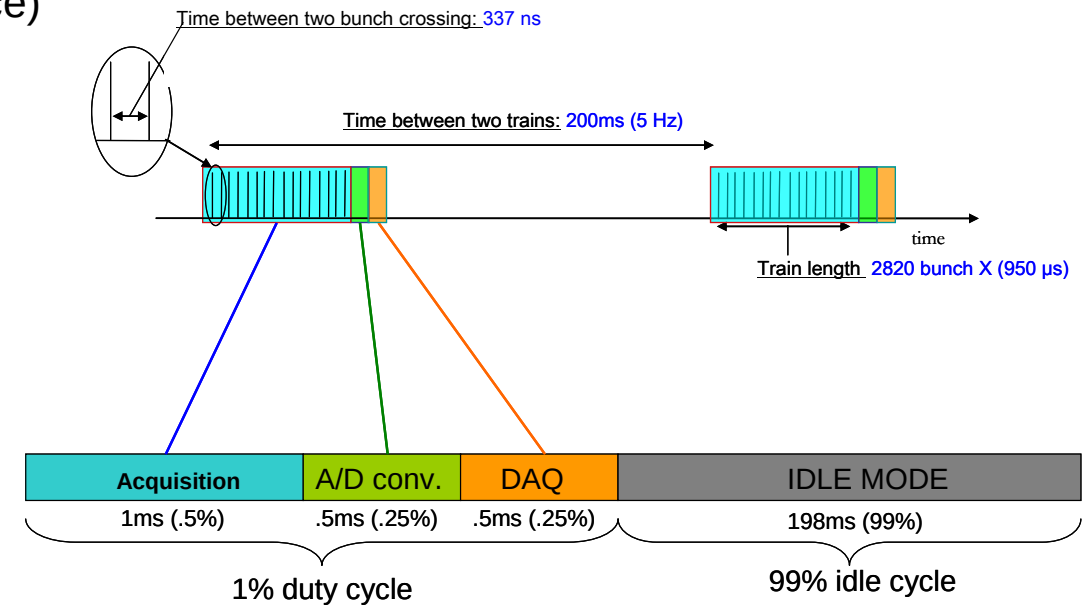
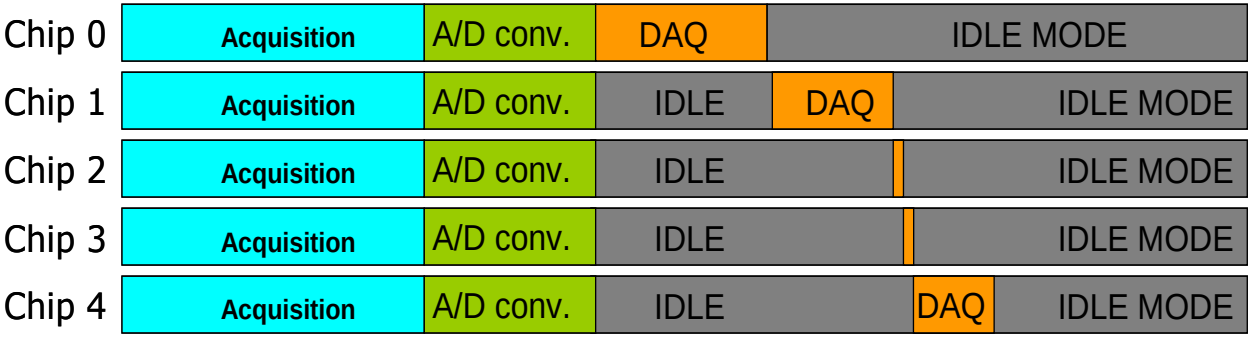
From 2nd generation…

- **2nd generation chips for ILD**
  - Auto-trigger, analog storage and/or digitization
  - Token-ring readout (one data line activated by each chip sequentially)
  - Common DAQ (common interface)
  - Power pulsing : <1 % duty cycle







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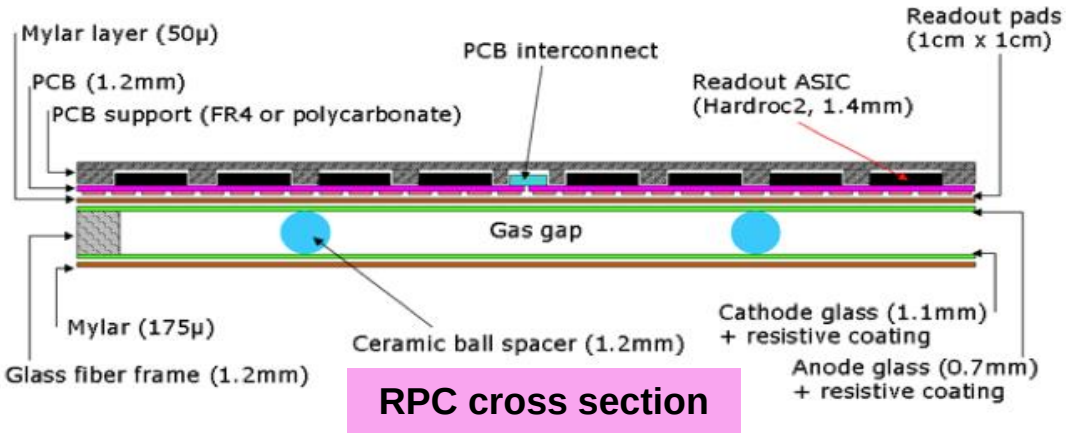
…To 3rd generation

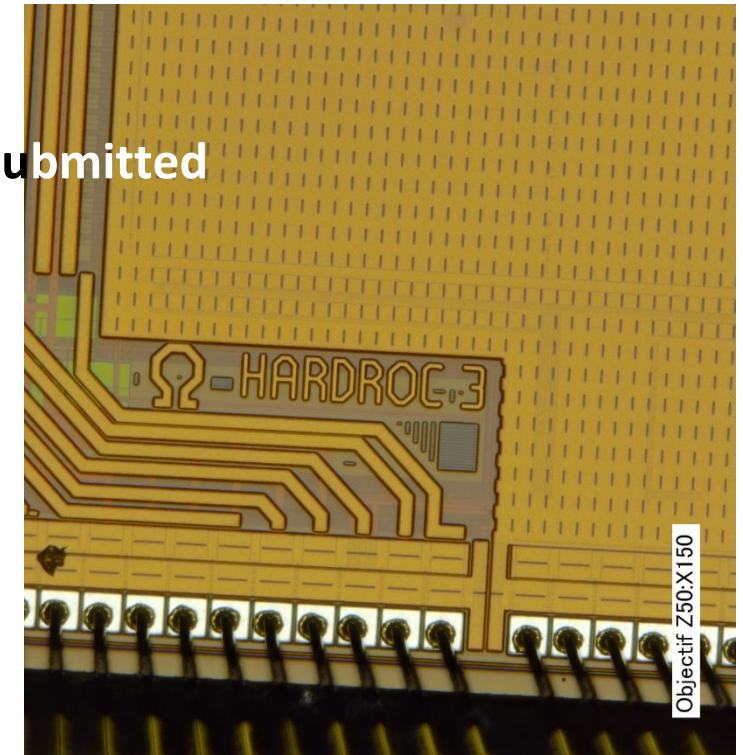
- **3rd generation chips for ILD**
  - **Independent channels (zero suppress)**
    - Huge change in digital part !!
    - Digital part power consumption and size (+30 to 50%)
  - **I2C link (@IPNL)** for Slow Control parameters and **triple voting**
    - configuration broadcasting
    - geographical addressing
  - **PLL** provides the Fast Clock (mainly used for digitization) from the Slow Clock
    - No Fast Clock to be provided to the ASICs !

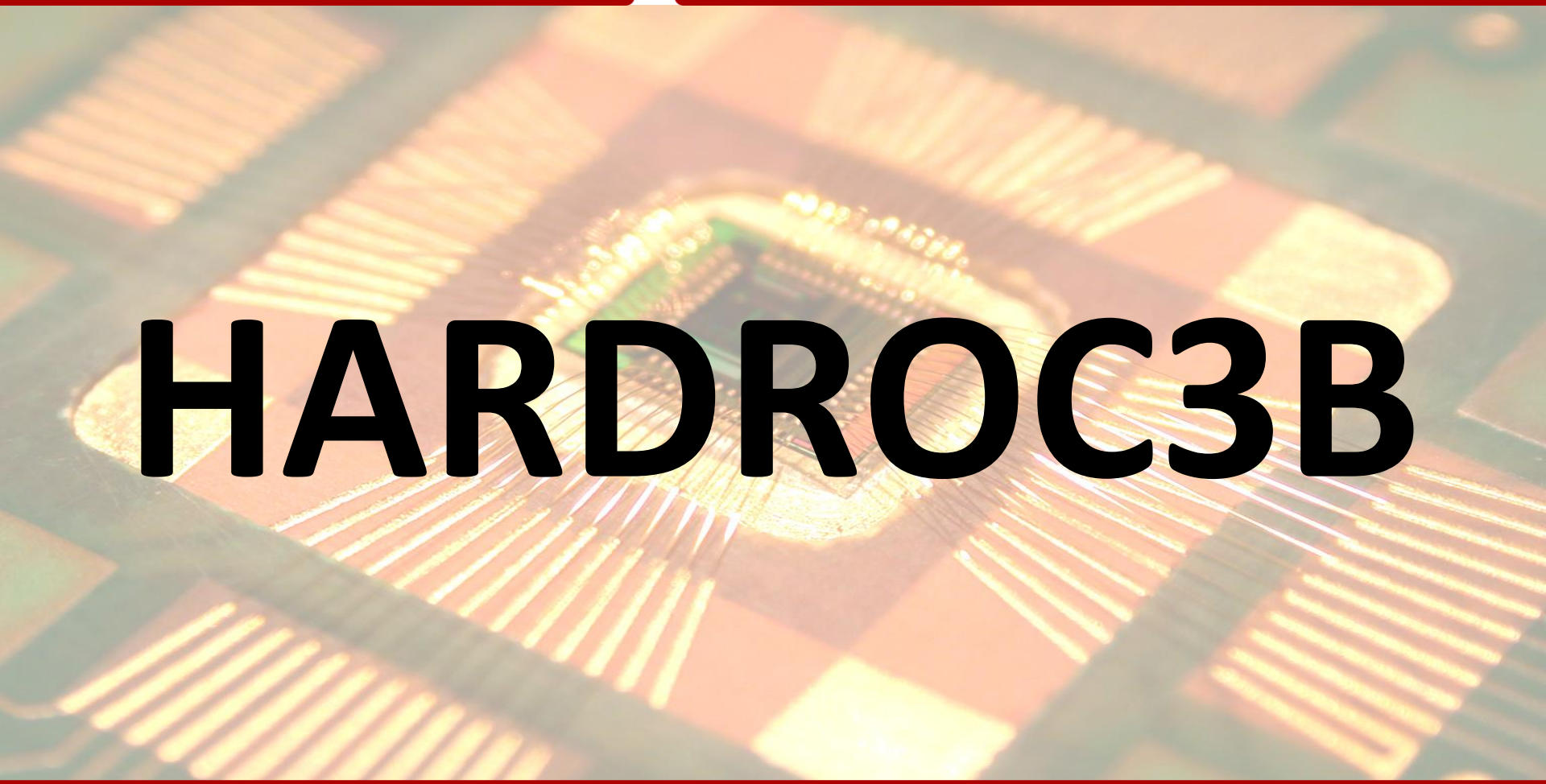
- **HARDROC3: 1st of the 3rd generation chip to be submitted**

  But all ILC R&D stopped since 2016, waiting for ILC decision



RPC cross section



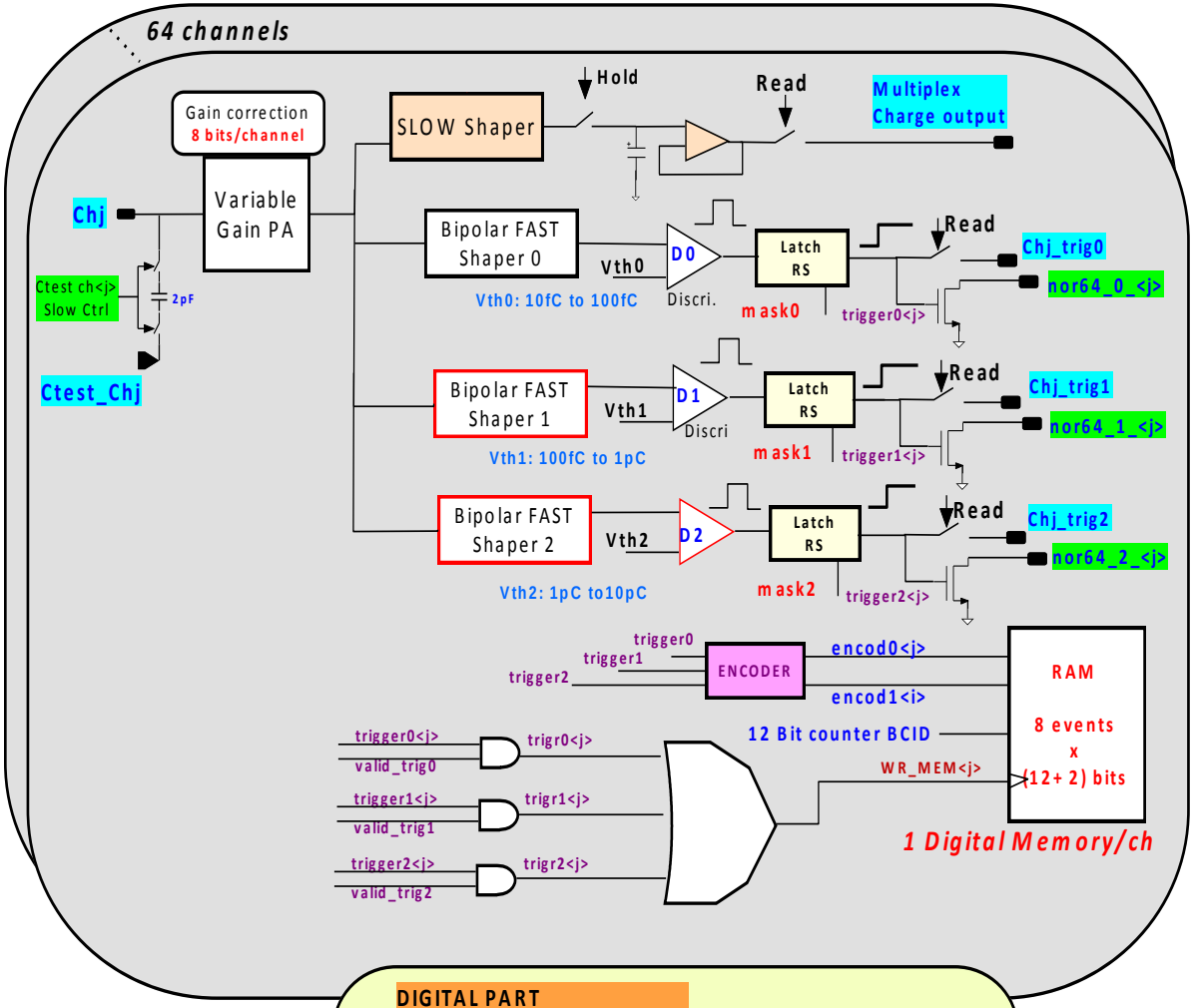


HARDROC3B

Organization for Micro-Electronics desiGn and Applications

HR3: Simplified schematics

- 64 channels with current preamplifiers
- Trigger less mode (auto trigger 15fC up to 50pC)
- Gain correction (max factor 2)
- 3 shapers + 3 discriminators (encoded in 2 bits for readout)
- I2C link with triple voting for Slow Control Parameters
- 64 Independent channels with zero suppress
- Max 8 events / channel with 12-b time stamping
- Integrated clock generator: PLL
- All bias and reference voltage internal (with power pulsing)
  - No decoupling capacitances required on bias and references voltages
- Token Ring ReadOut



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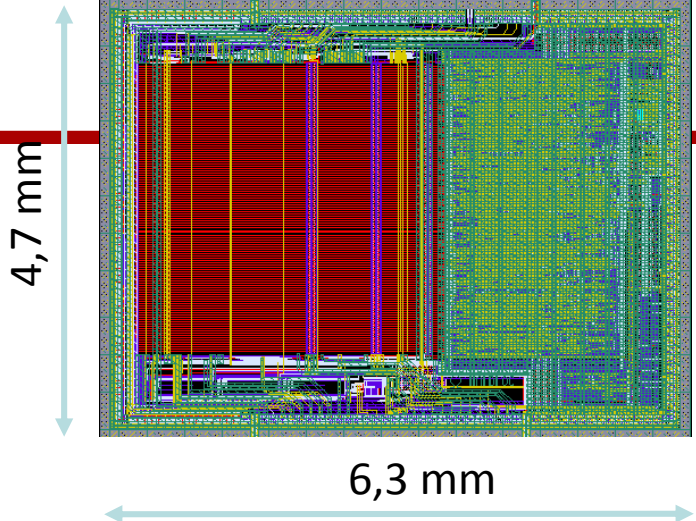
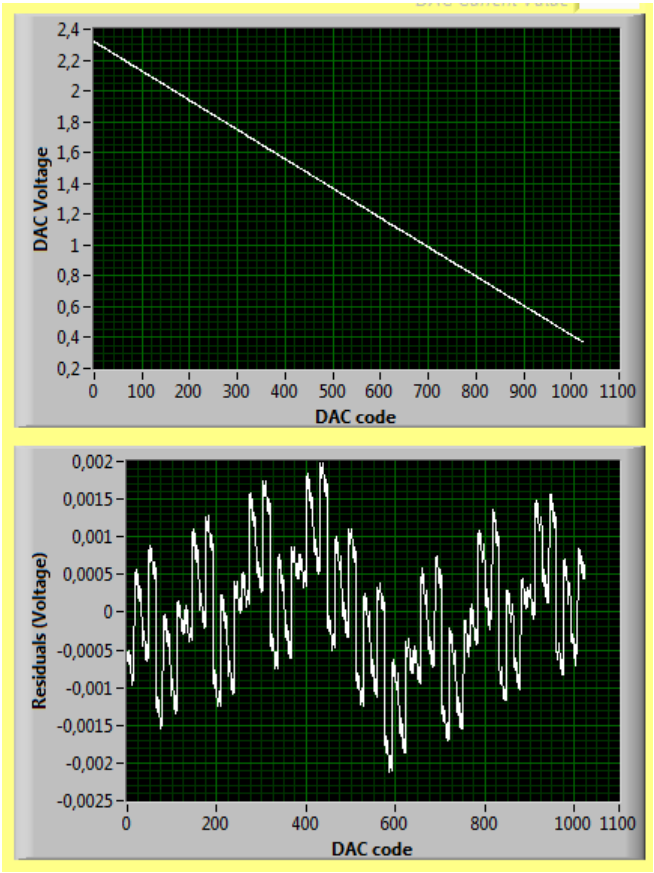
Trigger path : fast shaper and DAC

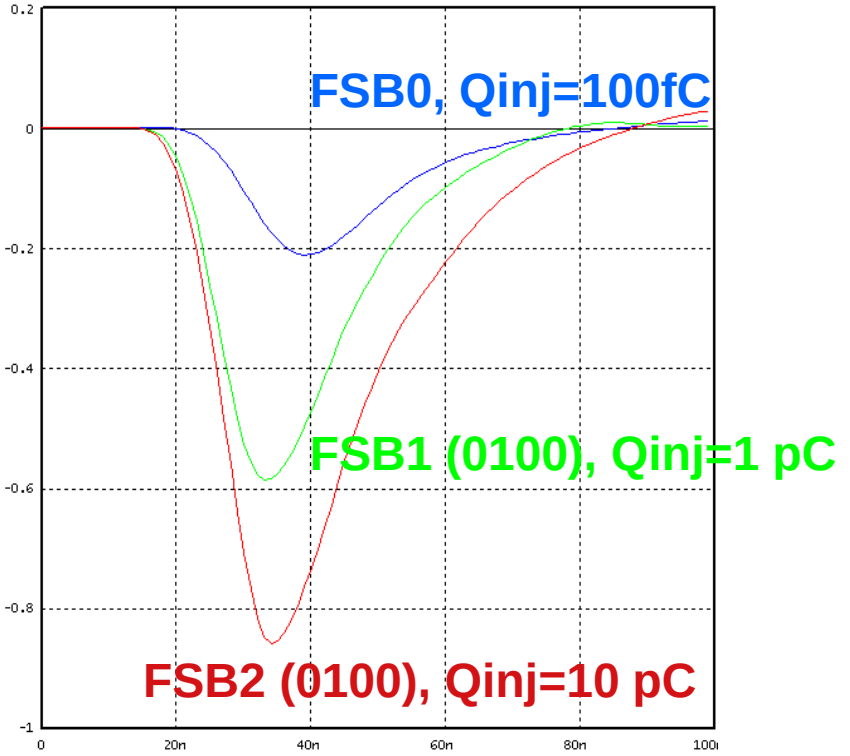
- Charge injected in one channel: 100fC
  - **Fsb0: Typically 2mV/fC** (variable by a factor 10)
- Scurves performed by varying the DAC value (Threshold)
  - 3 integrated DACs to deliver threshold voltages
  - Residuals within ±5 mV / 2.2V dynamic range.
    - INL= 0.2% (2LSB)





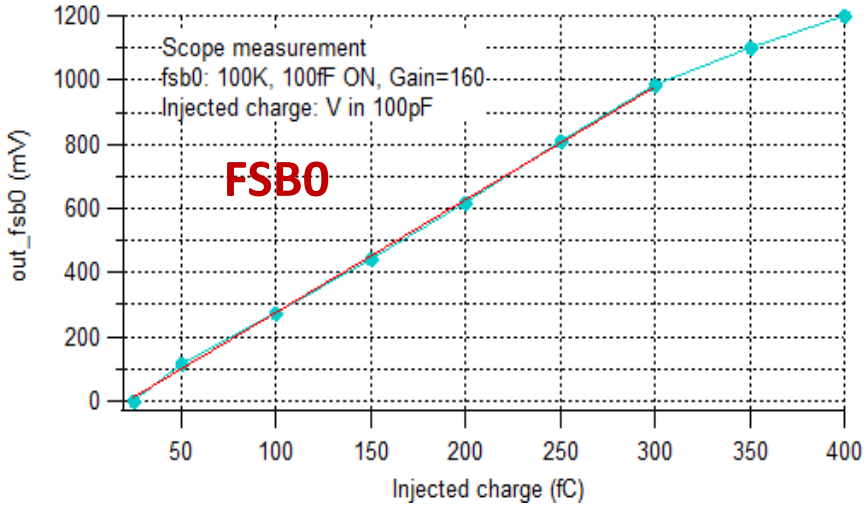
2.1mV/DACu

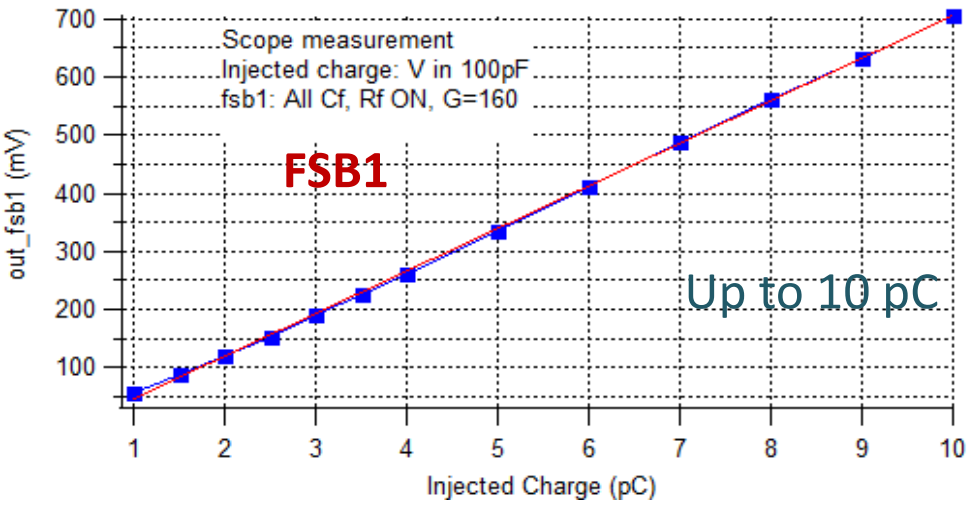
ie. 1 fC/DACu (fsb0)

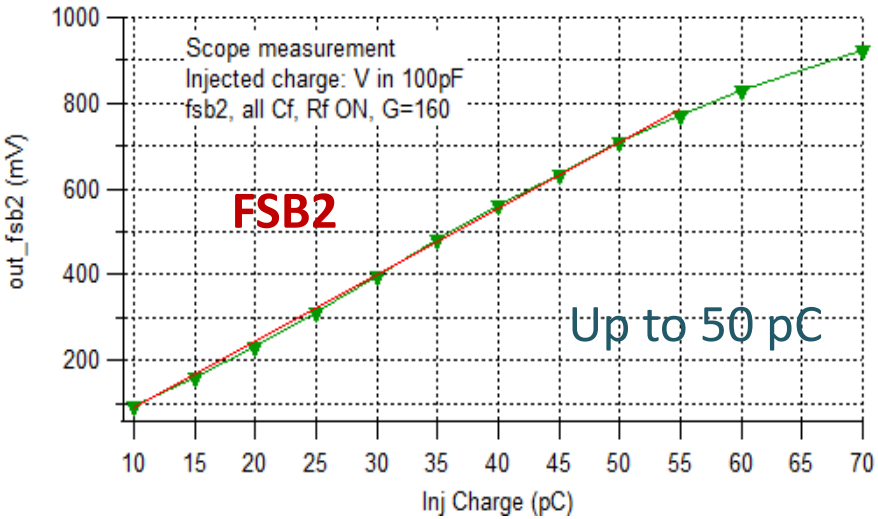


HR3: Analog linearity

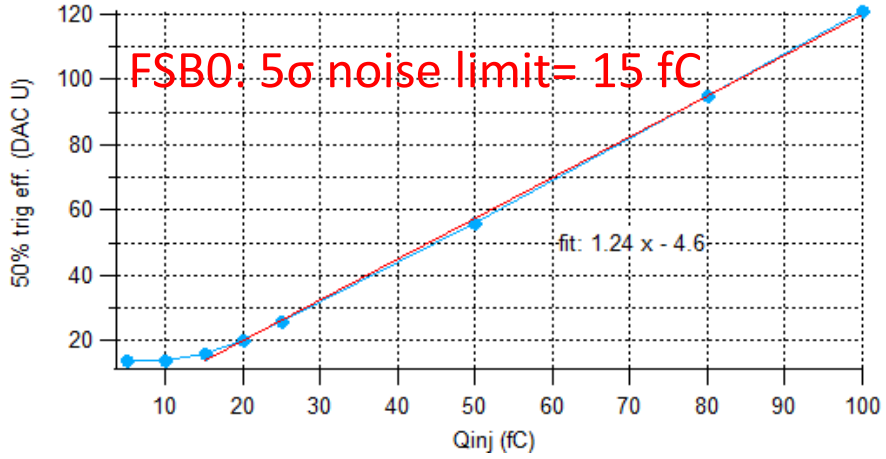
Fast shaper outputs (mV) vs Qinj (fC)







50% trig. Eff. (DAC units) vs Qinj (fC)



Dynamic range: 15fC - 50 pC

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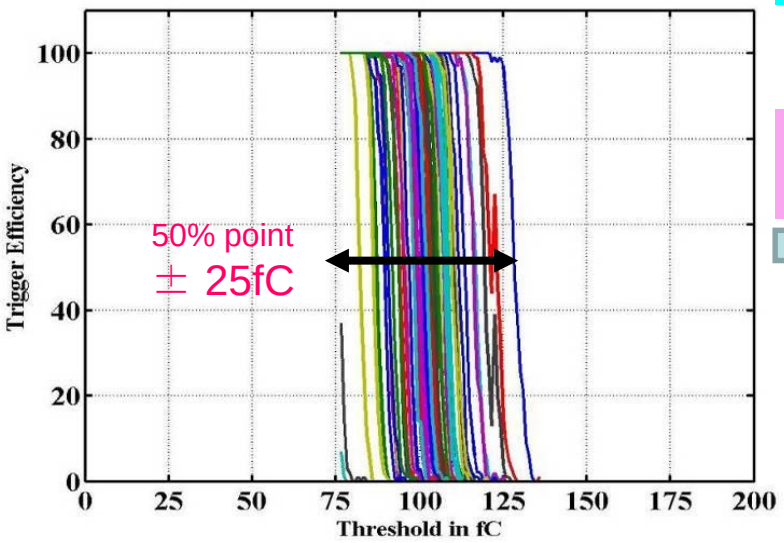
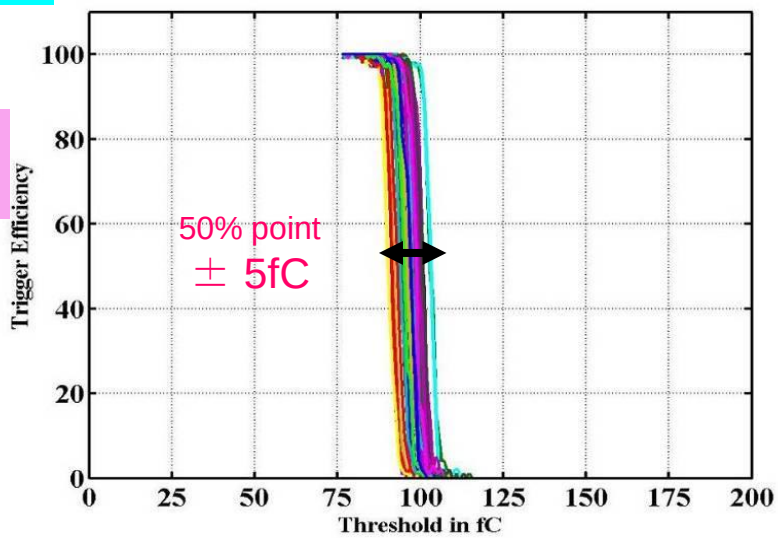
Gain correction / Scurves

Qinj=100fC



HR2 gain correction

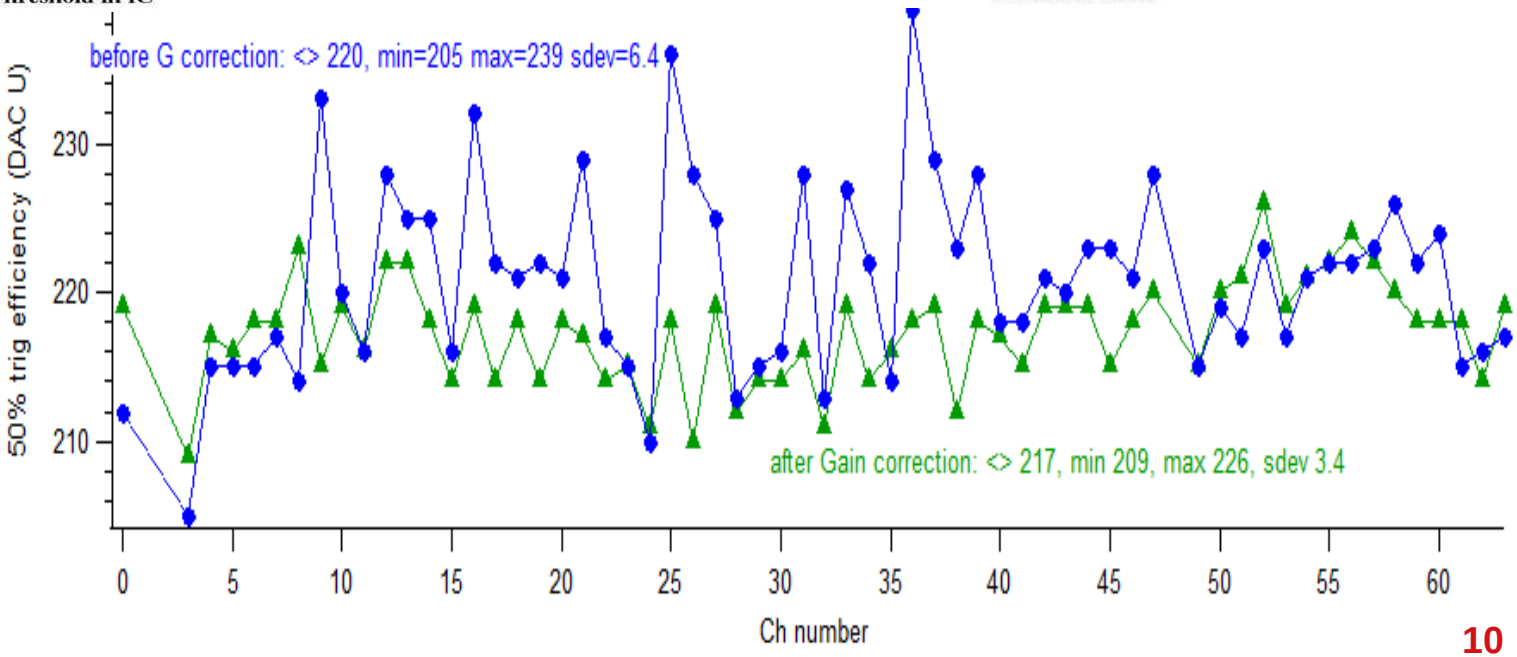


HR3: extracted 50% S-curves point vs Channel number

Before: ± 17 DACU

After: ± 8 DACU

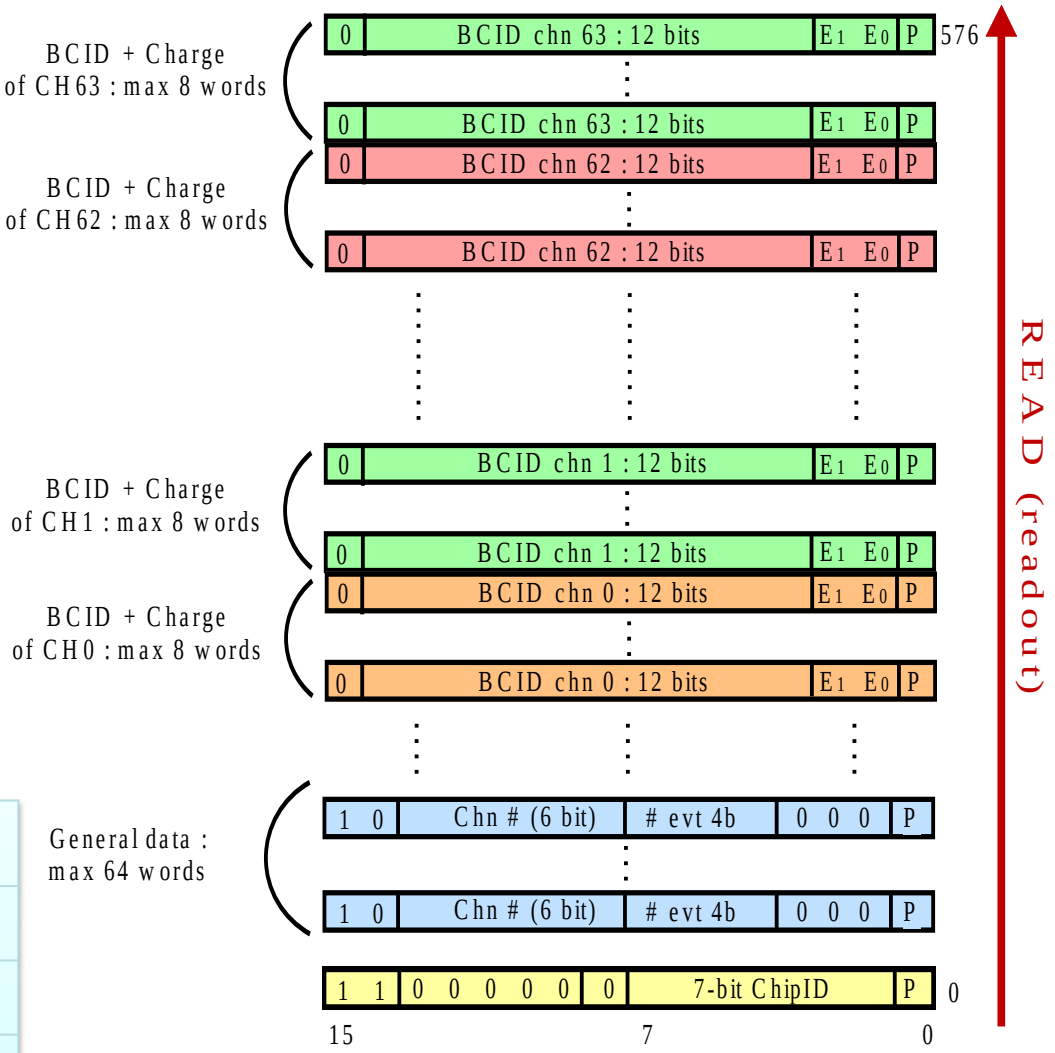
(± 6 fC)



Zero suppress: Memory mapping

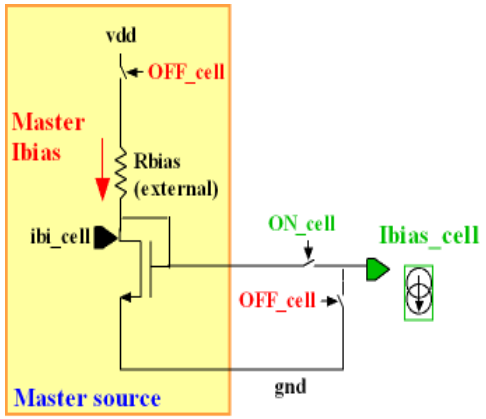
- Chip ID is the first to be outputted during readout (MSB first)
- MSB of each word indicates type of data:
  - "1": general data (Hit ch. number and number of events)
  - "0": BCID + encoded data
- A parity bit/word
- Up to 9232 bits (577x16) during readout
- Example of number of bits during readout:

	HR2	HR3
1 chn hit	160	48
8 chn hit	1280	272
4 chn hit @ same time	160	144
10 chn hit @ same time	160	336



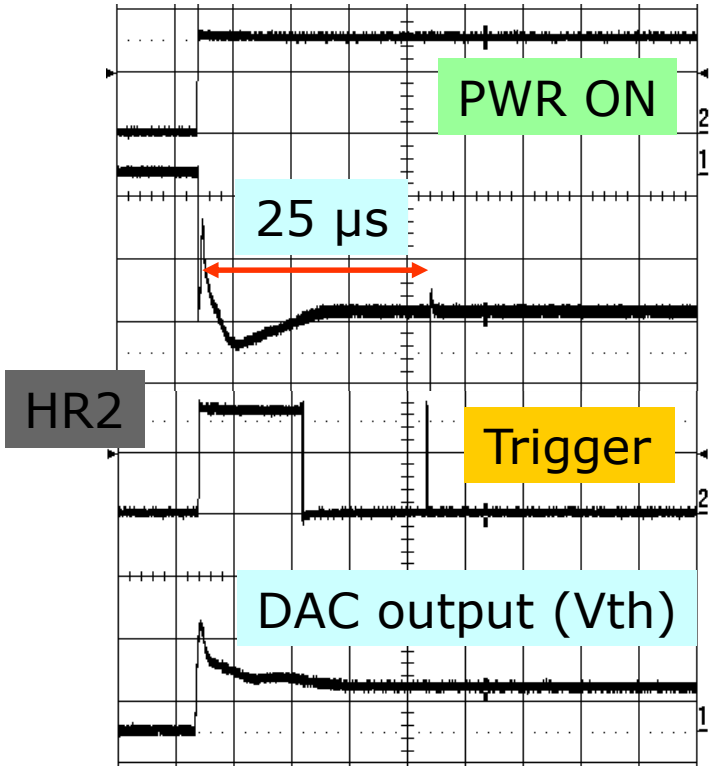
Power pulsing in HR chips

- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
  - No decoupling capacitance on bias and voltage references



- Compared to HR2, HR3 power consumption is higher due to:
  - The extended dynamic range (from 15pC to 50pC)
  - The integration of the zero suppress algorithm
- If the PLL is used, the power consumption is increased by 3% (due to the PLL VCO)

Power supply	HR3 with LVDS (5M + 40M) µW / channel	HR2 with LVDS (5M + 40M) µW / channel
PowerOnA (Analog)	1650	1325
Only PowerOnDAC	55	50
Only PowerOn D	725	50
Power-On-All	2430	1425
Power-On-All @ 0,5% duty cycle	**12,2**	**7,5**



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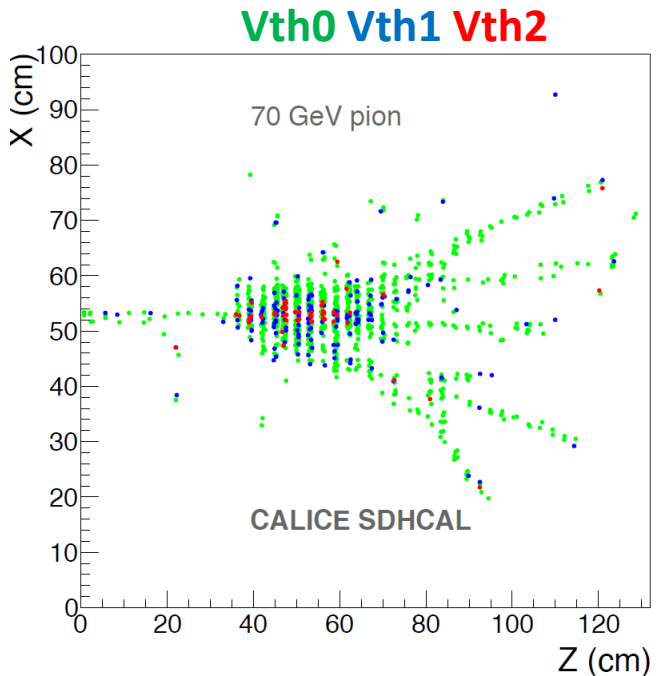
Power pulsing: Testbeam HR2

- SDHCAL technological proto with up to **50 layers** (7200 HR2 chips) built in 2010-2011.
  - High Granularity (PAD size : 1 cm x 1 cm)
- Scalable readout scheme successfully tested
- Complete system in TB with **460 000 channels**, **AUTOTRIGGER** mode and **power pulsing (5%)**

1m² RPC [IPNL] – 144 ASICS



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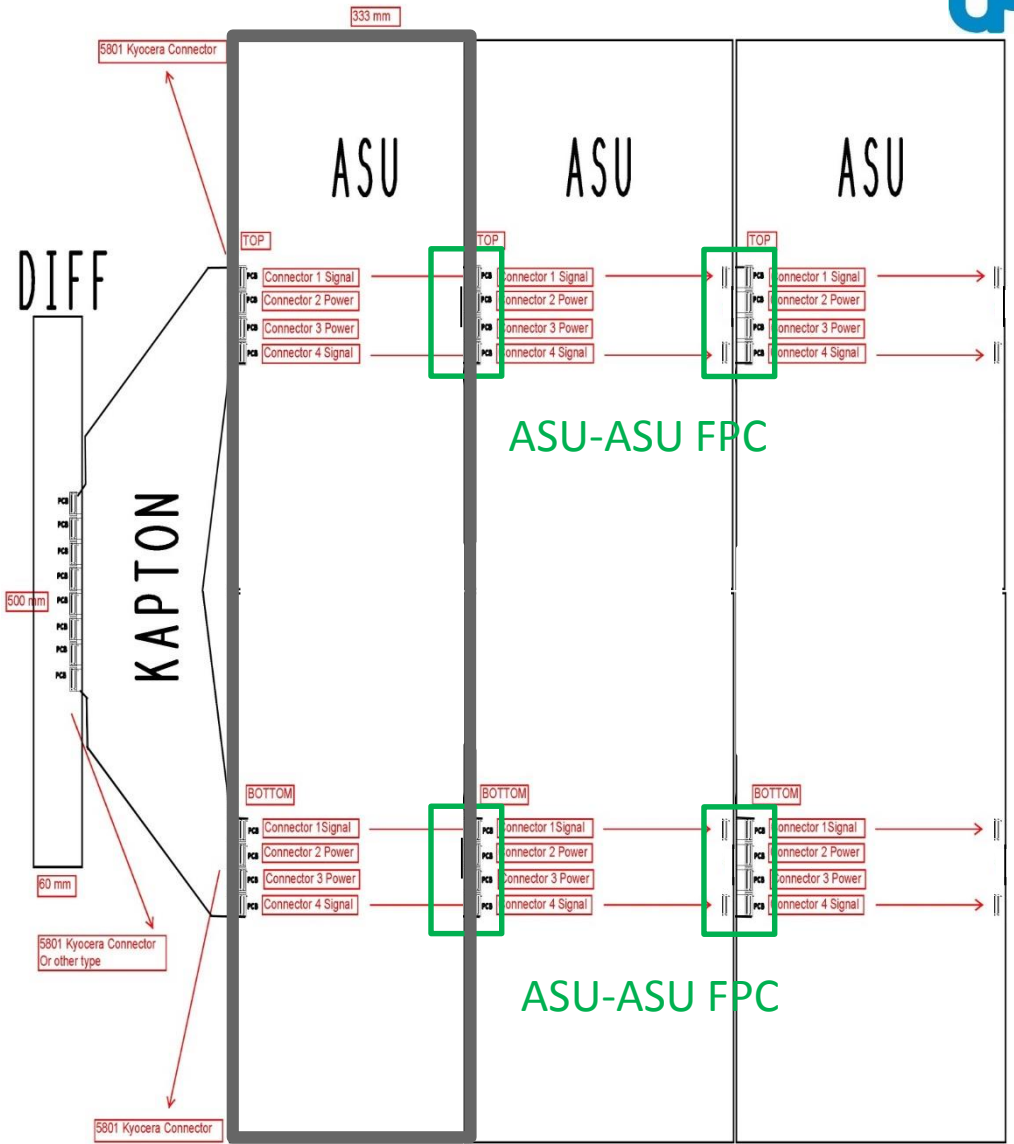
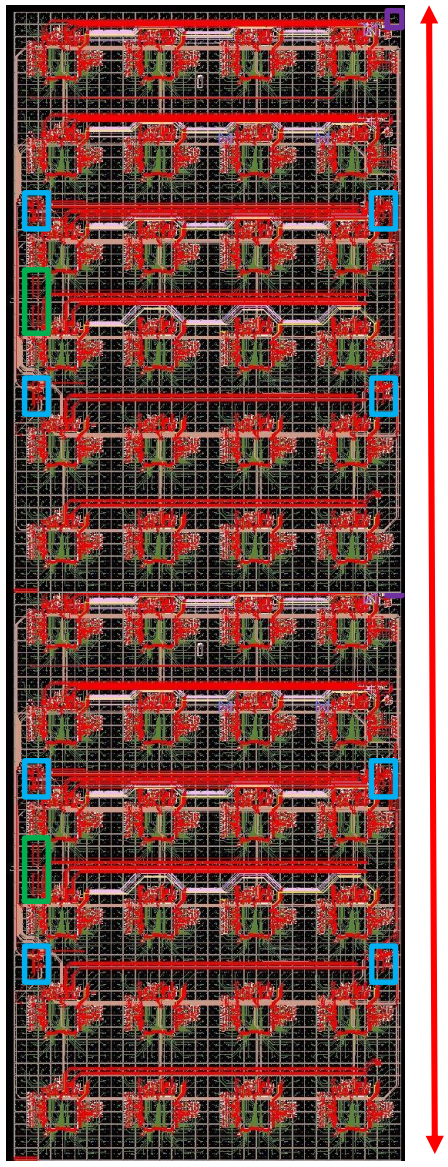
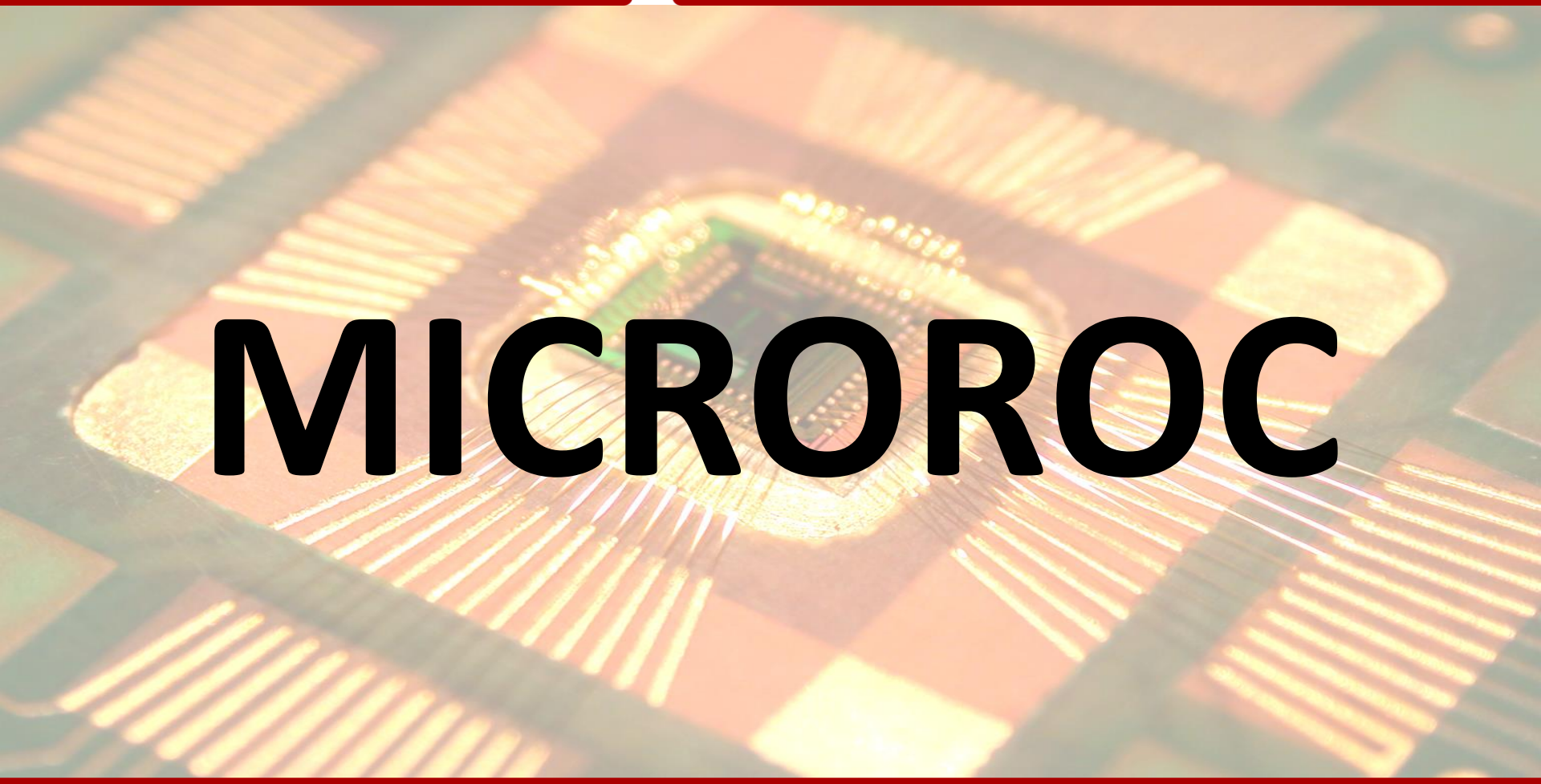
1 m² ASU architecture

- 1 ASU is 1m x 333mm composed with 48 HR3 chips
- Scalable up to 3 m²





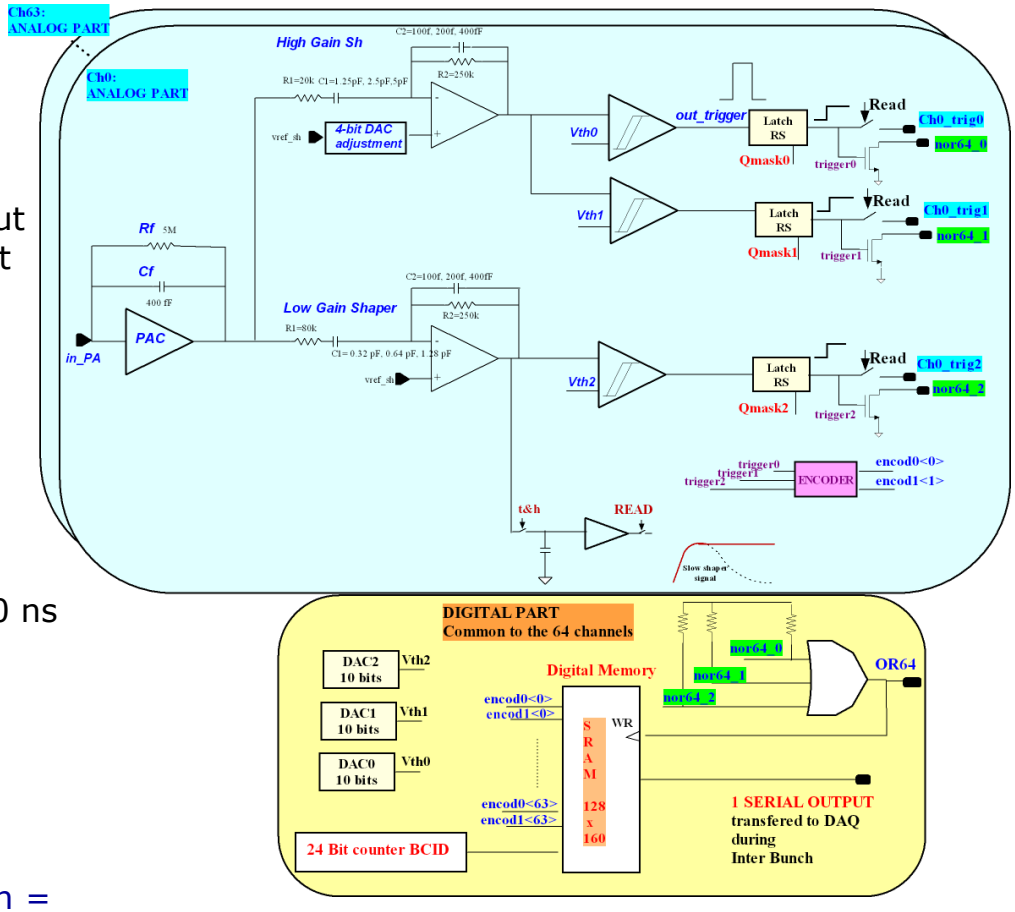


MICROROC

Organization for Micro-Electronics desiGn and Applications

MICROROC ~ HR2B

- Collaboration with LAPP Annecy
- 64 channels, 20 mm2
- Same as HARDROC but with charge preamp input stage + HV protection and slower shaping + 4bit DAC/channel
- Preamp optimized for Cd=80 pF, noise = 0.2 fC. Cf=0.4pF Rf=5M
- Maximum input charge : 500 fC
- Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
- 3 thresholds: Lowest threshold ~2 fC
- Pin to pin compatible with HR2
- Store all channels and BCID for every hit. Depth = 128 bits
- Data format : 128(depth)*[2bit*64ch+24bit(BCID)+8bit(Header)] = 20kbits
- **872 SC registers**, default config
- **Power pulsing**



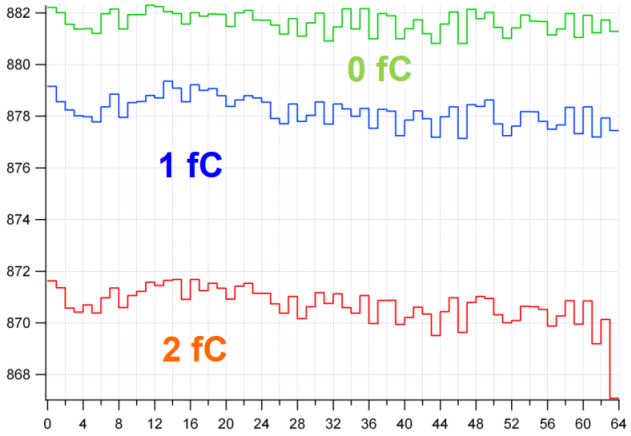
MICROROC

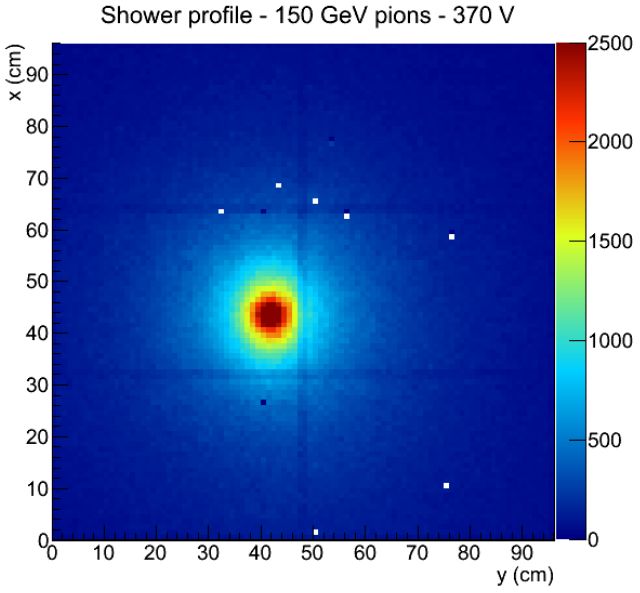
64 channels for µMegas (sDHCAL)

- Very similar to HARDROC except :
  - Input (charge) preamp
  - Slower shapers (100-150 ns)
  - HV Spark protections
- Noise: **0.2fC (Cd=80 pF). Auto trigger on 1fC** up to 500fC
- Pulsed power: **10 µW/ch** (0.5 % duty cycle)
- 4 Micromegas prototypes of 1x1 m2 were constructed in 2011-2012 and tested in particle beams inside the DHCAL steel structure in 2012

1m² Micromegas detector
Microroc : 10 000 channels

Very good performance of the electronics and detector (Threshold set to 1fC)





SKIROC2A

Organization for Micro-Electronics desiGn and Applications

SKIROC2 features

- Very low noise (0.4 fC = 2 500 e-) and very large dynamic range (2fC [½ MIP] up to 10 pC [2500 MIP]) charge preamplifier
  - With C*detector* = 20pF
  - PIN diode leakage current swallow capability (up to 10nA)

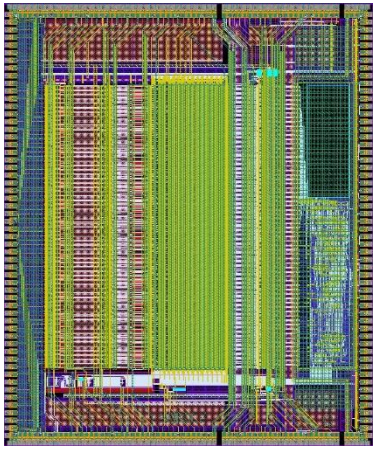
- 180ns shaping time Slow Shapers for Q measurement

  Antisaturation system in Gain 10 Slow Shaper

- 2-bit shaping time adjustable Fast Shaper (30 to 120ns)

  Antisaturation system in Fast Shaper

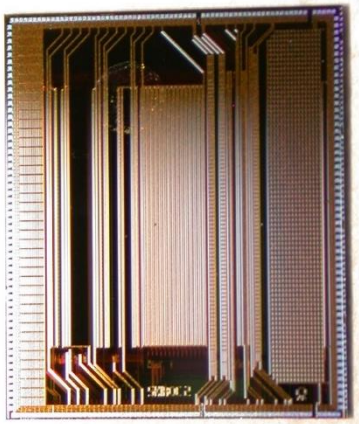
- 10-bit DAC for discriminator threshold
  - with 4-bit adjustment on each channel



- Analogue Memory depth : up to 15 events can be stored
- Trigger Discriminator for autotrigger on ½ MIP

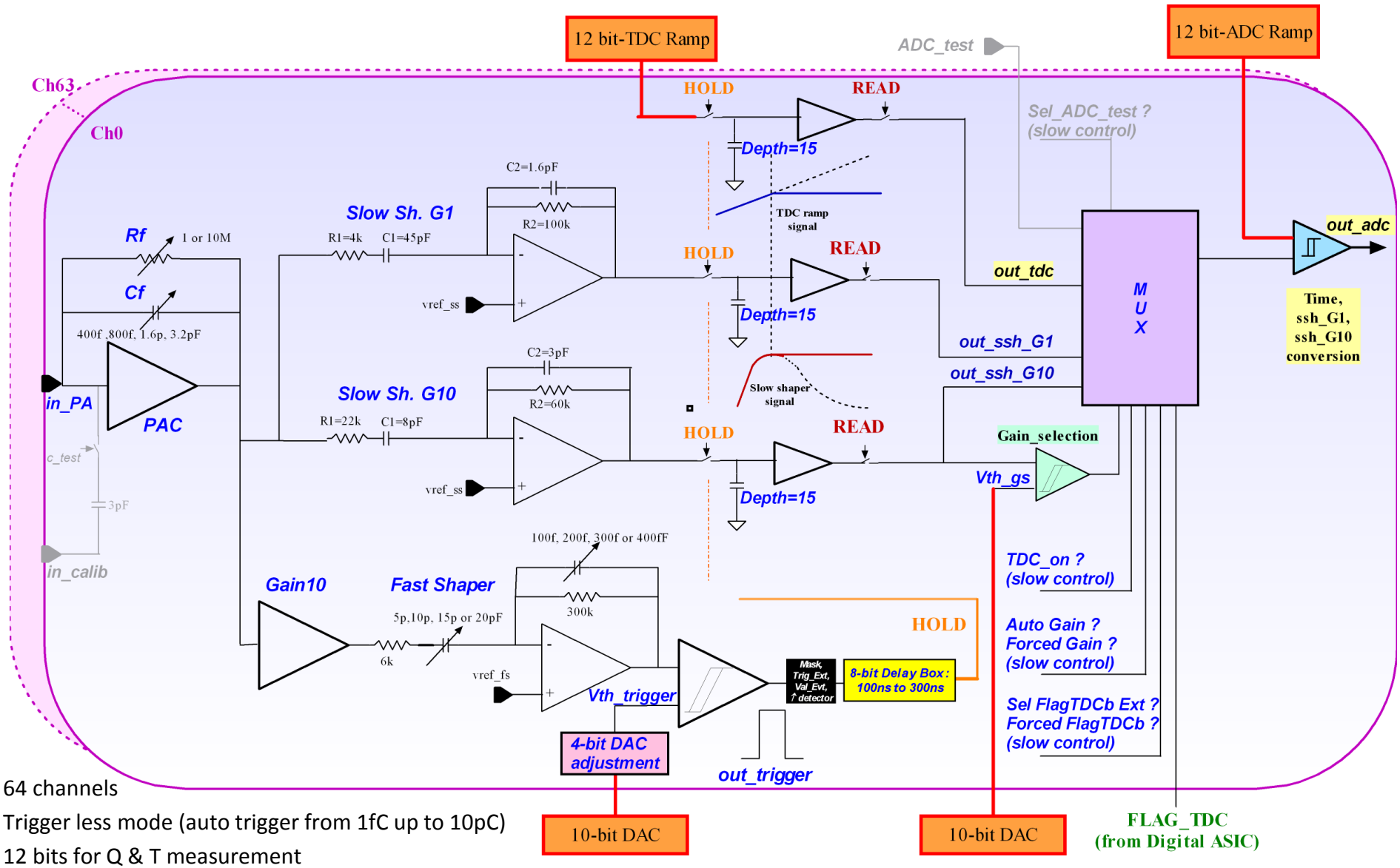
AMS 0.35 µm SiGe
7.5 mm x 8.7 mm

- 8-bit adjustable delay to position the Hold signal
- Digitization of either time and charge or of both charges
  - 12-bit Wilkinson ADC



Difficult layout:
1Mip=4fC, digital activity

SKIROC2A Analogue core



64 channels

Trigger less mode (auto trigger from 1fC up to 10pC)

12 bits for Q & T measurement

12 bits for coarse time (BCID)

Power pulsing mode

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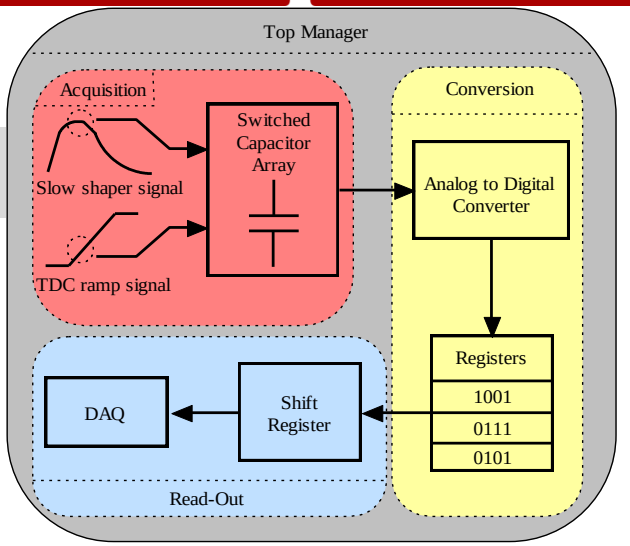
SKIROC2 digital features



SCA in SK2 and SP2

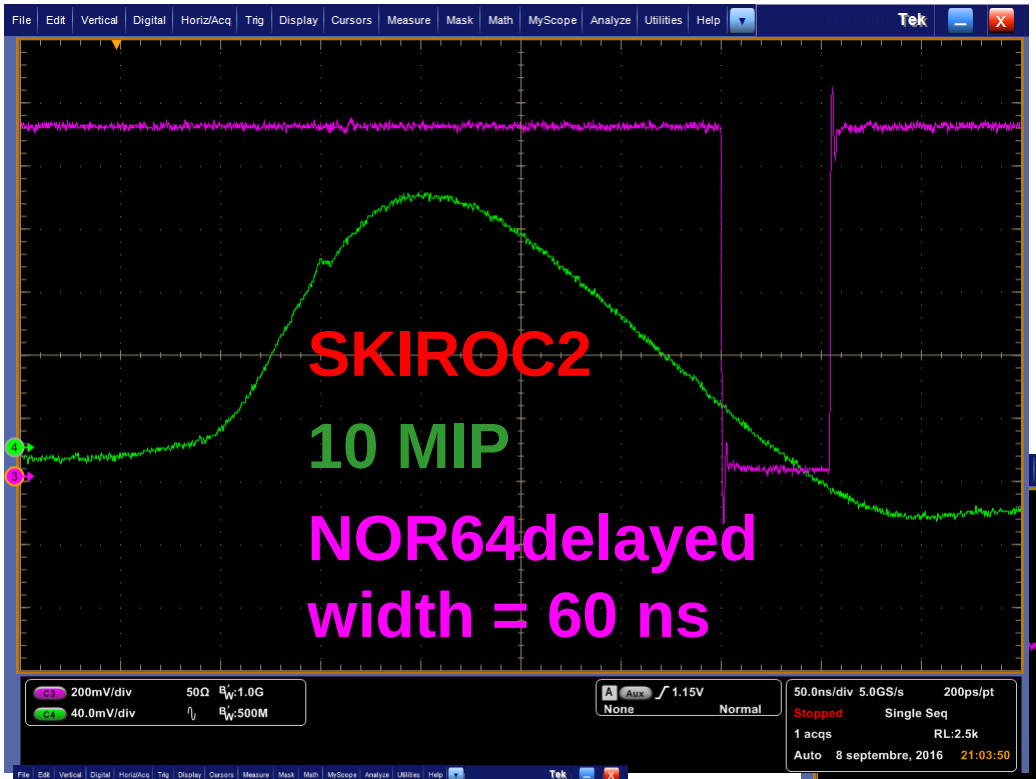
- Full Power Pulsing
  - 25 µW/ch => 24h operation of full slab with 2 AAA batteries !

- Common features with Hardroc & Spiroc
  (compatibility with any CALICE DAQ system)
  - Open Collector token-ring ReadOut
  - Redundancy on Data Out & Transmit On signal lines
  - 2 switchable StartReadOut Inputs & EndReadOut Outputs :
    - to prevent chip failure

- Slow Control (versatility) + Probe System (debug)
  - Multiplexed Slow Control & Probe

- Very Complex Digital Part (~10% of the Die)
  - Manage Acquisition, Conversion, 15 SCA control, RAM, I/Os…

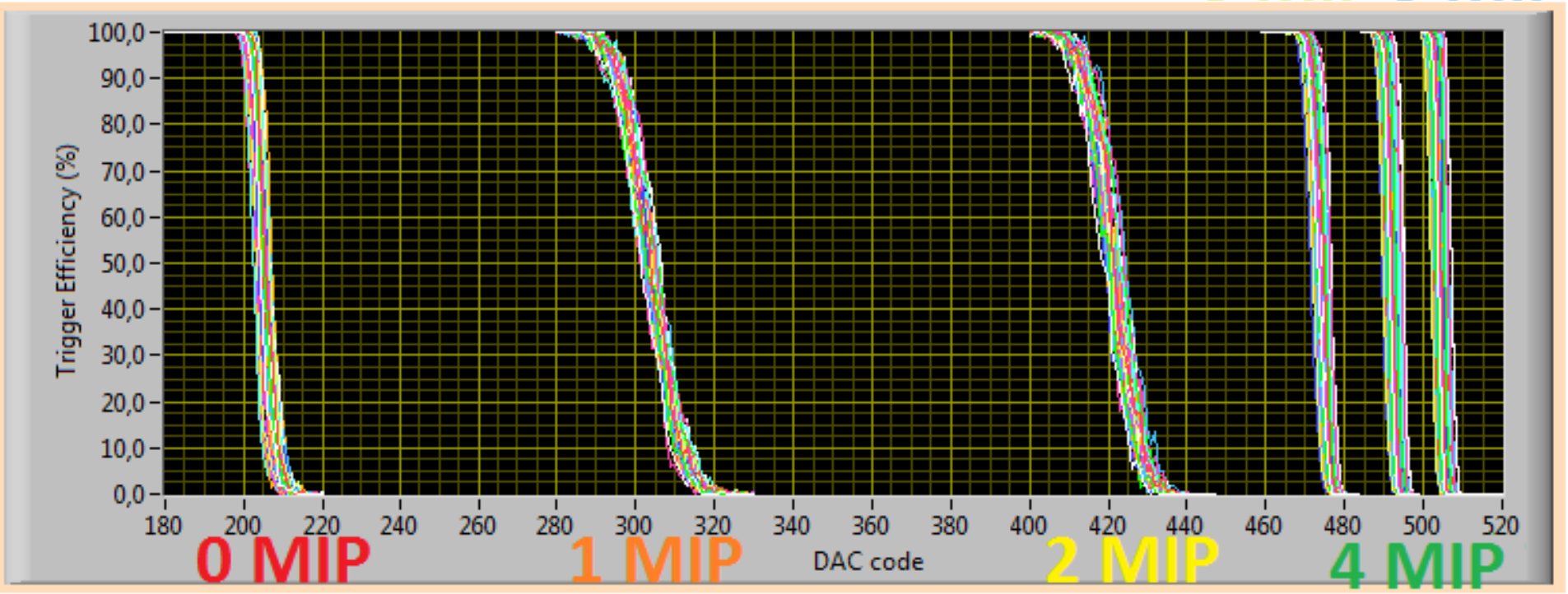
SKIROC2A : NOR64_delayed



SKIROC2A : S-Curves (trigger efficiency)

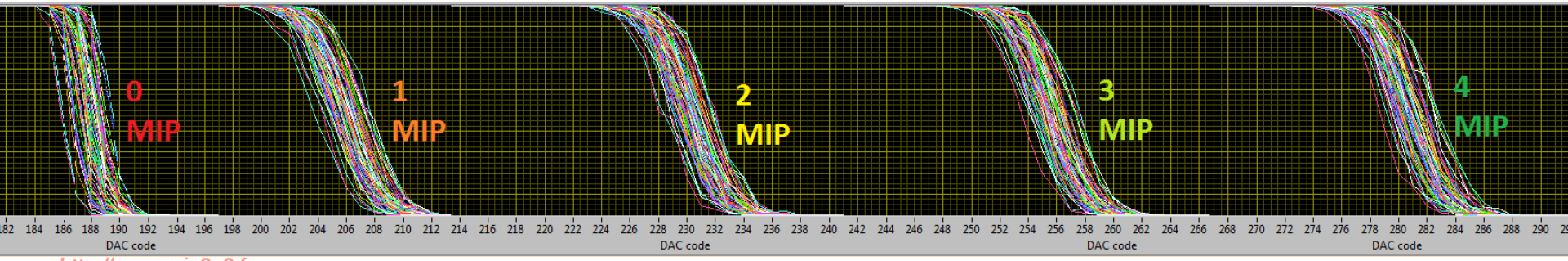
PA Gain = 1.2pF

3 MIP 5 MIP



S/N > 9

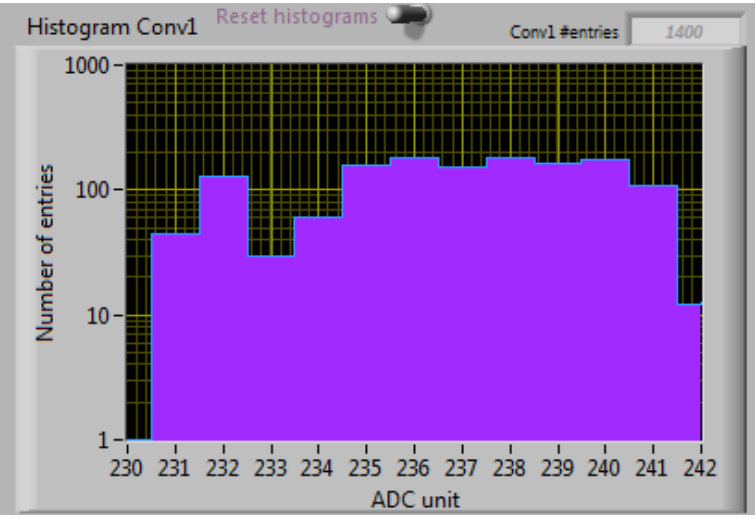
PA Gain = 6 pF



SKIROC2A : histogram

PA Gain @ 6pF

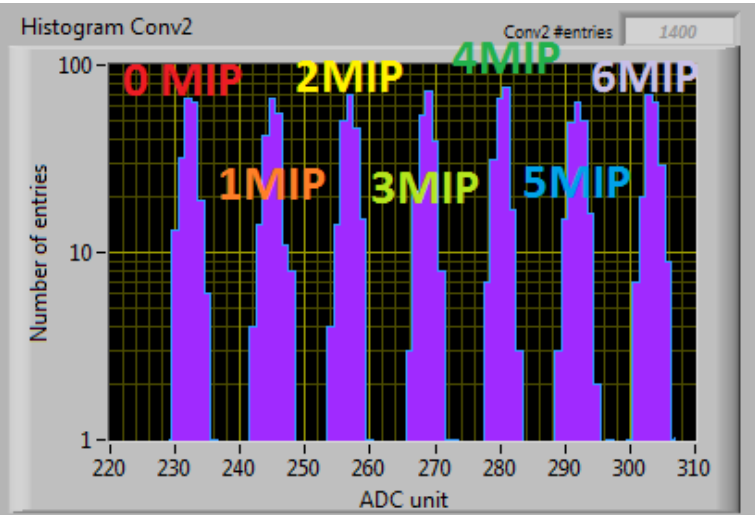
S/N > 10



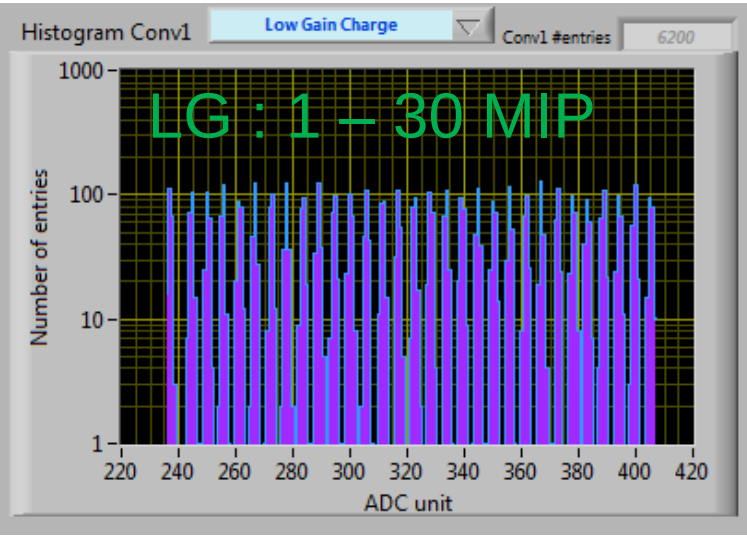
Data to analyze limits :

Cut max Conv1	Cut max Conv2
4095	4095
Cut min Conv1	**Cut min Conv2**
1	1

Conv1 max	Conv2 max
242	307
Conv1 min	**Conv2 min**
230	229
Conv1 mean	**Conv2 mean**
236,868	268,35
Conv1 sigma	**Conv2 sigma**
2,82091	23,7005



PA Gain @ 1.2pF

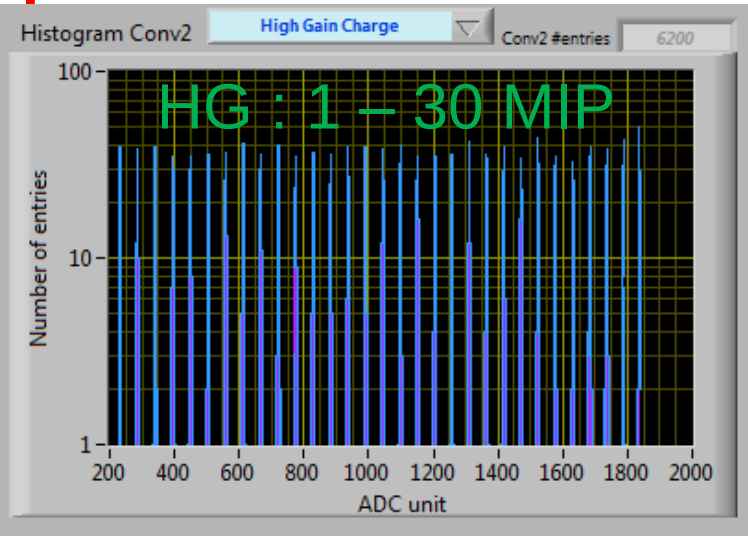


Reset histograms

Data to analyze limits :

Cut max Conv1	Cut max Conv2
4095	4095
Cut min Conv1	**Cut min Conv2**
0	0

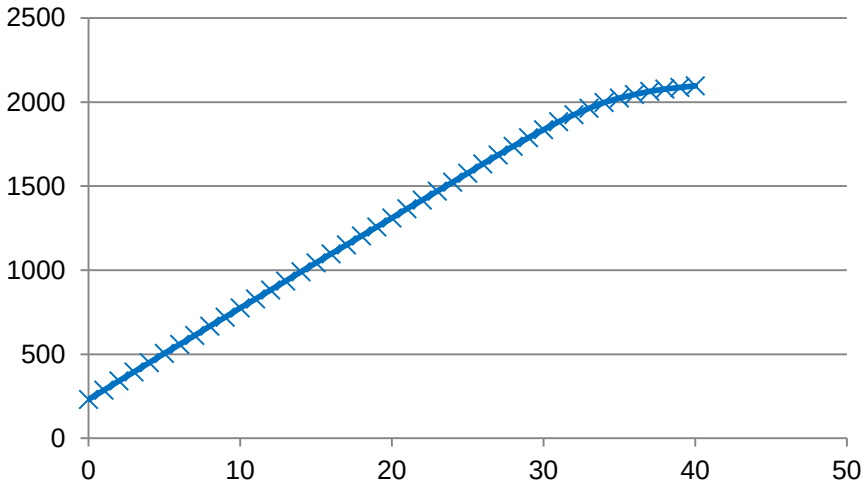
Conv1 max	Conv2 max
407	1842
Conv1 min	**Conv2 min**
236	227
Conv1 mean	**Conv2 mean**
322,456	1041,3
Conv1 sigma	**Conv2 sigma**
49,7609	479,782



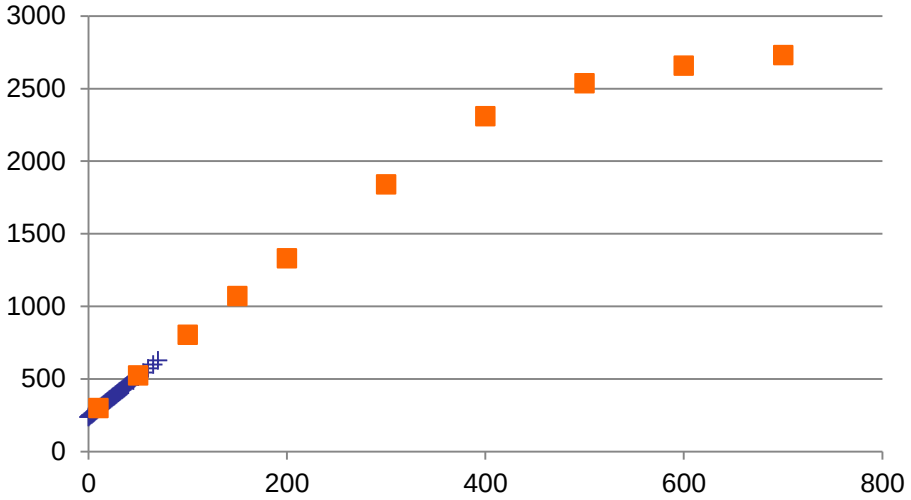
SKIROC2A Linearity

PA Gain @ 1.2pF

HG

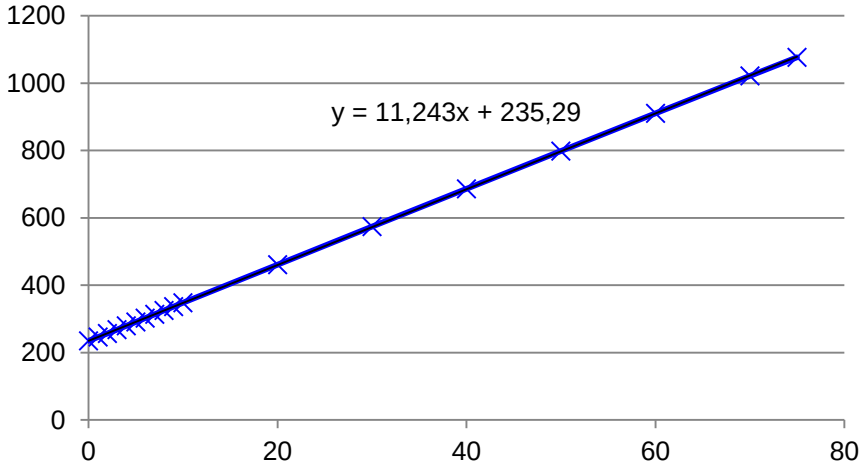


LG

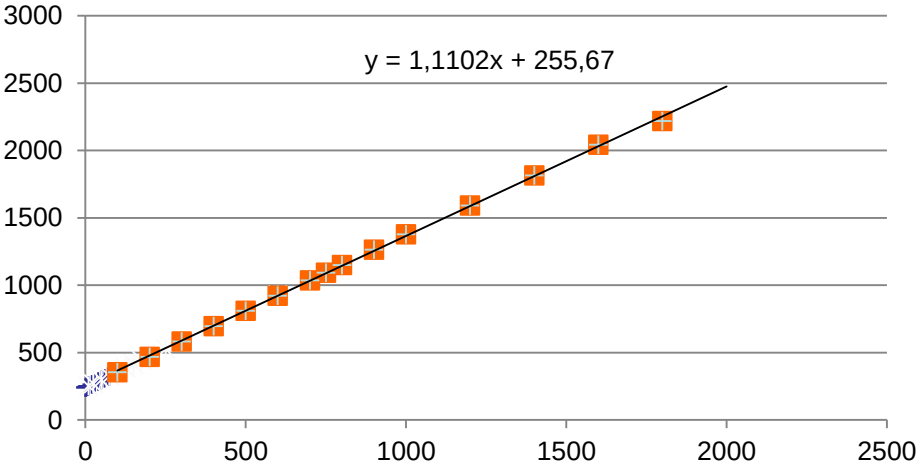


PA Gain @ 6pF (ILC request)

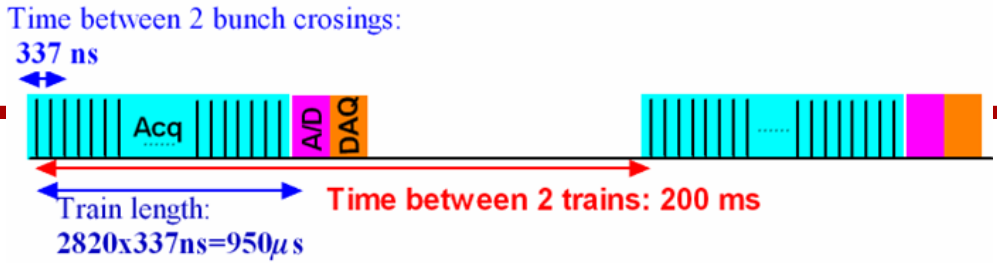
HG



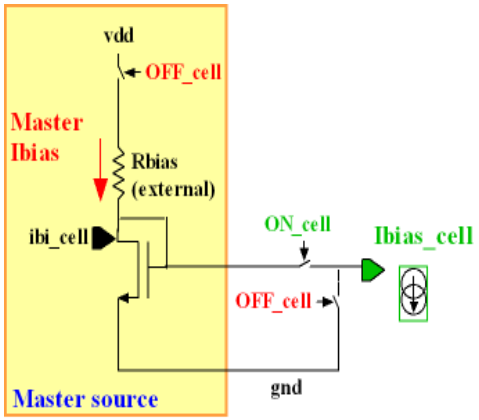
LG



POWER PULSING in SK2



- **Requirement:**
  - **25 µW/ch with 0.5% duty cycle**
  - **500 µA for the entire chip**



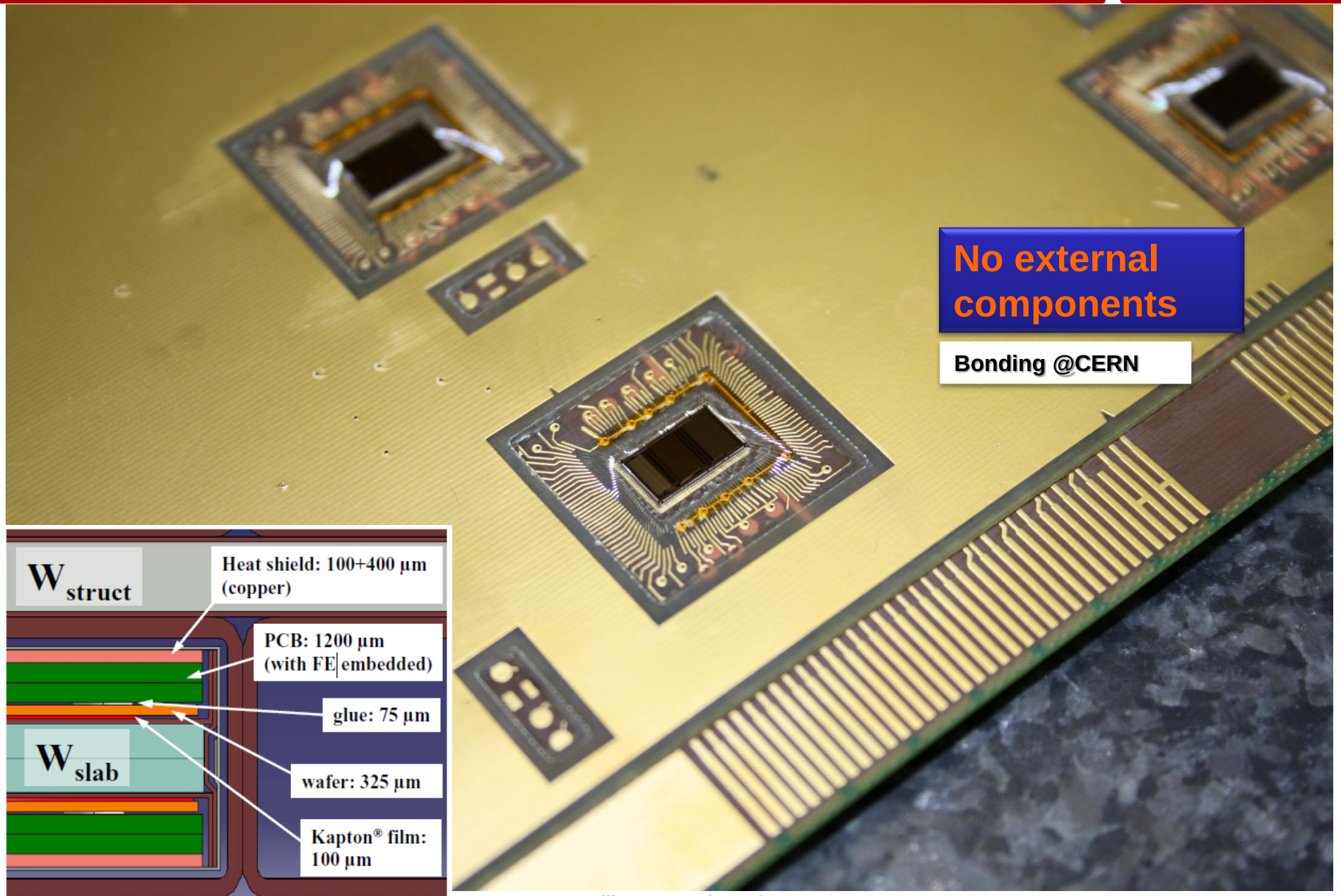
- **Power pulsing:**
  - Bandgap + ref Voltages + master I: switched ON/OFF
  - **Shut down bias currents with vdd always ON**
- **SK2 power consumption measurement:**
  - 123 mA x 3.3V ≈ 40 mW => **0.6 mW/ch**

- **4 Power pulsing lines** : analog, conversion, dac, digital
- Each chip can be forced **on/off by slow control**

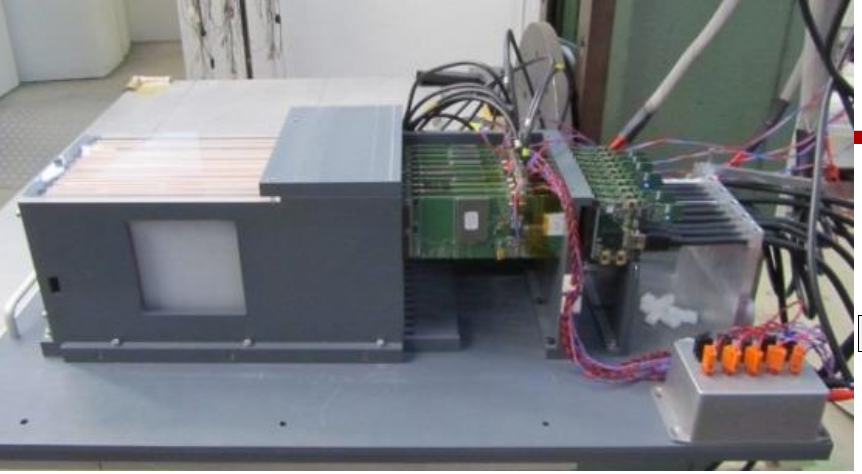
Measurements		
Acquisition	88 mA , 290 mW	Duty Cycle =0.5%, 1.45 mW
Conversion	27.3 mA, 90 mW	Duty Cycle =0.25%, 0.225 mW
Readout	8.0 mA, 26.4 mW	Duty Cycle =0.25%, 0.066 mW

Skiroc2 power consumption with Power pulsing: 1.7 mW ie 27 µW/ch

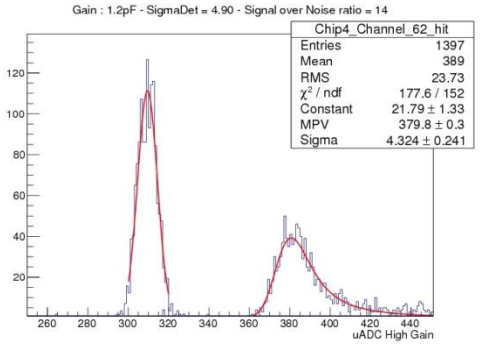
FEV board : Front End Board



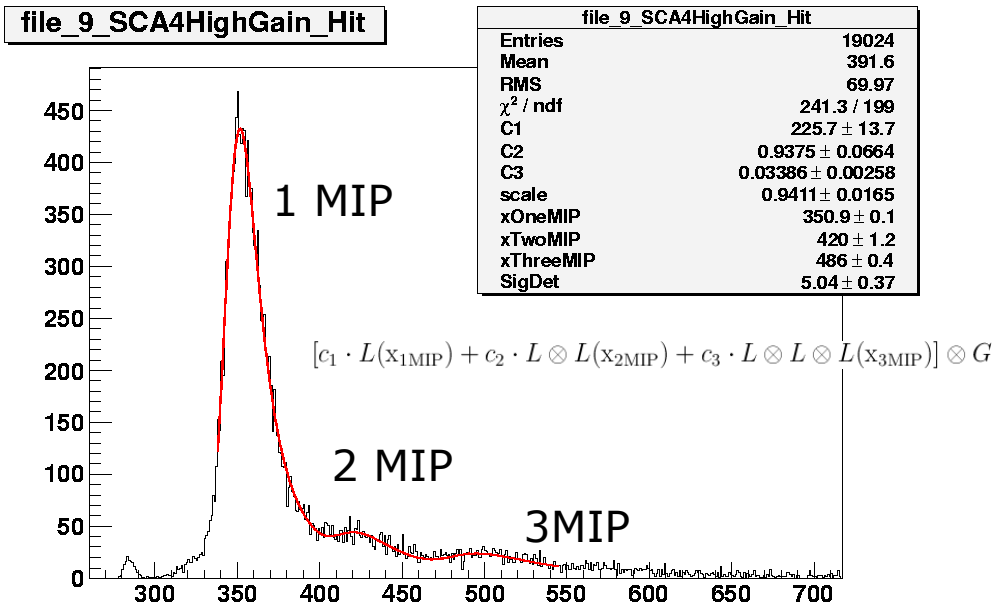
Skiroc2 in Test Beam

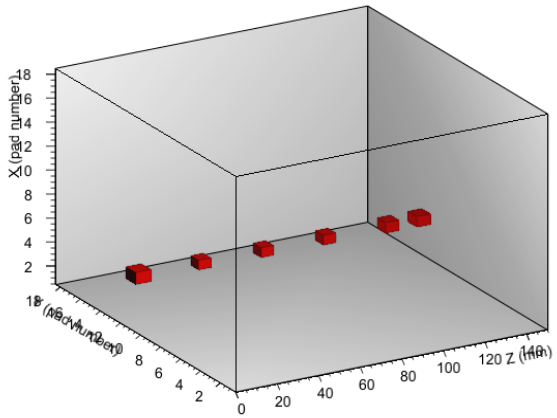


- Fit of the energy distribution (without W): expected result (physics studies)

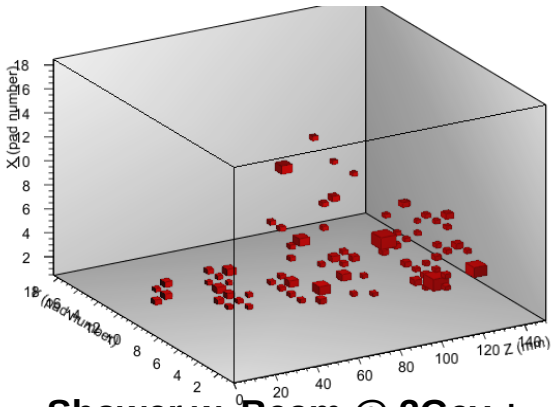


Pedestal 1 MIP

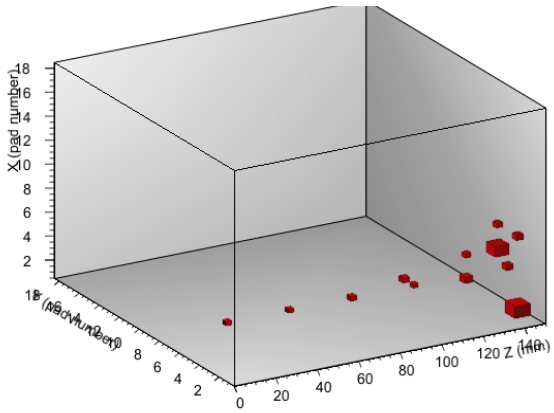




1 MIP (Beam without W)



Shower w. Beam @ 3Gev + 3x$_0$ W + W enclosed



Shower w. Beam @ 1Gev + W enclosed

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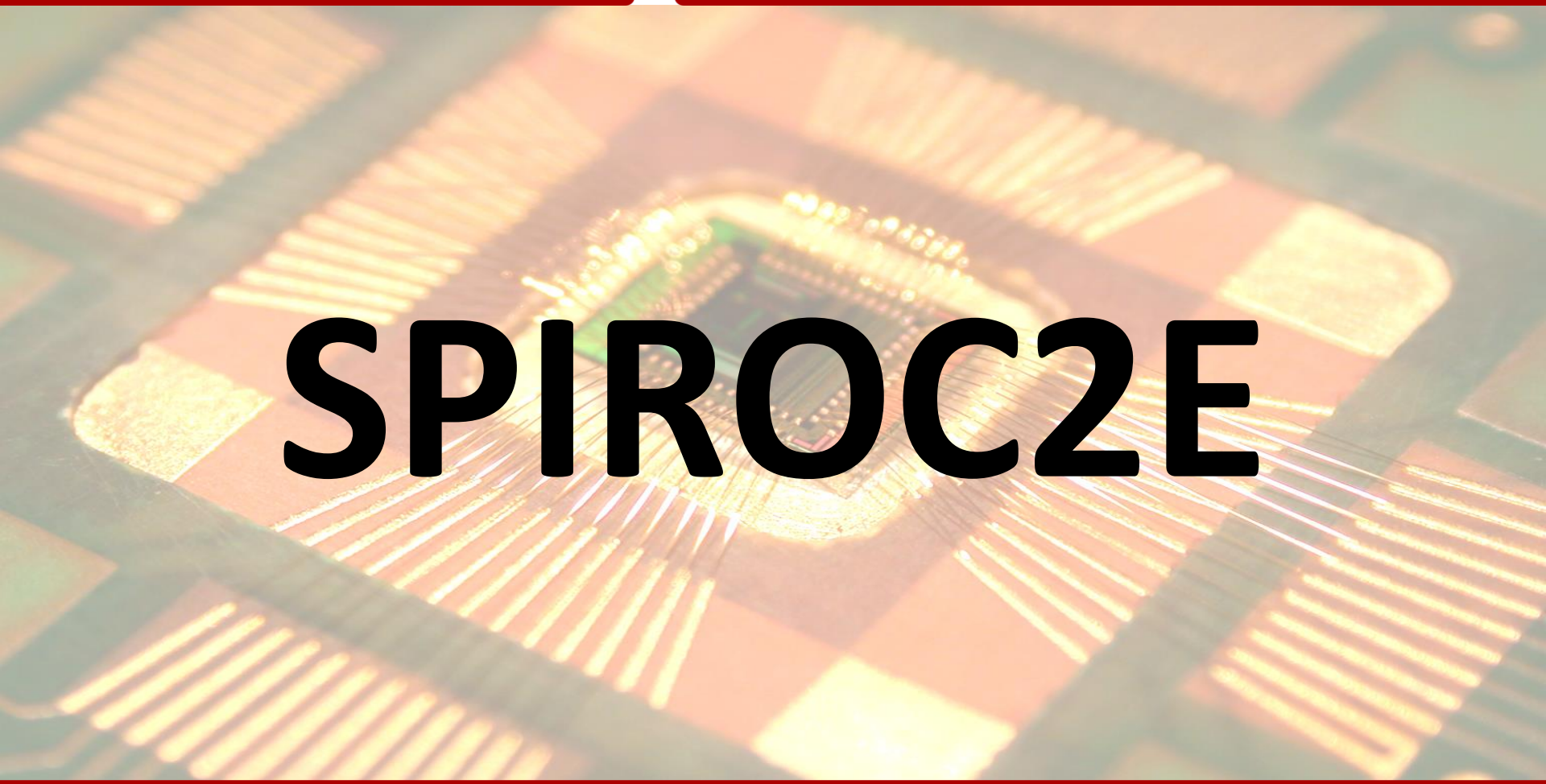
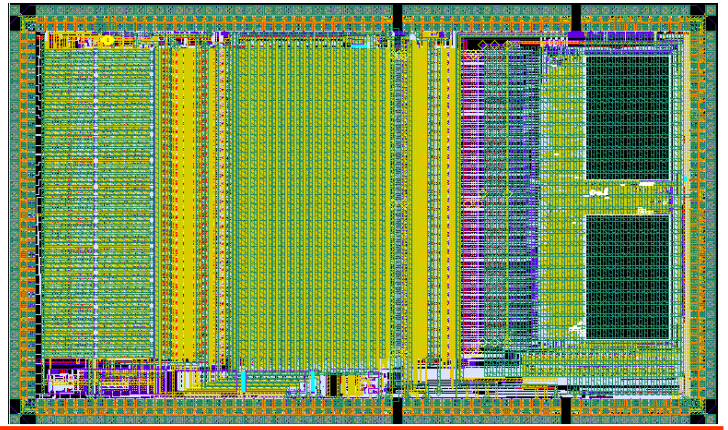


SPIROC2E

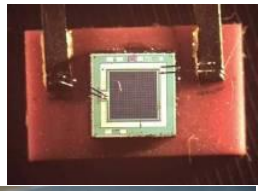
Organization for Micro-Electronics desiGn and Applications

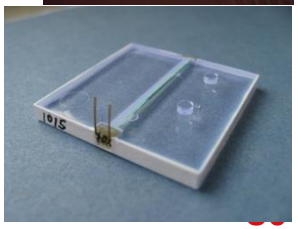
SPIROC main features

- 36-Channel ASIC
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 15 bits
  - 2 gains (1-10) + 12 bit ADC 1 pe → 2000 pe
  - Variable shaping time from 25ns to 175ns
  - pe/noise ratio : 11
- Auto-trigger on MIP or spe
  - pe/noise ratio on trigger channel : 24
  - Fast shaper : ~10ns
  - Auto-Trigger on 1/3 pe (50fC)
- Time measurement :
  - 12-bit Bunch Crossing ID (coarse time measurement)
  - 12-bit TDC step~100 ps (fine time measurement)
- Analog memory for time and charge measurement: depth = 16
- Low consumption : ~25µW per channel (in power pulsing mode)
- Individually addressable calibration injection capacitance
- Embedded features (bandgap, 10-bit DAC, etc.)
- Multiplexed analog output for physics prototype DAQ
- 4k internal memory and daisy chain readout



Fabricated in SiGe AMS 0.35 µm
Chip area: 30 mm² (4.4mm × 7.4mm)





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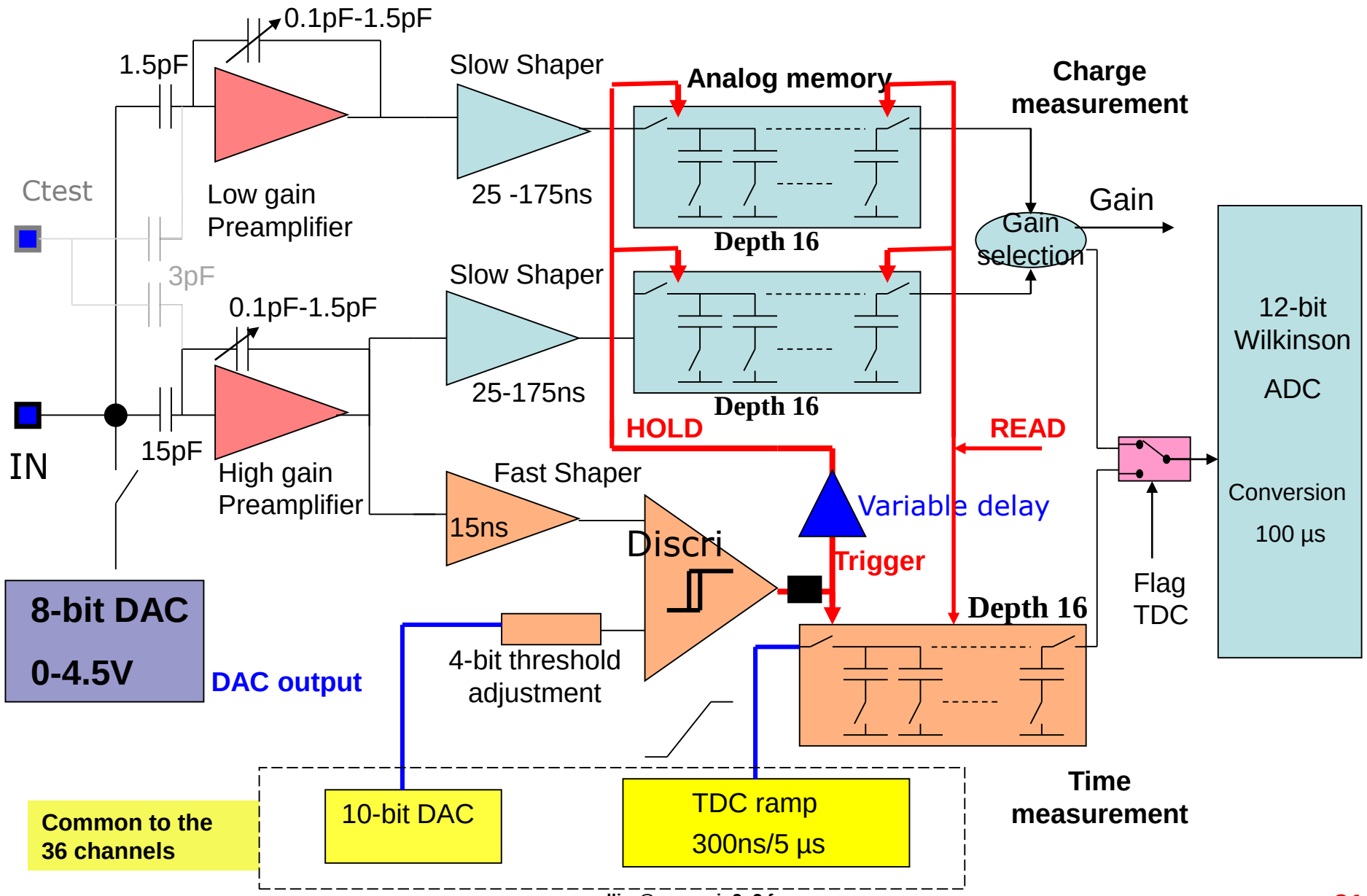
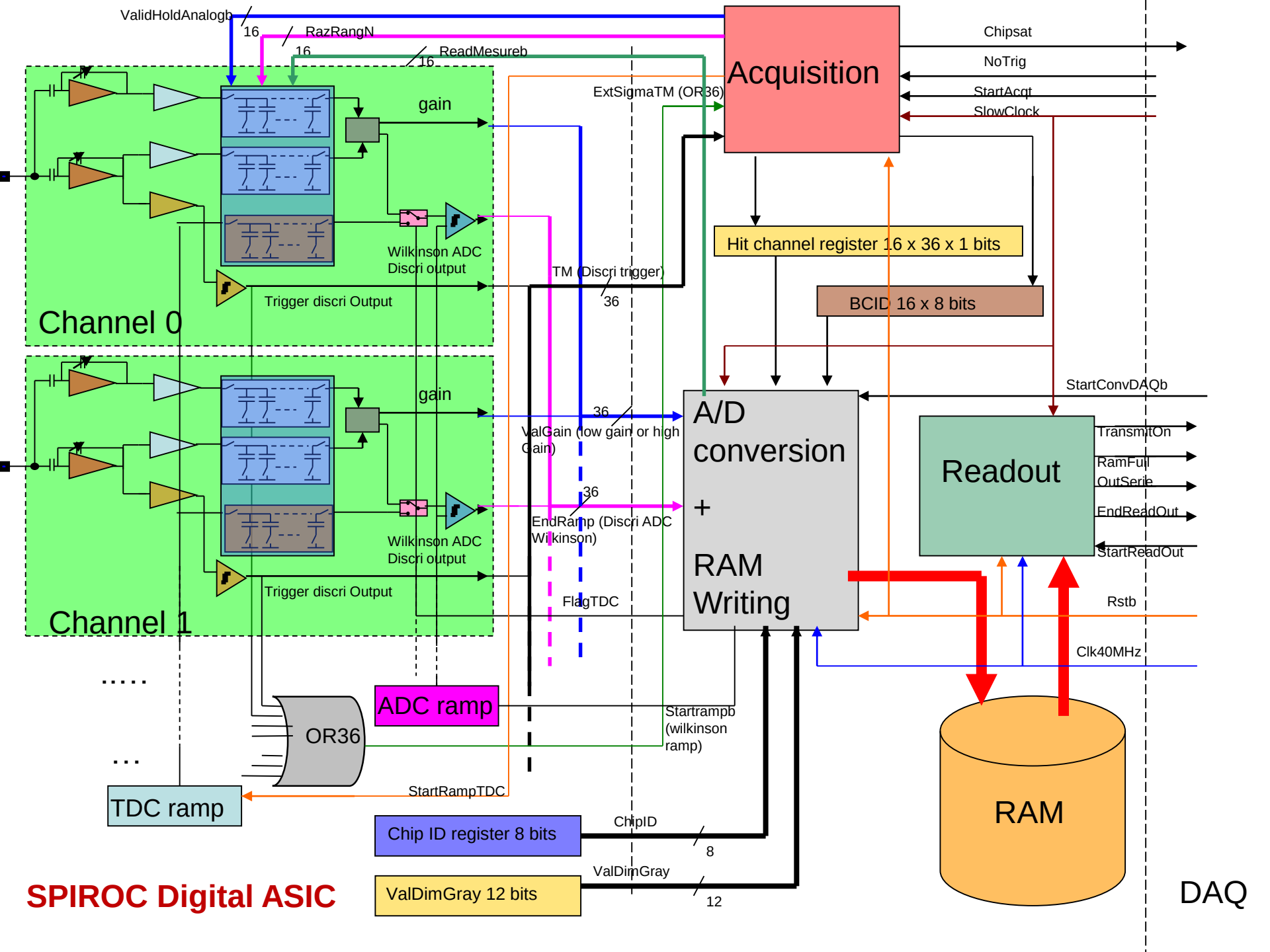
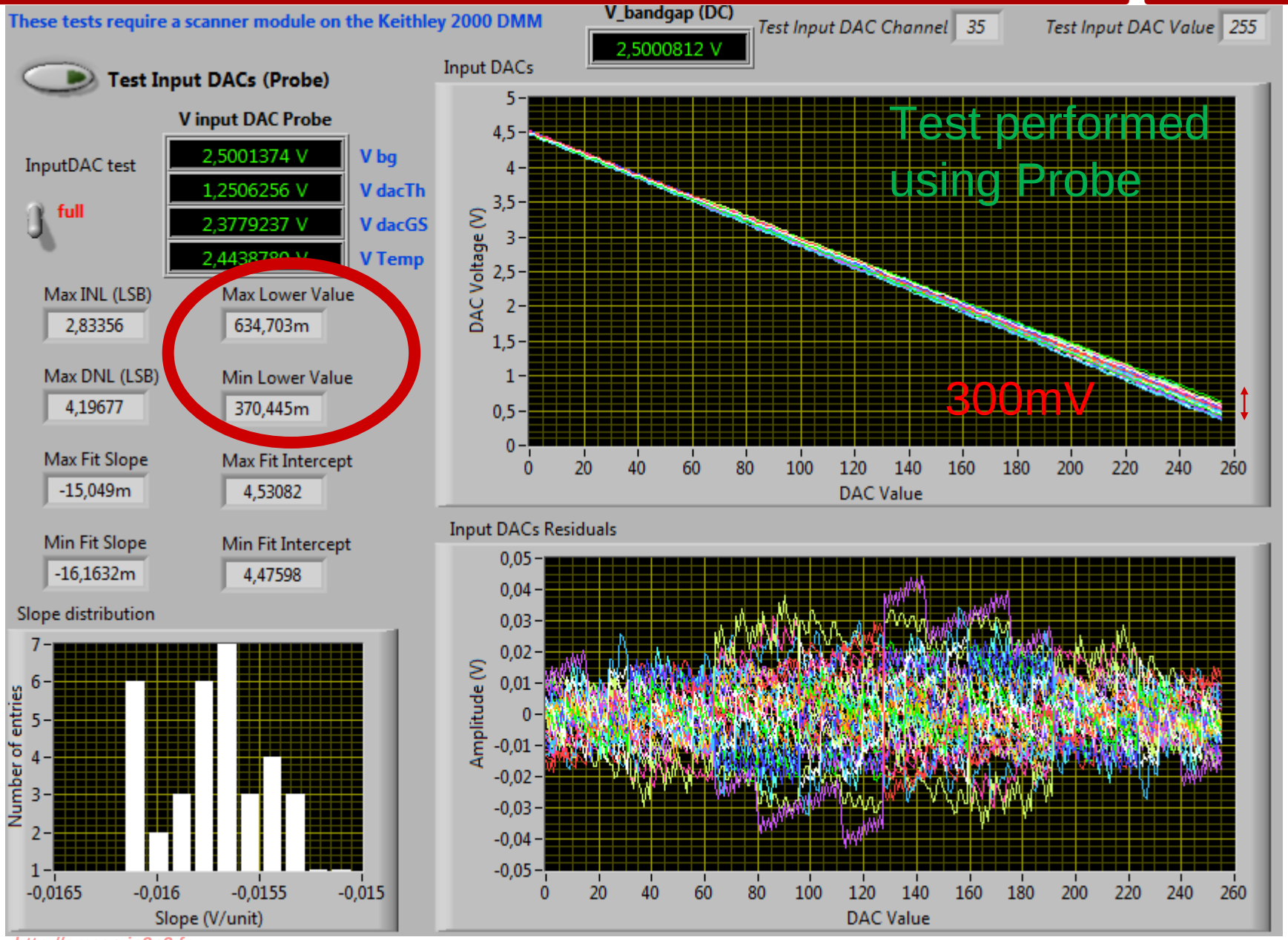
SPIROC : One channel schematic

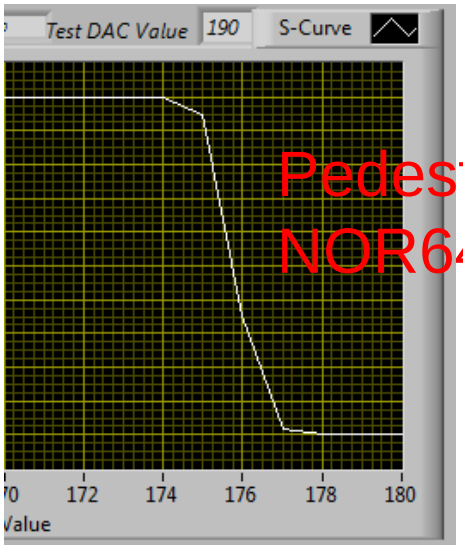



ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
Hit channel register 16 x 36 x 1 bits
TM (Discri trigger)
36
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or high Gain)
36
EndRamp (Discri ADC Wilkinson)
FlagTDC
A/D conversion + RAM Writing
StartConvDAQb
Readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb (wilkinson ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray 12 bits
ValDimGray
12
RAM
SPIROC Digital ASIC
DAQ

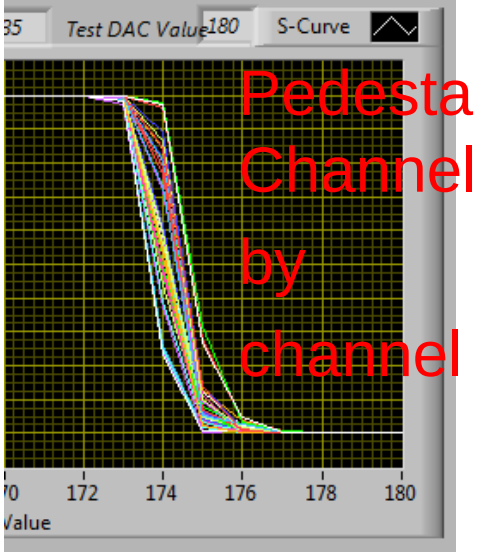
SPIROC2E : Input DACs



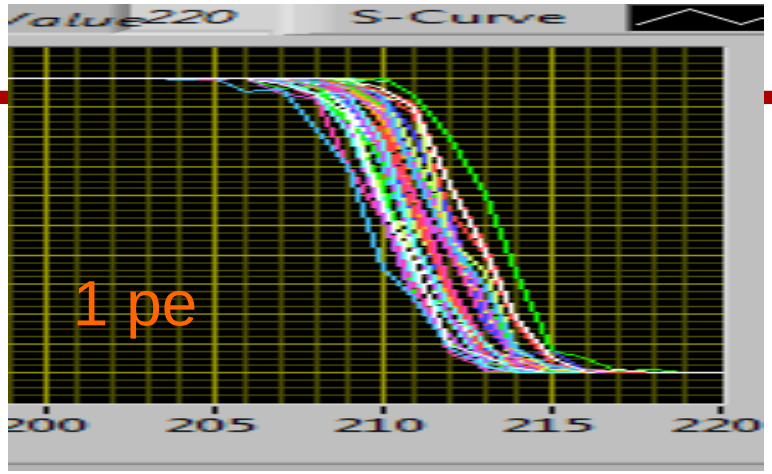
SPIROC2E : S-curves

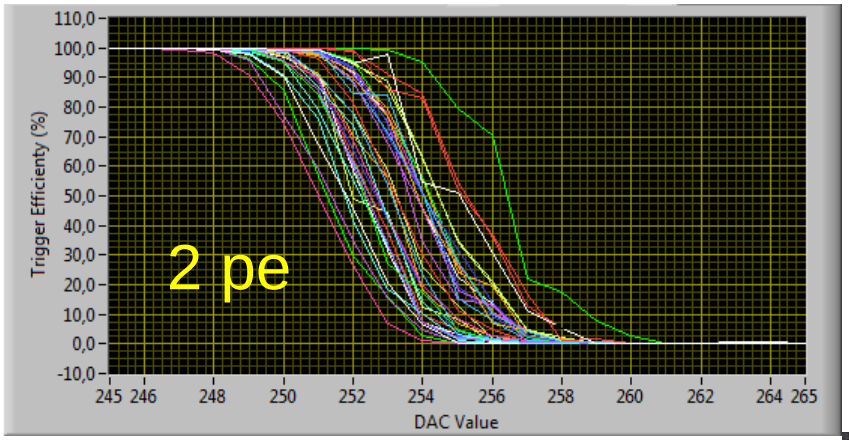


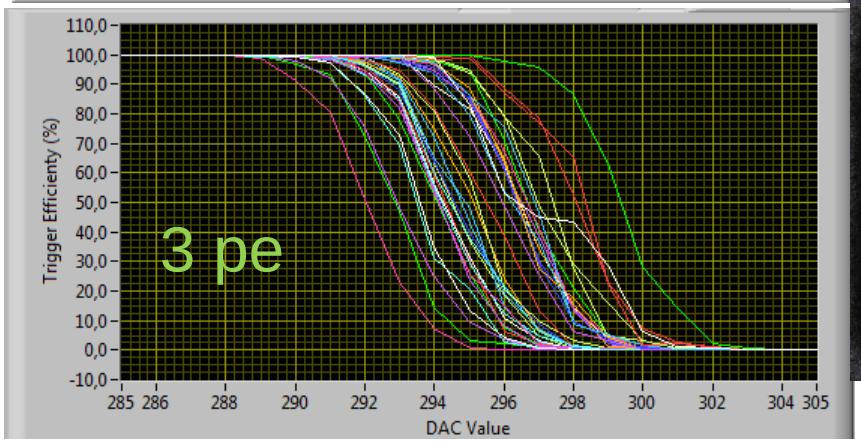
Pedestal NOR64



Pedestal Channel by channel







PA :

Cf = 200fF

50% trigger efficiency :

41 DACu / pe-

1 HBU : 36 cm x 36 cm
4 Spiroc2 , 144 SiPMs

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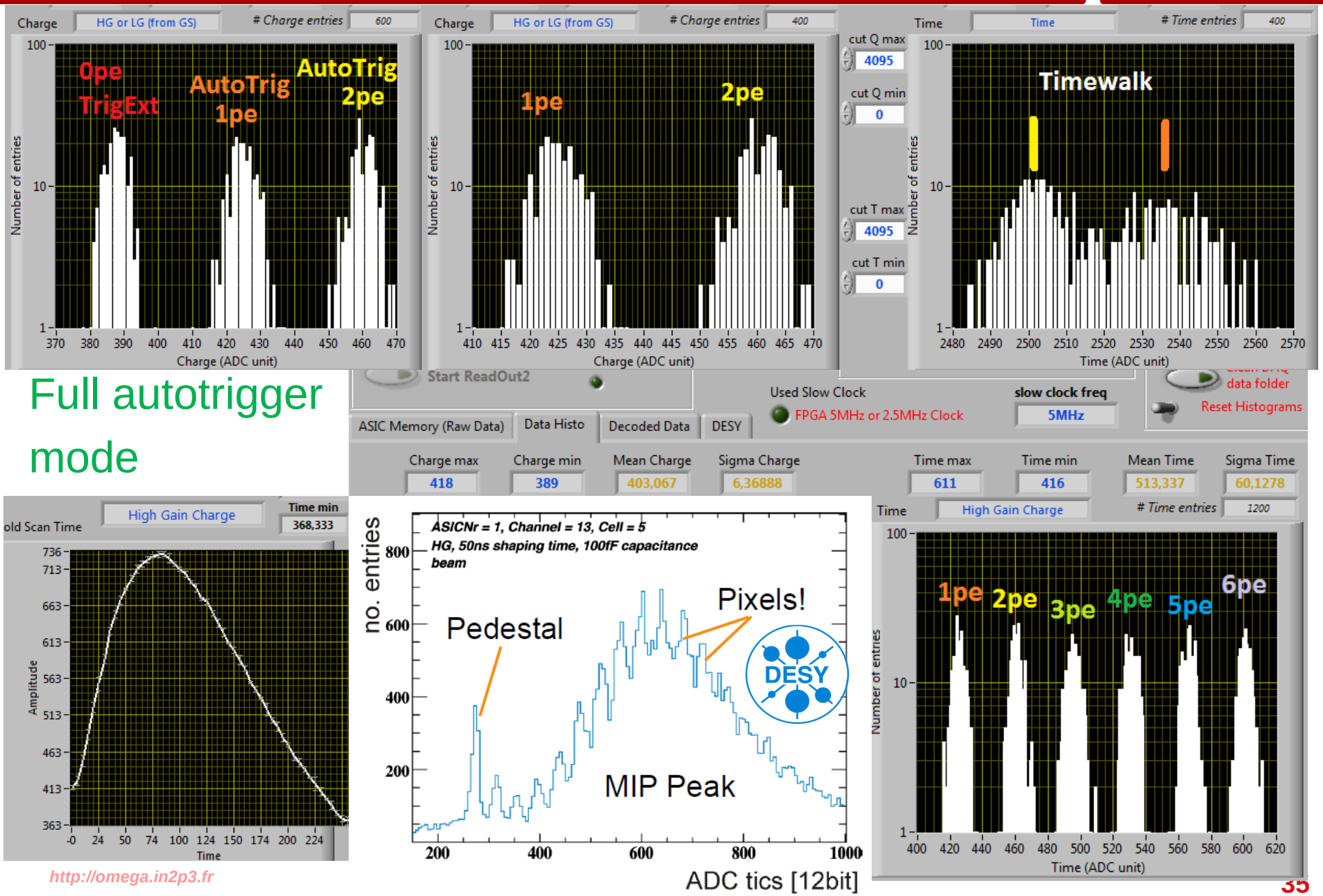
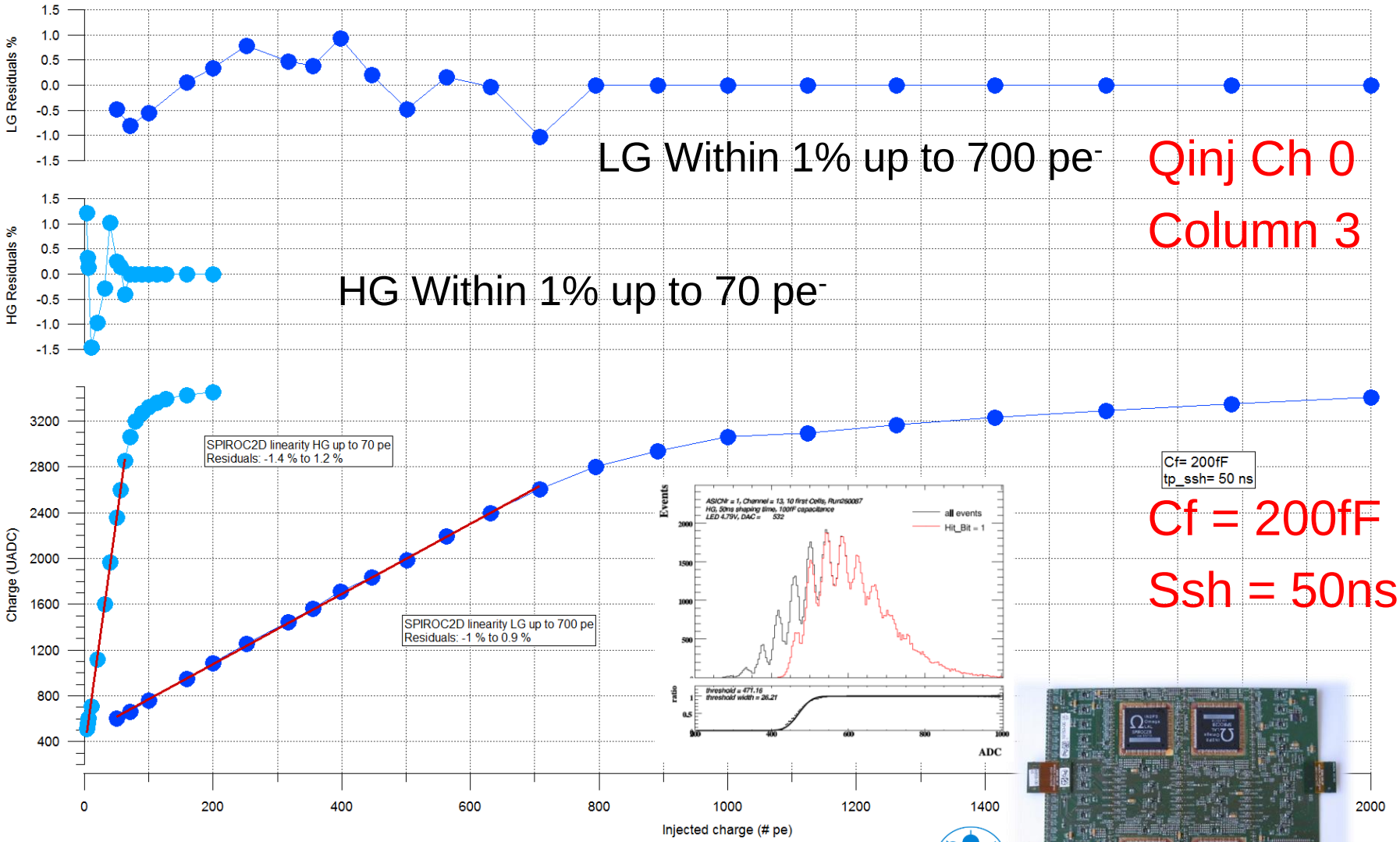
SPIROC2E : Auto-trigger

Full autotrigger mode



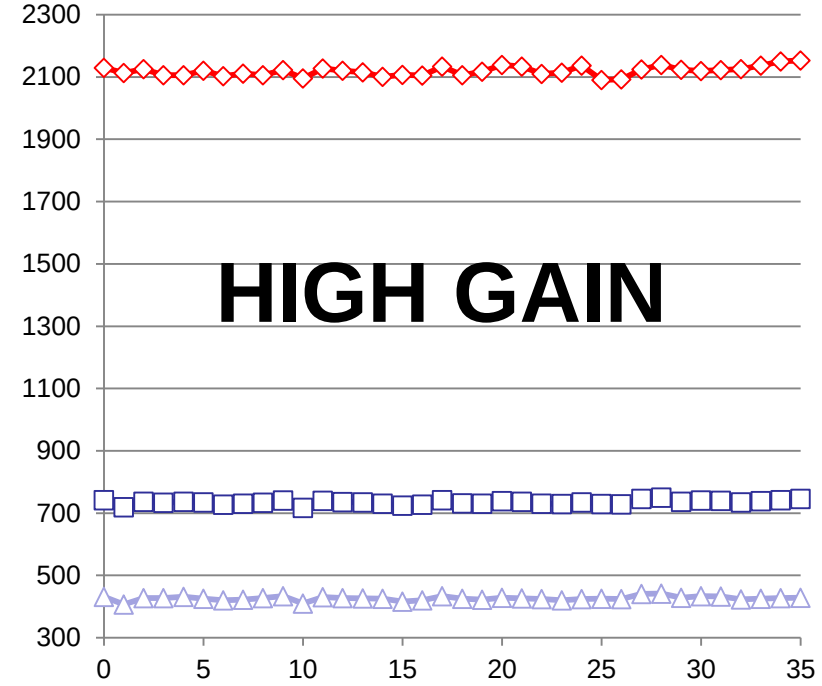
SPIROC2D : Linearity of Charge Measurement

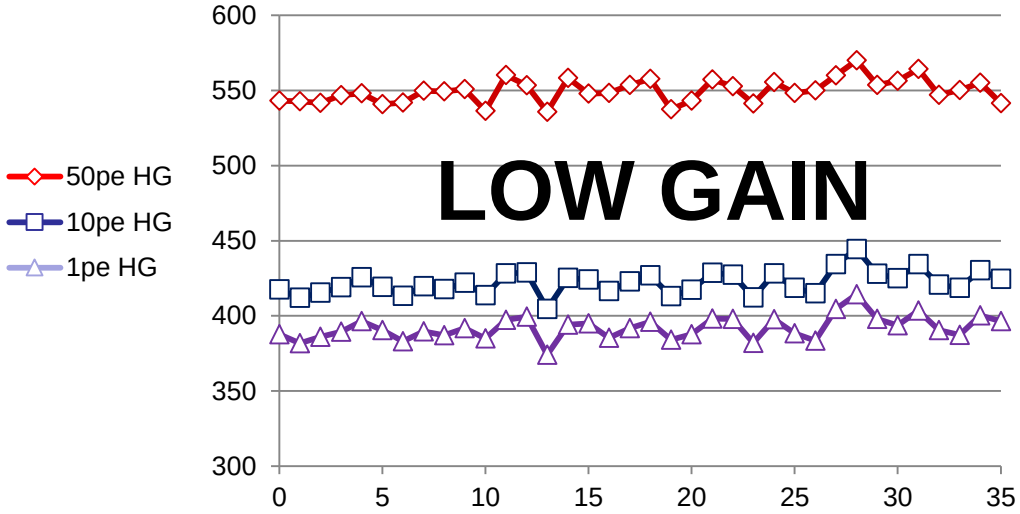


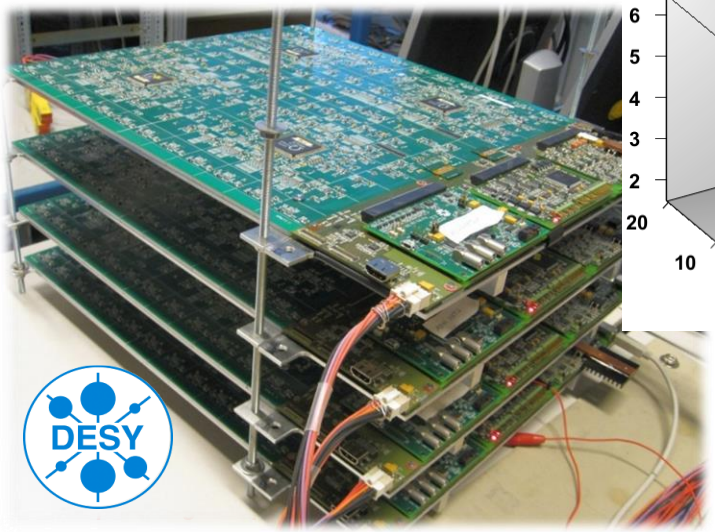
1 EBU : 18 cm x 18 cm
4 Spiroc2 , 144 SiPMs

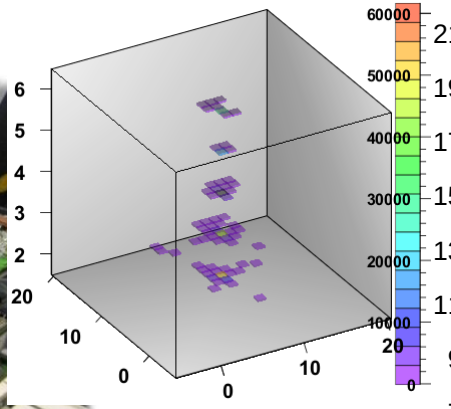
SPIROC2E : Channel Uniformity

Cf = 200fF Ssh = 50ns

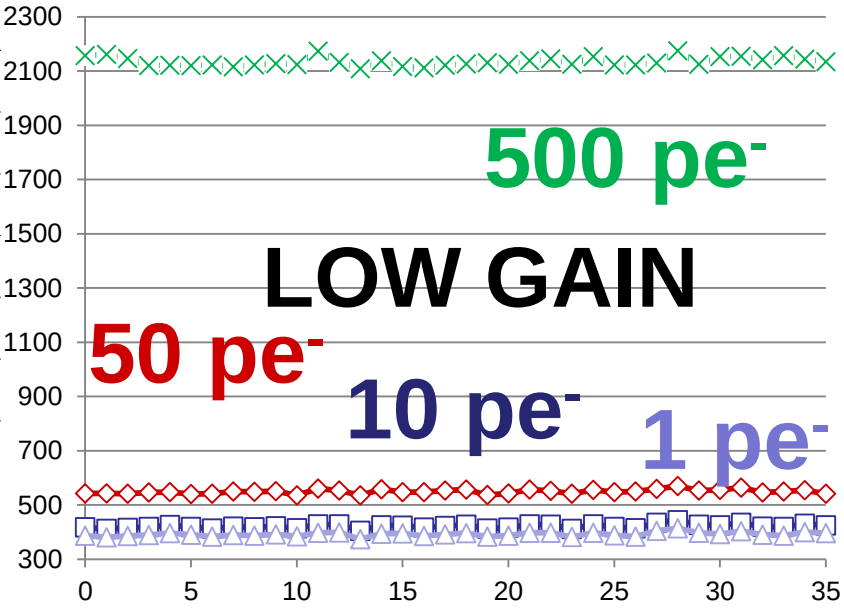








Shower in 5 AHCAL Layers (DESY testbeam)



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SPIROC2E : TDC

Start TDC Scan

AutoDAQ must be fully working

Delay Max (s): 500n

Delay Min (s): 0

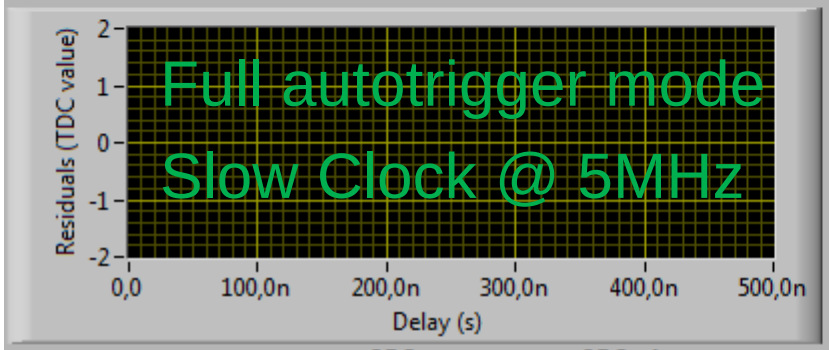
Delay Offset (s): 50u

Channel T?: 14

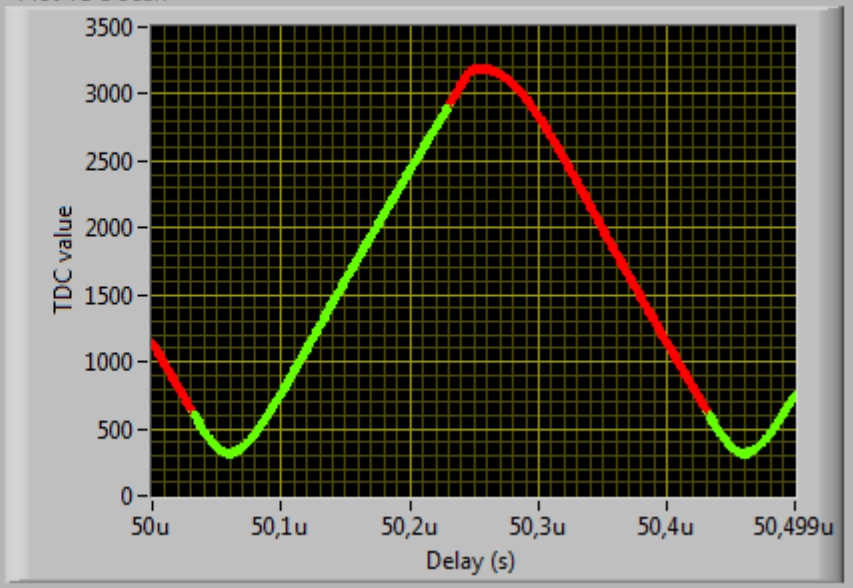
Column T?: 0

Delay Step (s): 1n

Nb of data / delay: 5



Plot TDC Scan



Current data / delay: 4

Current BCID: 243

Test delay value: 499n

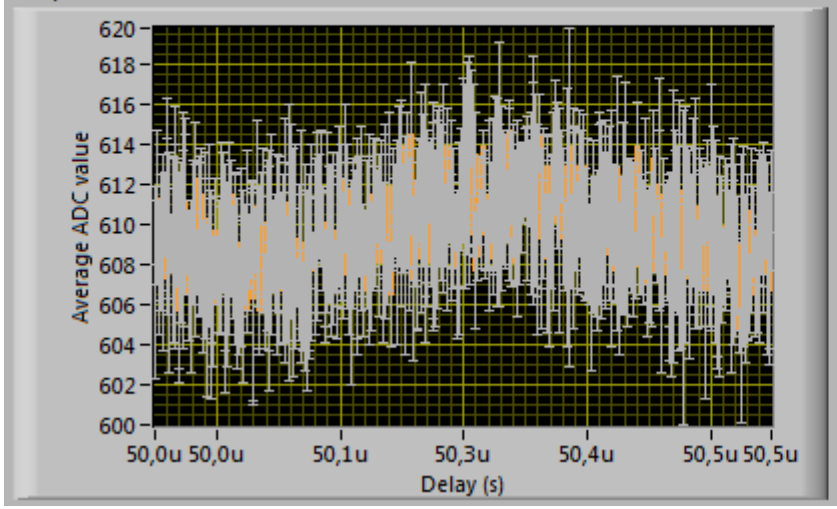
QDC max: 615,2

QDC min: 604,4

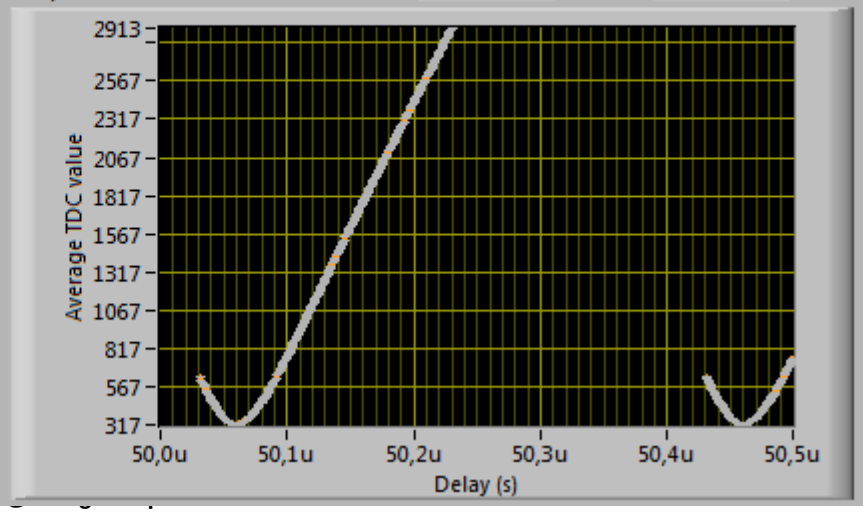
TDC max: 2912

TDC min: 317,6

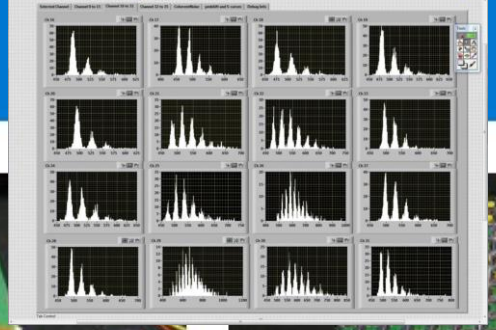
Graphe ADC w.TDC Scan

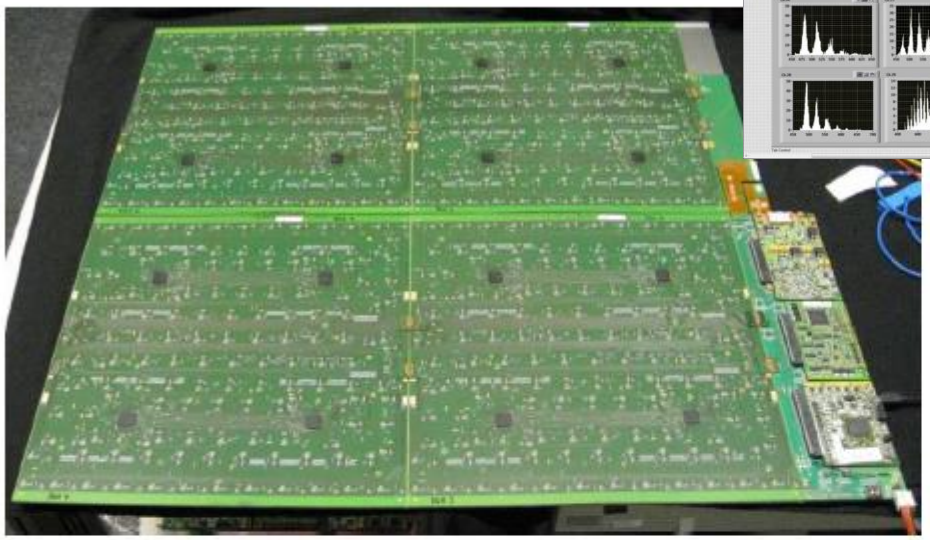


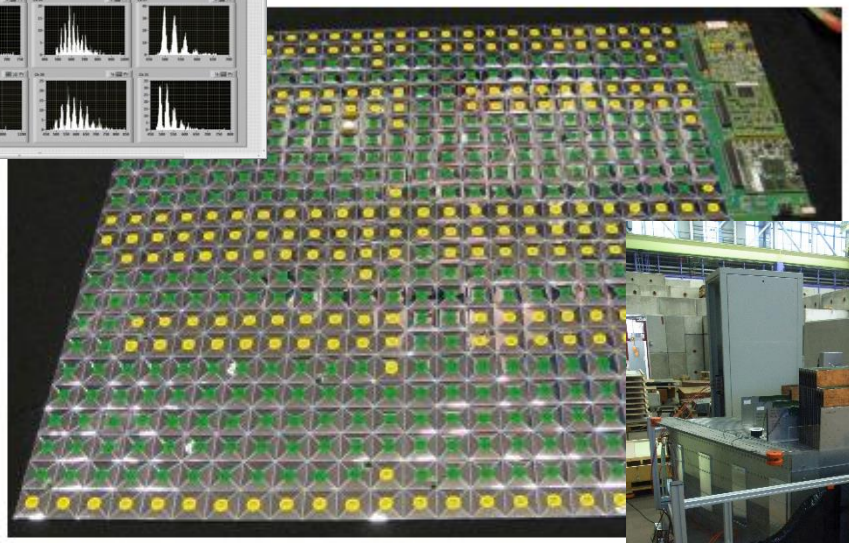
Graphe TDC Scan

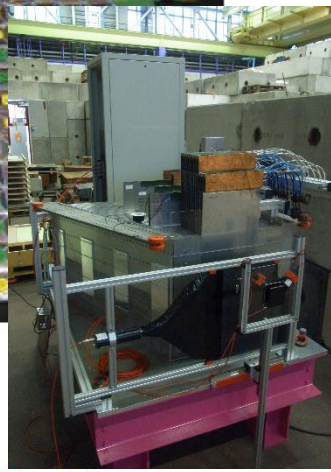


Testbeam Modules



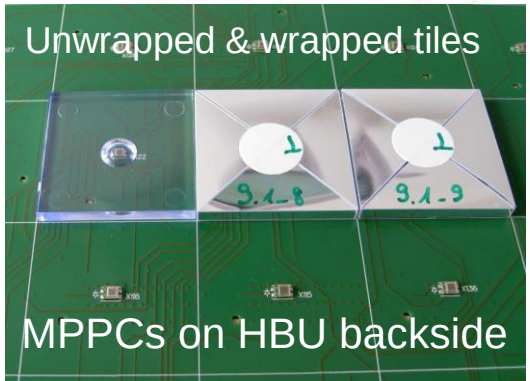


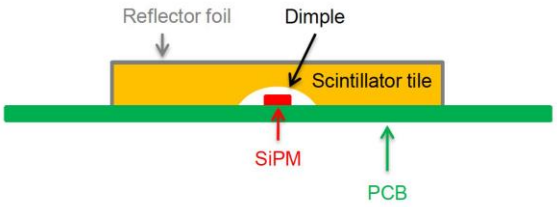


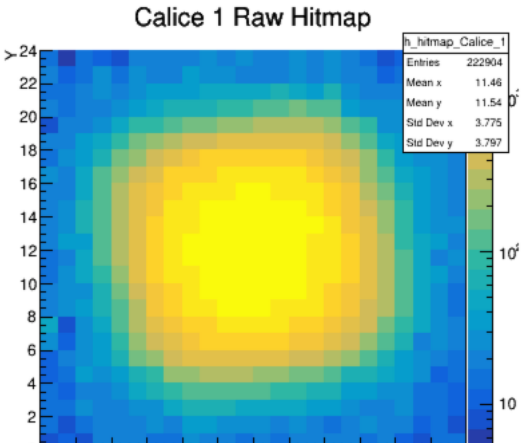


Front- and back side of an AHCAL testbeam detector module

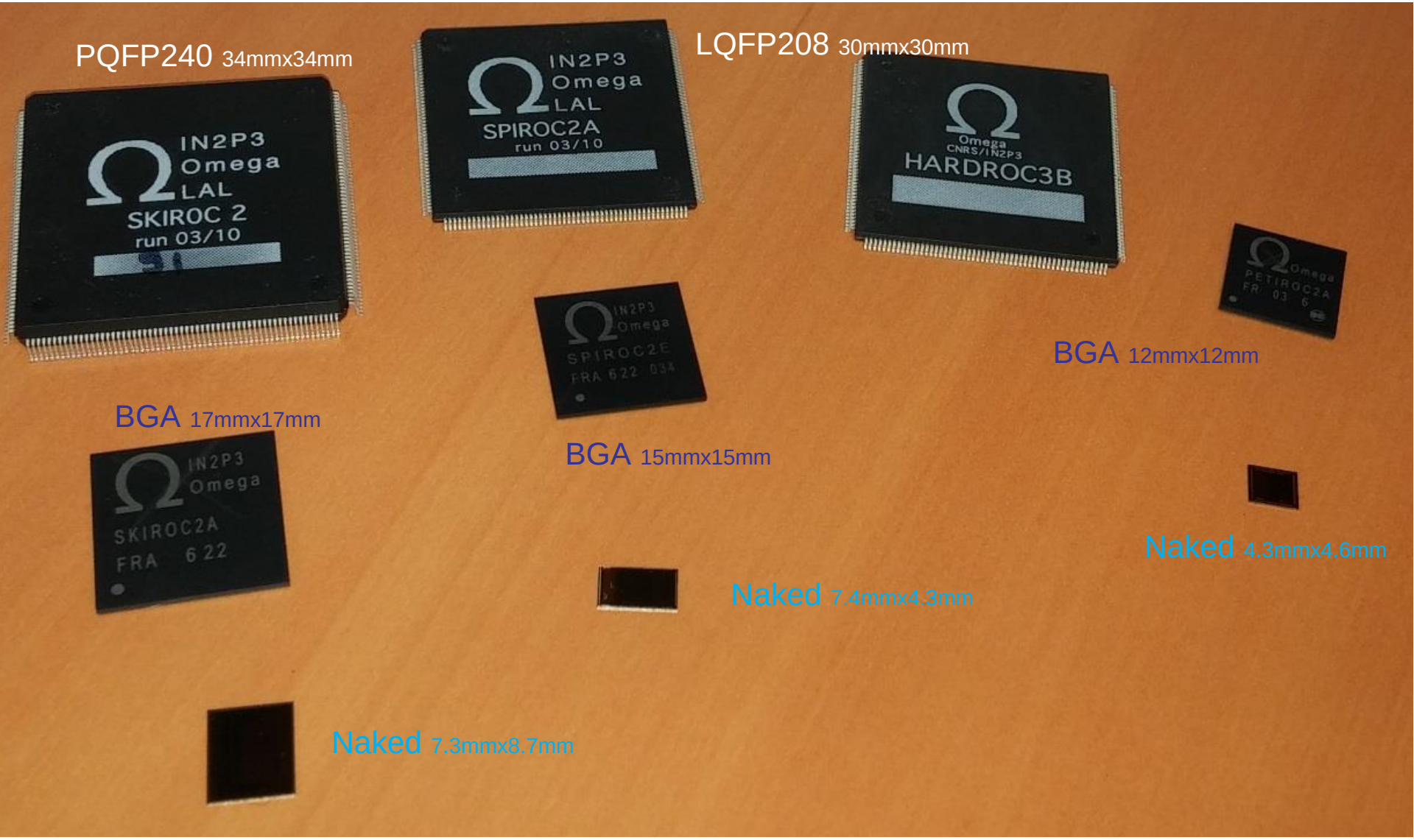
- 24 of 39 detector modules completed. All modules expected end March.
- Detector modules are tested with LED (ET), cosmics and at DESY electron testbeam facility (16 modules already tested).

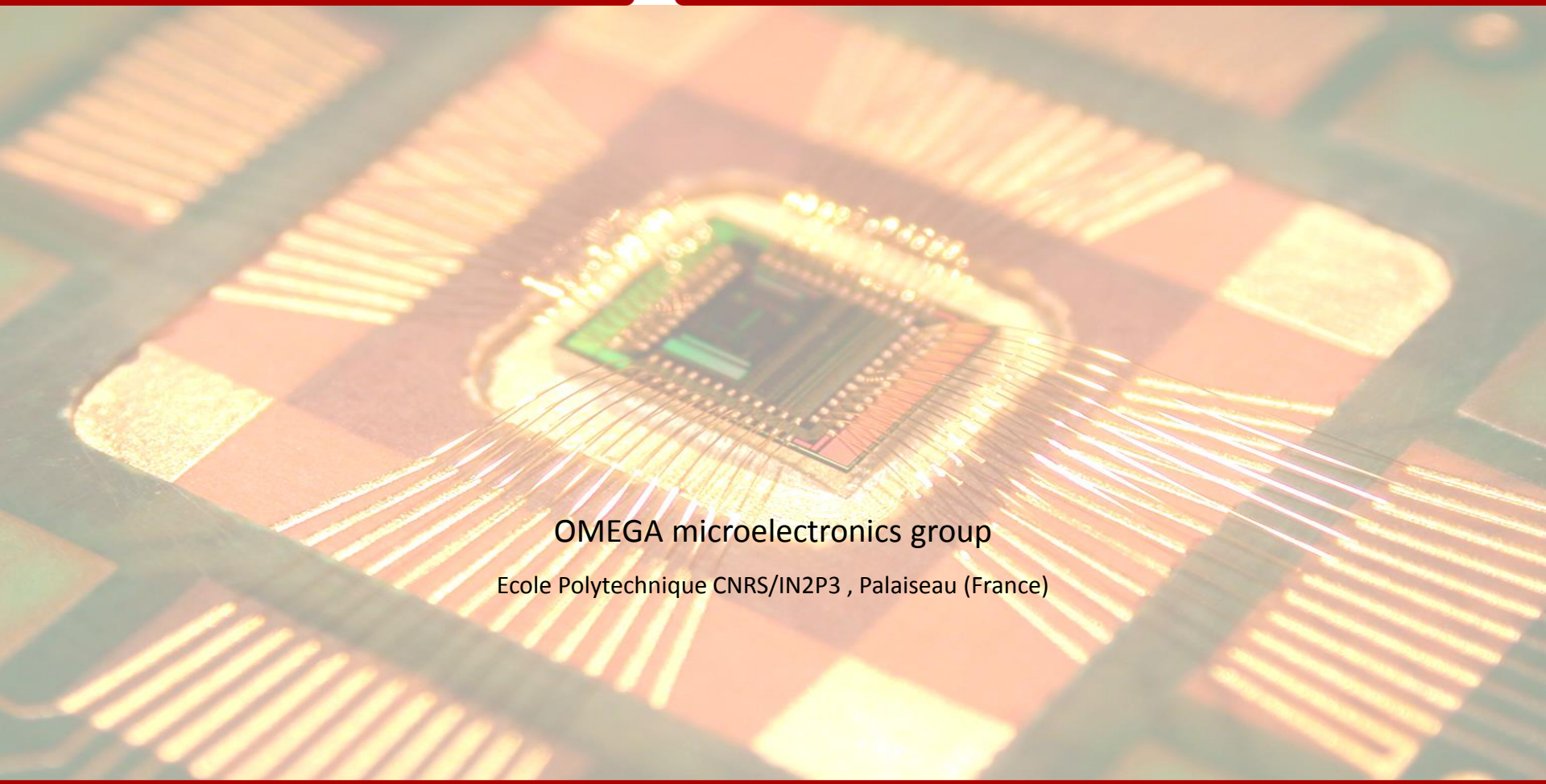






OMEGA ILC chip

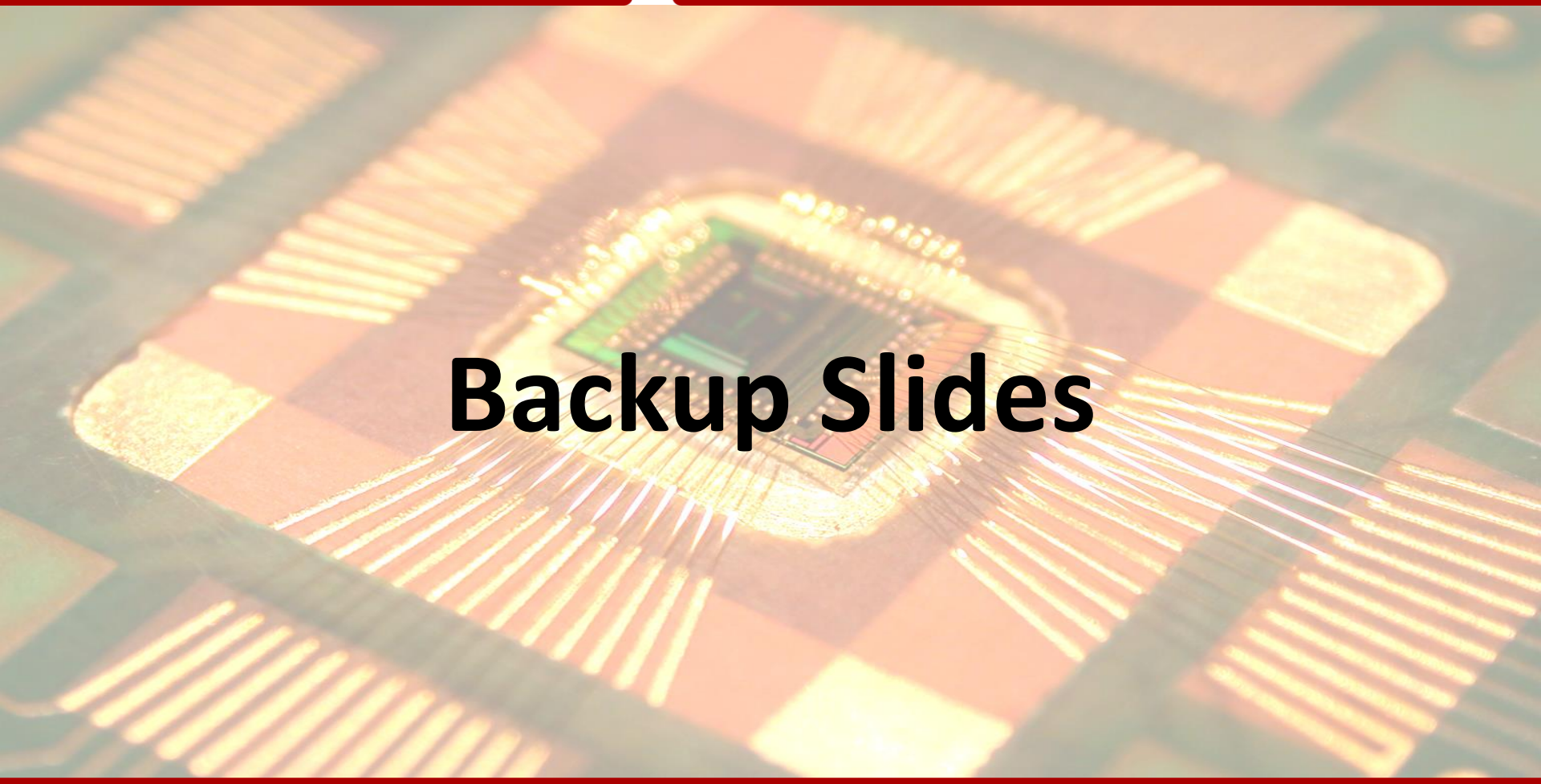




OMEGA microelectronics group

Ecole Polytechnique CNRS/IN2P3 , Palaiseau (France)

Organization for Micro-Electronics desiGn and Applications



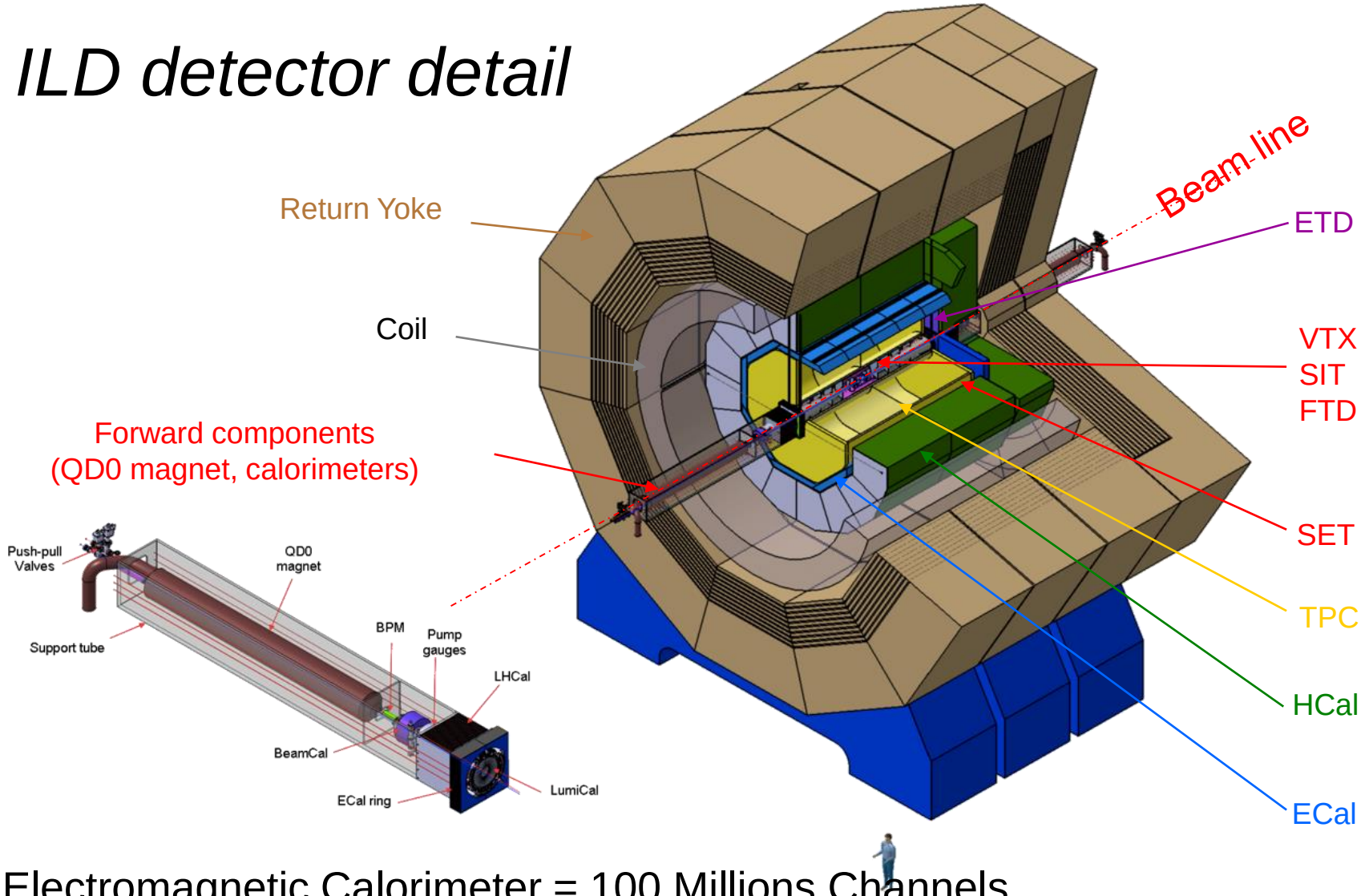
Backup Slides

ILD : subdetectors

Subdetector	Channels $[10^6]$	Occupancy [%]	Data volume $[MB]$
VTX	800	1.0	50
TPC	2	< 0.1	12
FTD	1	9	2
SIT	1	30	6
SET	5	1	1
ETD	4	10	7
ECAL	100	< 0.1	3
HCAL	8	1	130
MUON	0.1	< 0.1	≤ 1
LCAL	0.2	70	4
BEAMCAL	0.04	100	126
TOTAL	$\approx$920		$\approx$340

TABLE 5.1-1
Data Volume in MB per bunch train for the major ILD detector components

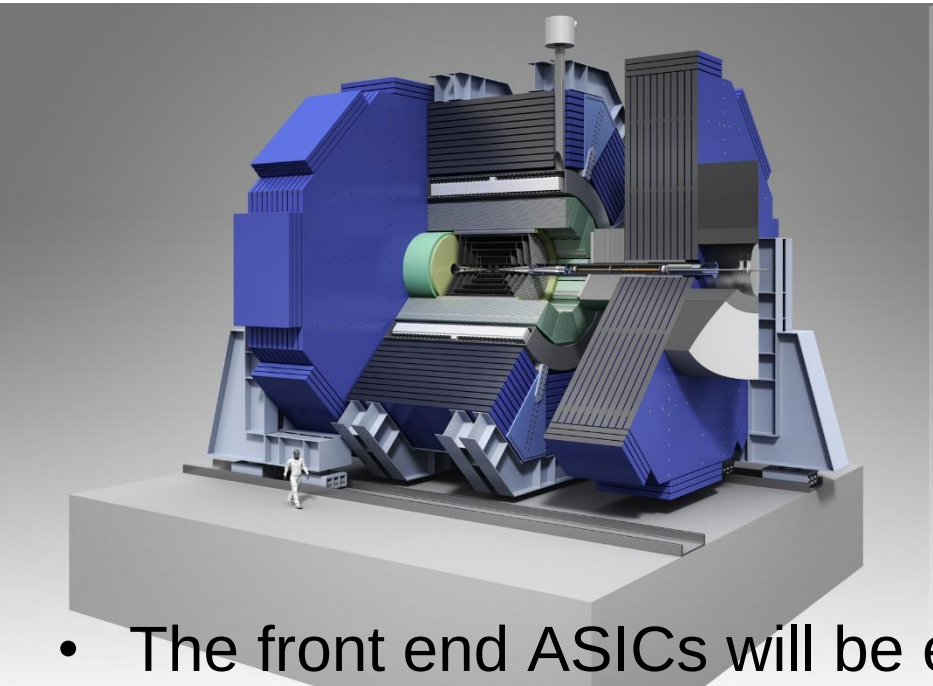
ILD detector detail

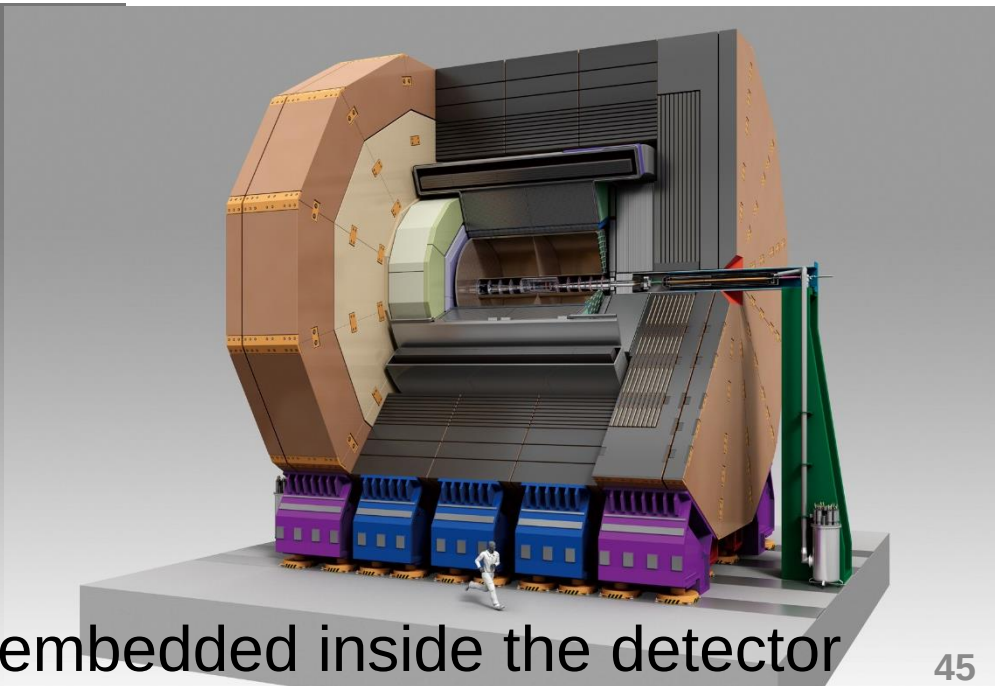


Electromagnetic Calorimeter = 100 Millions Channels
Hadronic Calorimeter = 8 Millions (Analog) or 70 Millions (semi-Digital)

Detectors : ILD / SiD

- Relevant physics processes at the future linear collider mostly lead to multijet final states
- The reconstruction of the final state will be based on the Particle Flow Algorithm (PFA), which aim to reconstruct every particle of the final state
- Particle flow techniques require highly granular calorimeters with a huge number of electronics channels

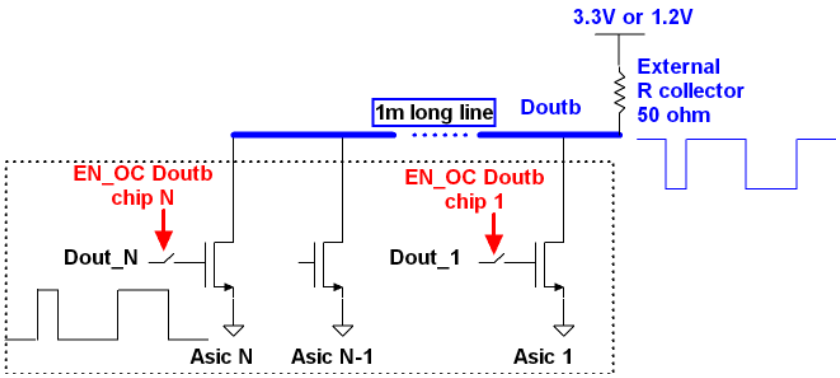


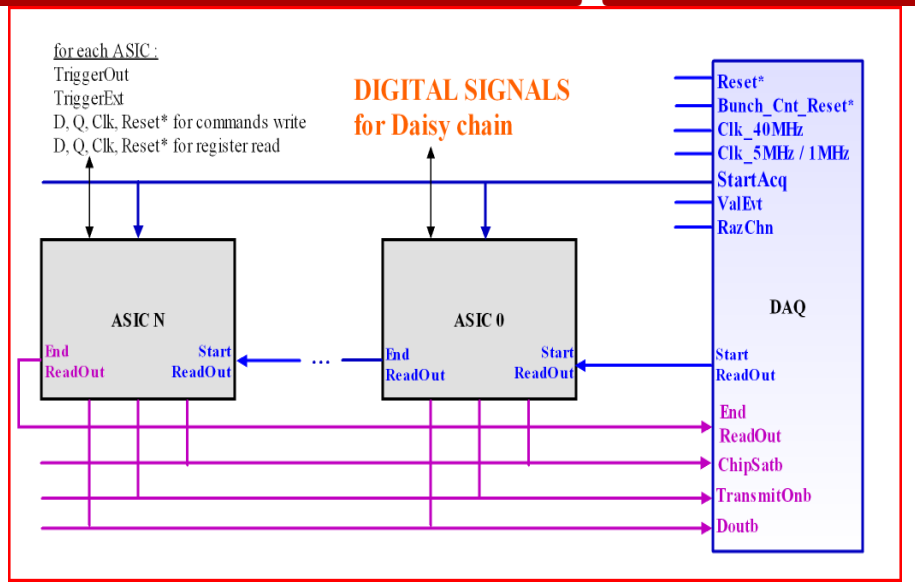


- The front end ASICs will be embedded inside the detector

DAISY CHAIN: Main signals

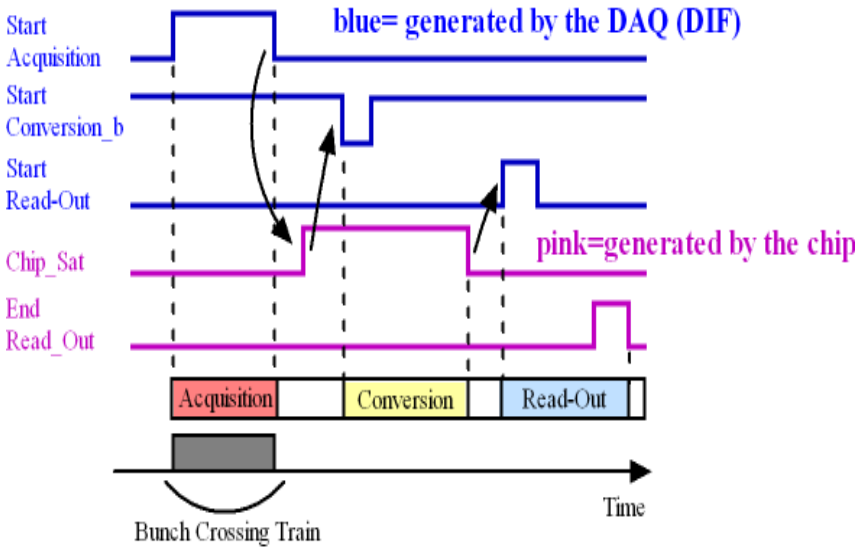
- **COMMON to all the ROC chips**
  - **StartAcq**
    - Start acquisition, generated by DAQ
  - **StartReadout:**
    - Generated by DAQ, start of the readout
  - **EndReadout**
    - Generated by chip, End of the readout
  - **ChipSat** (**O**pen **C**ollector signal):
    - Generated by chip, « 1 »: digital memory is full or acq is finished
  - **Dout:** data out (OC signal)
  - **TransmitOn** (OC signal)
    - Generated by chip, Data out are transmitted
- Buffers integrated for OC signals





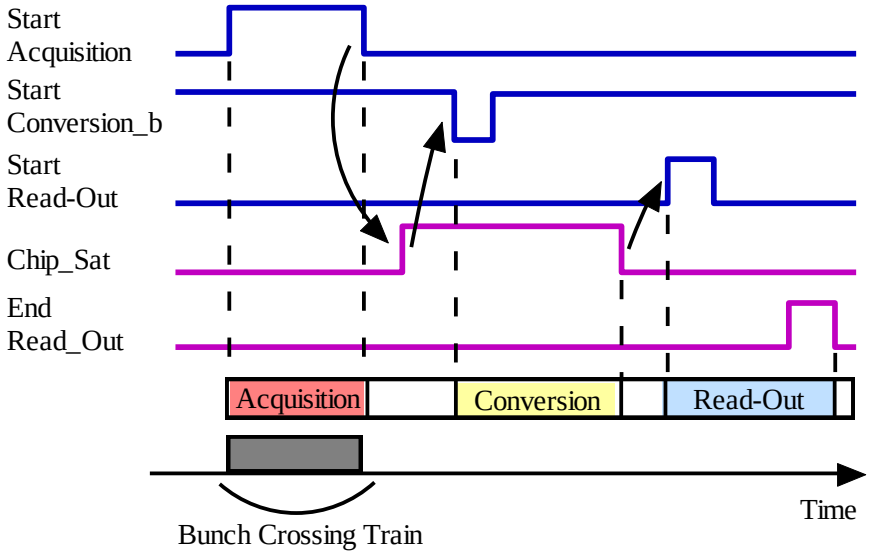
ILC

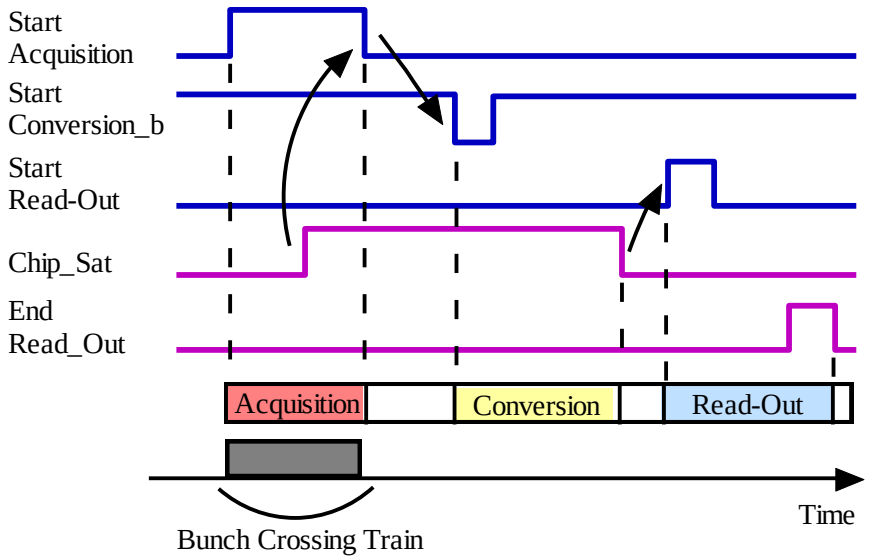
No conversion in Hardroc/Microroc



3Gen ROC chips: common features

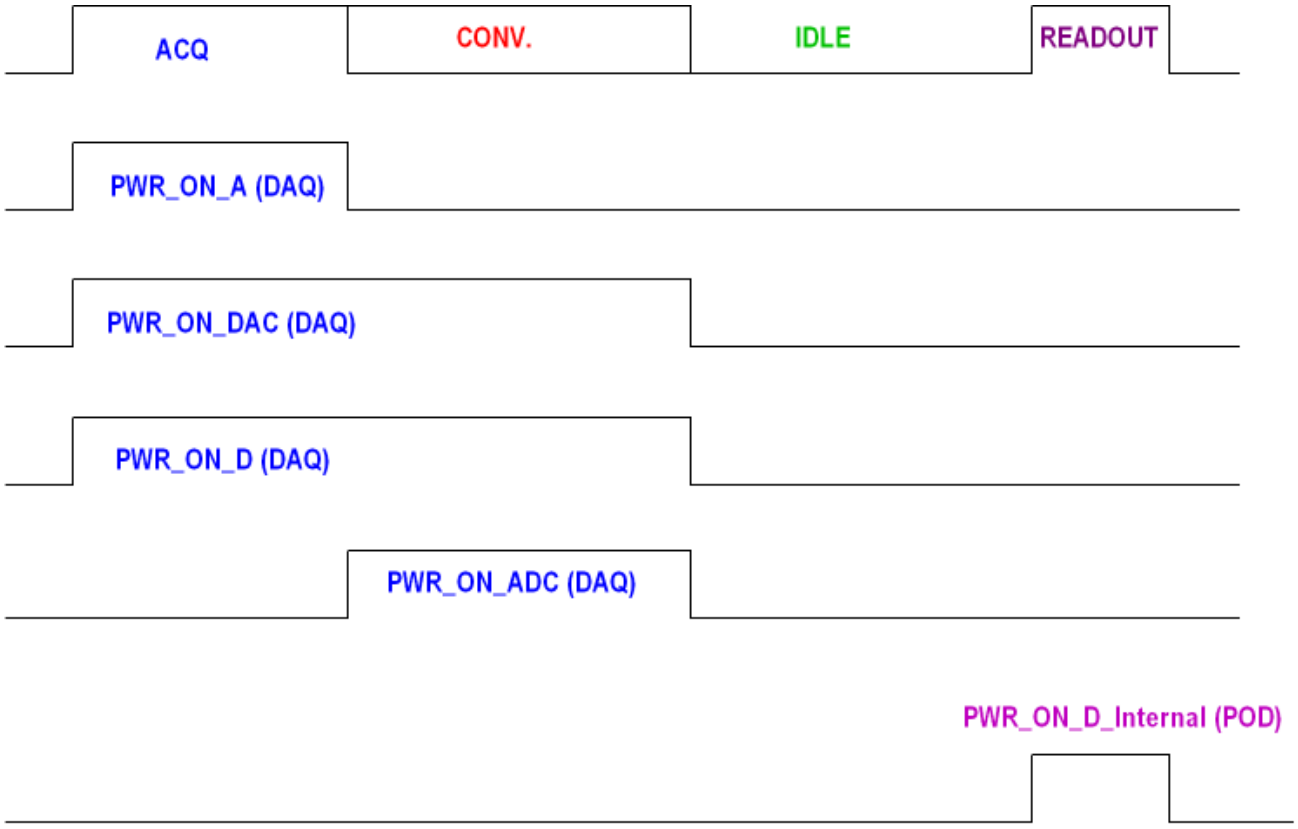
- DIF sequencing (Acq, Conv and Readout):
  - Backward compatibility with 2Gen ROC chips sequencing
  - Use of ChipSat signal
  - Daisy chained chips for readout





- Possibility to use Roll mode by Slow Control:
  - If RollMode = “0” ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = “1” ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored

Power pulsing lines timing



CONVERSION:

HARDROC2: NO conversion

SPIROC2: max time (Full chip)= 16 SCAx 2 (HG or LG/Time) x103 µs=3.2ms

SKIROC2: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms

READOUT:

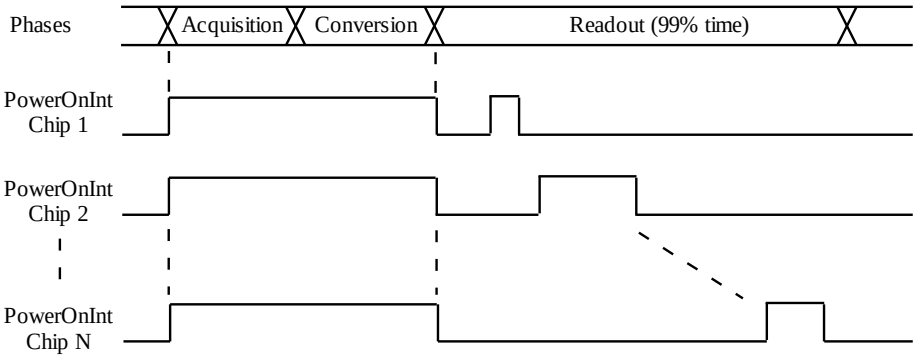
HARDROC2: 127 (memory depth)x [64 channelsx 2 trigger bits + 24 BCID bits + 8 Header bits]=20 320 bits => 200 nsx20k=4 ms/ Full Chip (WORST case)

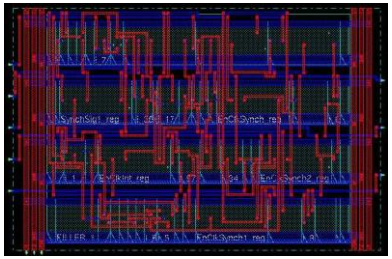
SPIROC2: 16 SCAx2 (HG or LG/Time) x 36 ch x 16 ADC bits + 16 SCAx16 BCID bits + 16 Header bits= 18 704 bits => 3.8 ms/Full Chip (Worst case)

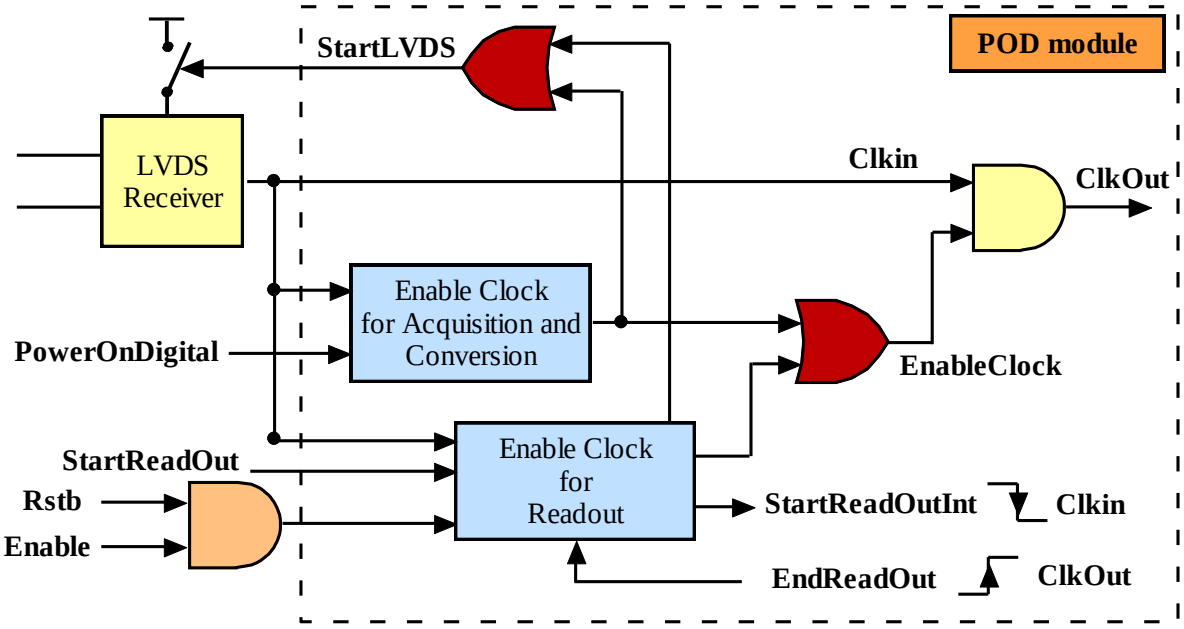
SKIROC2: 15 SCAx2 (HG or LG/Time) x 64 ch x 16 ADC bits + 15 SCAx16 BCID bits + 16 Header bits= 30 976 bits => 6 ms/Full Fhip (Worst case)

Power On Digital Module: POD

- POD module ("Clock-gating") to handle for the 2 LVDS receivers clock (40 MHz and 5 Mhz) and save power:
  - Starts and stops the Clocks, switches OFF LVDS receivers bias currents



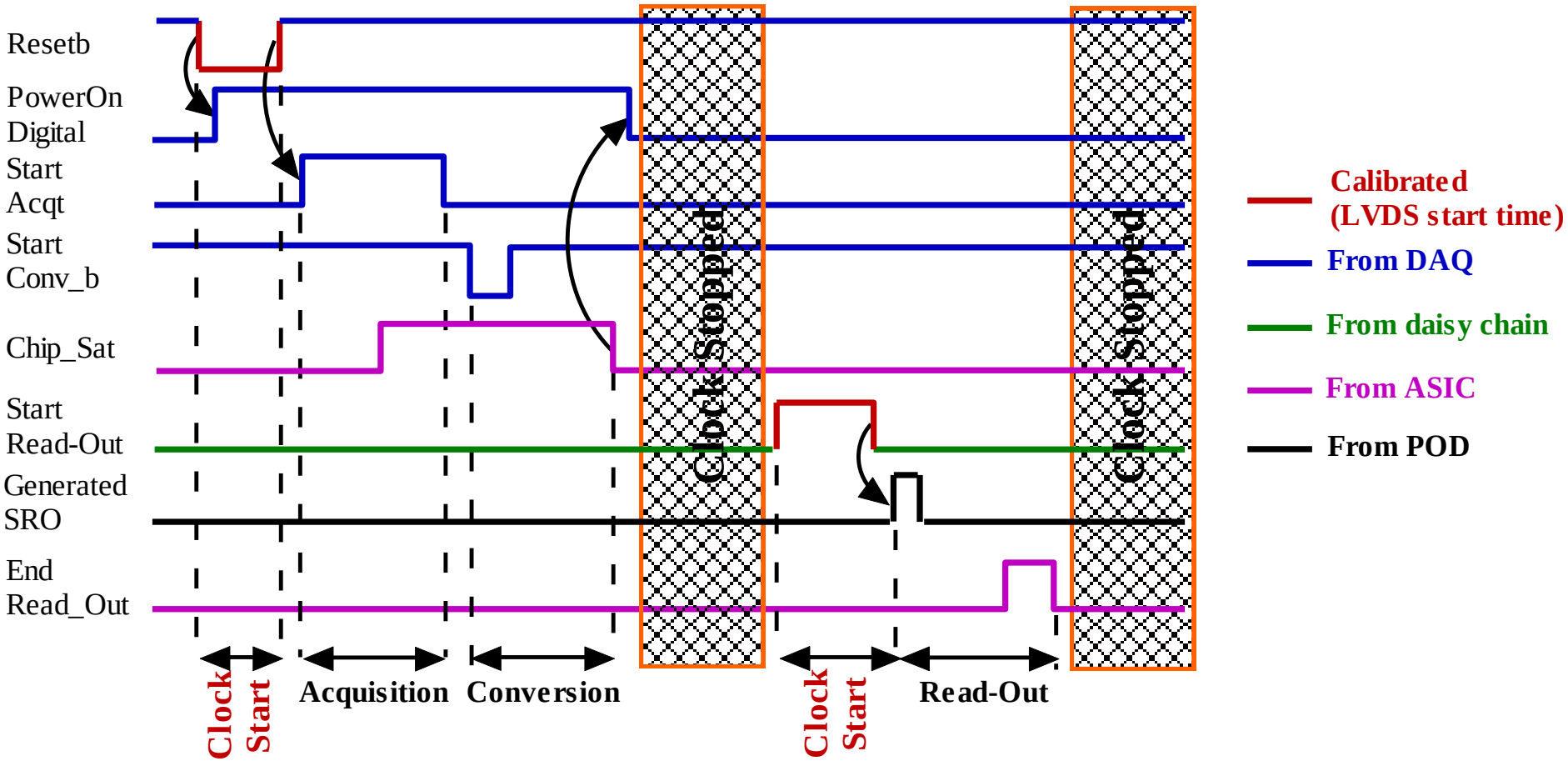




2 others LVDS receivers (RazChn/NoTrig and ValEvt) active during PowerOnAnalog (during bunch crossing)

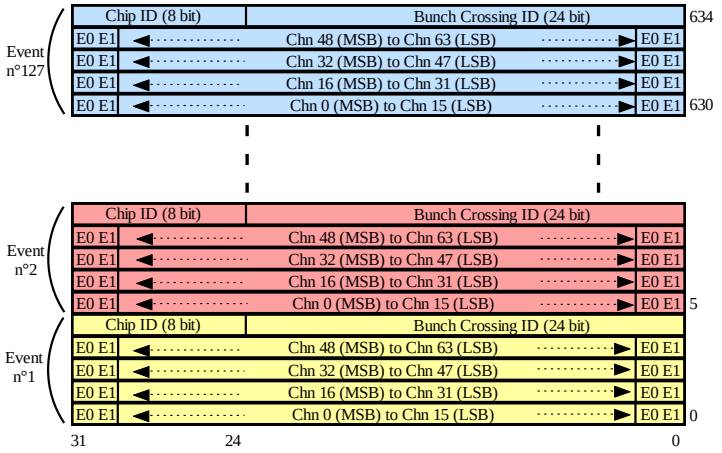
Power On Digital Sequence

- **End of Conversion**: clock stopped as not needed and LVDS receivers bias switched OFF
- **Readout**: Start ReadOut signal generated by the POD and stands for a PwrOnD => starts LVDS receivers and Clk.
- **End of the ReadOut**: The chip generates a EndRout signal which will be used by the next chip in the daisy chain to be read out.



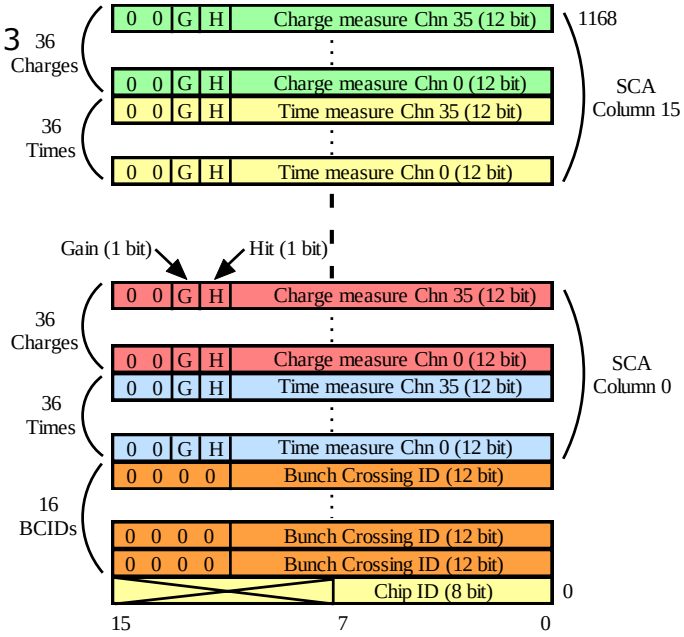
MEMORY MAPPING of the ROC CHIPs

- HARDROC2: 127 events on 2 bits for 64 channels. Maximum of stored data is 20320 bits
  - No conversion
  - Readout worst case: 200 nsx20k=4 ms/ Full Chip (WORST case)

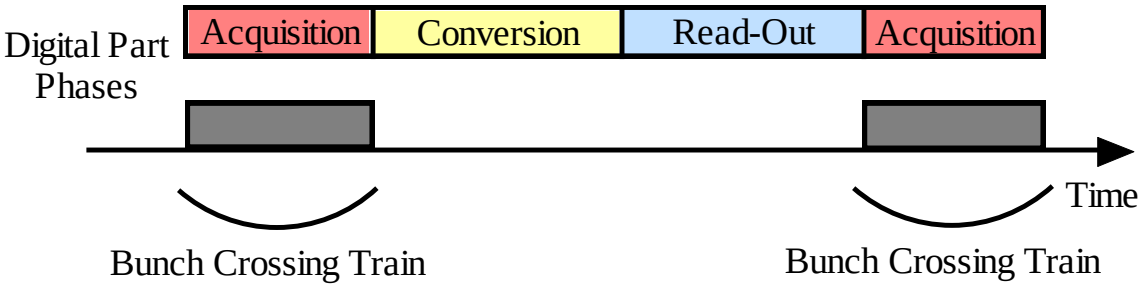


- SPIROC2: 16 events, 36 channels. 12 bits ADC for time and charge => max stored data= 18707 bits
  - Conv.: max time (Full chip)= 16 SCA x 2 (HG or LG/Time) x103 µs=3.2ms
  - RO: 3.8 ms/Full Chip (Worst case)

- SKIROC2: 15 events, 64 channels. 12 bits ADC for time and charge => max stored data= 30976 bits
  - Conv.: max time (Full chip)= 15 SCA x2 (HG or LG/Time) x103 µs= 3 ms
  - ReadOut: 6 ms/Full Fhip (Worst case)



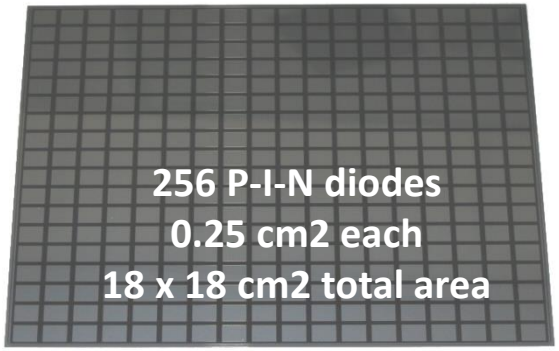
Physics simulation: 2 or 3 SCA are enough



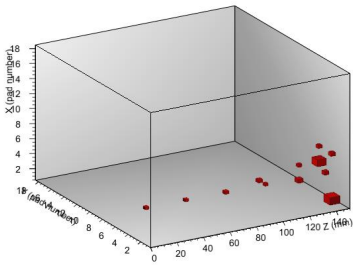
…To 3rd generation

3rd generation chips for ILD

- **Technology used for SKIROC3 & SPIROC3 ?**
  - ~~0.35µm AMS SiGe~~ -> TSMC 0.13µm
  - no plan to be submitted (waiting for Japanese decision for ILC)



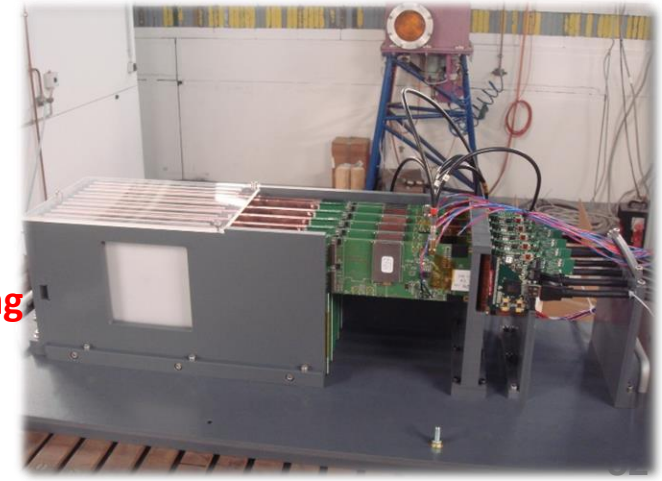
- **No major change in the analogue part**
  - MIP over Noise Ratio @ lower gain = 10
  - TDC scheme will change (PETIROC like)
  - Few optimization (Crosstalk, AutoGain, 4-bit DACs, external triggers, power consumption…)



- **PLL** provides the Fast Clock (mainly used for digitization) from the Slow Clock
  - No Fast Clock to be provided to the ASICs !

- **Independent channels (zero suppress)**
  - Huge change in digital part !!
  - Digital part power consumption and size (+30 to 50%)

- **I2C link (@IPNL)** for Slow Control parameters and **triple voting**
  - configuration broadcasting
  - geographical addressing



callier@omega.in2p3.fr

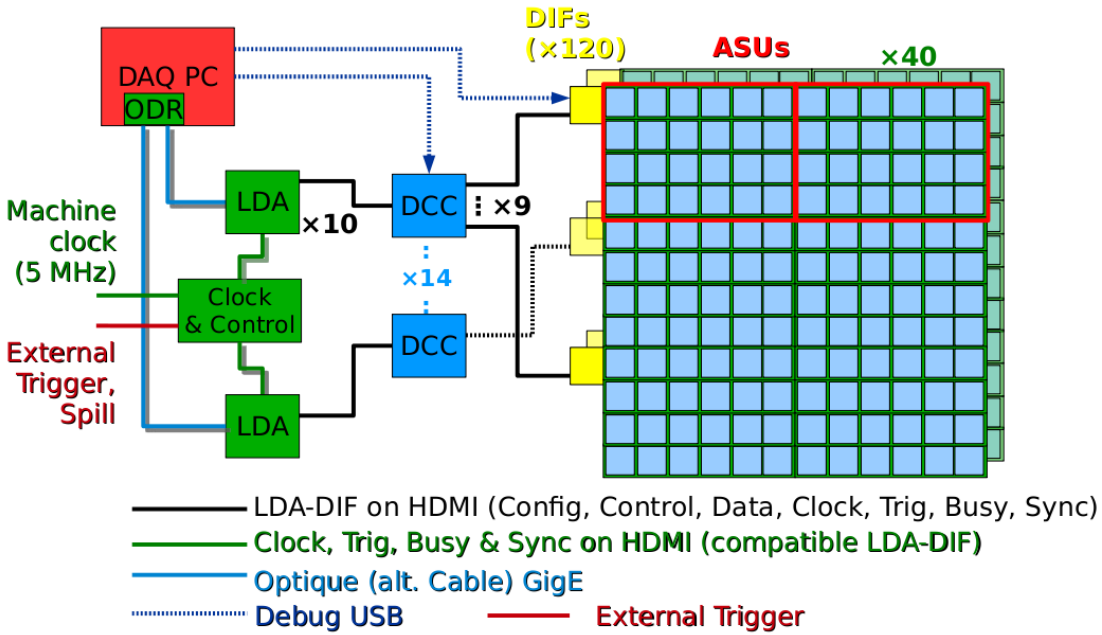
INTERFACE DAQ-ROC= DIF board

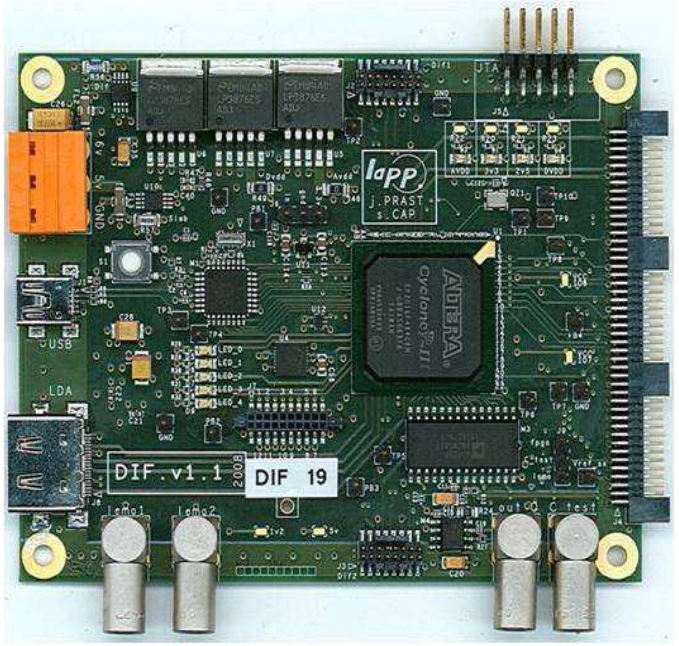
- Reception of the Slow Control parameters from a PC and transmission to the ASICs, launch acquisition, perform analog/digital readout and send all the data received from ASICs to a PC.

- Communication
  - with other DIFs
  - with DAQ either by USB or by HDMI

- The DIF should be able to handle more than 100 ASICs theoretically. The max which has been tested is 48

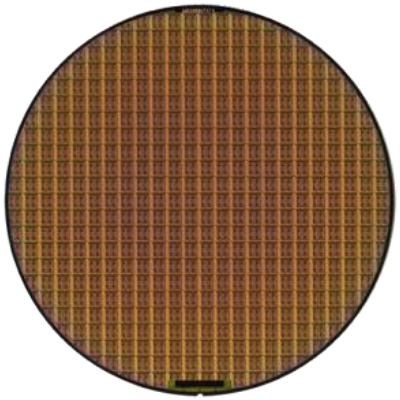
- **Regulators + Decoupling capacitors located on the DIF**





Engineering run 2016

- CITIROC1A
- CITIROC2
- DOPIROC
- GEMROC
- MAROC3A
- PHOTOROC1A
- SKIROC2A (PIN)
- SKIROC2-CMS
- SPACIROC3A
- SPIROC2E (SiPM)
- 1 other chip



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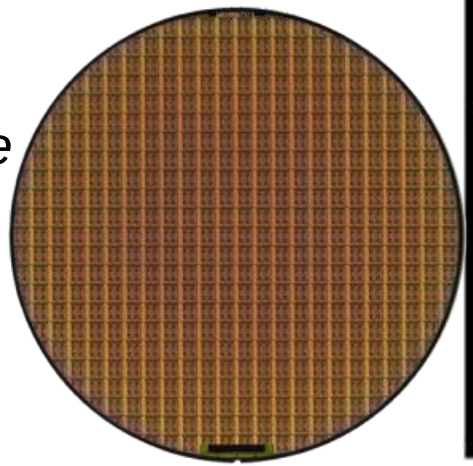
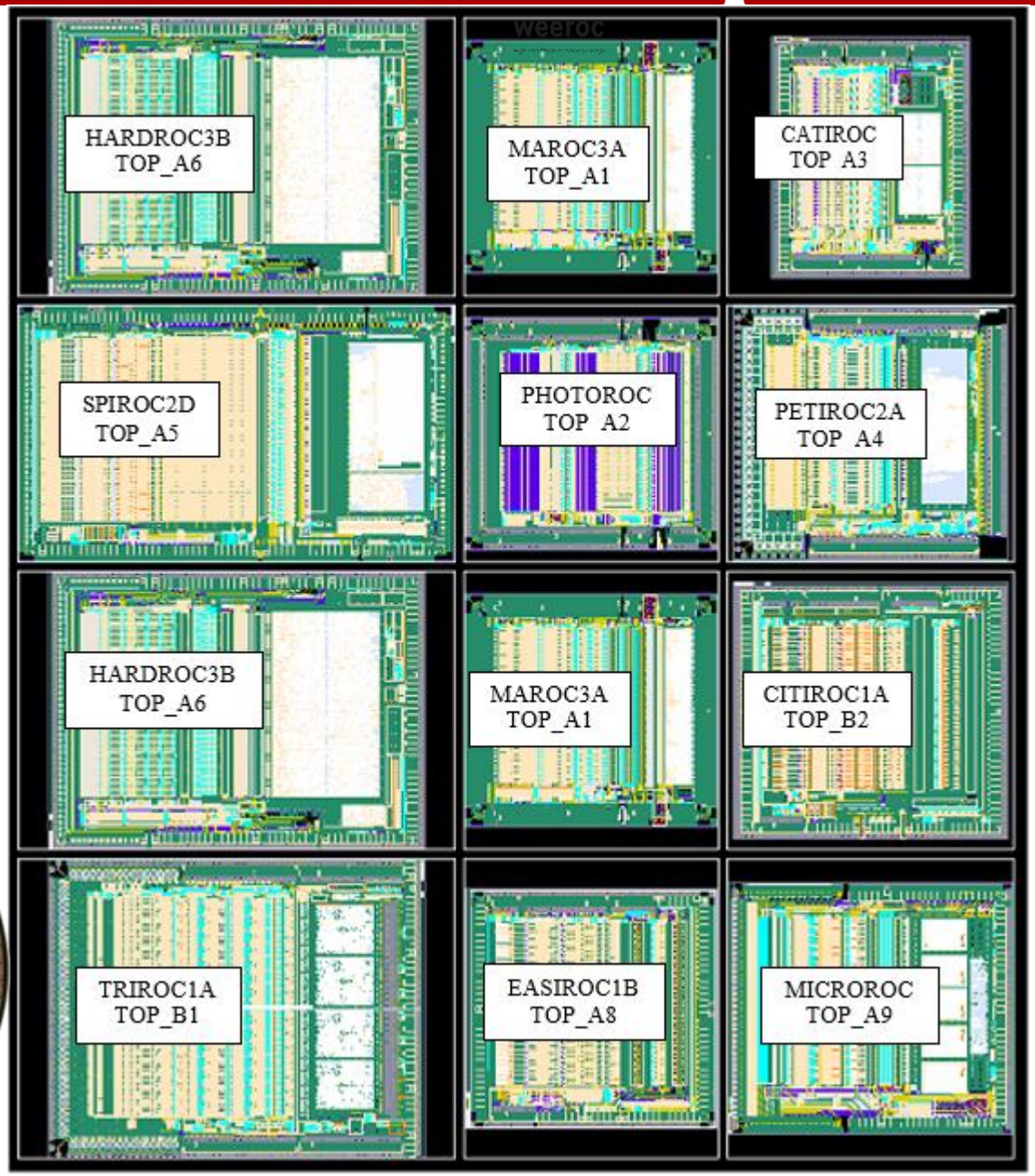
Engineering run 2015

- MAROC3A
- PHOTOROC
- HARDROC3B (RPC)
- SPIROC2D (SiPM)
- CATIROC
- PETIROC2A
- CITIROC1A
- EASIROC1B
- TRIROC1A
- MICROROC (µMEGAS)

Technology :

0.35µm SiGe





Reminder Production Run : Feb 2015

- MAROC3A
- MAROC4
- HARDROC3B
- SPIROC2D
- ~~SKIROC2B~~
- PARISROC3
- PETIROC2A
- ~~SPACIROC3A~~
- CITIROC1A
- ~~CITIROC1B~~
- EASIROC1B
- ~~DOSIROC1A~~
- DOPIROC2
- TRIROC1A
- MICROROC

Technology :

amu

0.35µm SiGe

SKIROC2B not submitted for funding issues :

70mm²

- Production Run 2010
  - EASIROC
  - HARDROC2B
  - MAROC3
  - SKIROC2
  - SPACIROC
  - SPIROC2A
  - SPIROC2B

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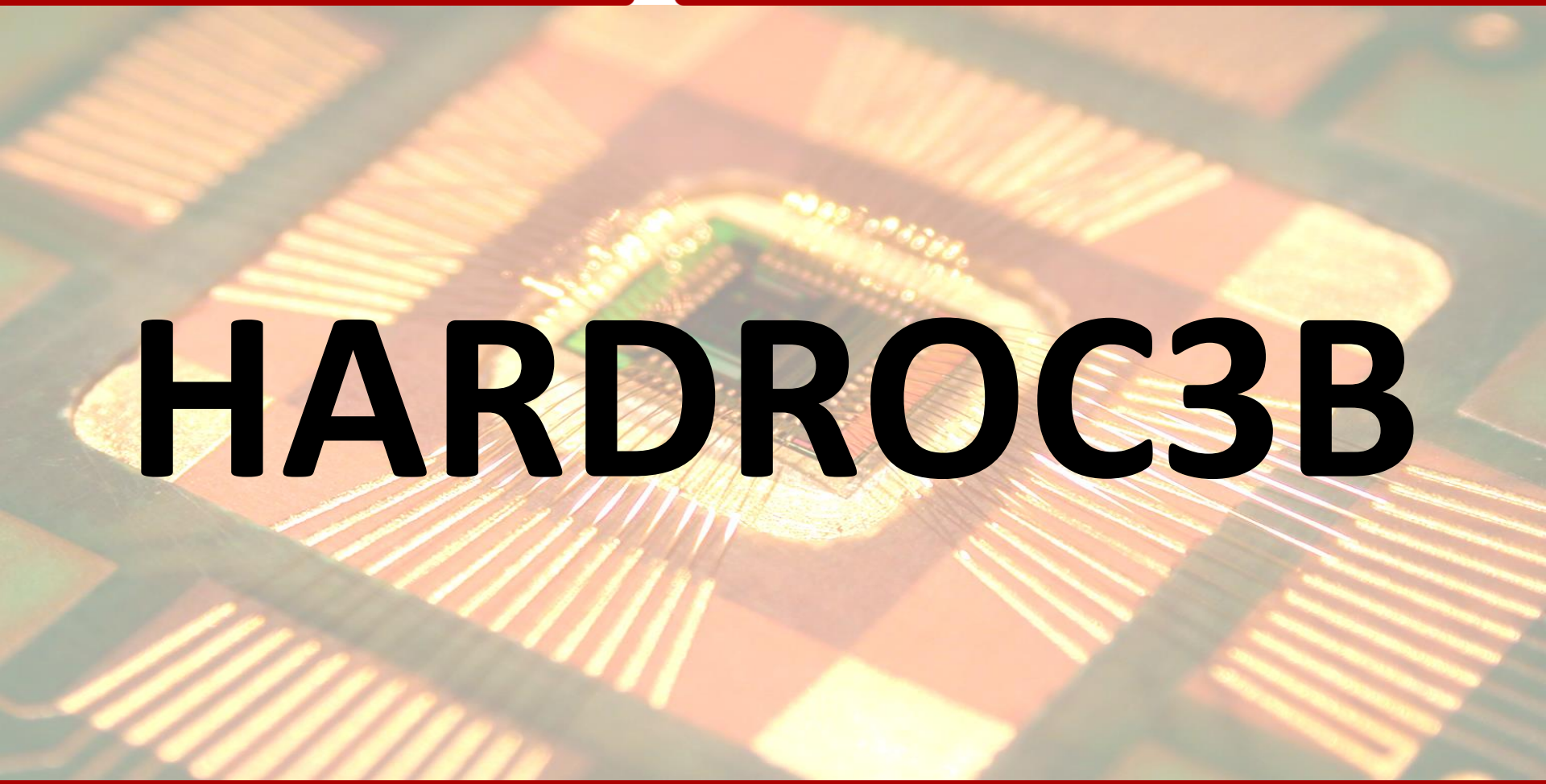


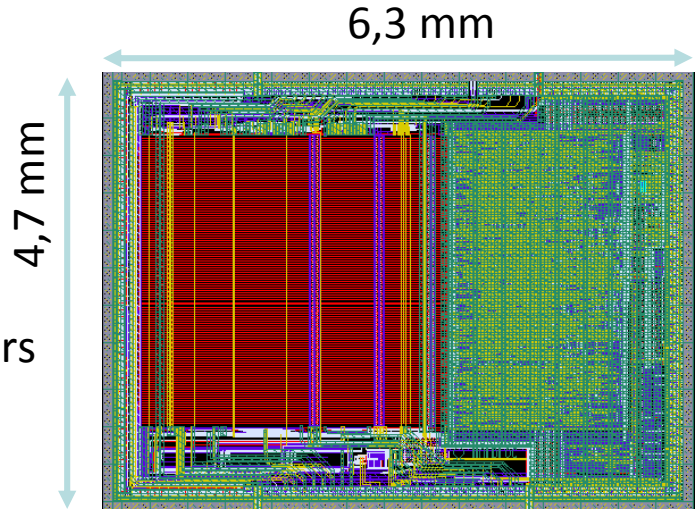
HARDROC3B

Organization for Micro-Electronics desiGn and Applications

HARDROC3 : overview

HR3 main features:

- Independent 64 channels
- Zero suppress
- Extended dynamic range (up to 50 pC)
- I2C link with triple voting for slow control parameters
- Token ring ReadOut
- PLL
- All bias and reference voltage internal (w. power pulsing)
  - No decoupling capacitances required on bias and references voltages

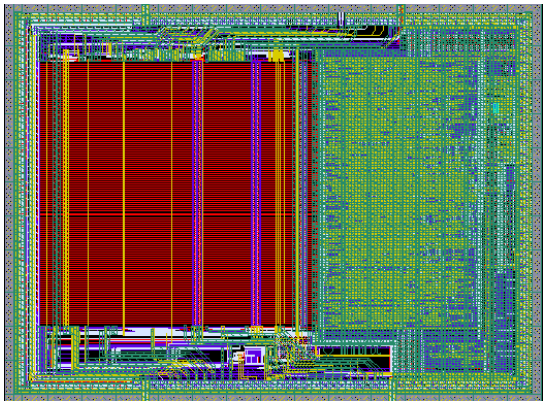


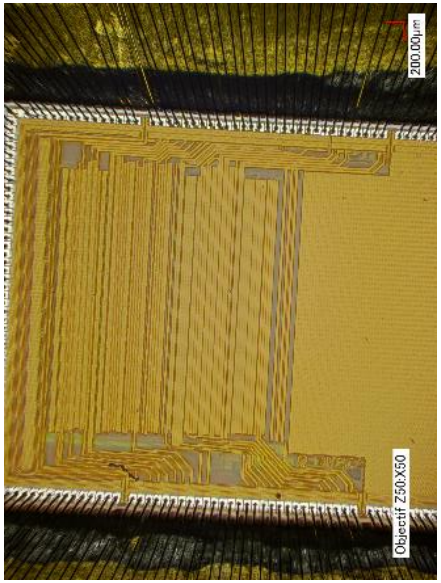
HARDROC3:

- Production run submitted February 2015 (AMS SiGe 0.35µm)
- Naked dies received mid-2015
- Chip packaged in a plastic QFP208
- Die size ~30 mm^2
- Around 800 chips were produced

HARDROC3B Modifications

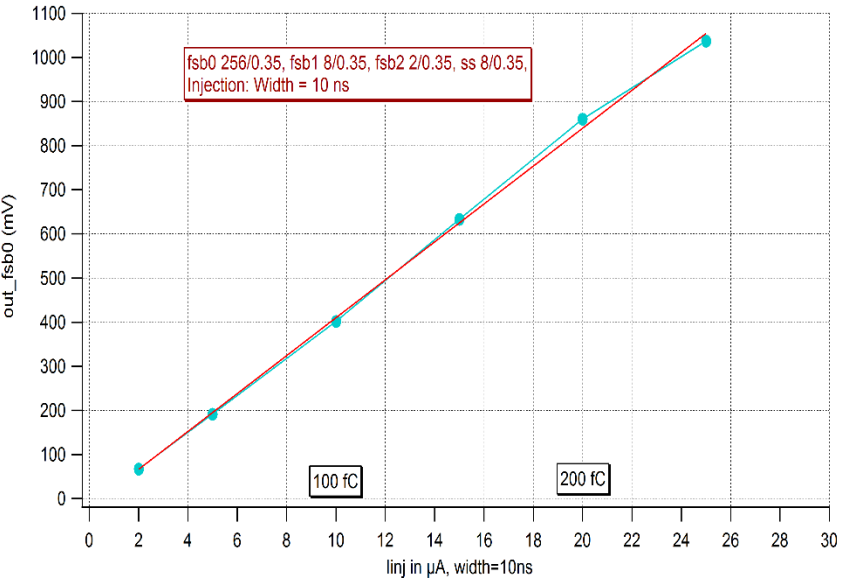
- HARDROC3 chip is properly working except :
  - I2C link : **CORRECTED**
  - PLL start : **CORRECTED**
- Capability to emulate a HARDROC2B : **ADDED**
  - (all channels trigger stored in digital memory when one event occurs)
- Internal Temperature sensor send to the Analog Multiplexed Output as 65th channel: **DONE**
- Power On Reset on READ Register : **ADDED**

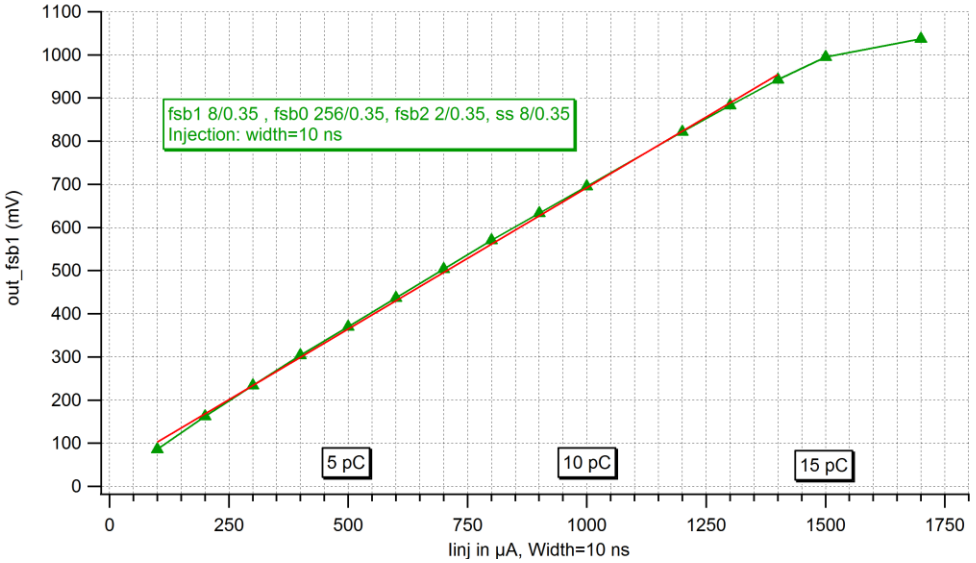


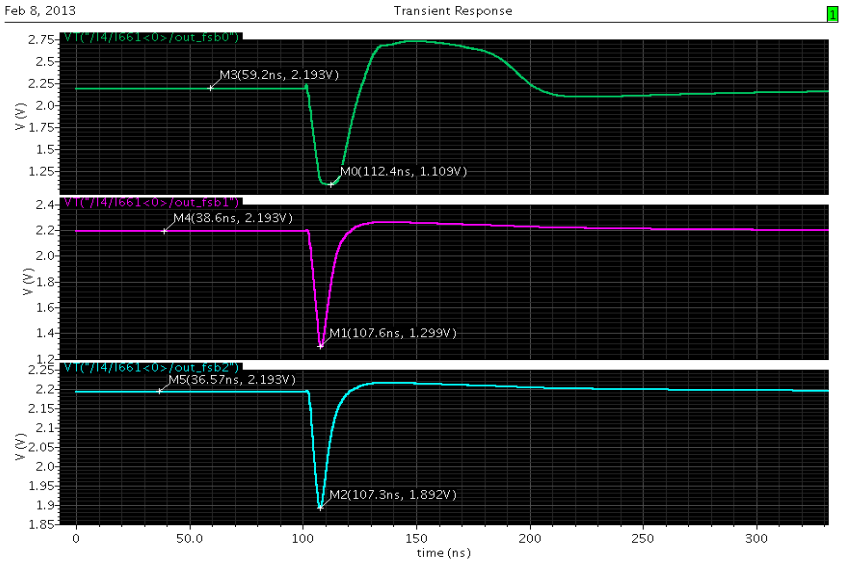


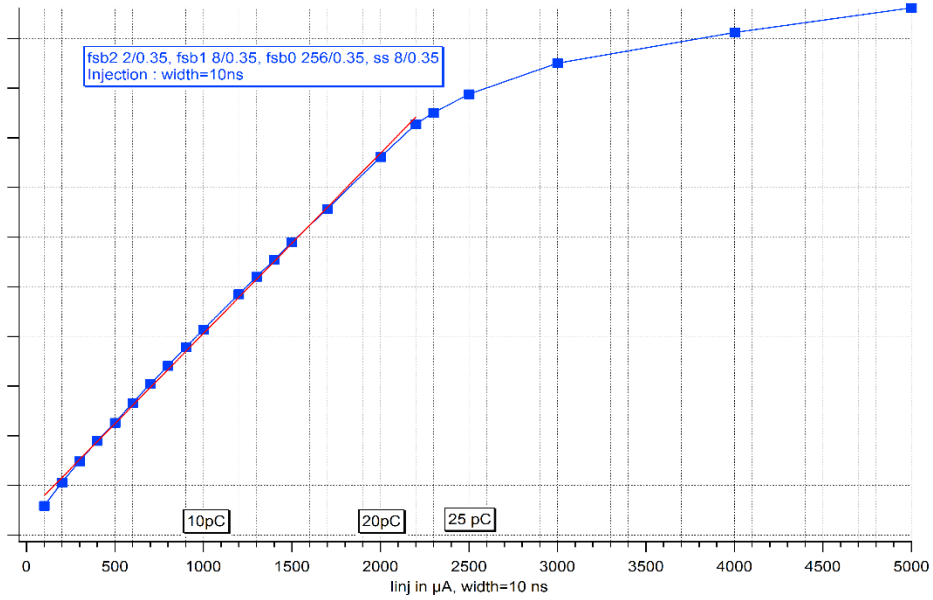
1 m^3 RPC detector, 40 layers
Hardroc2B: 400 000 channels

ANALOG PART (Simulations)







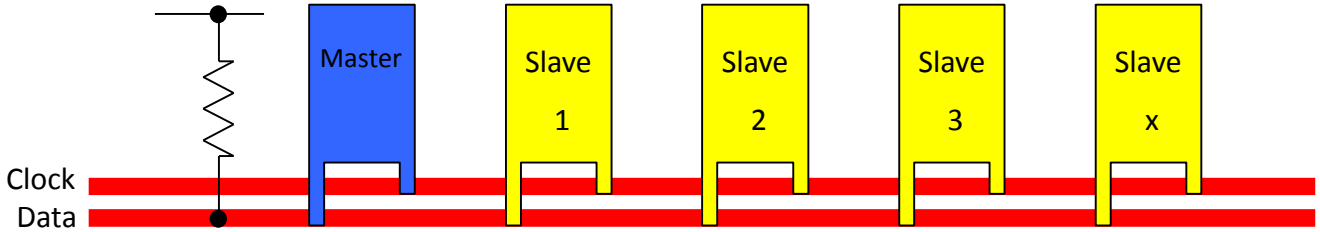


New Slow Control: I2C

- I2C standard protocol access (max 127 chips / line)

- Possibility to broadcast a default configuration to all the chips
- Read and write access to a specific chip with its geographical address

- Triple voting for each parameter (redundancy)
- Read back of control bit (even if the chip is running / non destructive)

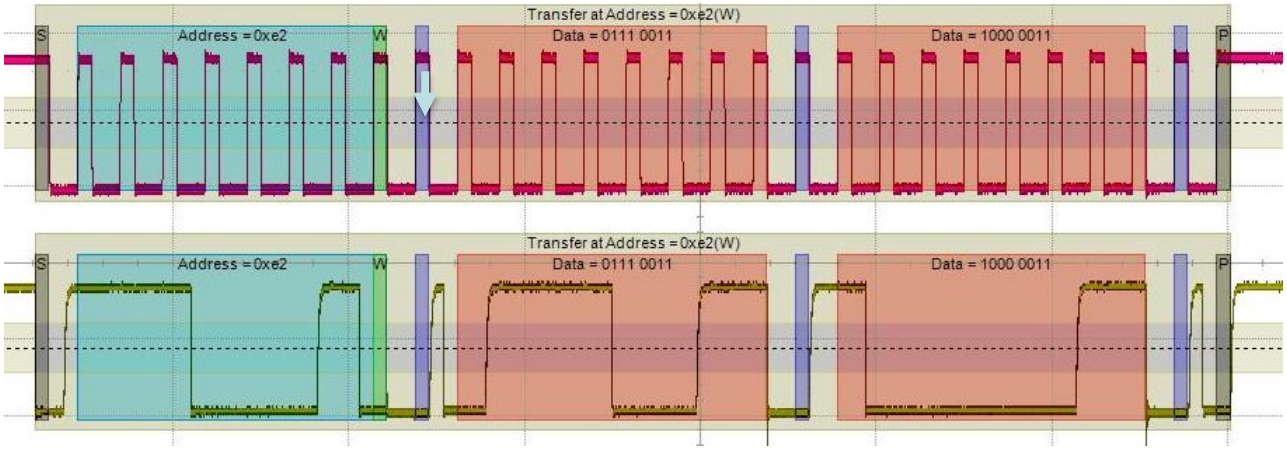


Write frame:

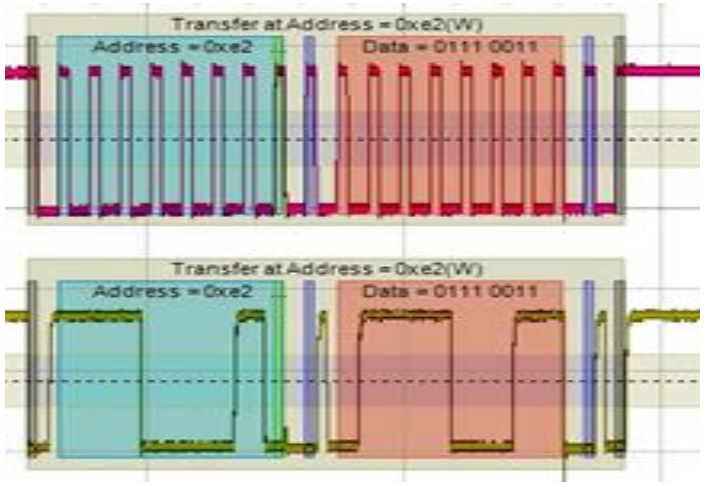
Read frame:

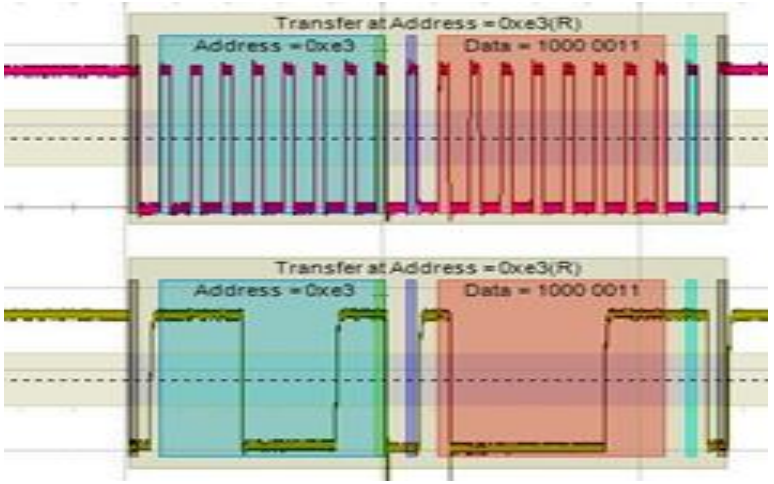
I2C measurements

- I2C Write access : Chip number (ID): 0xE2 / Reg @: 0x73 / WrData: 0x83



- I2C Read access : Chip number (ID): 0xE2 / Reg @: 0x73





3Gen ROC chips: Slow Control

- Extra pin needed for I2C / SC:
- Possibility to choose between old SC registers/ New I2C link (Select_I2C_SRb available on one pin)

HR 2		HARDROC 3		
sr_in	1	sr_in	1	
sr_out	1	sr_out	1	
sr_clk	1	sr_clk	1	Also for I2C
sr_rstb	1	sr_rstb	1	Also for I2C
		Loadb_sc	1	
		SC_WR_RDb	1	Read back SC
		Error_SCb	1	Triple V. error
		Select_I2C_SRb	1	Select old/new SC
		Select_I2C_Port	1	2 I2C ports
		7-bit I2C: ChipID<0:6>	7	PCB hardwired I2C address
		2 x (I2C_clk / I2C_data)	4	2 I2C ports
Total	4	Total	4+16	

Standard SC

SC with triple voting

I2C

SC parameters

- Old SC registers/ New I2C link: choice with Select_I2C_SRb

- Bank 1 (WR1, clk1, Load1):
  - 64x8 (gain preamps) + 64 Ctest = 576 bits

- Bank 2 (WR2, clk2, Load2):
  - 3x64 Mask= 192 bits

- Bank 3 (WR3, clk3, Load3):
  - 3 DACx(10 bits +pwr on +EN) + BG (EN+PP) + Temp sensor(EN, PP)=40 bits

- Bank 4 (WR4, clk4, Load4):
  - bias (10 digital and 39 analog) + trigger cell (12) +PLL + spare= 80 bits

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Acquisition :
Each channel contains a memory to store up to 8 events. For each event, 14 bits are written into the memory : 12-bit BCID counter + 2-bit encoded charge.

Readout :
The readout is in 3 phases :
- first phase : readout of Chip ID (I2C address on 7-bit)
- second phase : for each channels which contains events it sends general purpose data = channel number with its number of events stored
- third phase : readout of the memory in all the channels (only channels with events)

Clocks :
2 clocks are needed :
- fast clock for state machine (40-50 MHz)
- slow clock for BCID counter and readout (up to 10 MHz)

During acquisition : Fast and Slow clocks used (state machine and timestamps)
During readout : only slow clock is needed

I2C :
SDA / SCL lines duplicated for redundancy (SDA1/SCL1 and SDA2/SCL2) selectable by the "SelectI2C" port
Maximum frequency : to be tested (not more than 1MHz)
Pull-up resistor for open-collector lines : to be tested, depends on frequency
The physical chip address is on 7 bits and hard wired on PCB
Register address inside chip is on 8 bits (115 registers of 8 bits in HR3)

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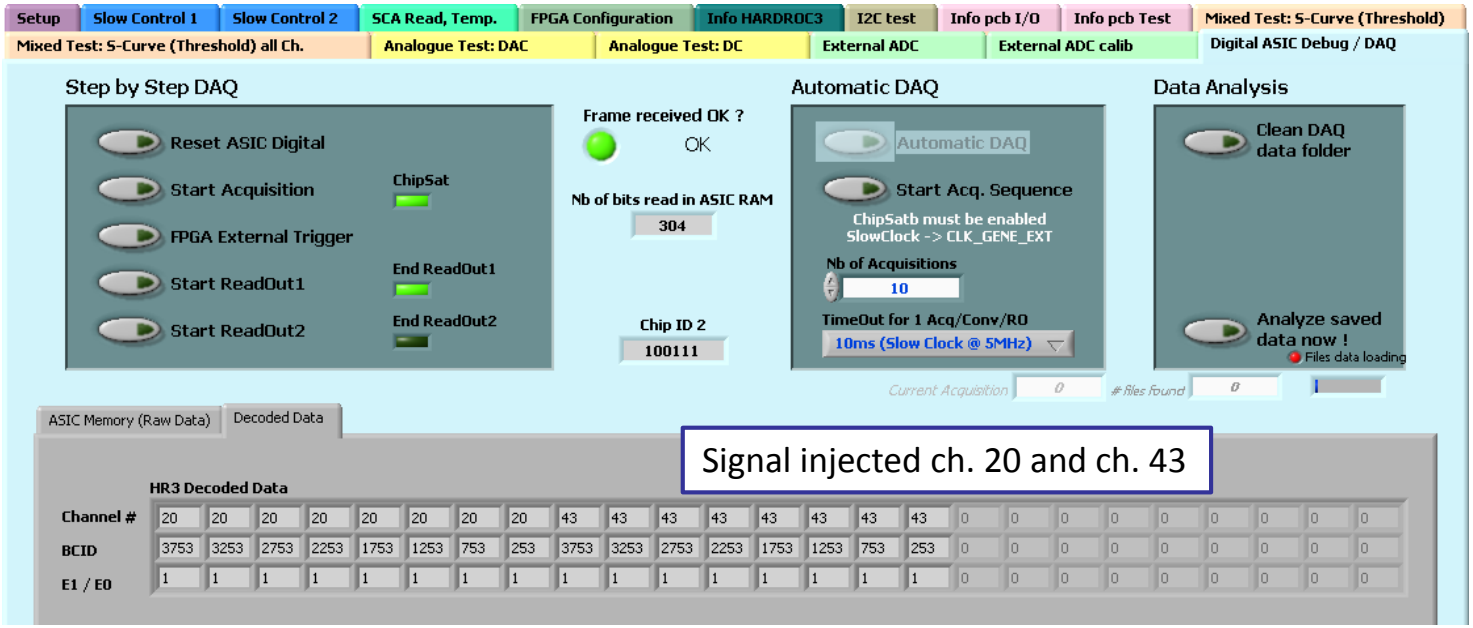
Zero suppress: Tests

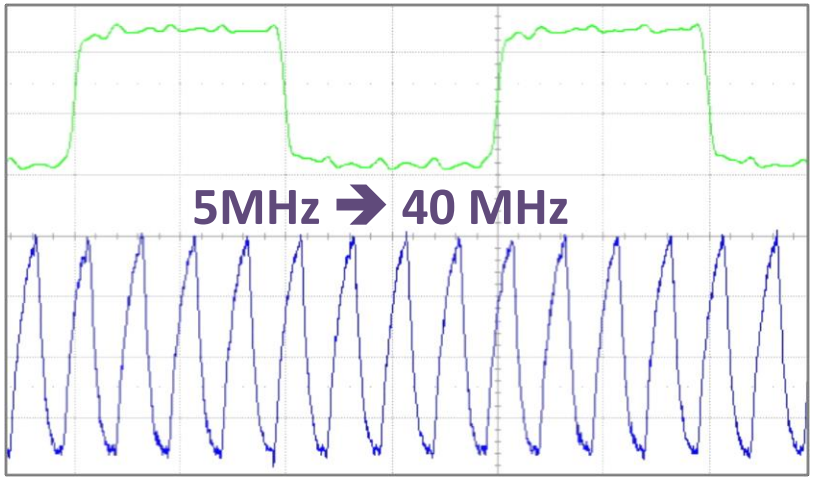
- Zero suppress (only hit channels are readout): test OK



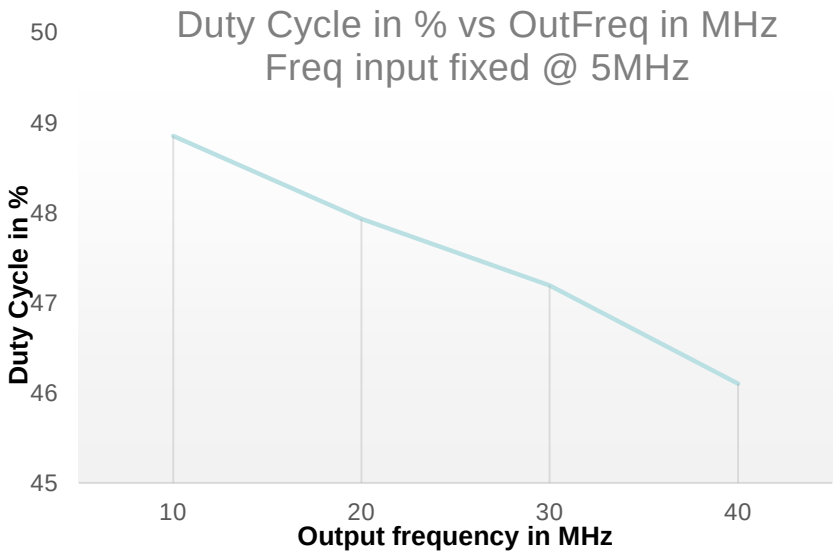
- Roll mode SC : test OK
  - If RollMode = "0" ➔ Backward compatibility with 2Gen ROC chips behavior
    - Only the N first events are stored
  - If RollMode = "1" ➔ 3Gen ROC chips behaviour
    - Use the circular memory mode
    - Only the N last events are stored
- "Noisy Evt" SC: 64 triggers => Noisy event => no data stored : test OK
- "ARCID" SC (Always Read Chip ID): test OK
  - If ARCID = 0 ➔ Backward compatibility: No event ➔ No readout
  - If ARCID = 1 ➔ New behavior: No event ➔ Read CHIP ID

PLL measurements

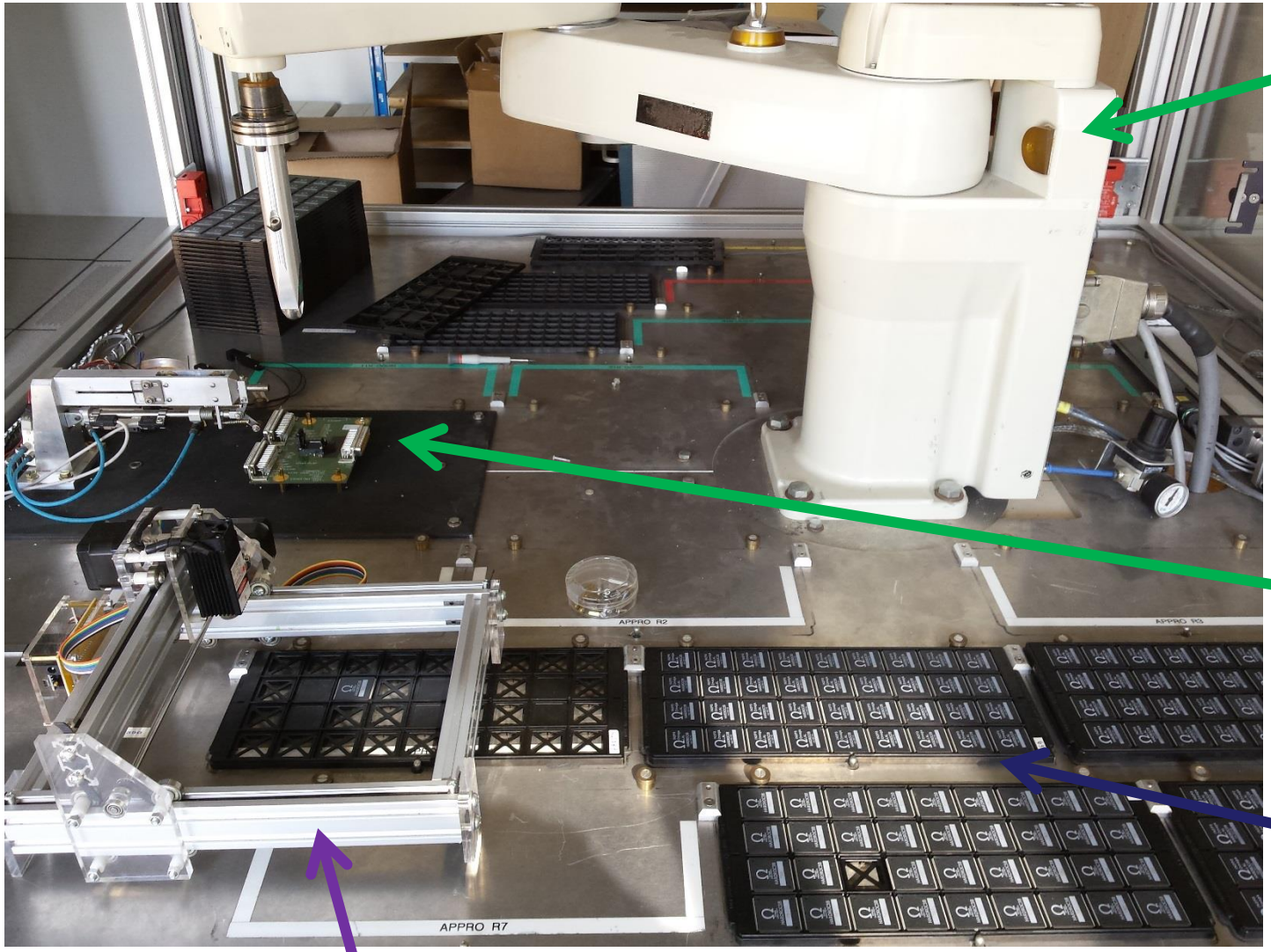
- **2 clocks are needed to start the chip**
  - Slow Clock (1-10 MHz) related to the beam train (for Time stamping and data readout)
  - Fast clock (40-50 MHz) for internal the state machines



- **A PLL (clock multiplier) has been designed to generate the fast clock**
  - Multiplication factor is (N+1) / N is a SC parameter (1 to 31)
  - Full chain tested using PLL



HR3 production tests setup



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HR3 production tests

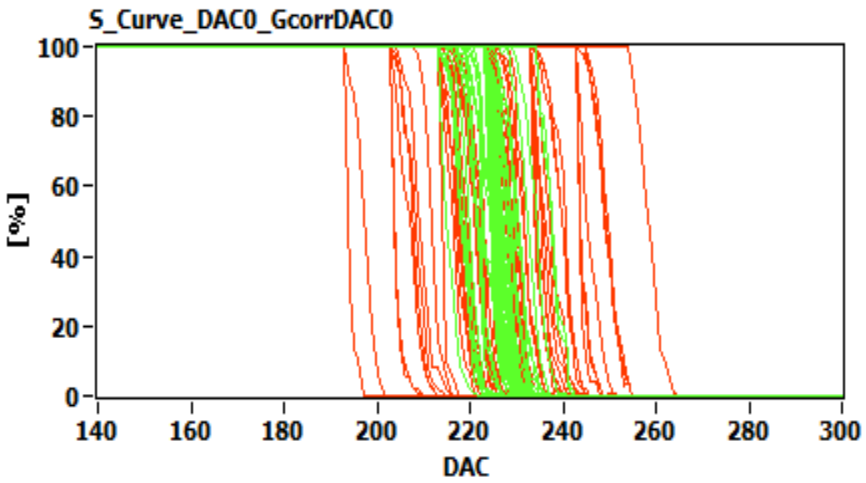
Laser engraving with a robot @ IPNL

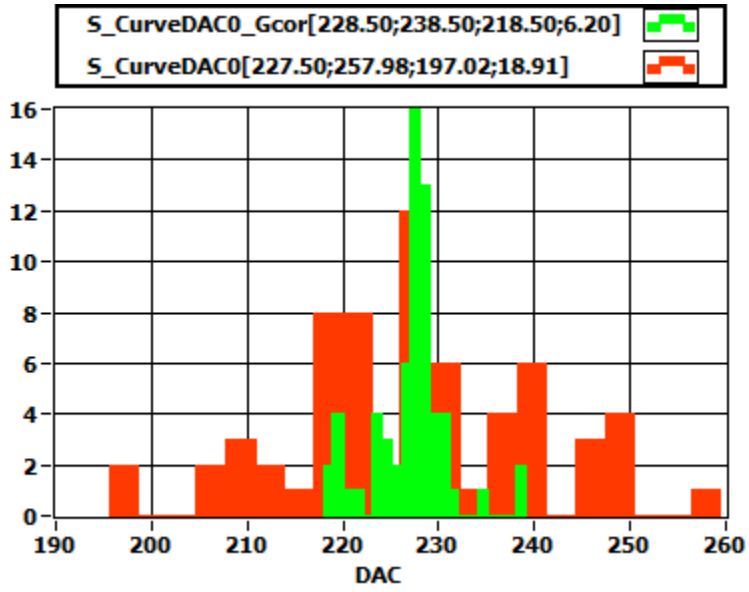
H3B TESTED : 786

Yield : 83.3 %

The majority of discharges :
Dead Channels

Injection : 100 mV on Ctest (64 Ch)
Gain = 144

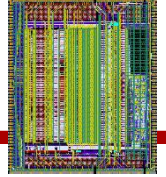




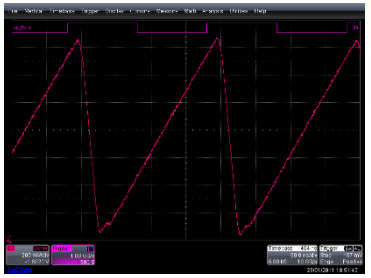
SKIROC2A

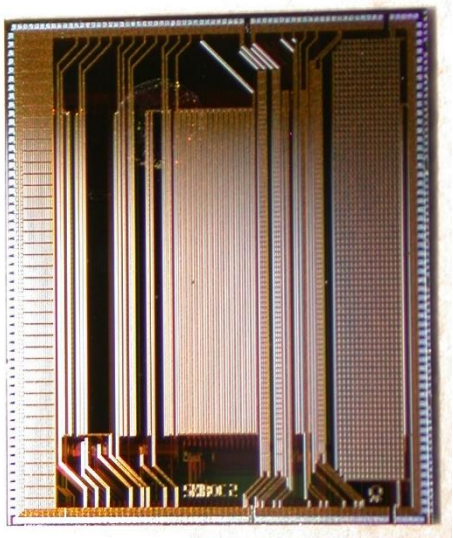
Organization for Micro-Electronics desiGn and Applications

SKIROC2(A)



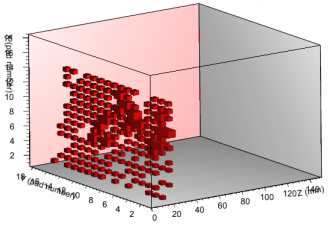
- Properly working, but few bugs/mistakes/coupling
  - Event w/o hits (artefact due to ASIC clock/beam synchronization)
  - Plane events (modify the power management on the FEV itself)
  - Channel to Channel cross talk for large signal
  - Channel to Channel Trigger Adjustment (too little effect)
  - Different pedestal per memory cell (would require power)
  - External Trigger creates noise
  - Some ‘0’ events during readout
  - Auto Gain selection when using TDC
  - TDC has 30% of dead time @5MHz
  - TDC noisy, avoid 1MIP trigger
  - Test system for naked dies





Skiroc2A : Corrected / No change

Small internal improvements



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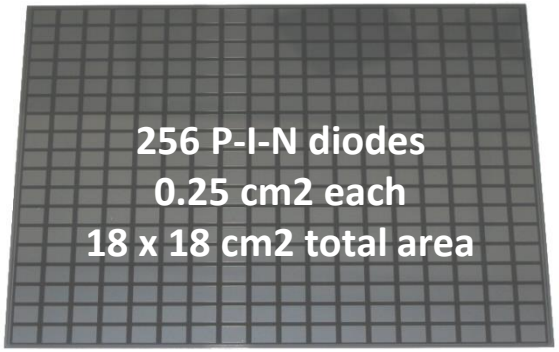
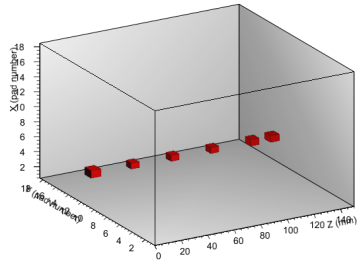
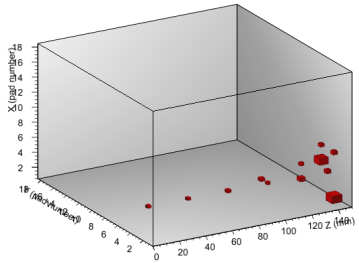
SKIROC2A Modifications

- BUG CORRECTIONS
  - Some « Zero events » during digitization **: OK** (added delays, cf. SP2C)
  - Substrate Shielding, Inputs Shielding **: IMPROVED** (added connections)
  - Test mode for naked dies (voltage drop off & missing pads) : CORRECTED (but not tested, N/A in BGA package)
  - Trig Ext path no more thru delay cells to store the analog data **: OK**
- IMPROVEMENTS
  - 4-bit DAC for trigger level adjustment **: OPTIMIZED to 1 DAC unit**
  - Bandgap **: CHANGED** (from HR3)
  - Delay Cell : Slightly IMPROVED
  - AutoGain Selection **: CHANGED : OK** (from SP2C)







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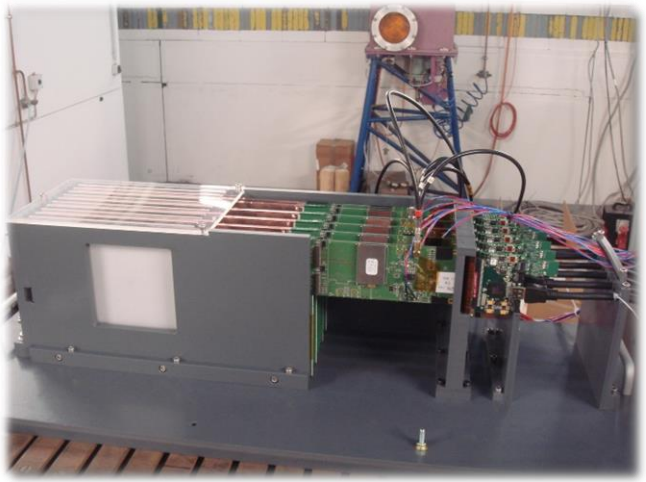
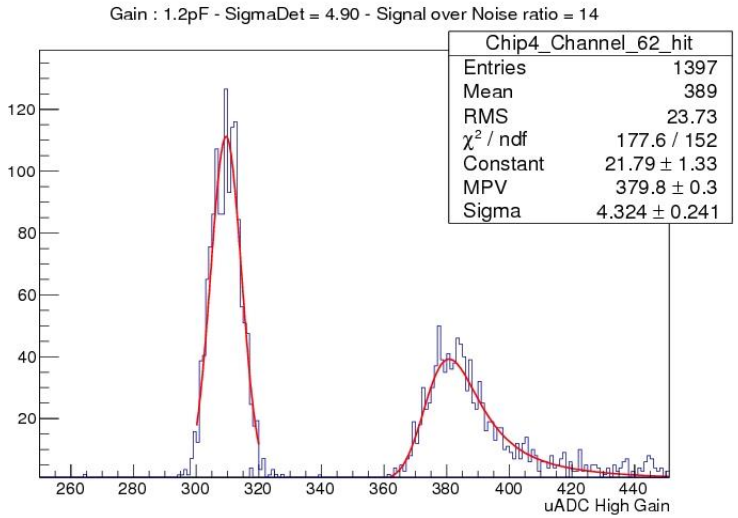
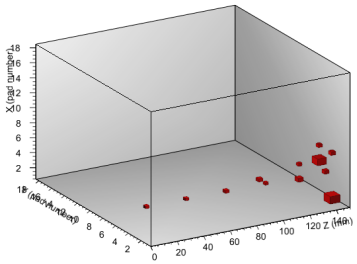
SKIROC2A Modifications

- SUGGESTIONS
  - PLL to generate the 40MHz (avoid 40MHz clock distribution) **: not in SK2A**
  - 15 depth SCA dynamically switched ON w.r.t. the events occured **: not in SK2A**
  - TDC architecture change **: YES, FROM SP2E**
  - Power ON reset for probes **: ADDED**
  - Peak Detector to sample the maximum **: NO**
  - Power DAC_trigger and DAC_Gain_Select independent **: not relevant**







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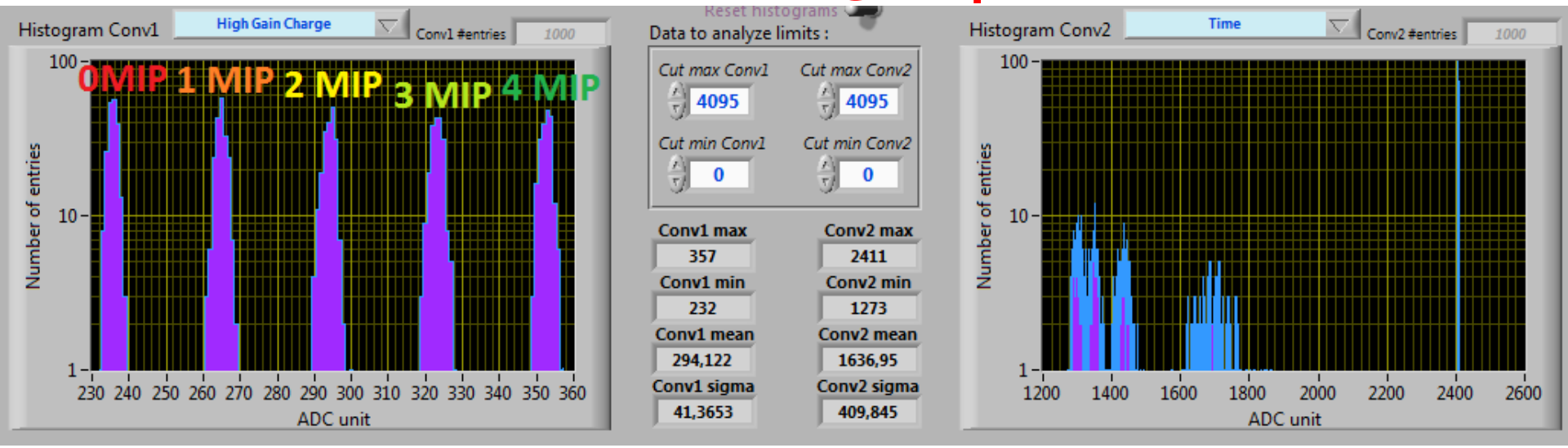
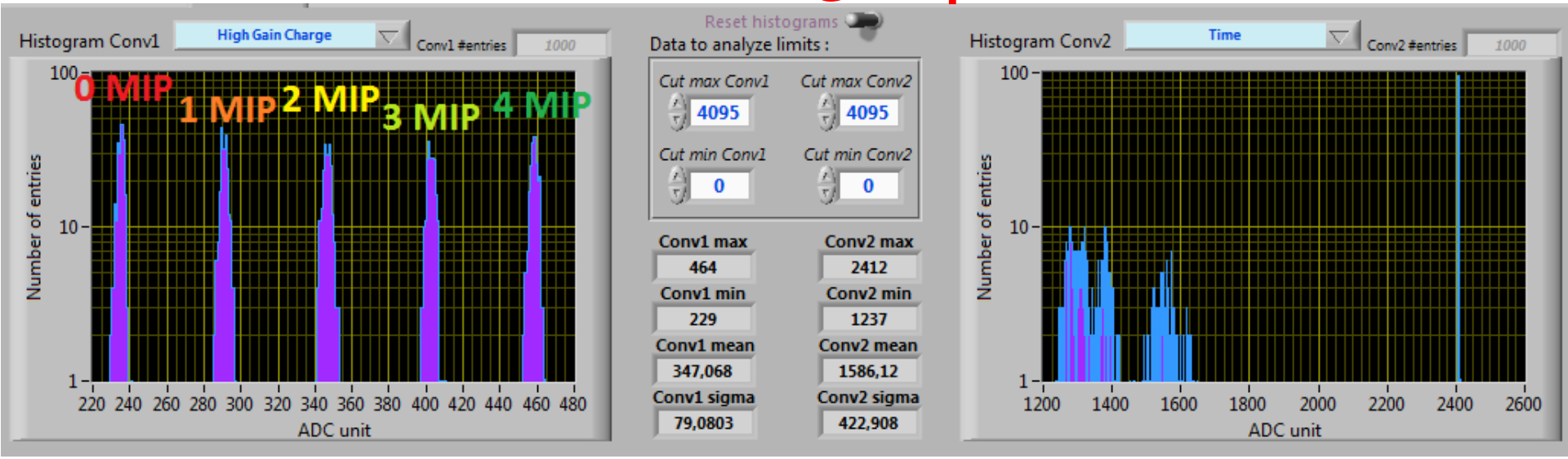
SKIROC2A : histogram

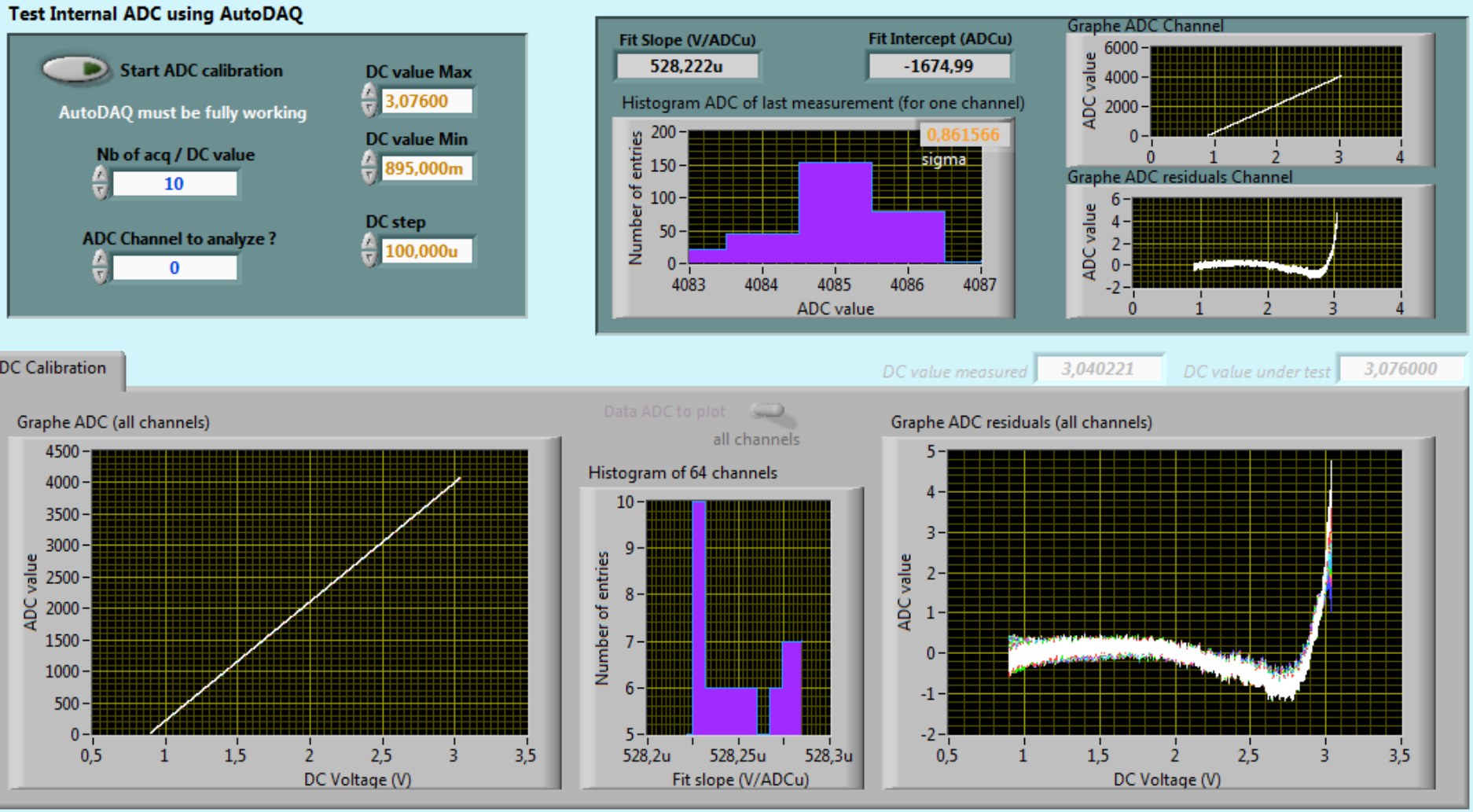
PA Gain @ 2.4pF



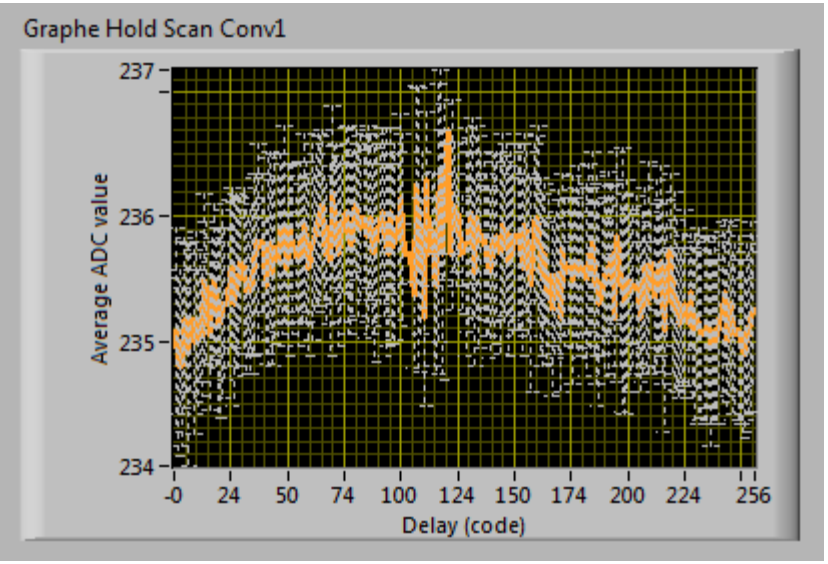
PA Gain @ 1.2pF



SKIROC2A : ADC Linearity



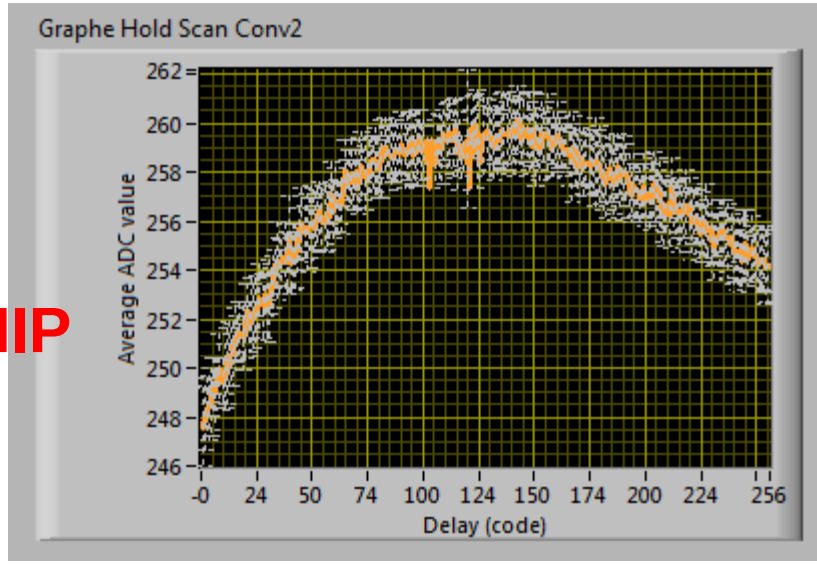
SKIROC2A : Hold Scan



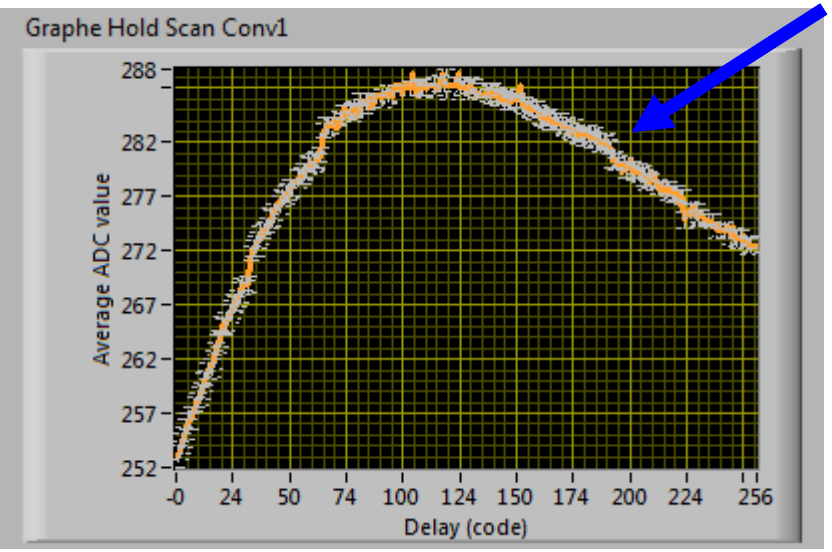
PA Gain

@ 6pF

Qinj = 2MIP



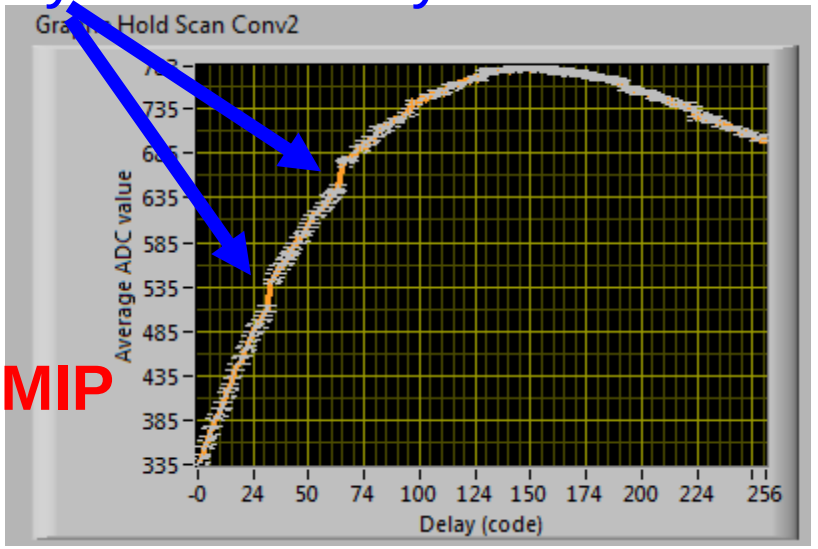
Non linearity due to delay box



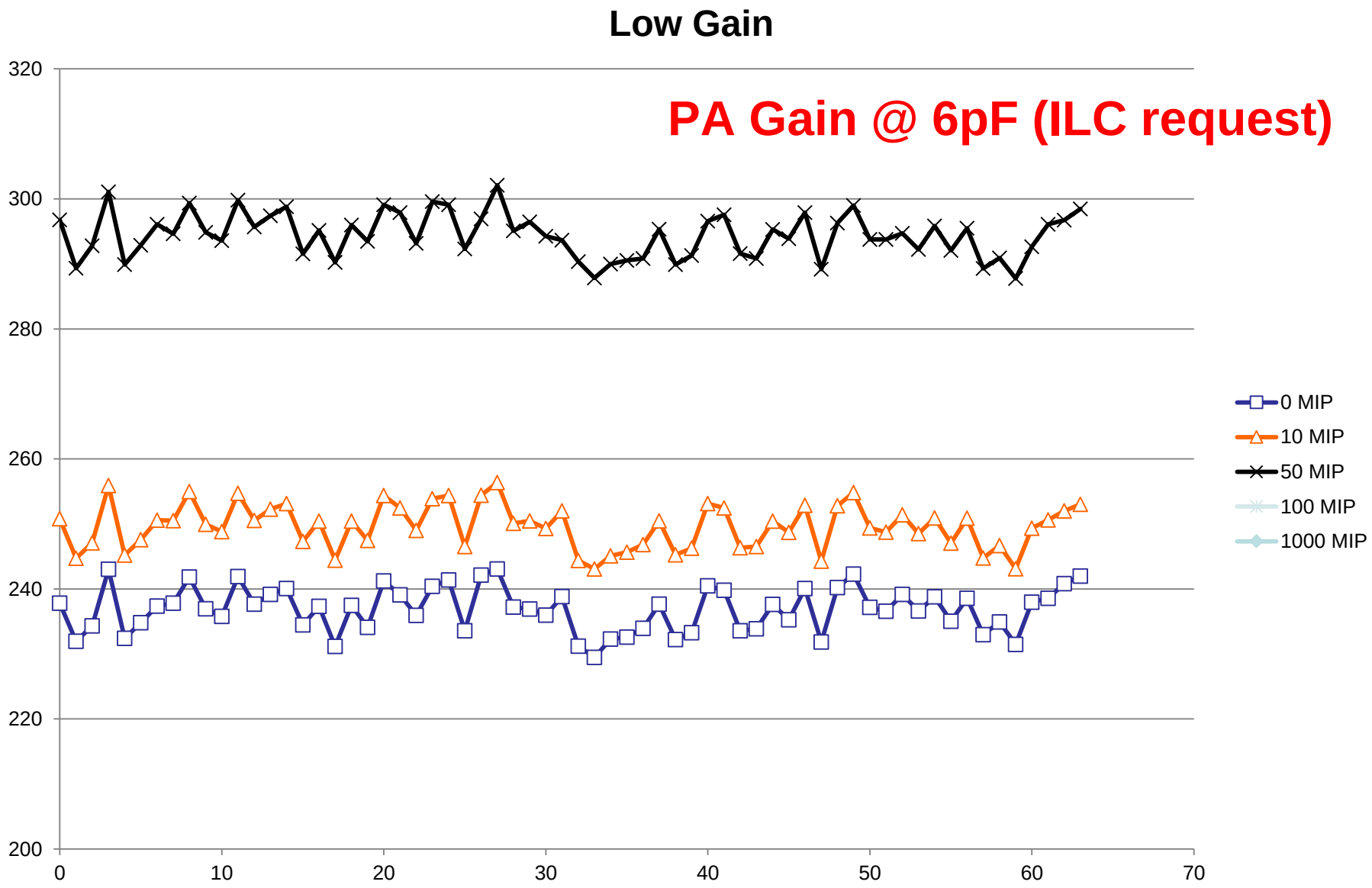
PA Gain

@ 1.2pF

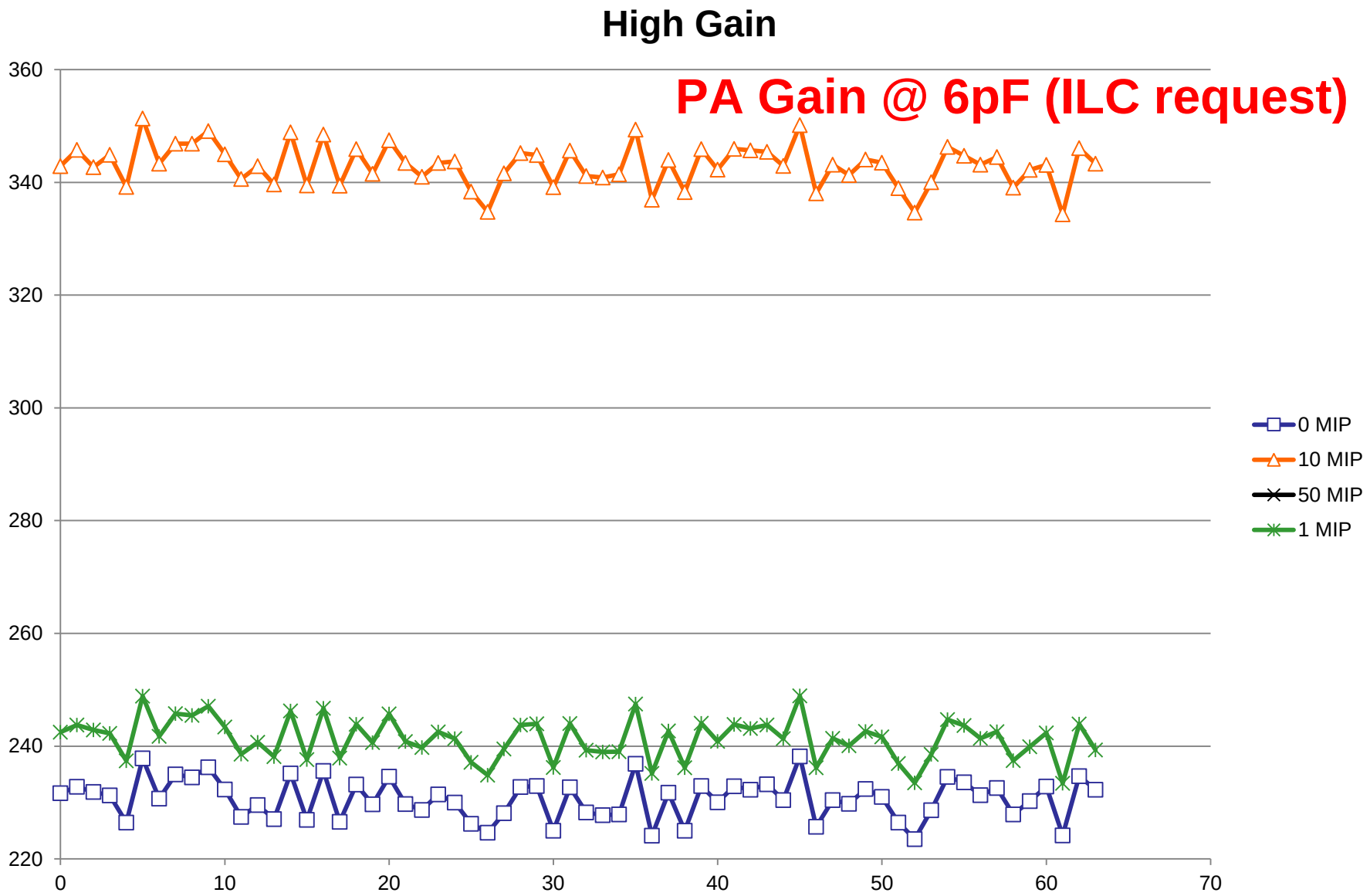
Qinj = 10MIP



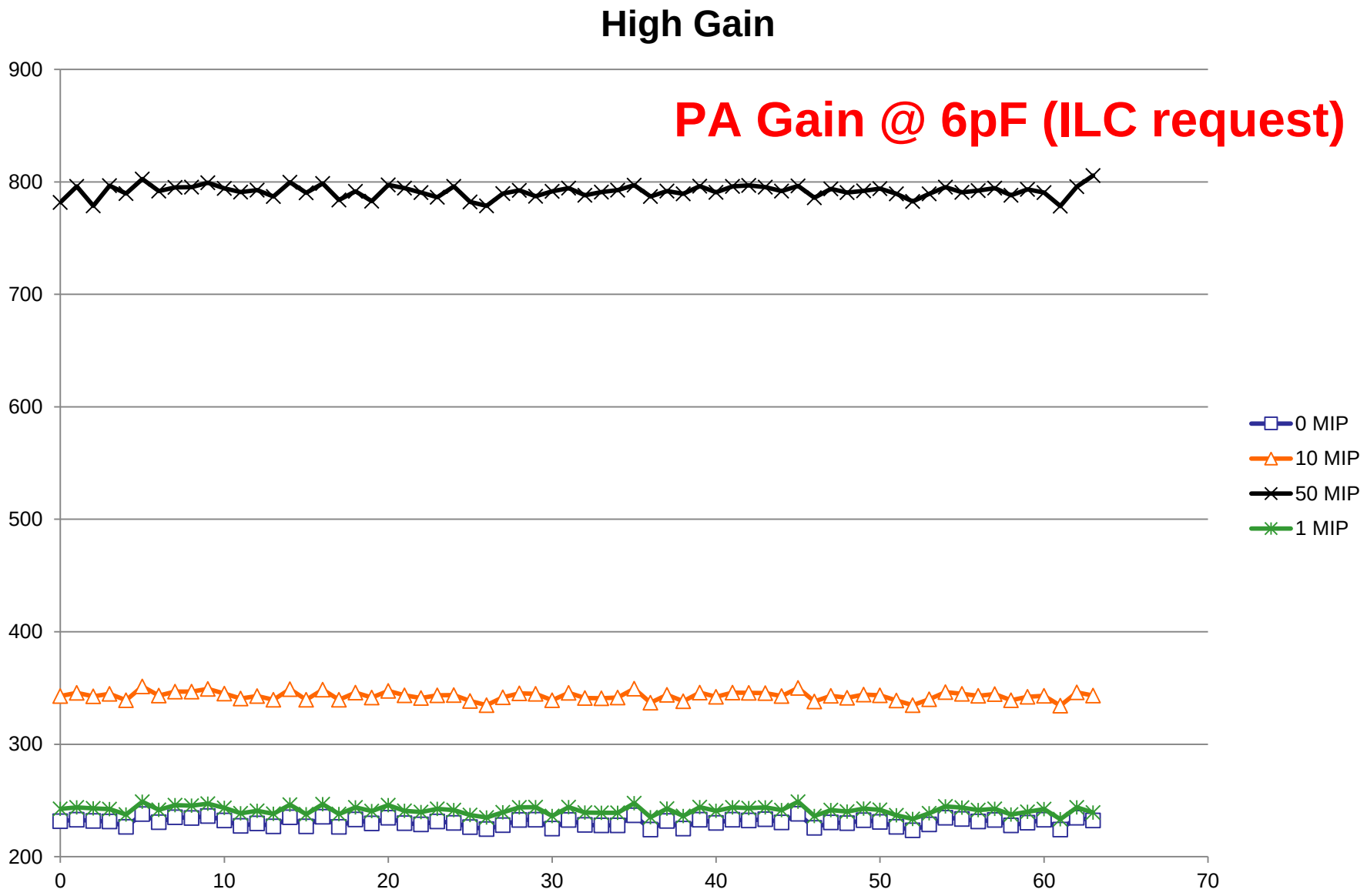
SKIROC2A : Low Gain Uniformity



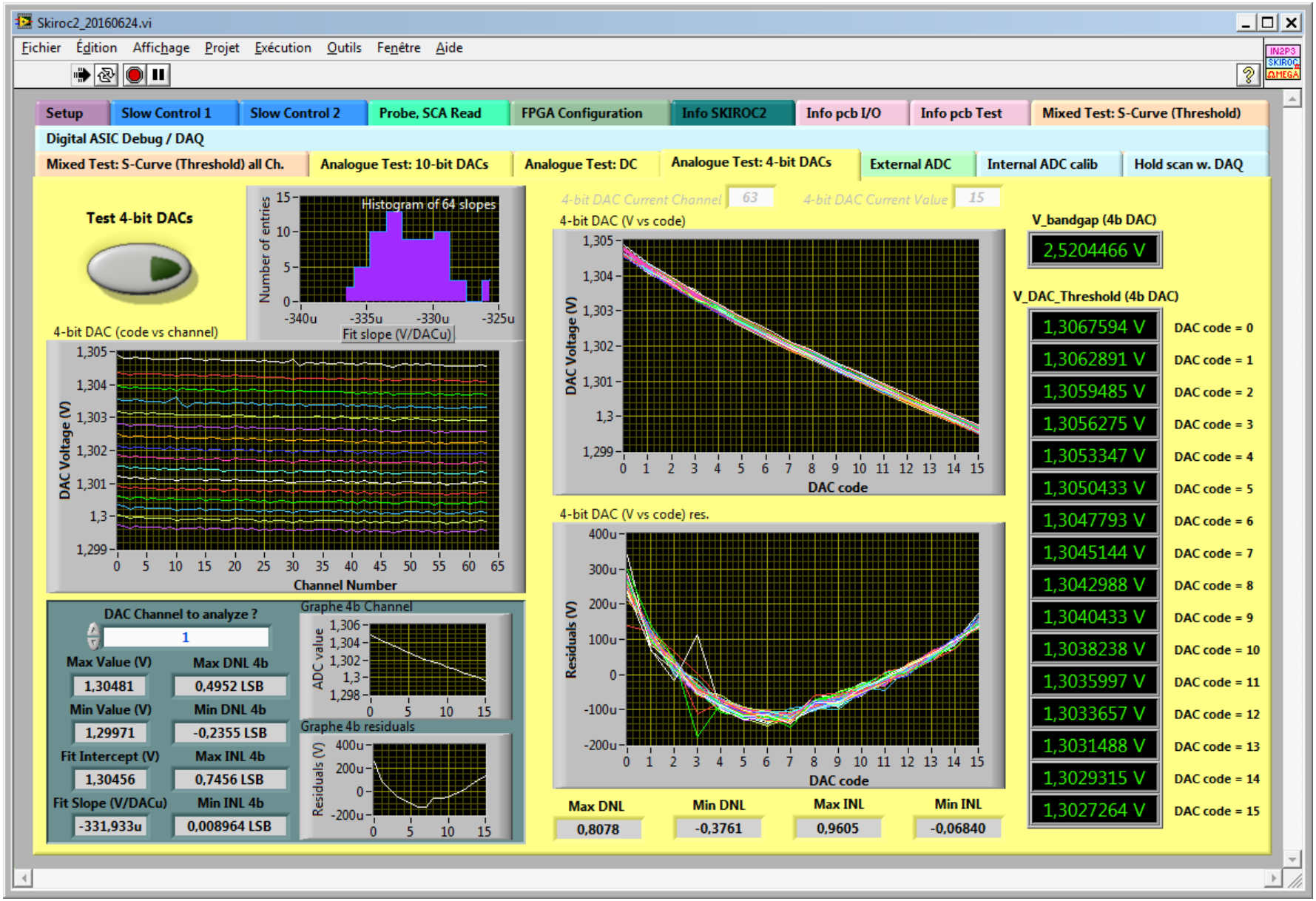
SKIROC2A : High Gain Uniformity



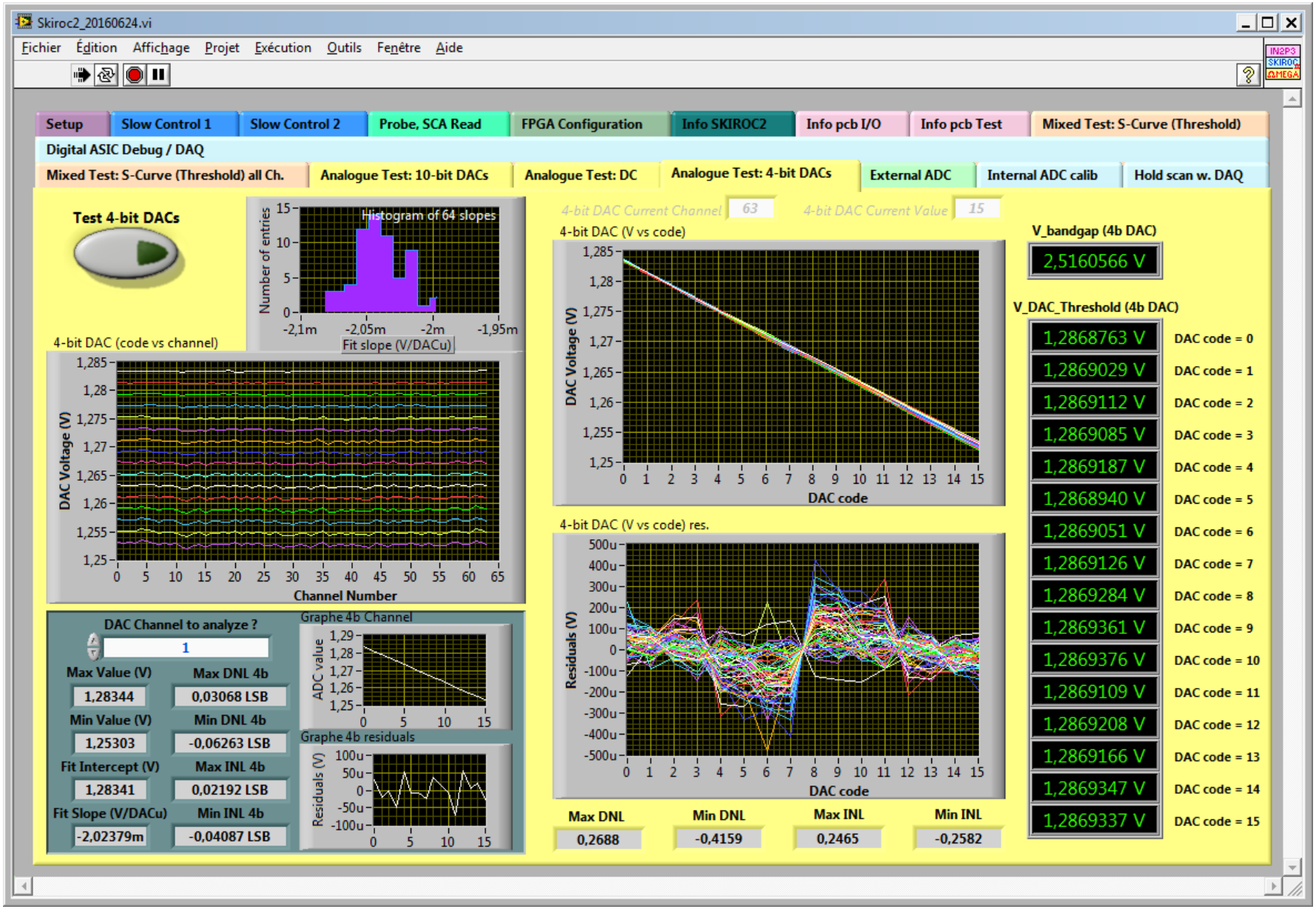
SKIROC2A : High Gain Uniformity



SKIROC2 : 4-bit DAC

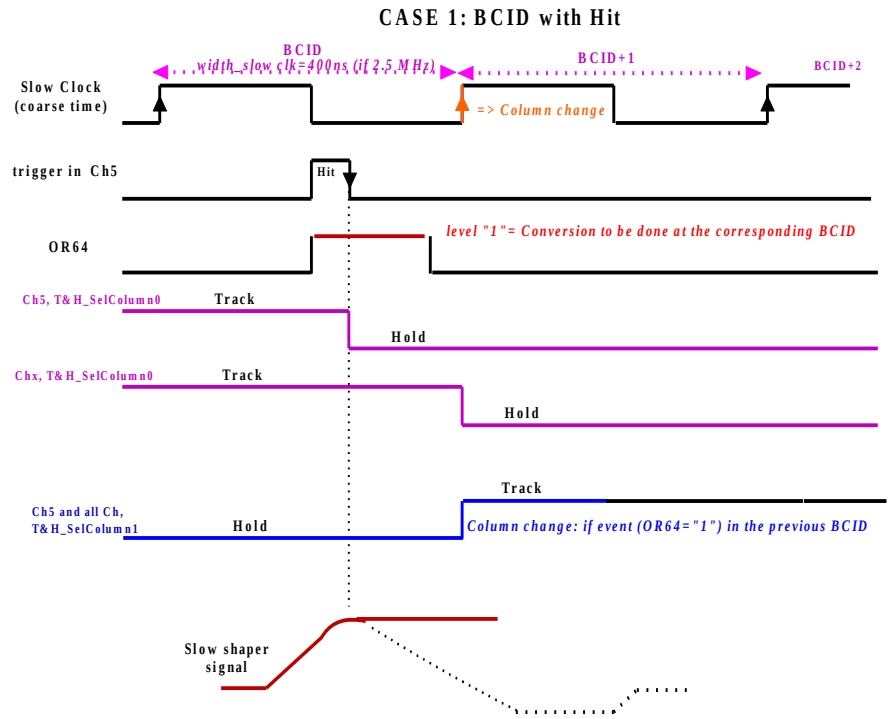


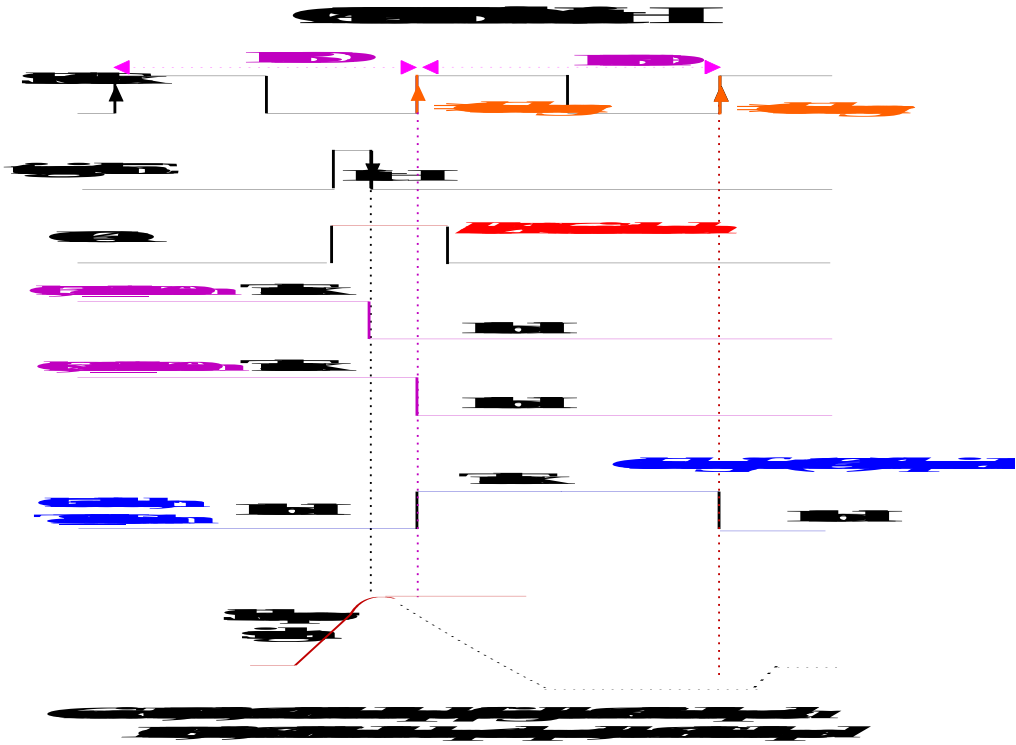
SKIROC2A : 4-bit DAC



BCID+1 without Hit in SKIROC2

Probability of such events= Width NOR64_delayed / width Slow Clock

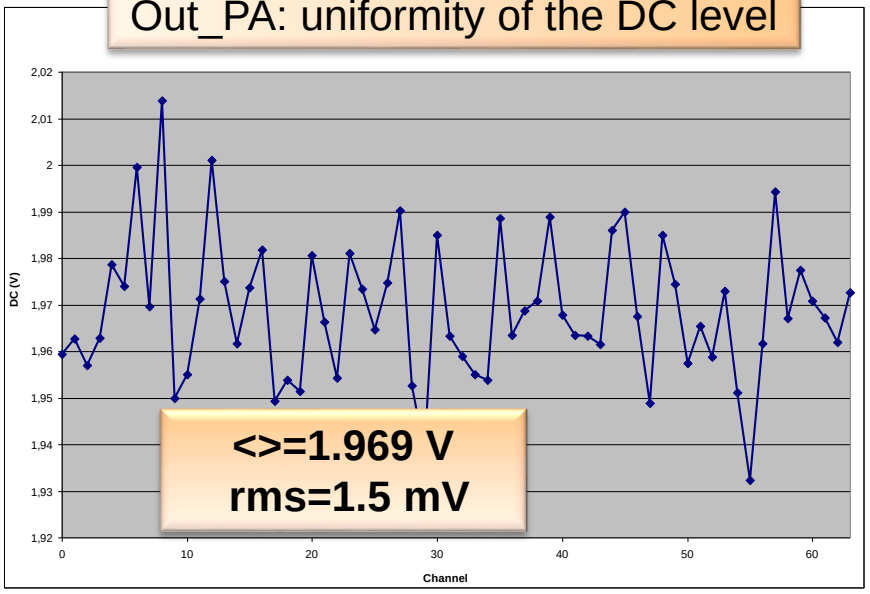




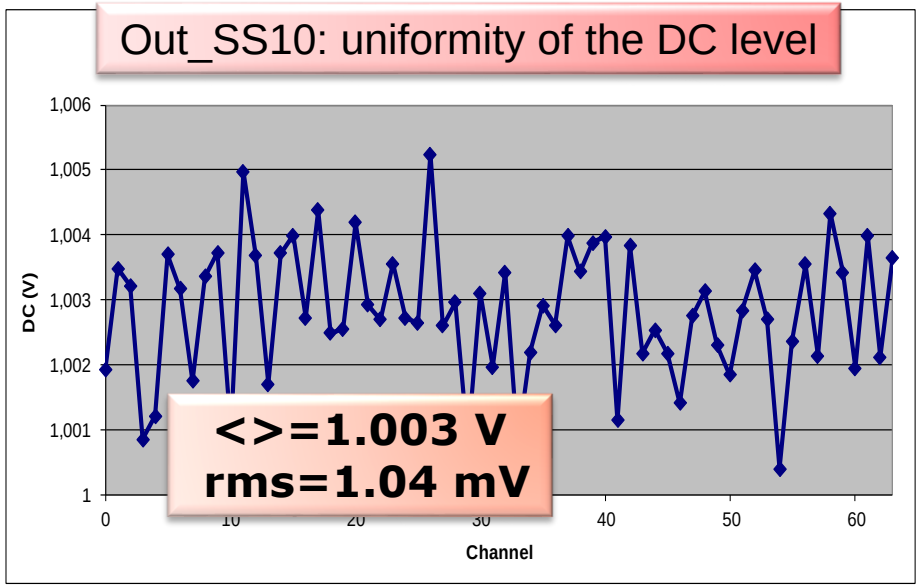
Conversion: BCID with one hit, SCA0 ch5: holded value= peak of the signal, other SCA0= holded value=pedestal, other SCAi= ped
BCID+1: No conversion because OR64 level=0 during this BCID+1

SKIROC2: DC PreAmp, Fast and Slow Shapers

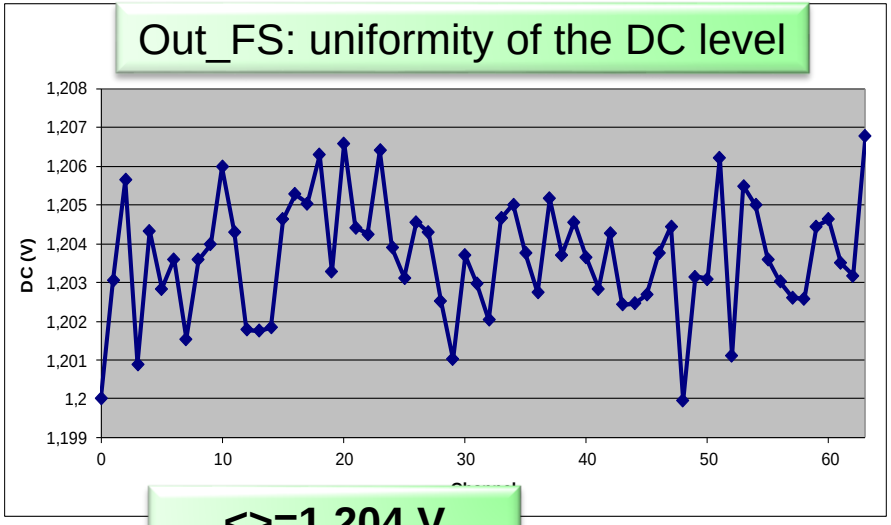
Out_PA: uniformity of the DC level



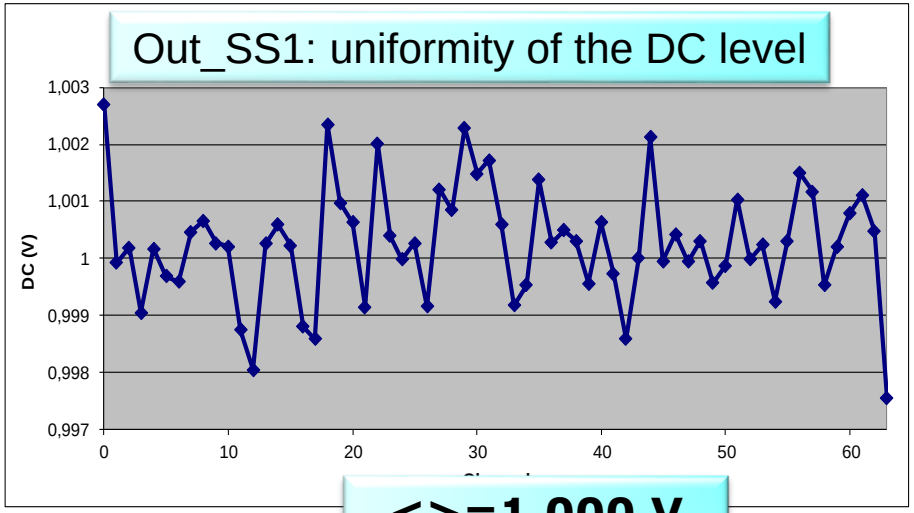
Out_SS10: uniformity of the DC level



Out_FS: uniformity of the DC level



Out_SS1: uniformity of the DC level



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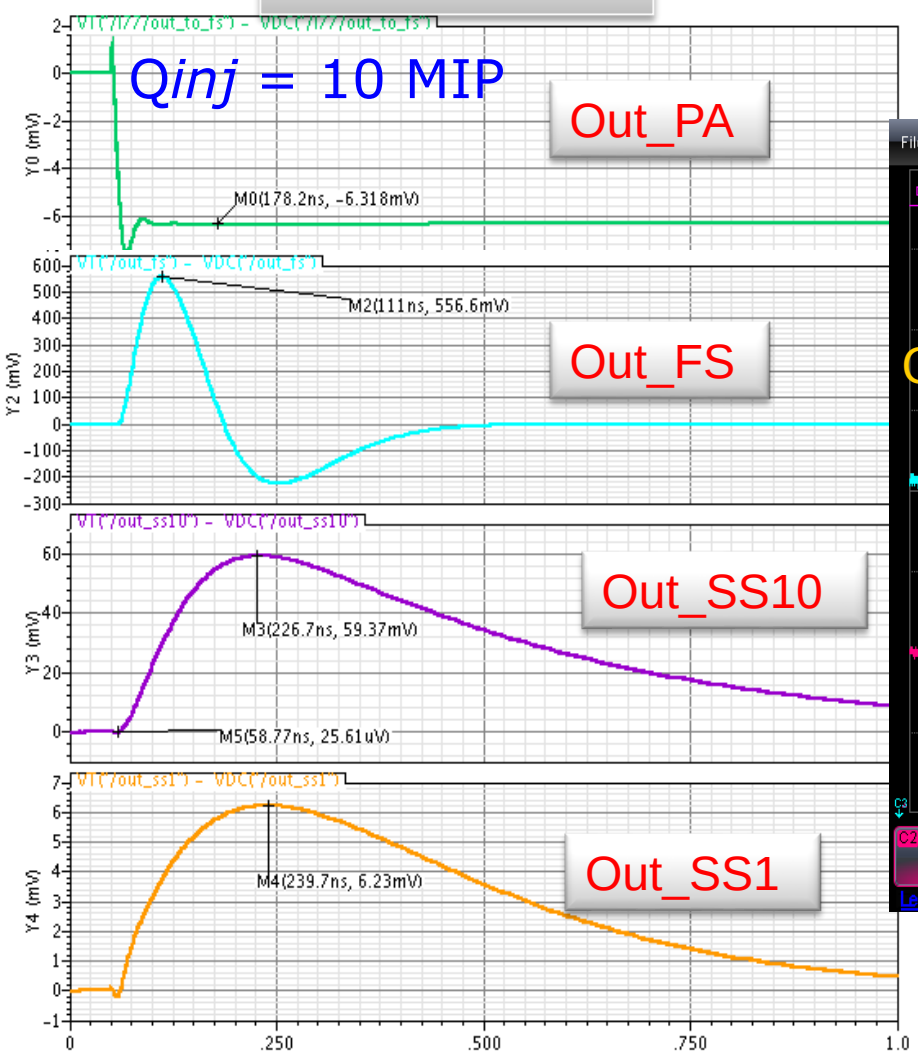
SKIROC2 Analogue Simulations

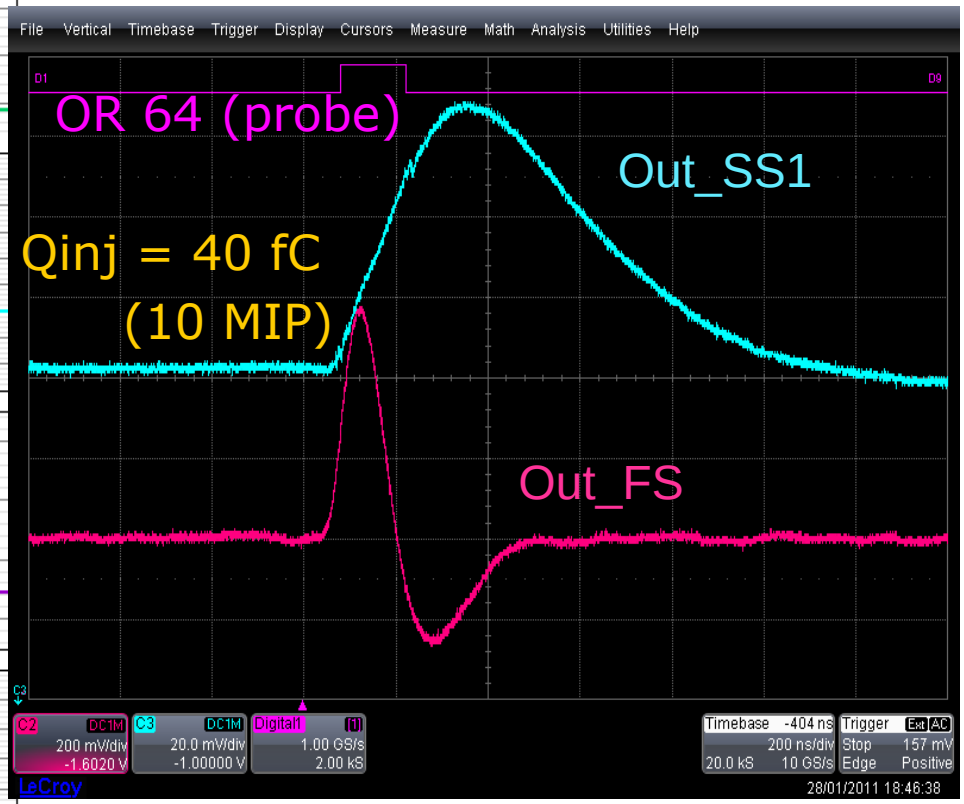
Q inj	Out_PA	Out_SS1	Out_SS10
1 MIP	639.6 µV	623.7µV	6.65 mV
10	6.32 mV	6.236mV	66.47 mV
100	63.2 mV	62.33 mV	664.1 mV
200	126.4mV	124.7 mV	1317 mV
500	315.9 mV	311.5 mV	Saturation to 1.5V
1000	631.6 mV	622.4 mV	
2000	1252 mV	1234 mV	
2500	1465 mV	1437 mV	

SKIROC2 Analogue Simulations/Measurements

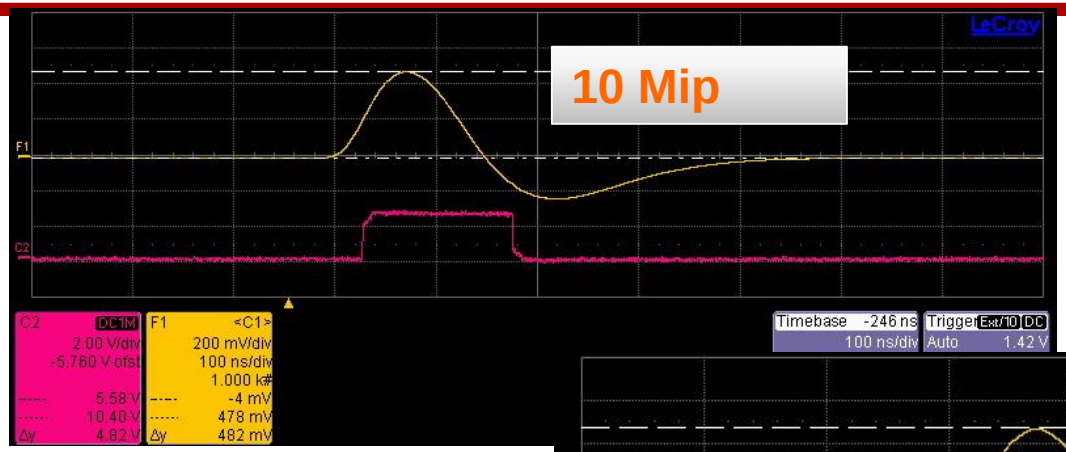
SIMULATIONS

MEASUREMENTS

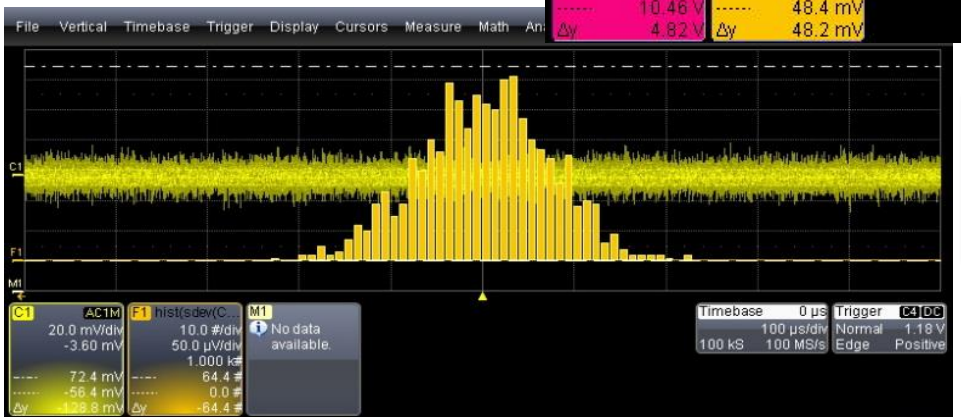




SKIROC2: Fast Shaper noise



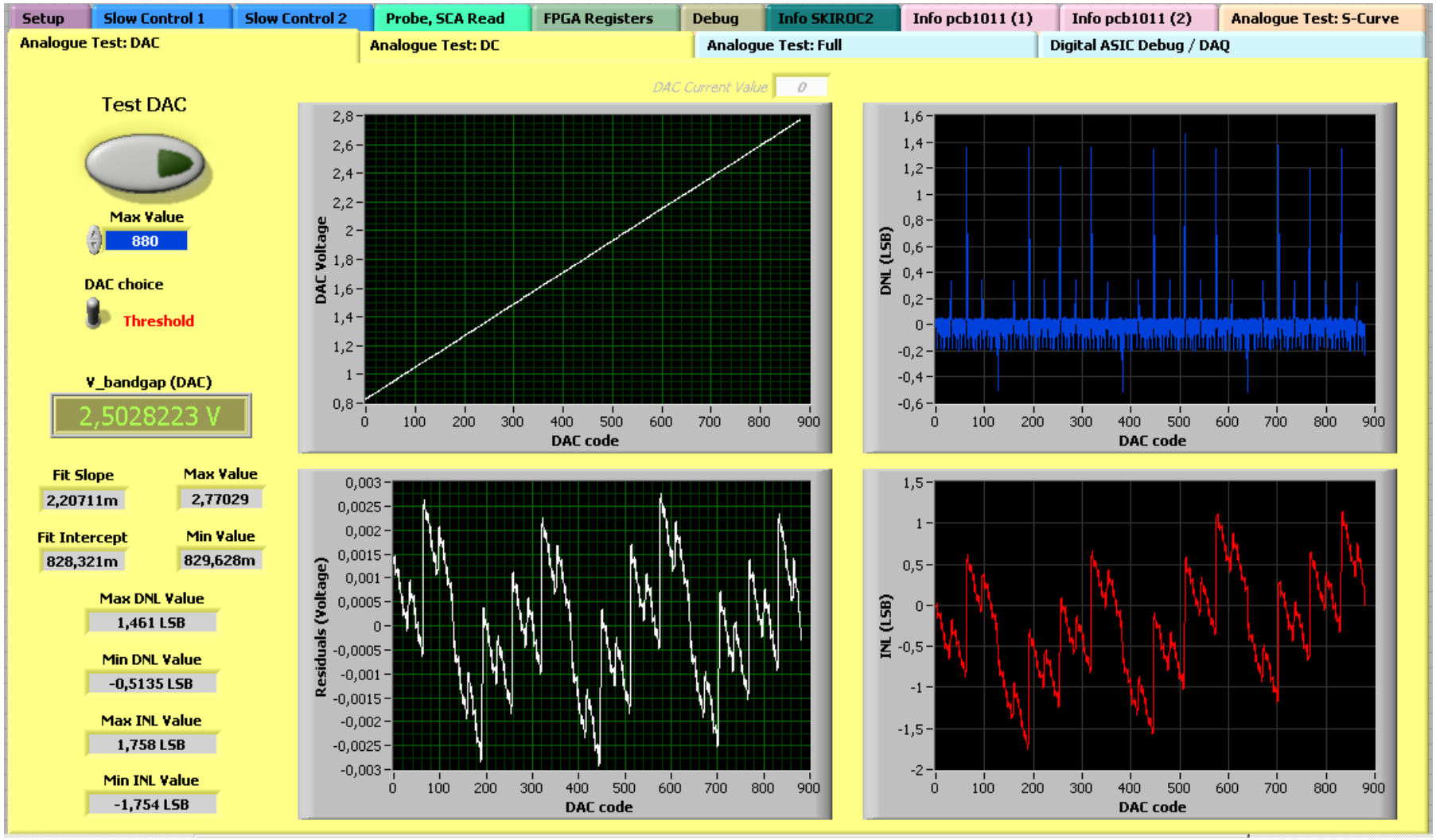
Fast Shaper
~ 48mV/Mip



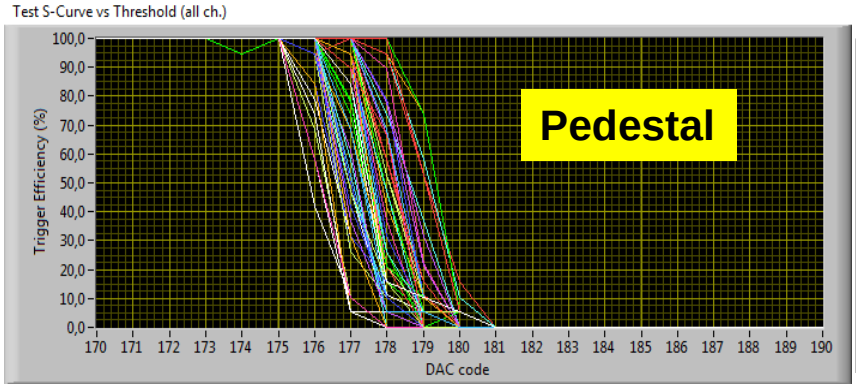
rms noise= 5.3 mV ie 1/9 MIP
S/N=9

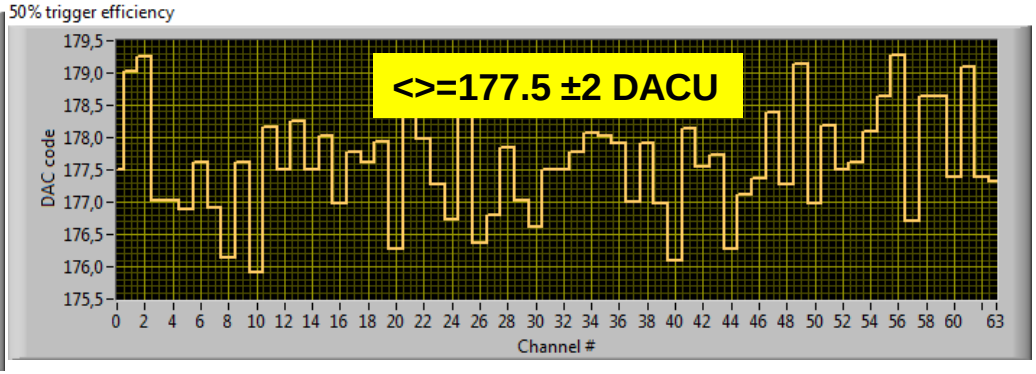
DAC Threshold Linearity

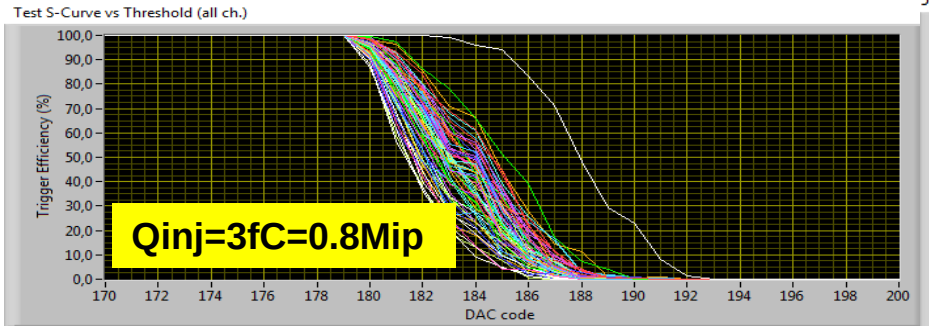
Slope 2.2 mV/DAC Unit, DNL ±1LSB INL= ±1.7LSB

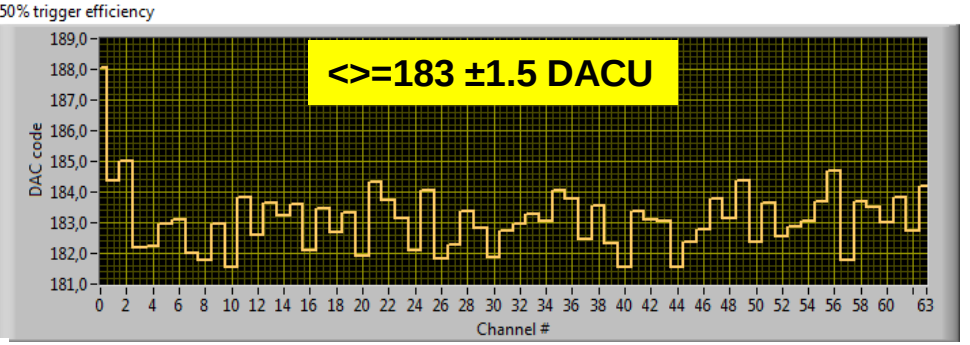


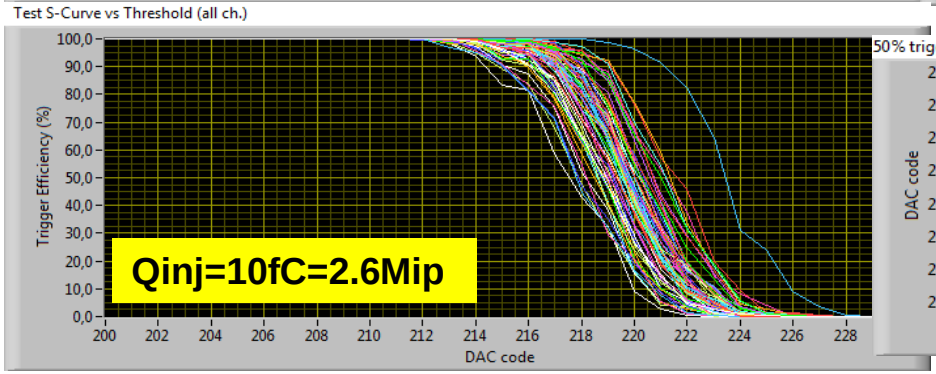
Trigger efficiency (1)

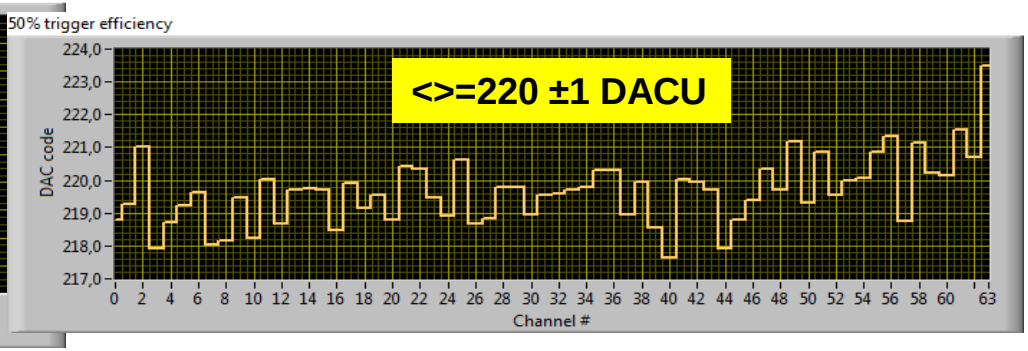




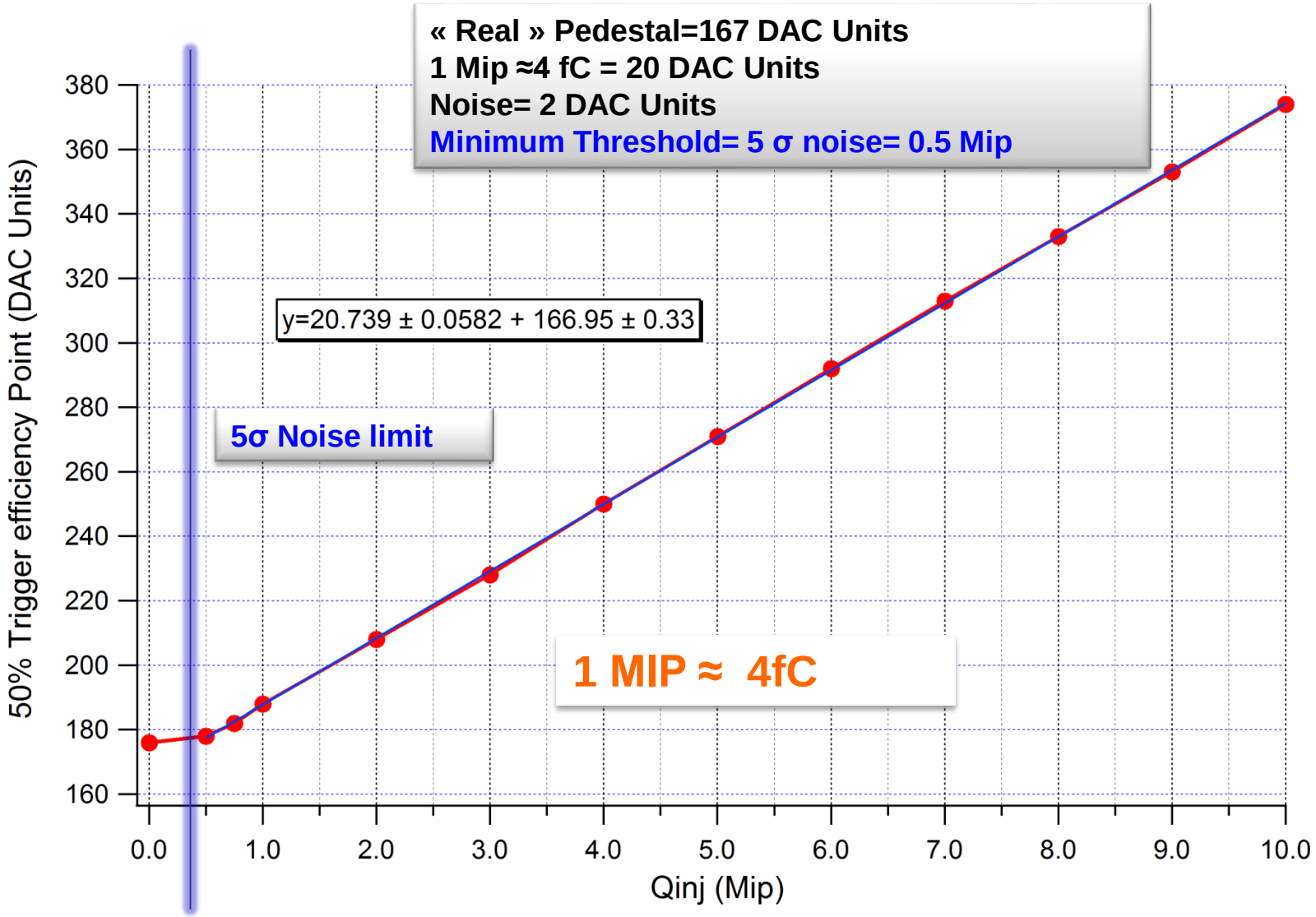




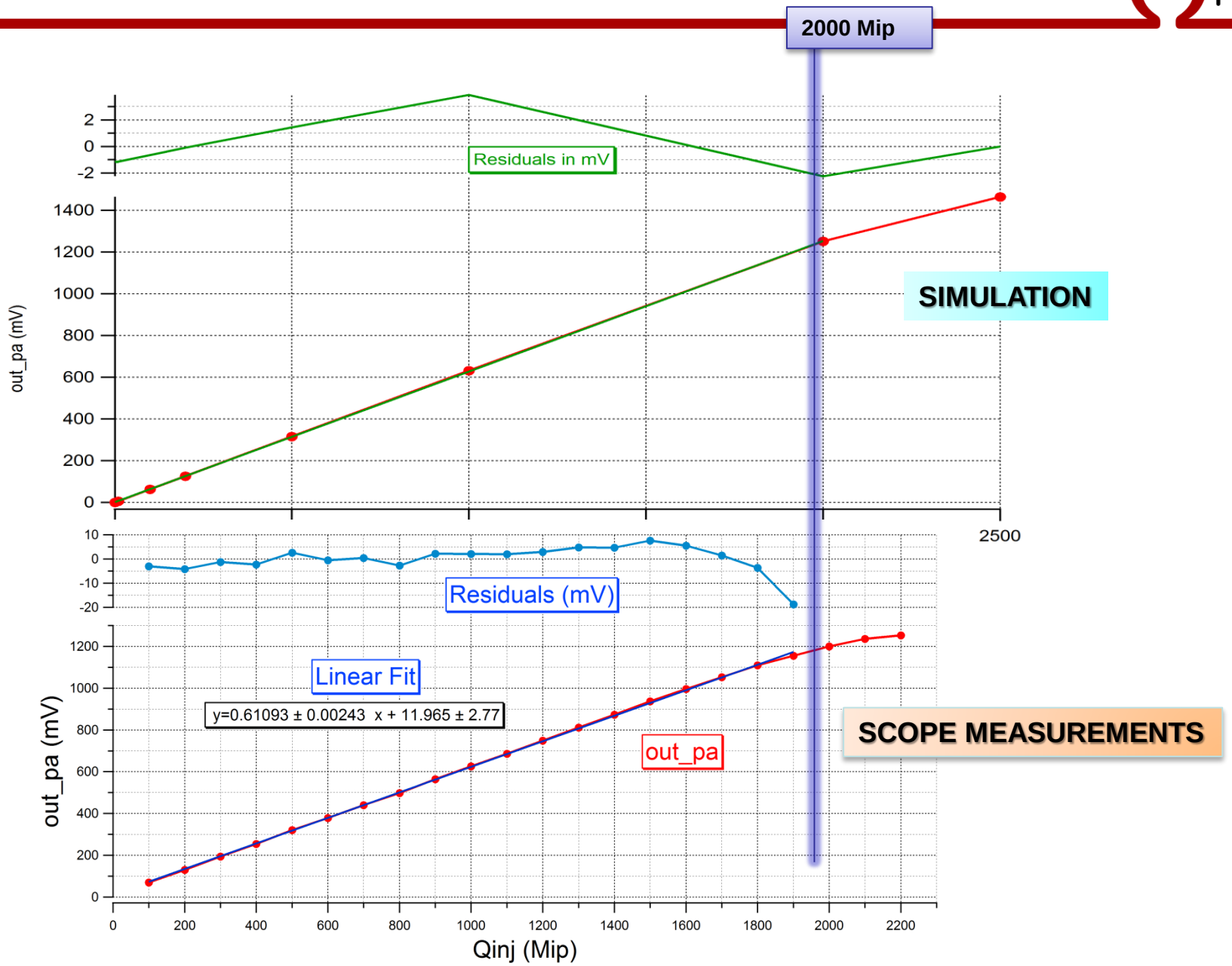




Trigger efficiency (2)

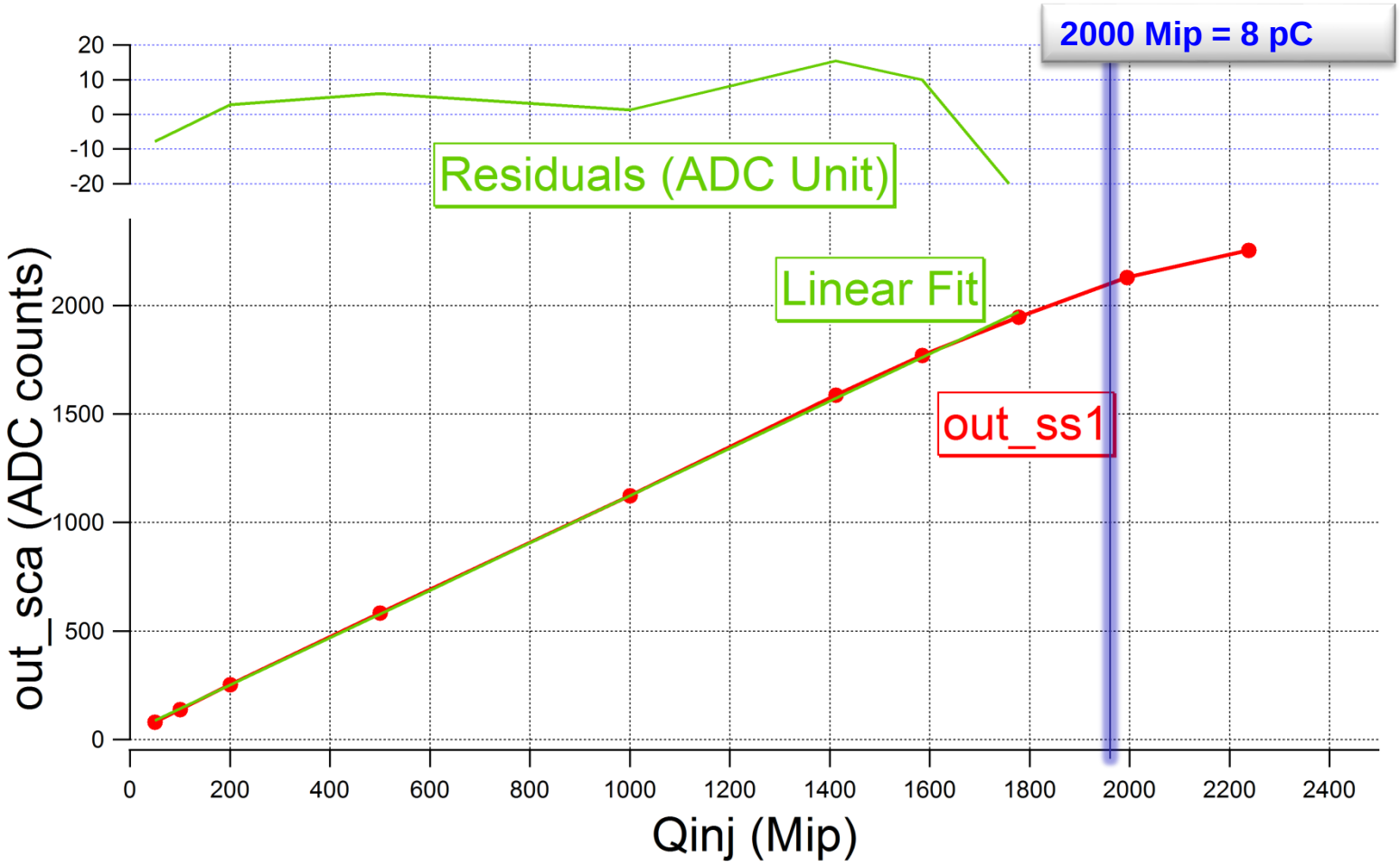


Linearity of the Charge Preamp



Linearity of the Low Gain Shaper

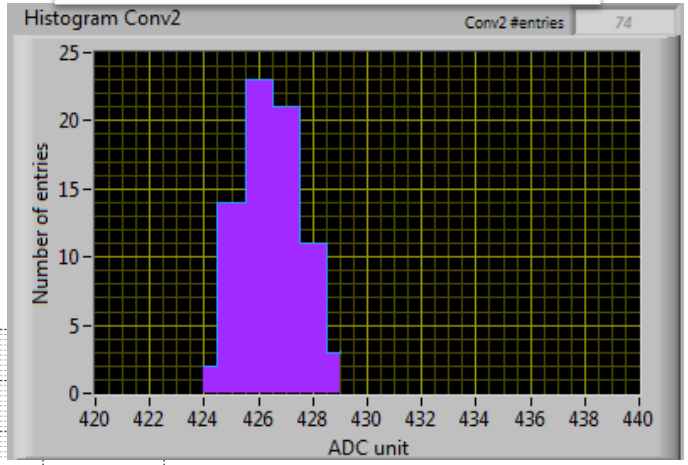
MEASUREMENTS using SCA and internal ADC
Autotrigger mode
1 MIP (4fC) threshold



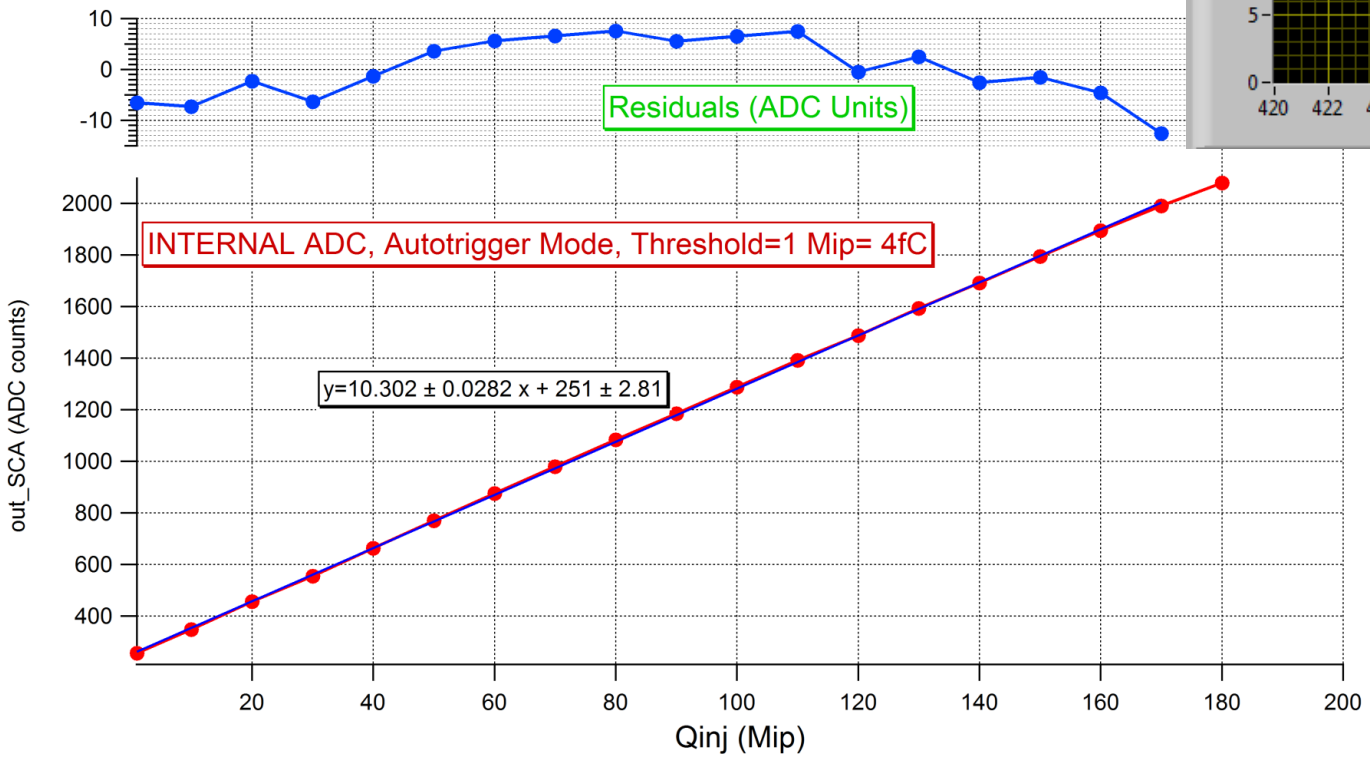
Linearity of the High Gain Shaper

Noise = 630 µV
1 Mip gives 5.7 mV
S/N=9

SS10@20 MIP
Rms =1.16 ADC
U=600µV



MEASUREMENTS using SCA and internal ADC
Autotrigger mode
1 MIP (4fC) threshold



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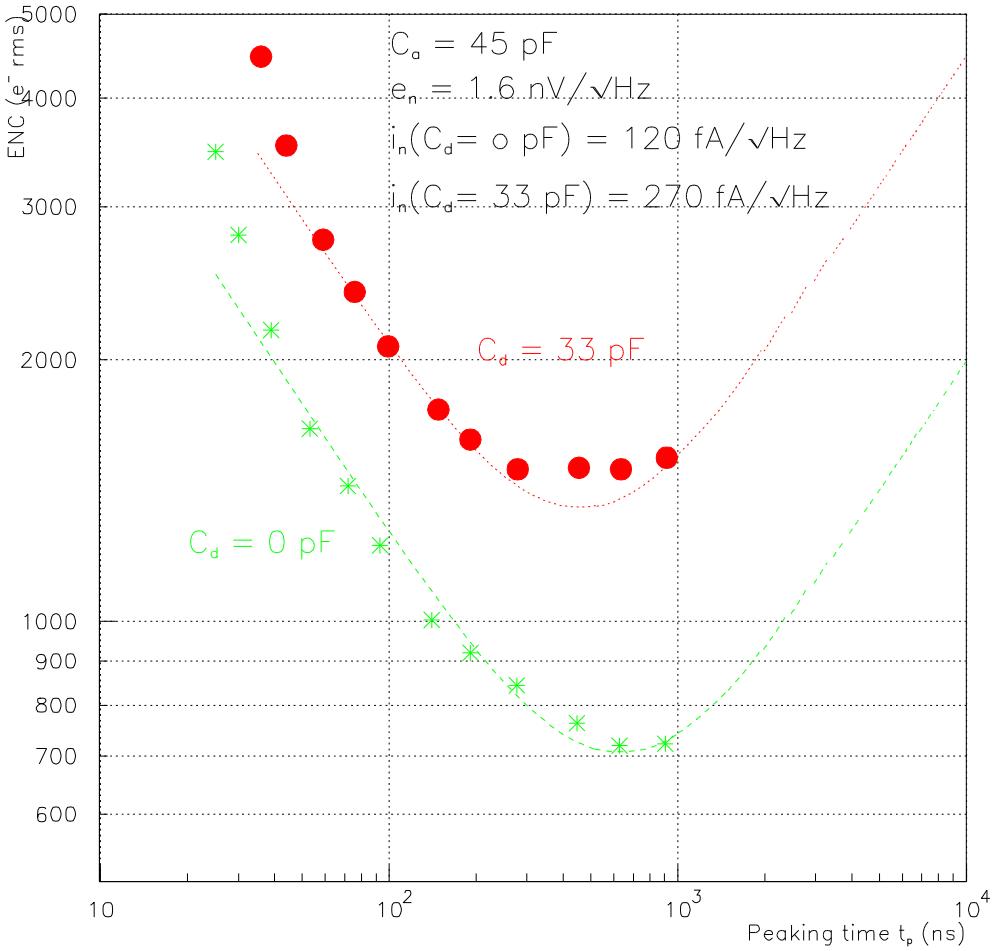
SKIROC2 : PreAmplifier ENC

SKIROC2
Cf=6pF, Qinj=2510^6 e-
CRRC2 x 100

C_d (pF)	A	A*181.5	B	C	e_n x C_t
0	0.4	72.6	664700	0	72.6
33	0.7	127.05	1400000	0	127.05

e_n nV/sqrt(Hz)	i_n fA/sqrt(Hz) (Cd= 0pF)	i_n fA/sqrt(Hz) (Cd= 33pF)	Ca pF
1,6	120	270	45



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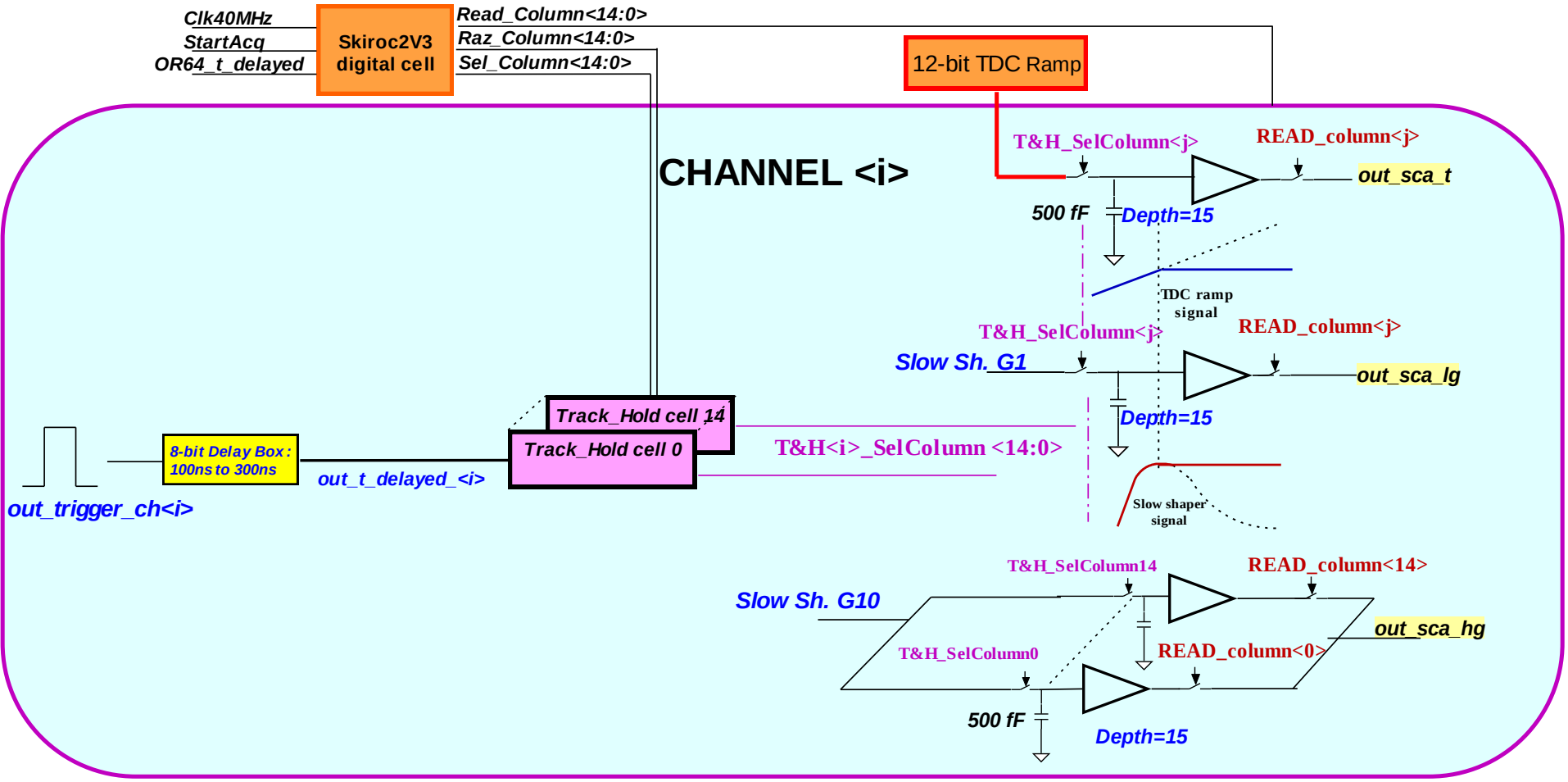
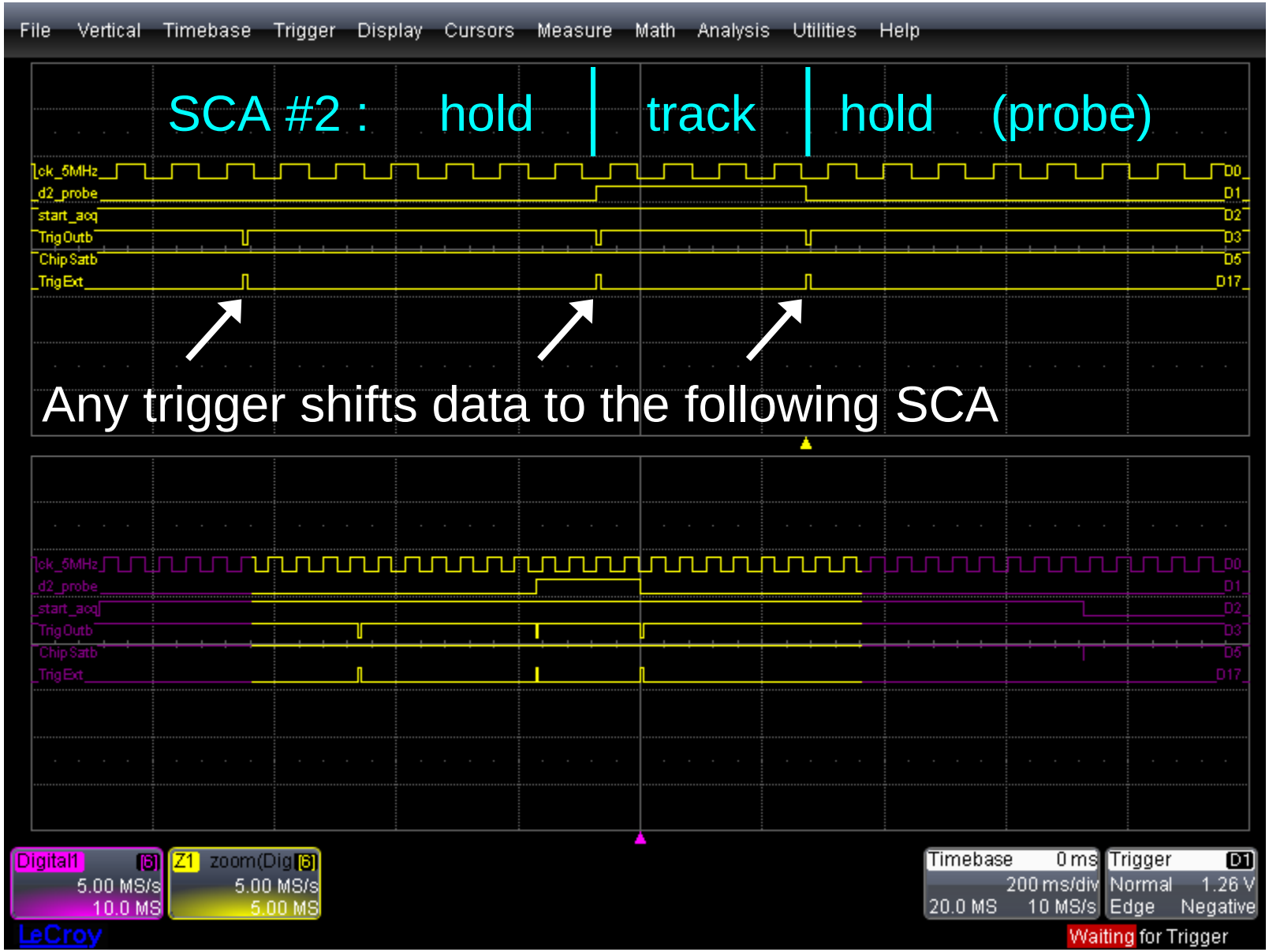
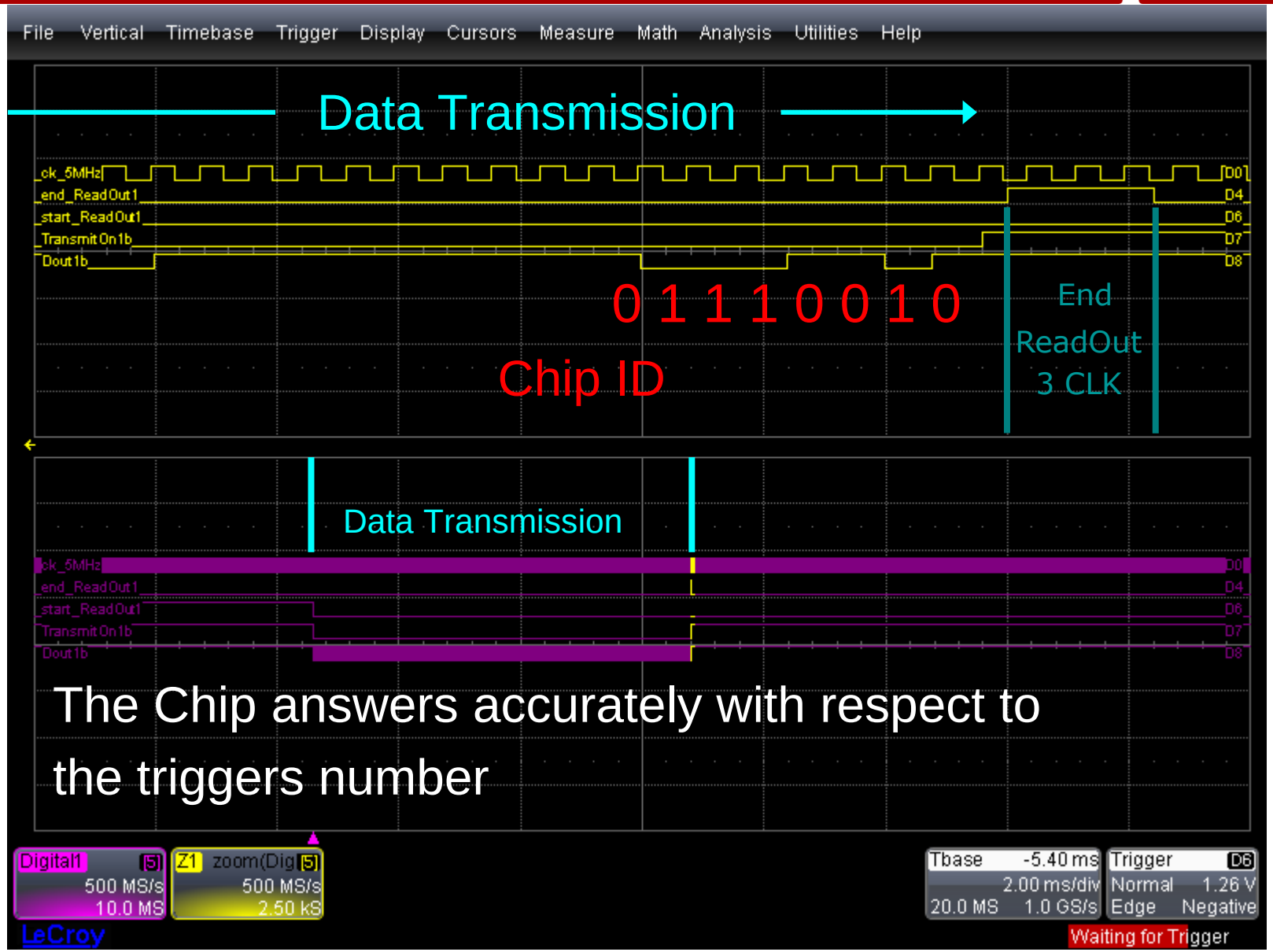
SCA detail


Clk40MHz
StartAcq
OR64_t_delayed
Skiroc2V3 digital cell
Read_Column<14:0>
Raz_Column<14:0>
Sel_Column<14:0>
12-bit TDC Ramp
CHANNEL <i>
T&H_SelColumn<j>
READ_column<j>
out_sca_t
500 fF
Depth=15
TDC ramp signal
T&H_SelColumn<j>
READ_column<j>
Slow Sh. G1
out_sca_lg
Depth=15
Track_Hold cell 14
Track_Hold cell 0
T&H<i>_SelColumn <14:0>
8-bit Delay Box : 100ns to 300ns
out_t_delayed_<i>
out_trigger_ch<i>
Slow shaper signal
T&H_SelColumn14
READ_column<14>
Slow Sh. G10
out_sca_hg
T&H_SelColumn0
READ_column<0>
500 fF
Depth=15

SKIROC2 Digital Features



SKIROC2 Digital ReadOut



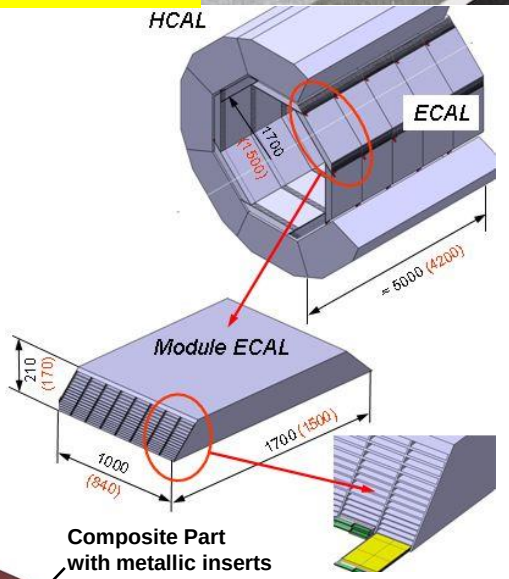
E-CAL Design

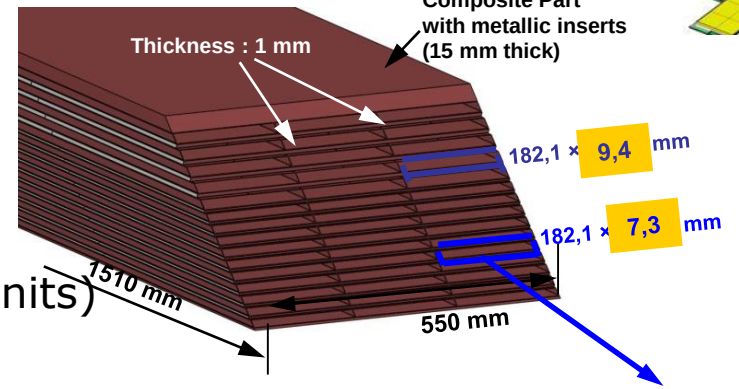
E-CAL design

Technological prototype:
Completed Jan. 2012

- « Imaging » calorimetry for « particle flow algorithm »
  => 30%/√E jet resolution
  - **High granularity and segmentation of the calorimeters**

- ECAL: **Si W Calorimeter**
  - **Active medium: SILICON SENSORS (WAFERS)**
  - 325µm thick Silicon Wafers => 26000e⁻/MIP ie 1MIP=4.2 fC
  - High granularity : **5.5x5.5 mm²**
  - High segmentation =>
    - **45 000 cells with embedded electronics for the technological prototype**



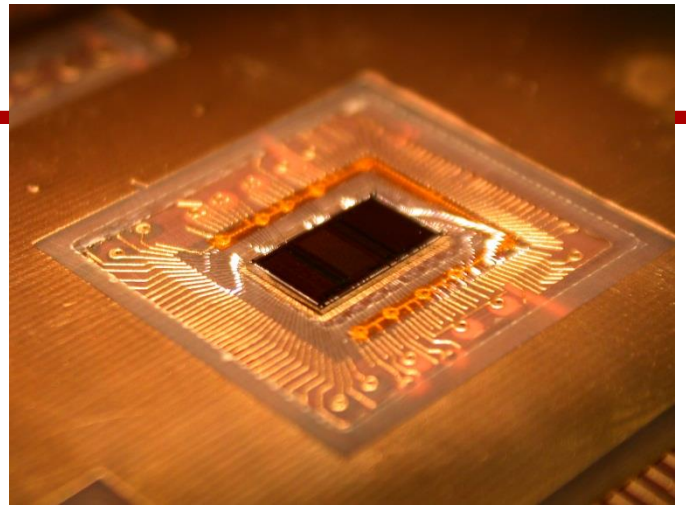


- Final ECAL: 30 layers, **100 M channels**
  - **SKIROC2 embedded** inside the detector
  - **No (few) external components**

- "stitchable" motherboards (Active Sensor Units)
  - Minimize connections between boards

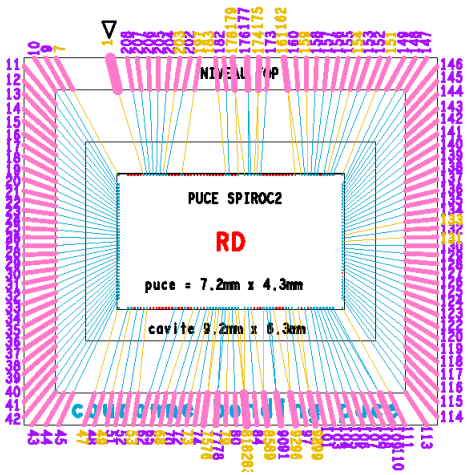
- Low cost and industrialization are the major goal

PCB with embedded Chip

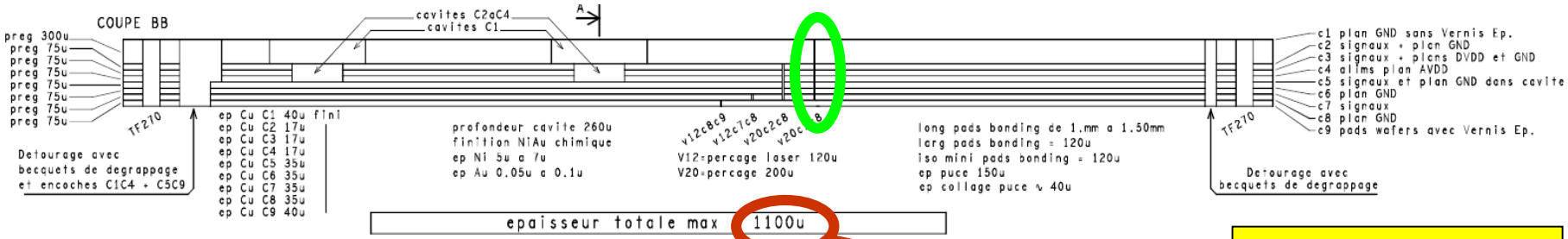


Pile-up	
Top	GND cover layer
C2	GND + Input chip signal
C3	horizontal routing + DVDD + GND
C4	AVDD
C5	GND + vertical routing
C6	GND (pads signal shielding)
C7	pads routing
C8	GND (pads shielding)
BOT	PADS

Front End Board (FEV board)



5 drilling sequences :
- Laser C8-C9 120µ filled
- Laser C7-C8 120µ
- Mechanical C2-C8 200µ
- Mechanical C1-C8 200µ
- Mechanical C1-C9 (for PCB fastening)



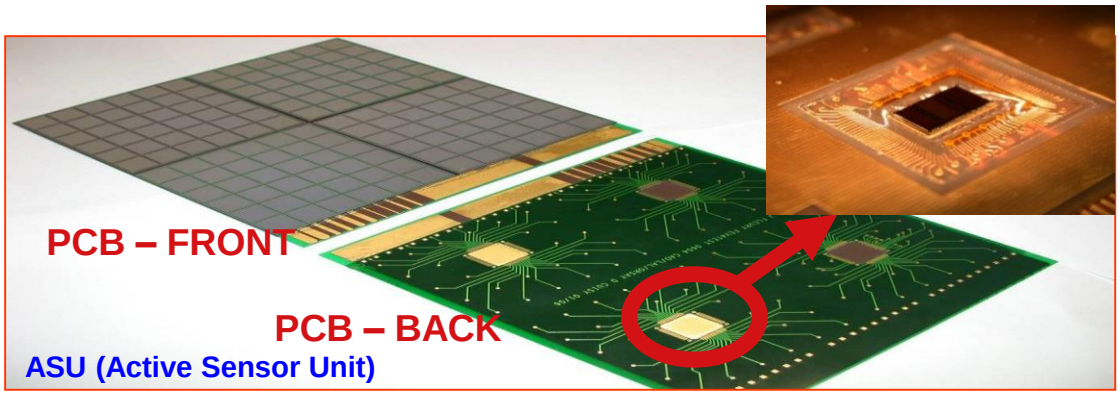
PCB Thickness 1100 µm

SKIROC : ECAL readout

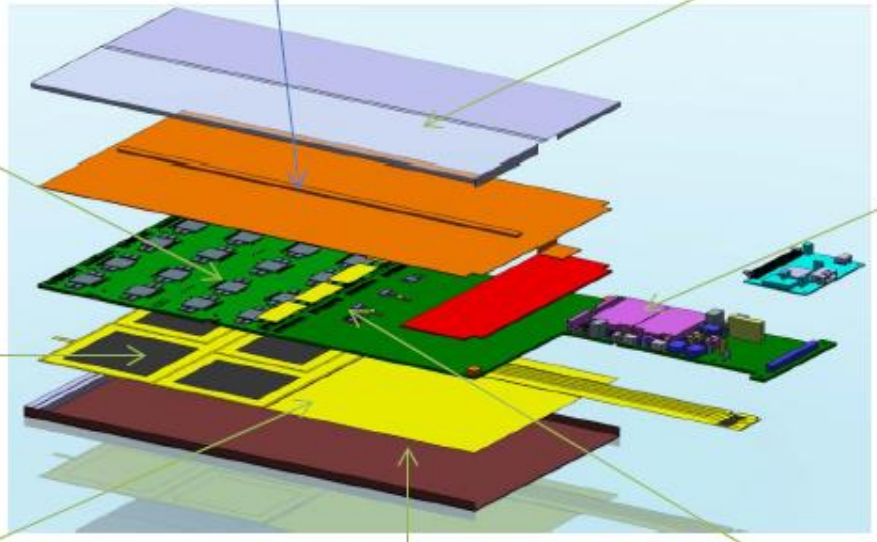
- SKIROC2 : Silicon Kalorimeter Integrated Read-Out Chip
  - 64 channels, AMS SiGe 0.35 µm, 70 mm^2
  - **Very large dynamic range**:
    - HG for 0.5-150 MIP, LG for 150-2500 MIP
  - Auto-trigger, Analog storage, Digitization & Token-ring ReadOut
  - Testability at wafer level

- Front End boards crucial element
  - Collaboration with LLR and SKKU (Korea)

C detector with PCB ≈ 20 pF



A detector module



Coper sheet for cooling

Cover (EMI shielding)

PCB 1024 chn. 16x skiroc2

Power pulsing circuitry (400 mF)

Si PIN diodes

Front-end, DAQ, TFC Not shown

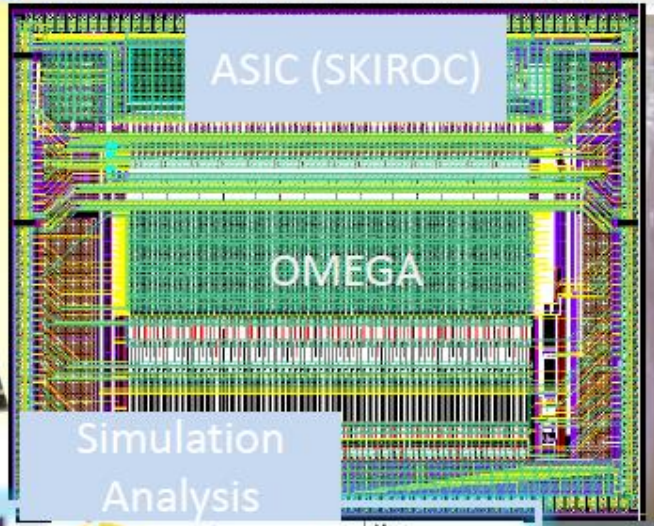
HV kapton

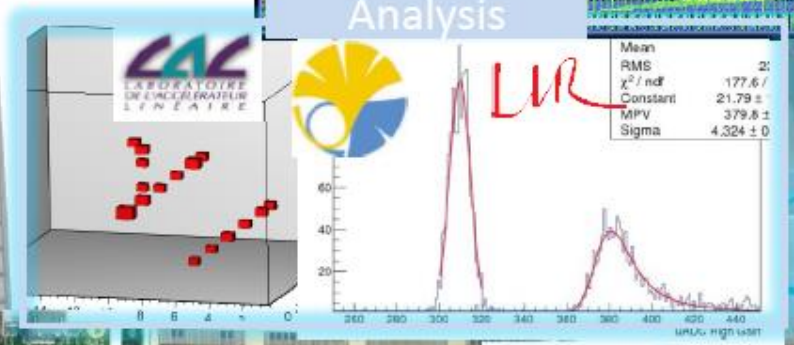
A "short SLAB"

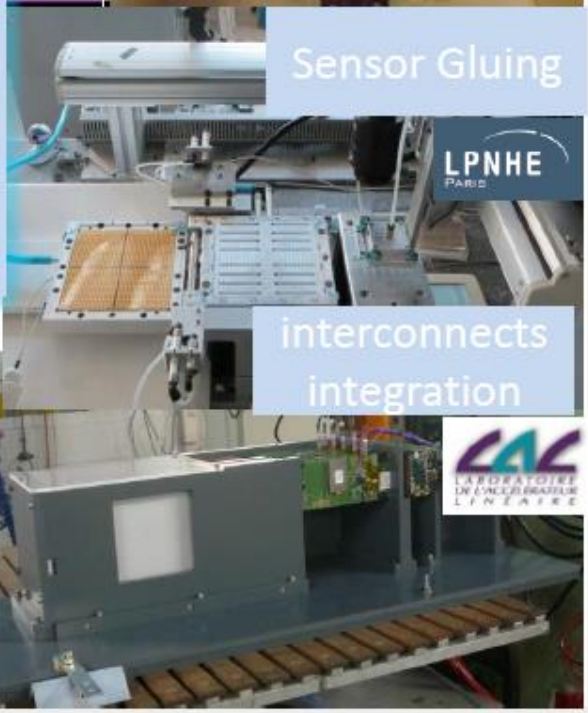
FCC Interconnects

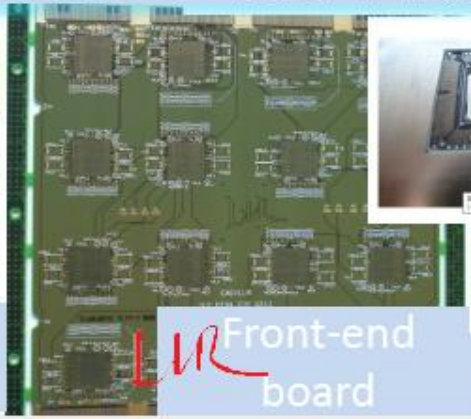
Stiffener, Absorber Carbon fiber + W

Prototyping : who is doing what



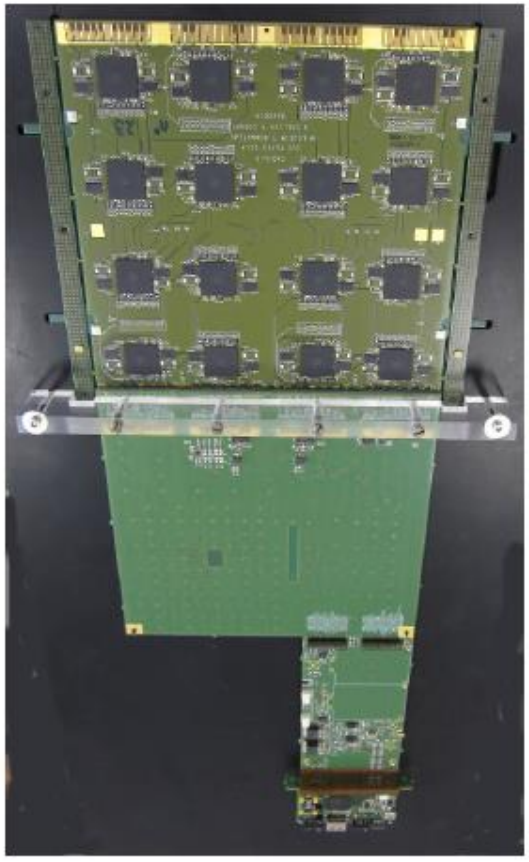






Next version(s) of VFE board

18 x 18 cm^2 front-end board includes 1024 channels (16 chips),
almost perfect flatness required for gluing the sensors : 1.6mm symmetrical stacking

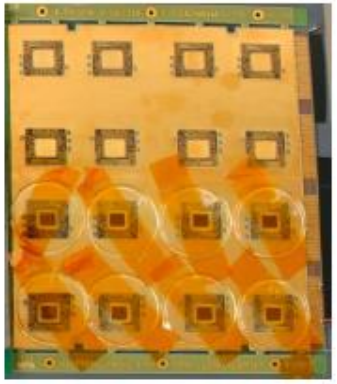


LFBGA packaged chips
and Panasonic Sp-CAP CX series
⇨ 1.1mm thick components envelop

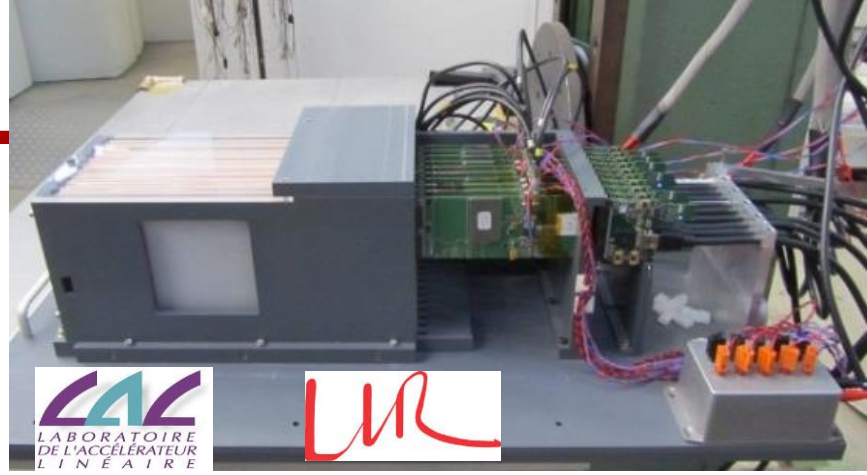
With packaged chips version the overall module thickness would be 5.5 mm (+absorber) : >4600 ch/dm^3

Naked die version would provide optimal module thickness (<4mm in total, >6000 chn/dm^3)

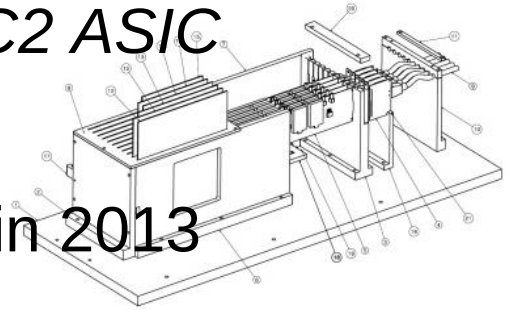
Electrical tests are ok but flatness is incompatible with sensor gluing.



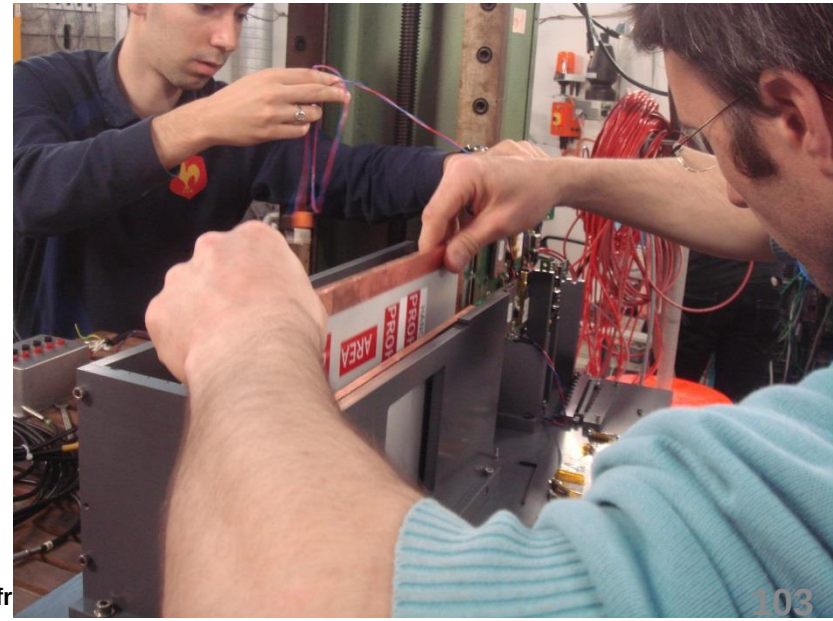
Skiroc2 in Test Beam



- Refer to publication by
  Thibault FRISSON :
  2012 Beam test performance of the SKIROC2 ASIC
  http://cds.cern.ch/search?p=AIDA-PUB-2015-004

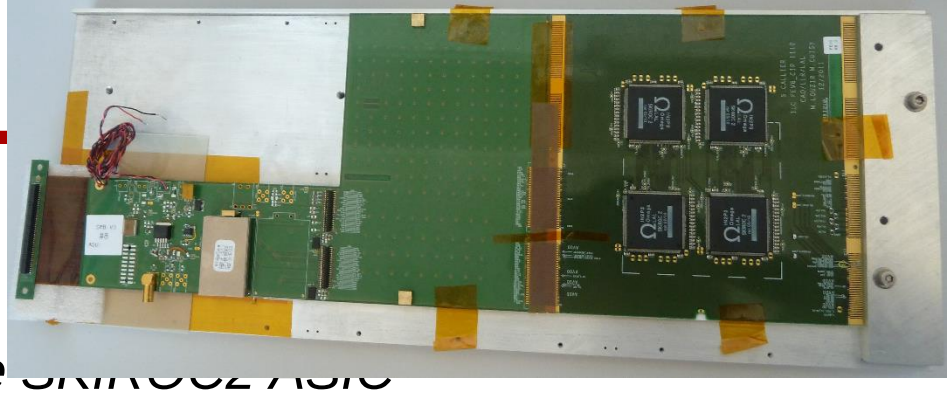


- 2 tests performed at DESY in 2012, 2 others in 2013
  - Using same Technology for the ASIC
    (PQFP240)
  - Not suitable for the ILD E-Cal design



- Next test beam expected
  in November 2015 (at CERN ?)
  - Using finer Packaging for
    the ASIC : BGA, relevant for ILD

Skiroc2 in Test Beam

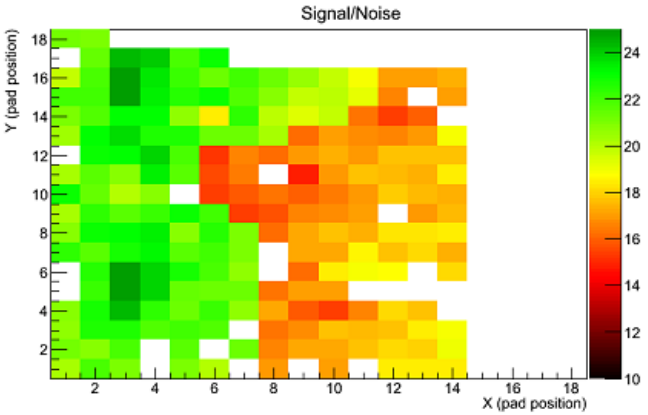


- Refer to publication by
  Thibault FRISSON :
  2012 Beam test performance of the SKIROC2 ASIC
  http://cds.cern.ch/search?p=AIDA-PUB-2015-004

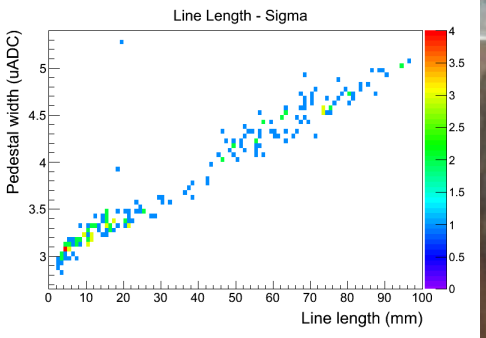
- Beam Results : data taken in autotrigger mode on FEV8-CIP using PQFP240 Skiroc2

- Detector showed nice performances

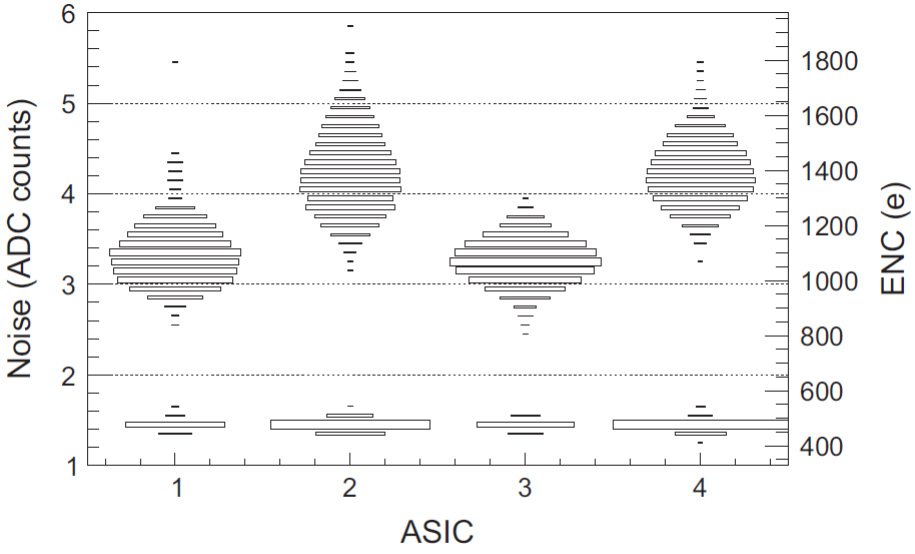
Pedestal noise vs PCB channel Capacitance
Measurement performed on technological prototype



S/N > 10



FEV8-CIP : Test Beam Results



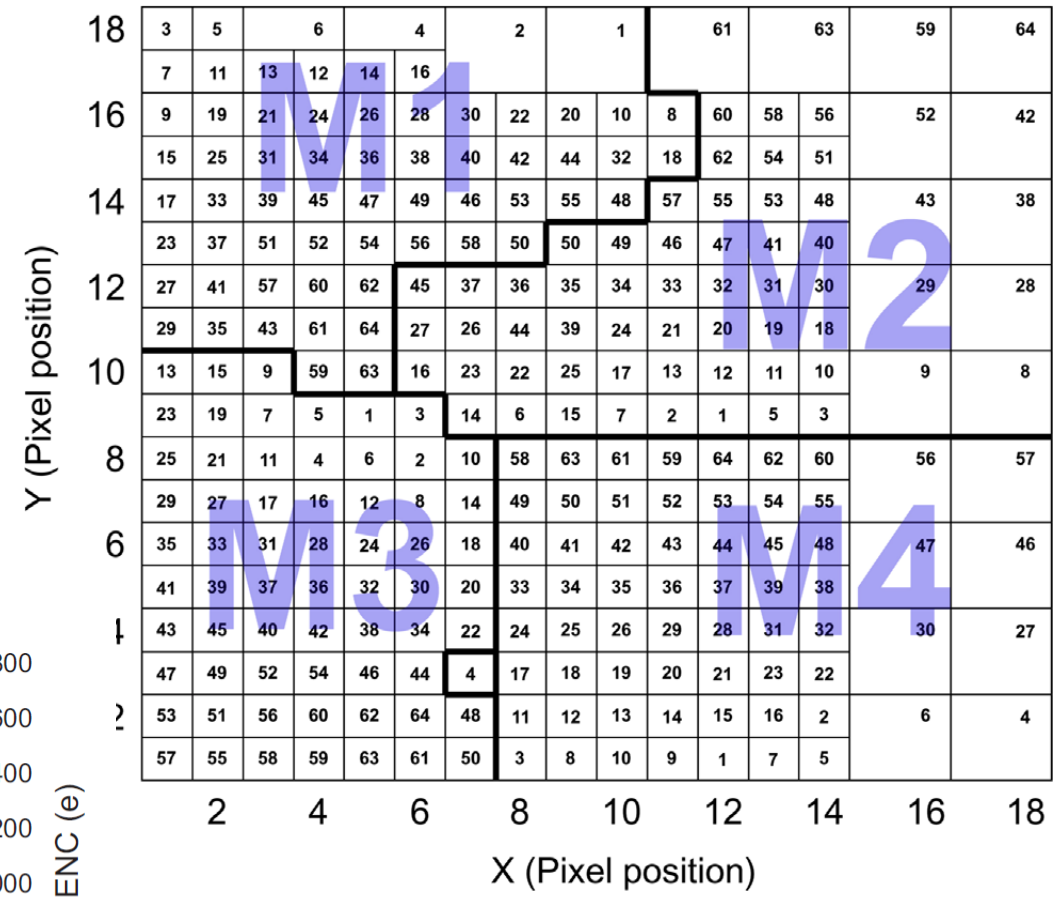
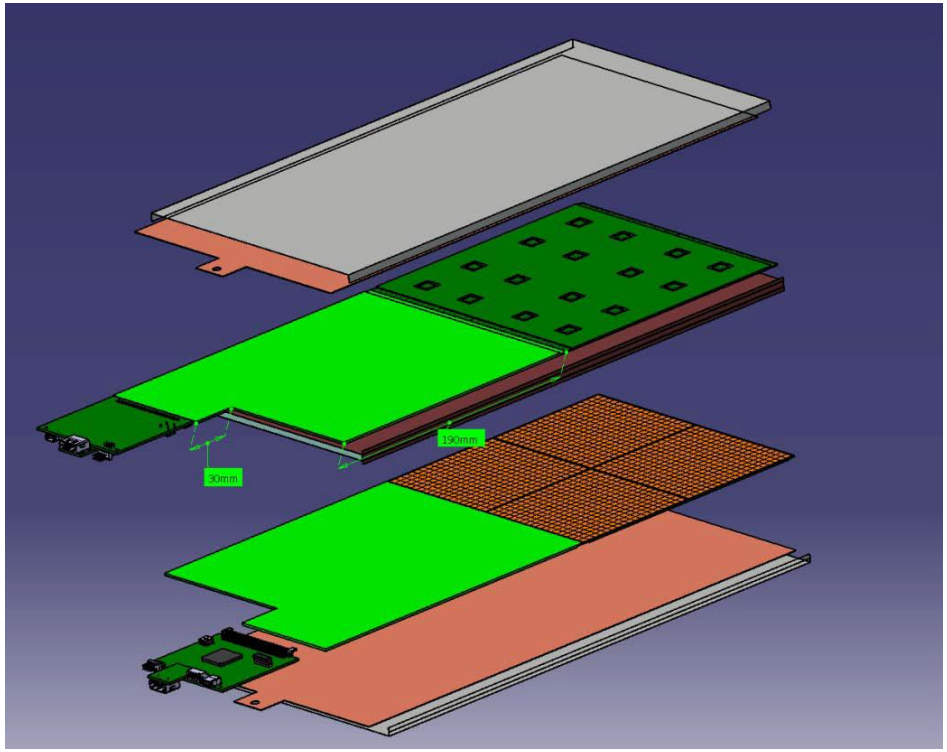


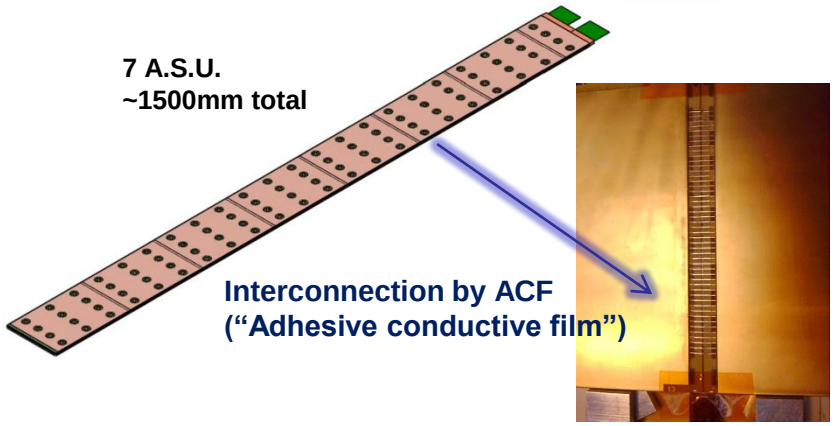
Fig. 5. Noise distribution as a function of the ASIC number for all layers. The left *y*-axis is the noise in ADC counts. The right *y*-axis is the equivalent noise charge.

EUDET/AIDA ECAL technological prototype (2)

- In each alveola: 2 layers of 1 to 7 Active Sensors Units (ASU)

- 1 ASU
  - 1 kapton (HV bias of the PIN diodes)
  - + 1 layer of PIN diodes
  - + 1 PCB with embedded SKIROC2
  - + 1 thermal drain (copper)

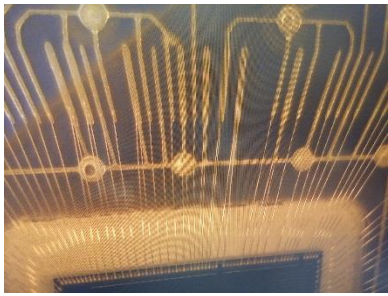




ASIC Requirements

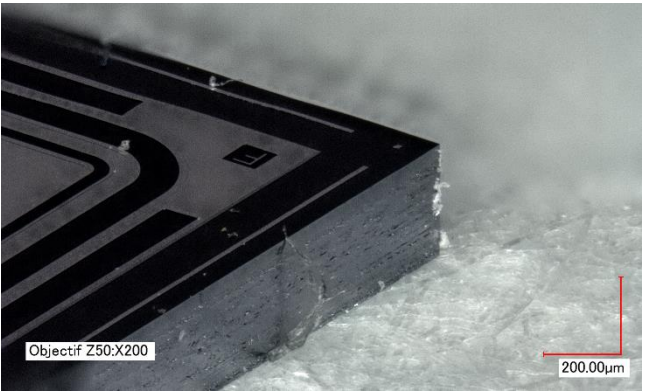
DETECTOR INTEGRATION

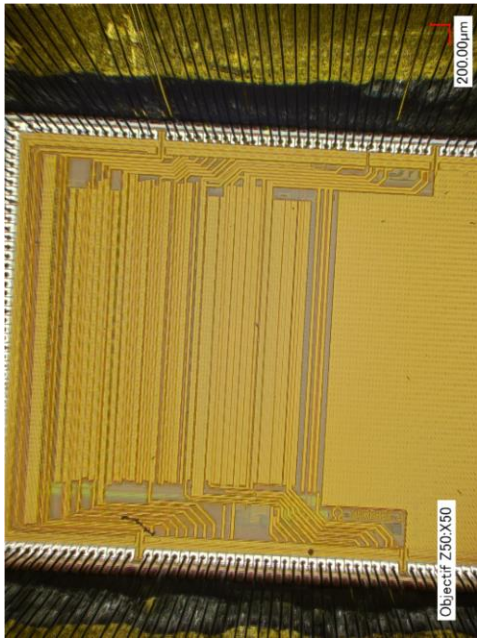
- Full power pulsing capability
  - 25 µW/ch => 24h operation of full slab with 2 AAA batteries !



- Dynamic Range : from ½ MIP up to 2500 MIP
- Auto-trigger on ½ MIP
- Analog storage, Digitization & Token-ring ReadOut
- On Chip zero suppress (~few kbytes/s/slab)

"TRACKER ELECTRONICS WITH CALORIMETRIC PERFORMANCE "





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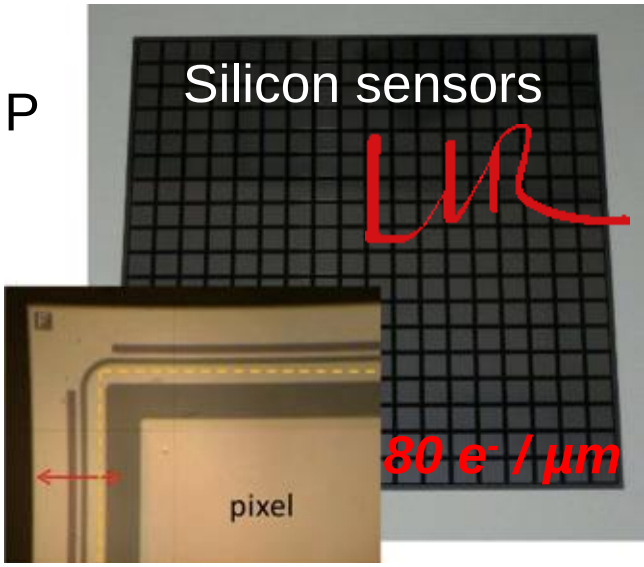
E-CAL Detector Integration

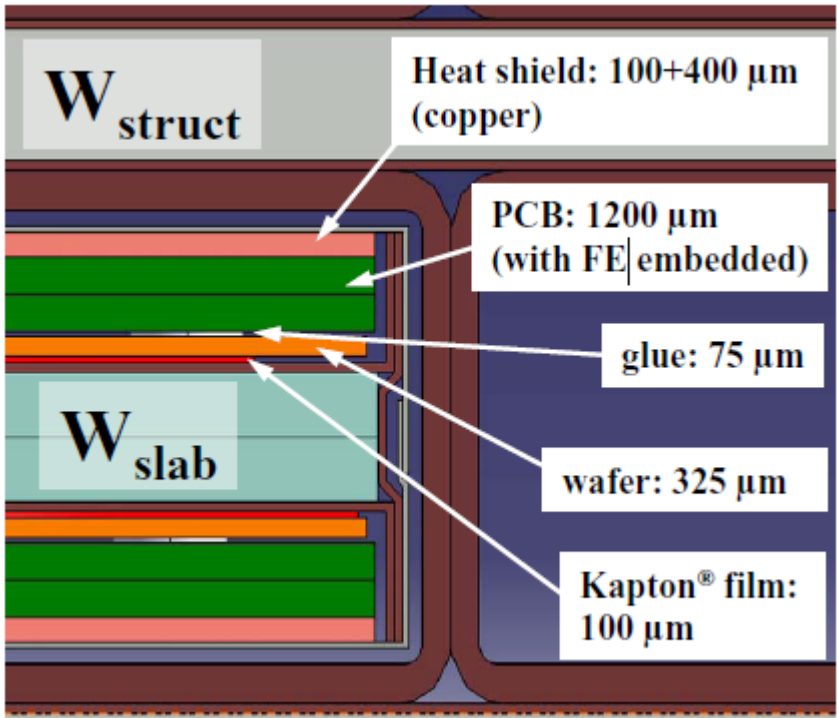
SILICON SENSORS (WAFERS) :

- Using 325µm thick Silicon Wafers => 26000e$^-$/MIP
- $C_{detector}$ estimated 9pF
  - Add also 10pF due to PCB pads' capacitance
- PIN diode leakage up to 10nA / channel
  - Chip has leakage current capability



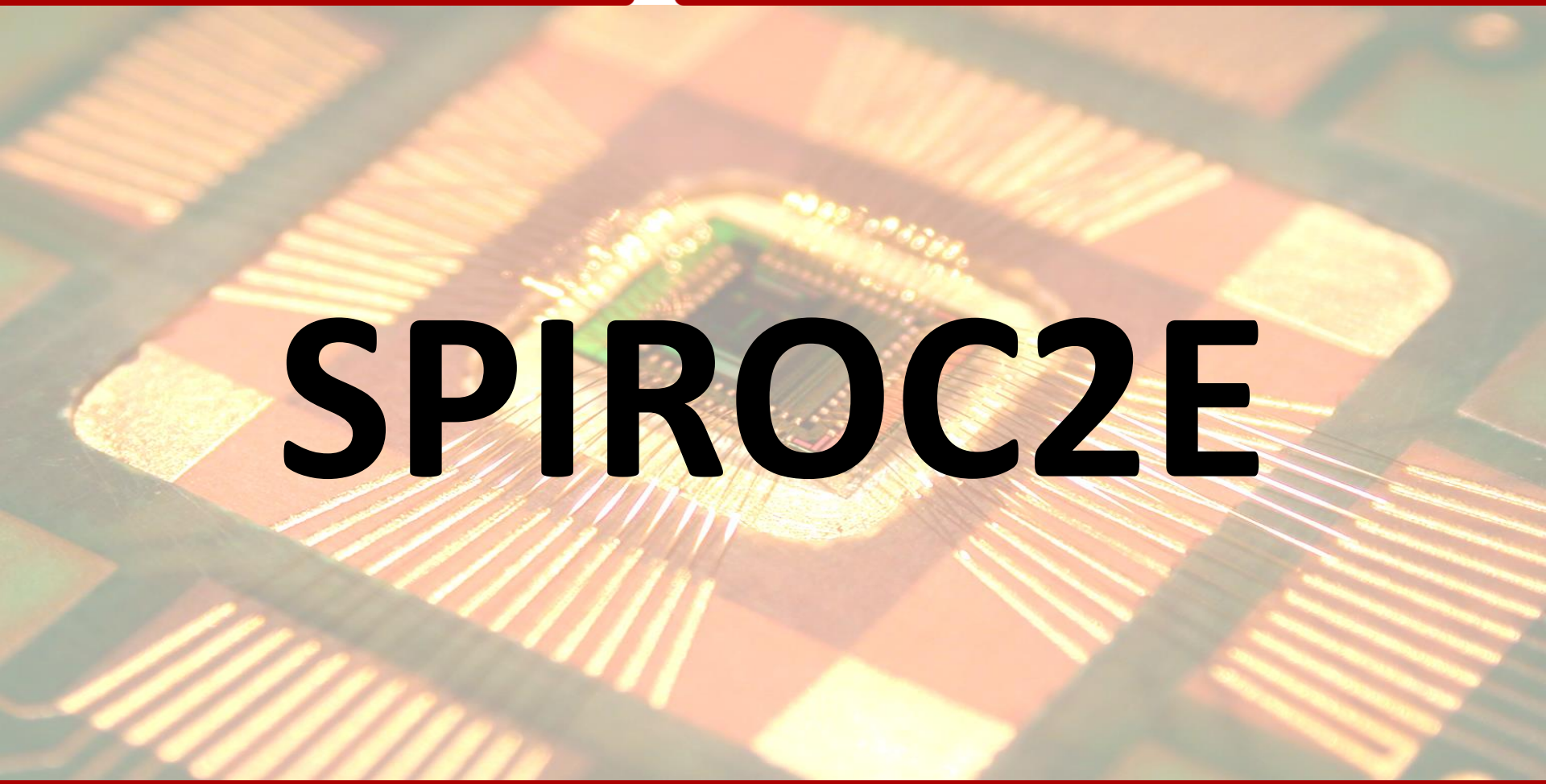
DETECTOR INTEGRATION

- Front End embedded in detector
- Ultra low power consumption
  => to Minimize cooling !
  - 25 µW/ch with Full Power Pulsing



- **In each alveola: 2 layers of 1 to 7 Active Sensors Units (ASU)**
- **1 ASU**
  1 kapton (HV bias of the PIN diodes)
  + 1 layer of PIN diodes
  + 1 PCB with embedded SKIROC2
  + 1 thermal drain (copper)

callier@omega.in2p3



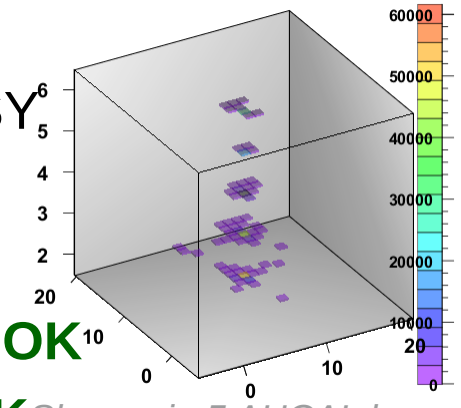
SPIROC2E

Organization for Micro-Electronics desiGn and Applications

SPIROC2E Modifications

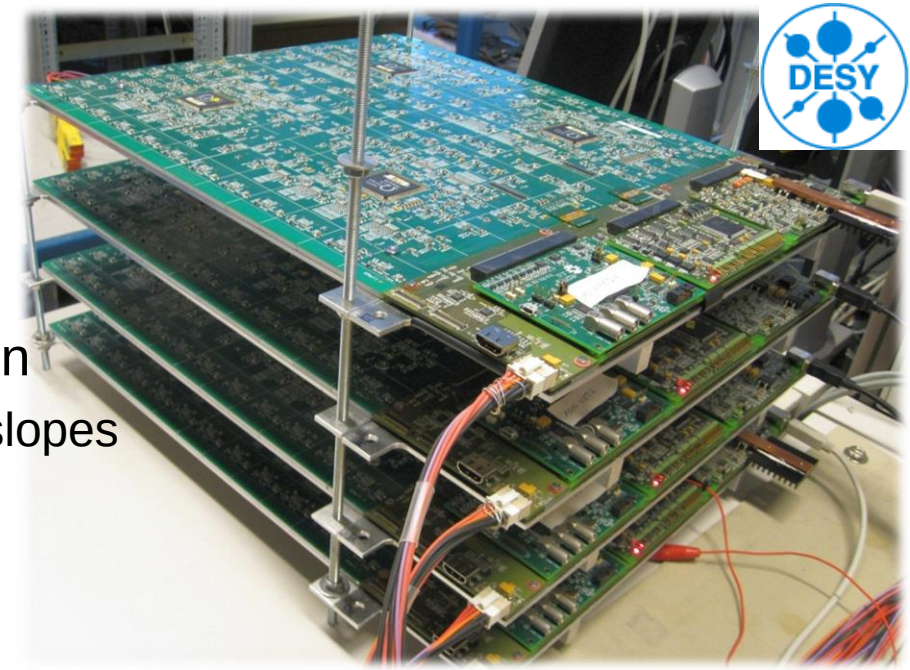
- Starting from SPIROC2D
  - Refer to previous presentation 9th december @DESY

- BUG CORRECTIONS
  - Fast Shaper & Threshold on discriminator **: Fixed : OK**
  - Reset on Delay cells (column 0, 10, 14) **: Fixed : OK**
  - Gain dependency on last channels **: Cured : OK**
  - 5V DAC Probe Register :
    - **uses 5V pads & probes : OK**



Shower in 5 AHCAL layers (DESY testbeam)

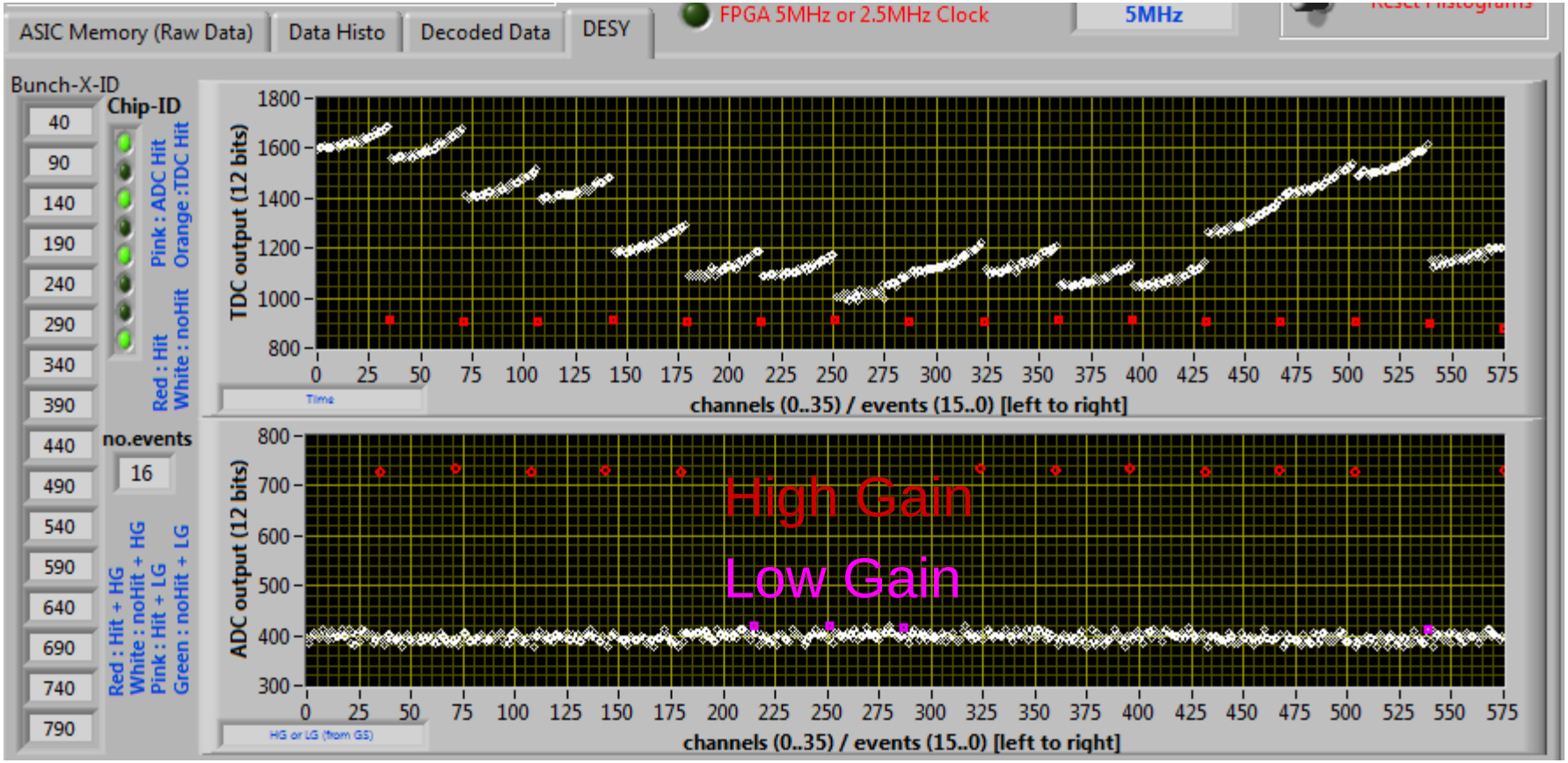
- IMPROVEMENTS
  - TDC : CHANGED for a new design
    - 1 unique current source for both slopes
  - Delay cells : Noise Improvements



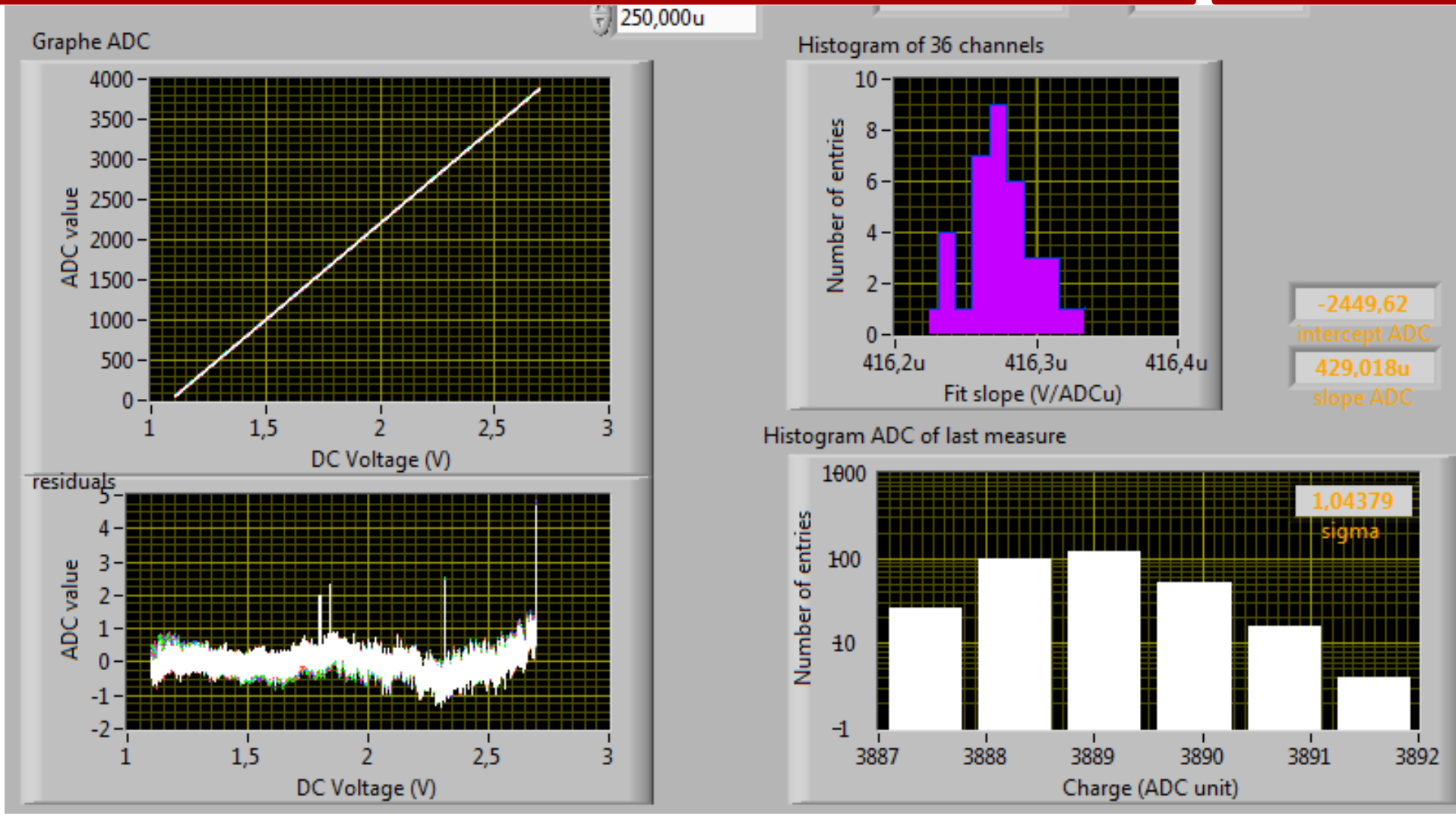
SPIROC2E : AutoGain

Full autotrigger mode

Q inj = 10pe- DAC_GS=252



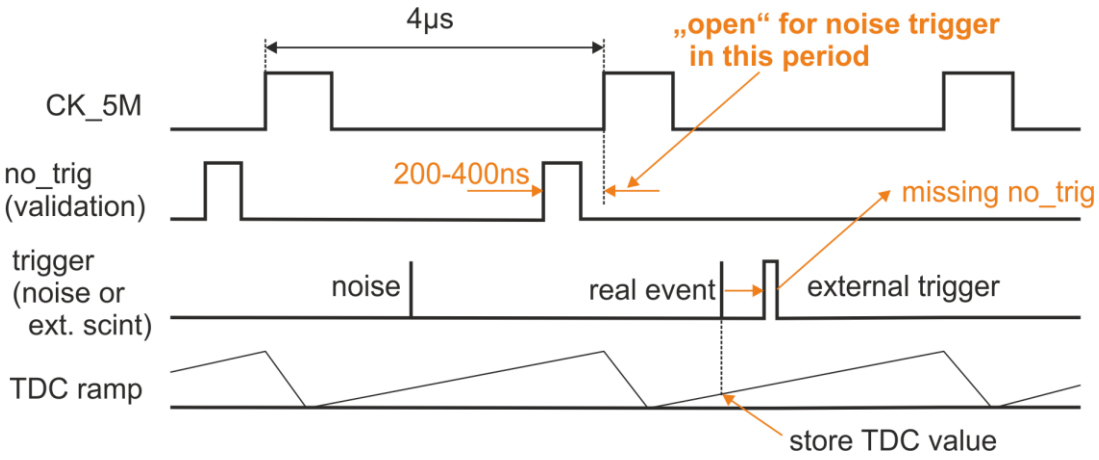
SPIROC2E : ADC Linearity



Test performed using 250uV steps

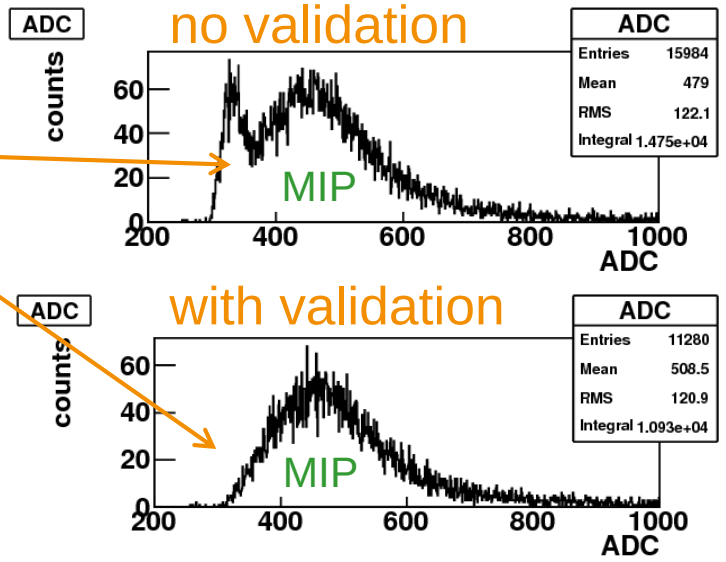
No external resistor

Trigger Validation (Testbeam mode)



- Only stores events that are validated by an external trigger signal

- **Validation works fine**: Histogram only shows MIP events without noise/pedestal contributions.
- Problem: Validation does not work for noise hits between no_trig and rising CK_5M edge (200-400ns). **Triggers in this period should be rejected (=> dead time).**
- Now: Factor 10 noise reduction. Improve 400ns window size.



SPIROC2D

Organization for Micro-Electronics desiGn and Applications

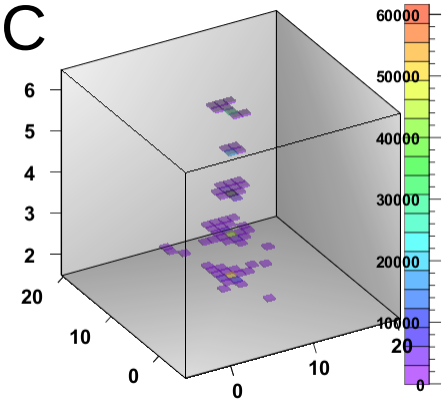
SPIROC2D Modifications (1)

- Starting from improvements done in SPIROC2C

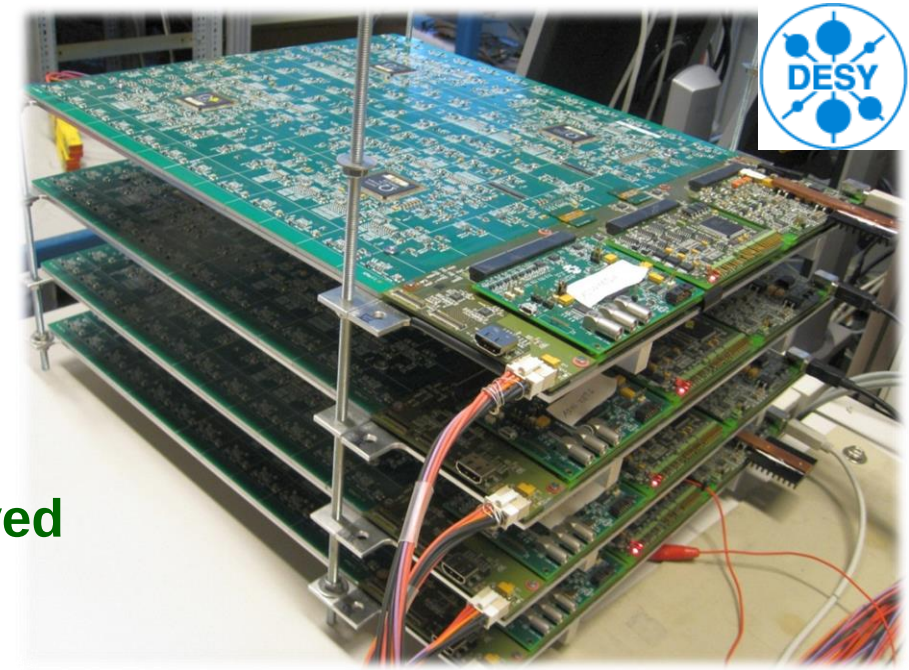
- BUG CORRECTIONS
  - Some « Zero events » during digitization **: Fixed**
  - Crosstalk between HG and LG **: OK, IMPROVED**
  - Rate dependency **: IMPROVED**
  - AutoGain Selection **: Fixed**
  - Probe Register : **Fixed**

- IMPROVEMENTS
  - Individual Tunable Gain LG, HG
  - Pedestal Shift for large

  Signal injected **: Improved**
  - Delay Cell **: New Design, Improved**
  - TDC : **IMPROVED …**



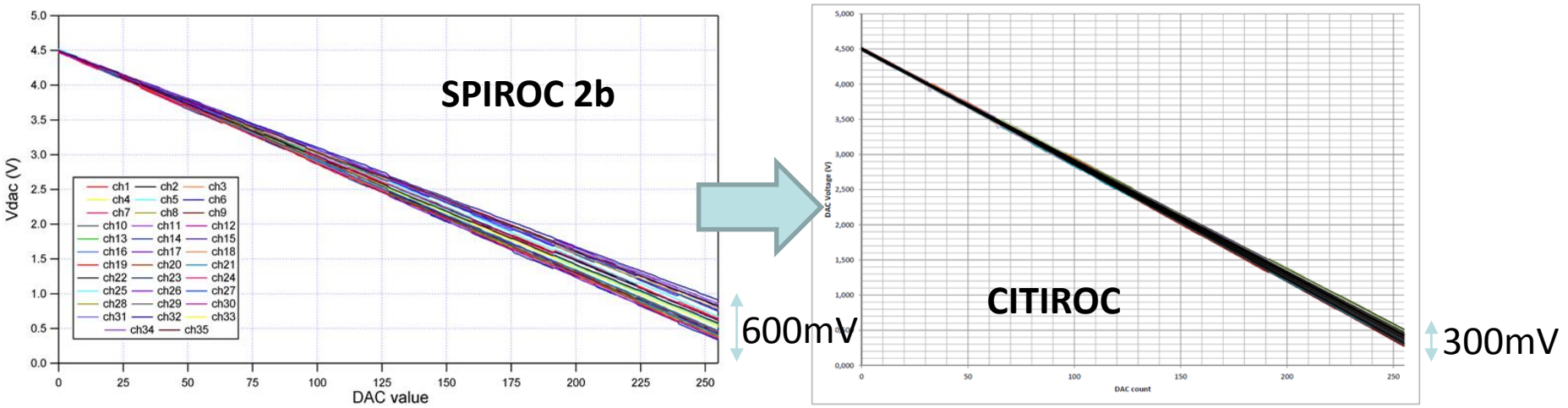
Shower in 5 AHCAL layers (DESY testbeam)



SPIROC2D Modifications (2)

- Pinout compatible with Spiroc2B (ok for current EBUs/EBUs)
  - Input DAC Probe system ADDED (no use on HBUs), useful for characterisation before assembly

- Improvements inherited from CITIROC
  - PreAmplifiers from CITIROC **: LOWERED CROSSTALK**
  - 8-bit input DAC from CITIROC **: IMPROVED UNIFORMITY**
    - performance widely improved but not yet satisfying (difficult due to the small power budget)

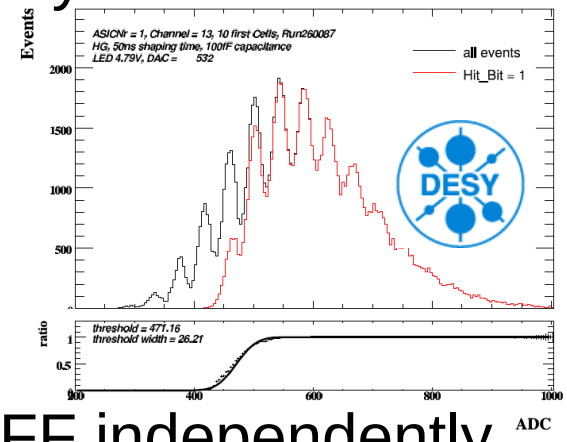


SPIROC2D Modifications (3)

- Digital Part : 16 bits for BCID
  - **Major change ! New layout !**
- Power Consumption when OFF **: Optimized**
  - Including new POD (Power On Digital modules)
- Channel to Channel Gain Uniformity **: Improved**
- 4-bit DAC for trigger level adjustment **: Range optimized**
- 8-bit input DAC protection added (internal 100 ohm)
  - Input PADs protecting diodes strengthened

SPIROC2D Modifications (4)

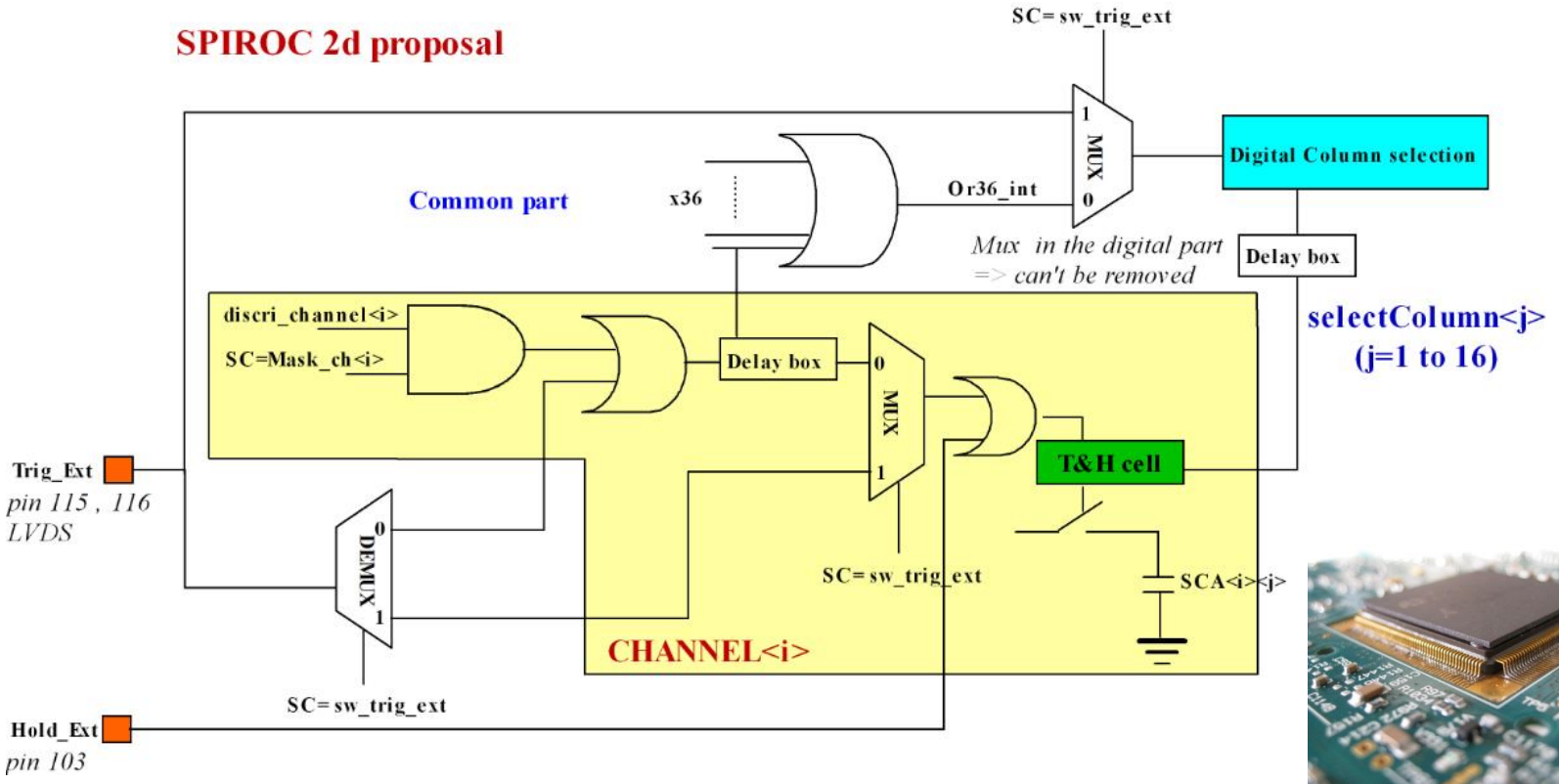
- No_Trig / Raz_Chn **: LVDS Receiver Boosted**
  - *note that optimization has to be done in the DIF*
- Power ON reset on Probe & Read Registers **: Added**
- LVDS Receivers switched OFF independently **: OK**
- Temperature Sensor **: Added**
  - Readout by both analogue and digital outputs



- Gain Select & Threshold DACs switched OFF independently
- Bandgap **: Changed (CITIROC)**

SPIROC2D Modification (5) : External Trigger

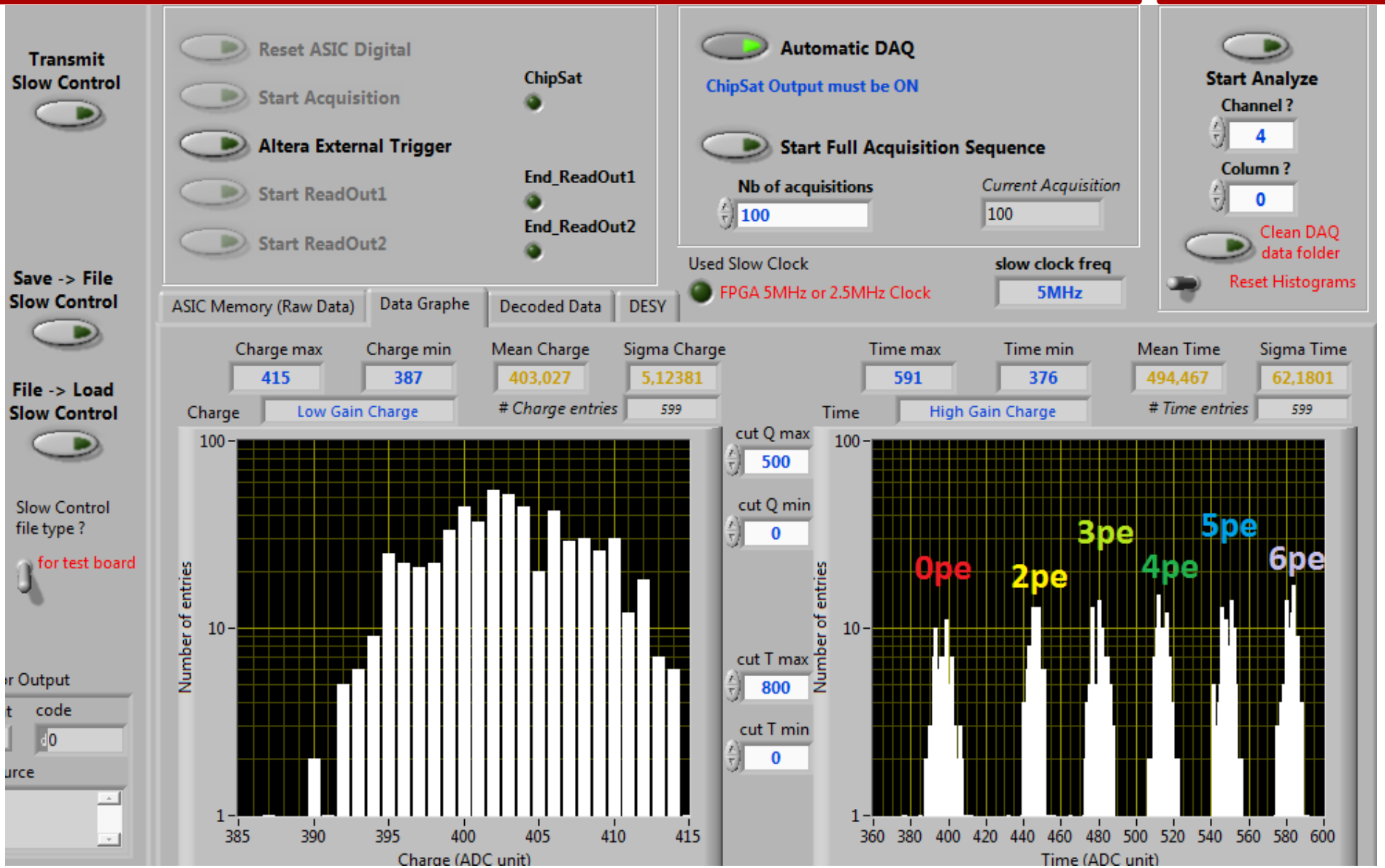
- Behaviour like SP2 available
  - Hit Bit saved in exclusive External Trigger mode
  - With internal pull down, allow NC pin on Hold_ext (pin 103)
- External Trigger delayed and used as hold for internal mode



SPIROC2D : Main improvements

- Many modifications
  - ✓ Most of them tested in Spiroc2c
    - Individual Tunable Gain LG, HG
    - Crosstalk between HG and LG
    - “Zero event” suppression **: CHECKED, OK !**
    - Rate dependency **: CHECKED, OK !**
    - new TDC
    - new Delay cell **: CHECKED, 1 ch fired shows same delay as 36 ch fired**
    - AutoGain fixed **: CHECKED, OK !**
  - ✓ New External Trigger scheme **: CHECKED, OK !**
  - ✓ **Digital part**: Timestamp counter 12 ➔ 16 bits **: CHECKED, OK !**
  - ✓ Improved Input DACs (with probe system)
    - Protection added (PAD Diodes + internal 100ohm) : on 3.3V probe system
  - ✓ Channel to channel uniformity **: CHECKED, OK !** : issue for last ch, HG
  - ✓ 4-bit DAC adjustment ch. by ch. : no influence on global threshold **: CHECKED, OK**
  - ✓ Temperature sensor added
  - ✓ LVDS receiver boosted for NoTrig/RazChn

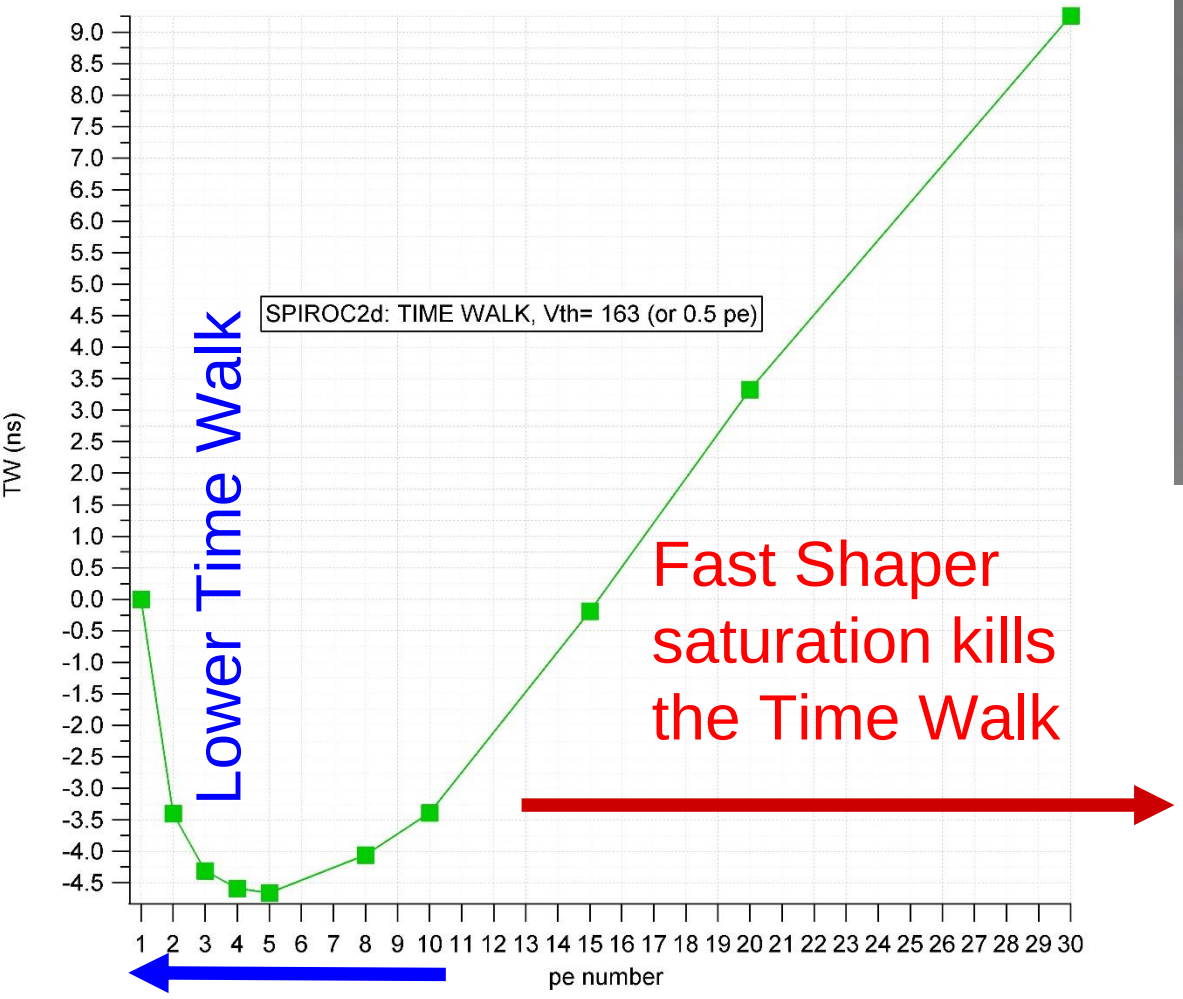
SPIROC2D : Full Auto-trigger Mode with all Ch.

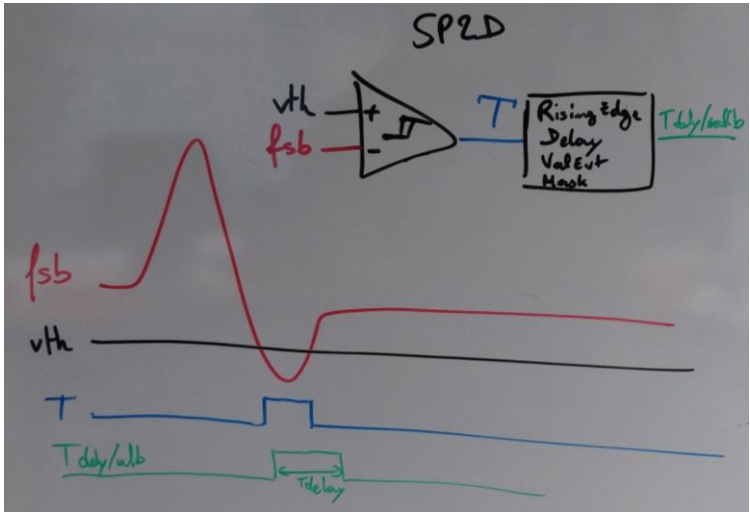


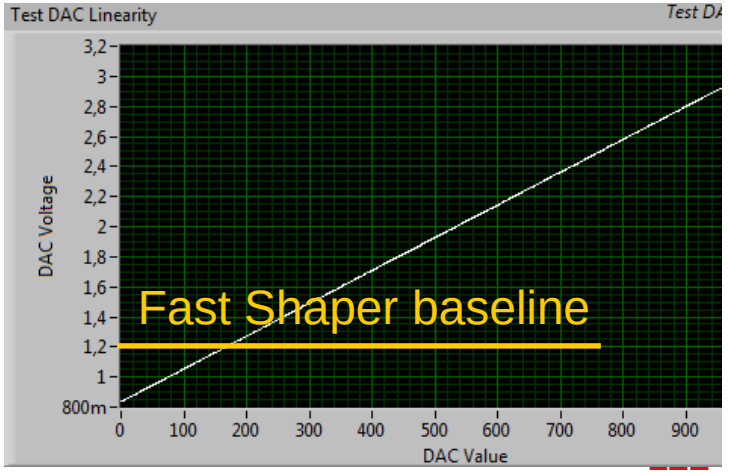
35 Channel active, Threshold @1.5pe- : We can do nice measurements !

SPIROC2D : Time Walk studies

- Studies concerning the discriminator and using it as a Zero crossing were performed in simulation… unfortunately this change has been embedded in the submitted chip !



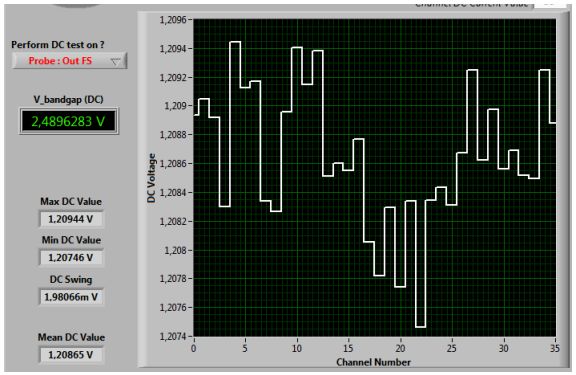


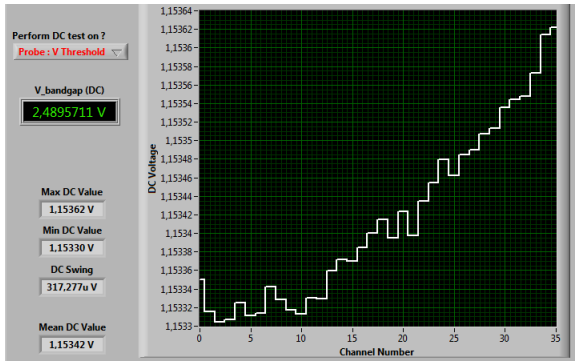


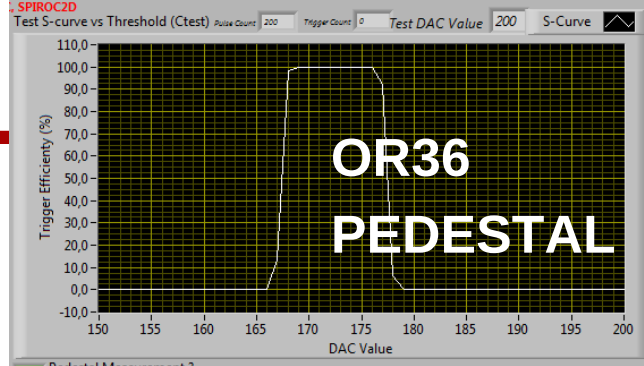
SPIROC2D : S-Curves

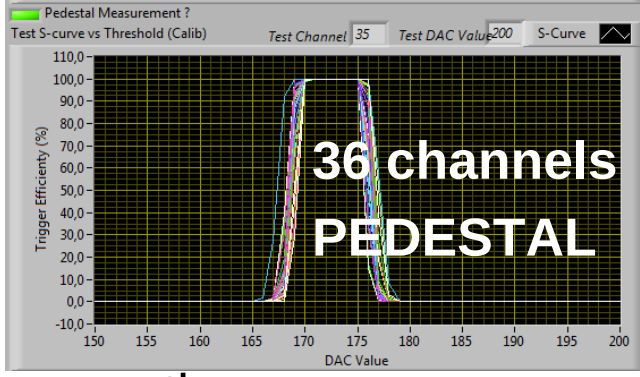
We can set a threshold as low as ½ pe⁻

Analog Measurement : swing on FSB pedestal <2mV, on Vth <350µV

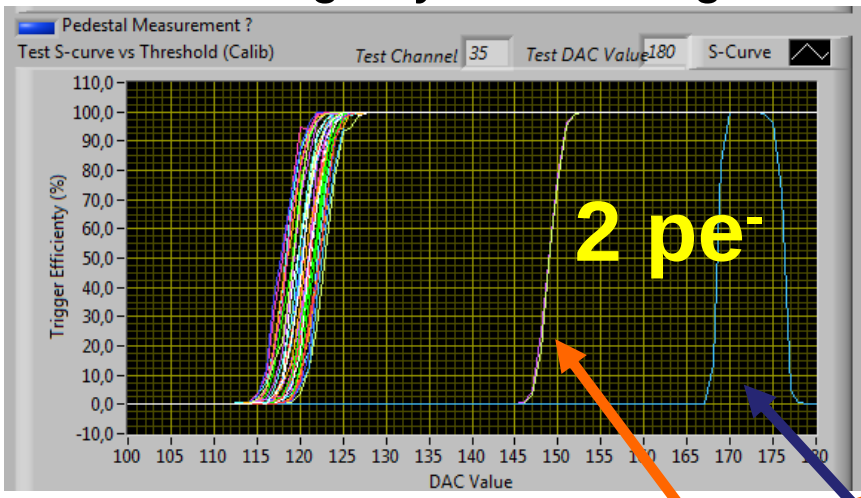


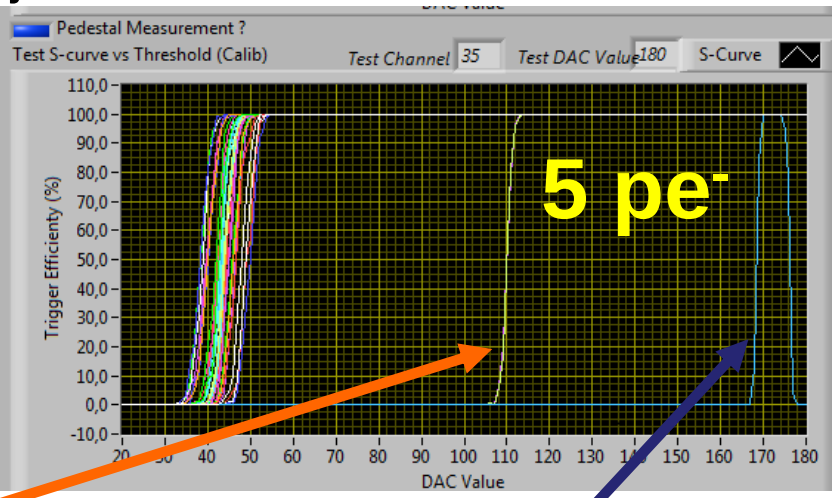






Without using any individual gain adjustment or DAC correction



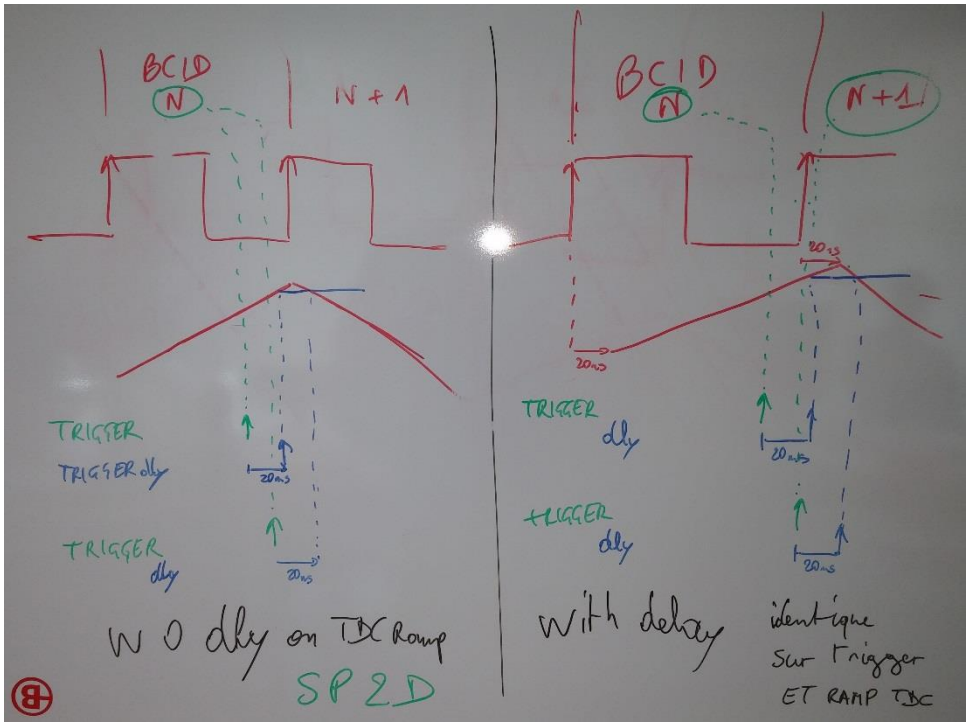


1 bad Channel shows lower gain

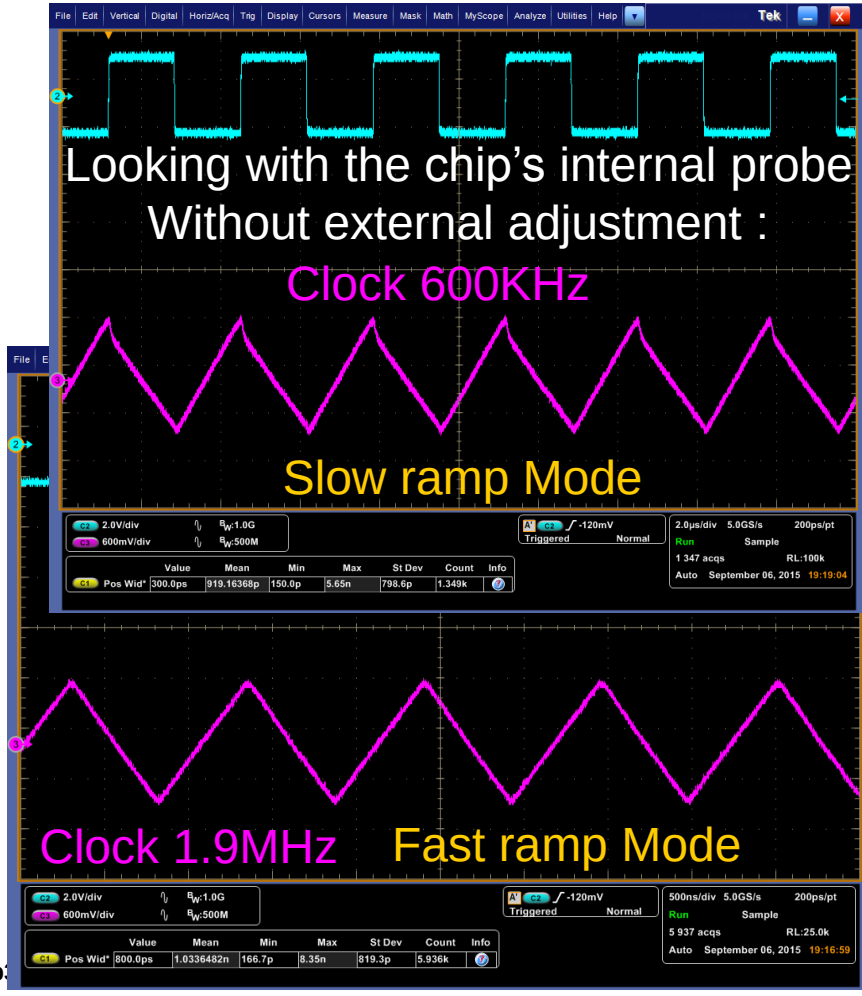
1 noisy Channel muted

SPIROC2D : TDC

- To decrease dead time during transition => alternation of a rising and a falling ramp implemented
- Conservative modification but not completely satisfying solution, a new TDC must be re-designed in SPIROC 3
- Shape looks good…

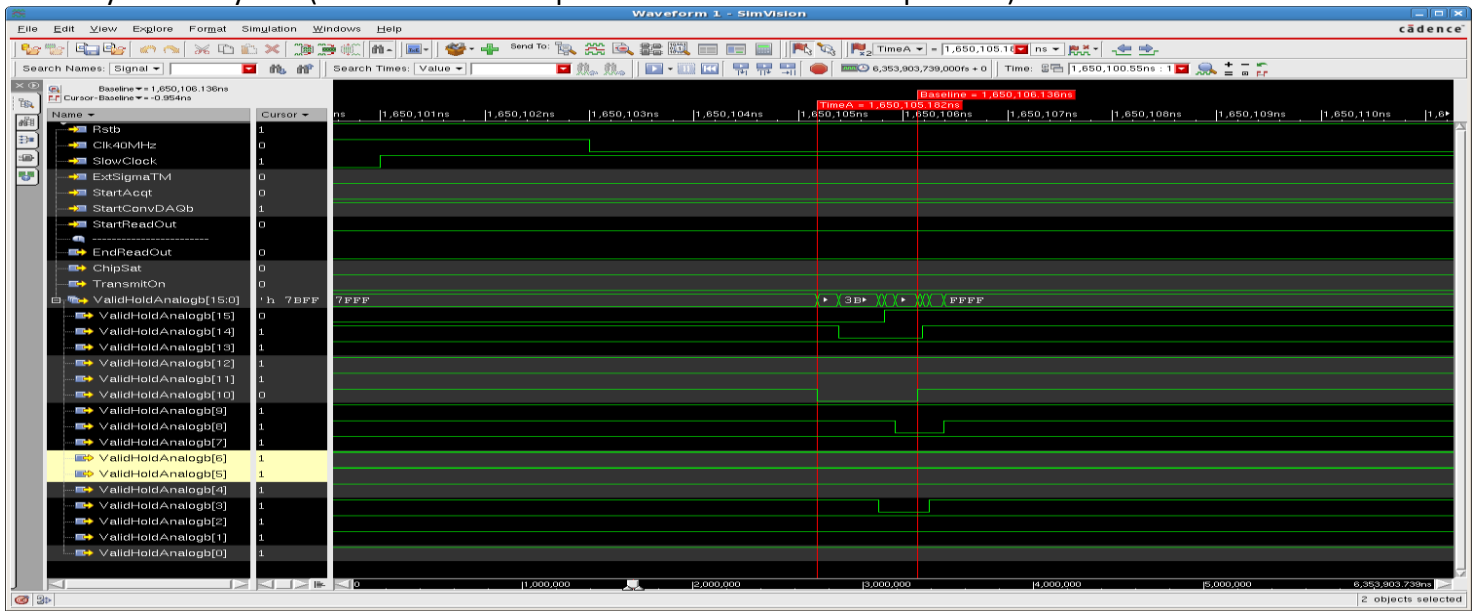


But due to a missing delay on the ramp start, 2 Triggers can be tagged by the exactly same time (fine [TDC] + coarse [BCID])



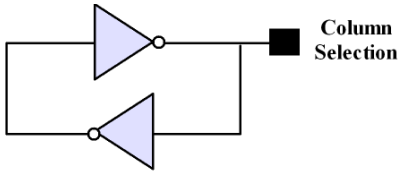
SPIROC2D : Bugs : Column issues

- Some columns “seem” not initialized (column 10 / 14 + sometimes 0)
  - We focused on the digital part as this block was completely modified
  - In simulation, some glitches are seen in the “column selection block” only at the end of the conversion ➔ should not be taken into account by the delay box (because a reset is performed before each acquisition)



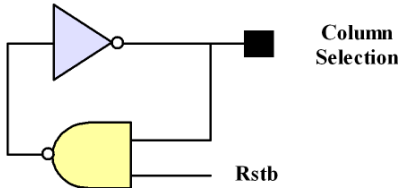
- Delay box : not correctly initialized➔ it memorizes the glitches and the column is not usable
  - All “column selection” are in an undetermined state after a reset

Output stage of the delay cell of spiroc2d

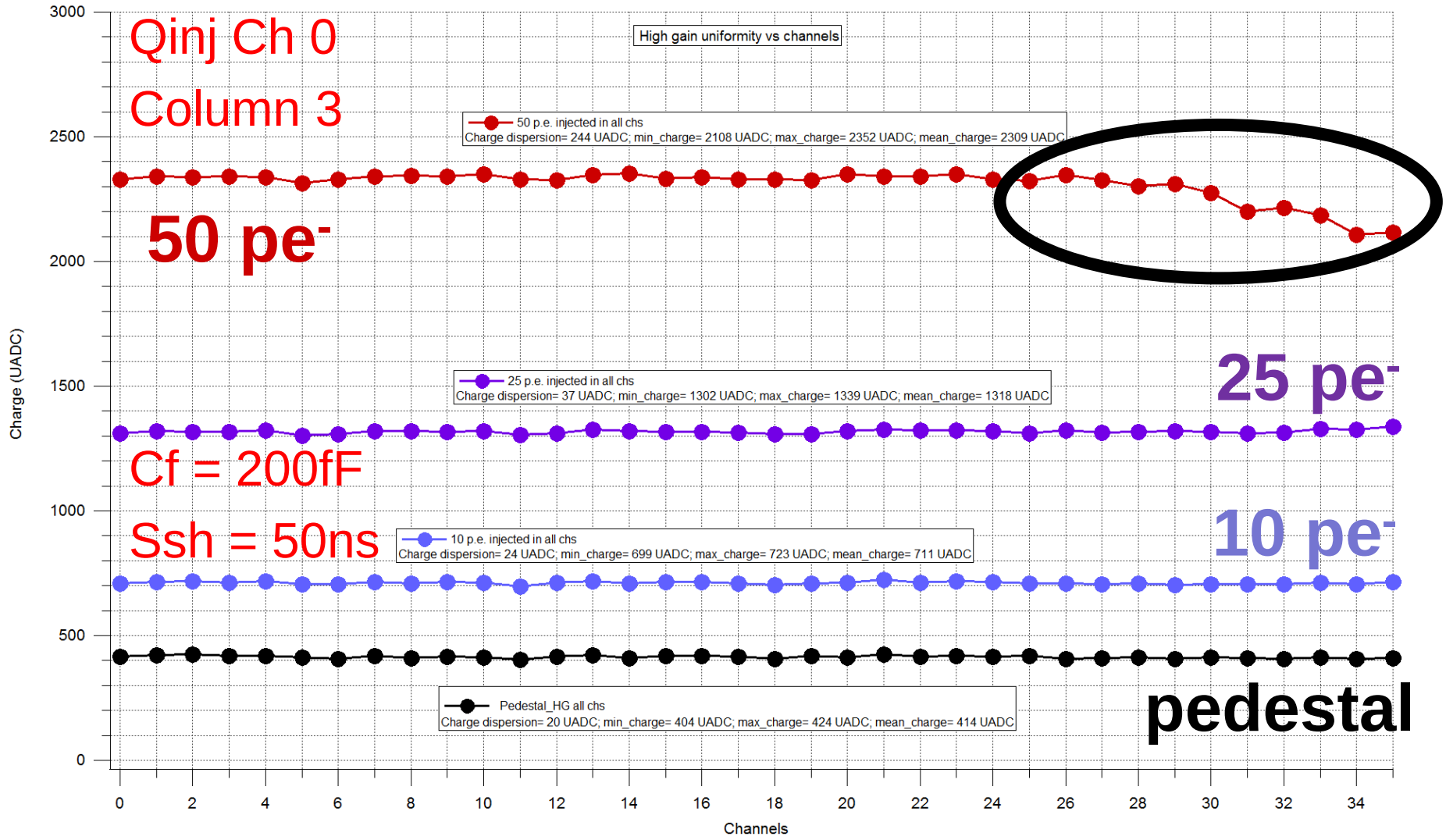


- Solution
  - Reset of the delay box when the acquisition is finished
    - Connect StartAcq to Rstb_delay in Spirod2d **: ISSUE CURED ON THE TESTBOARD**
    - initialization block with reset to be designed (next version)

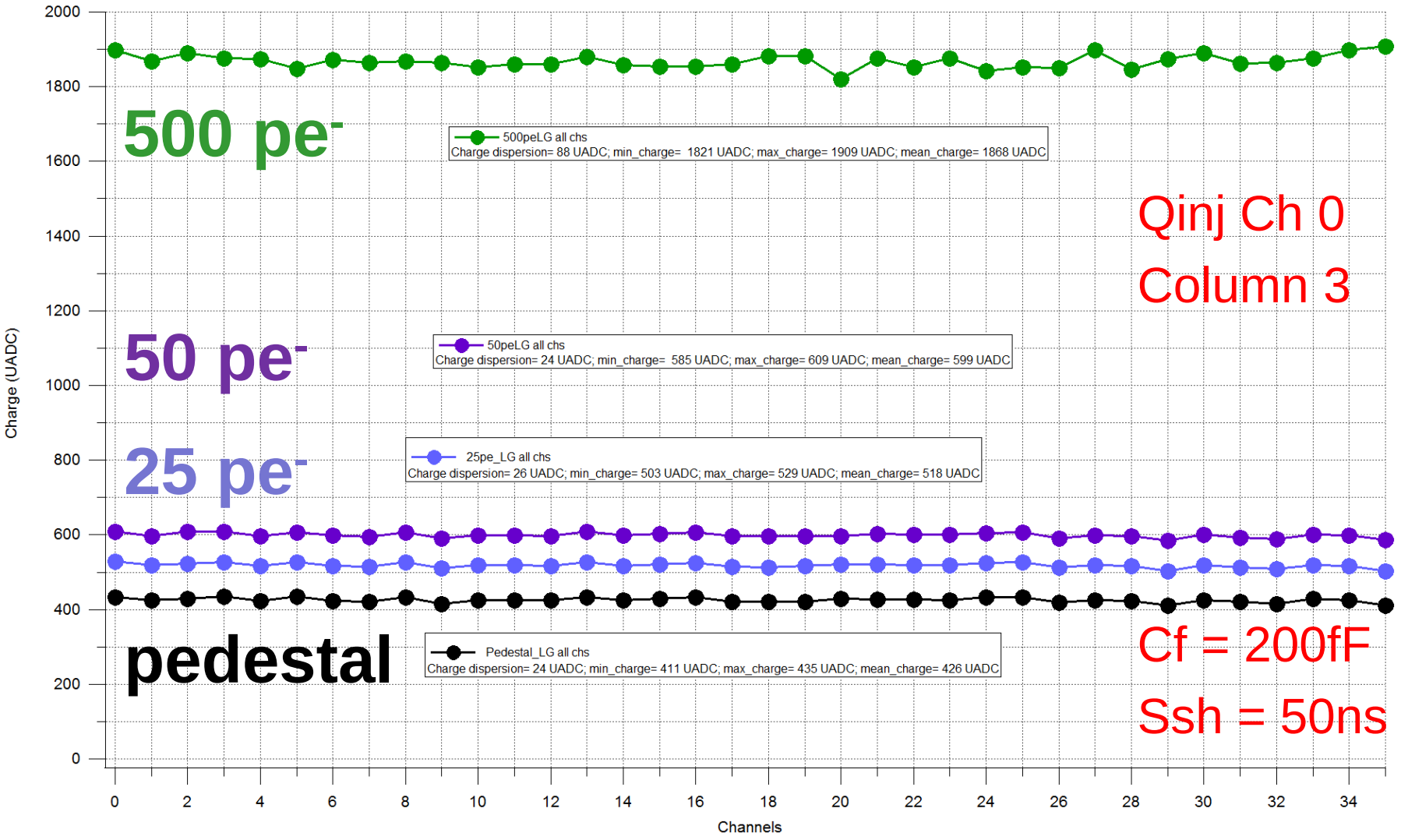
To be done



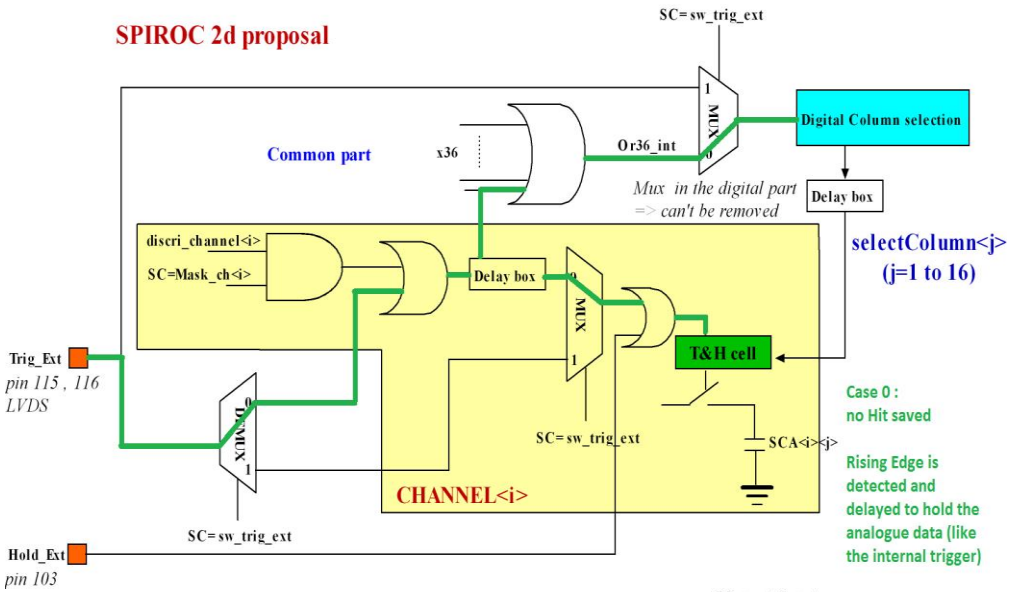
SPIROC2D : High Gain uniformity

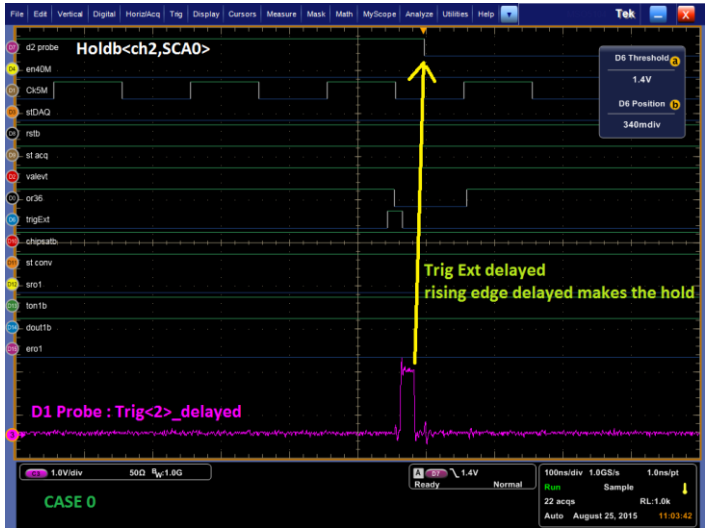


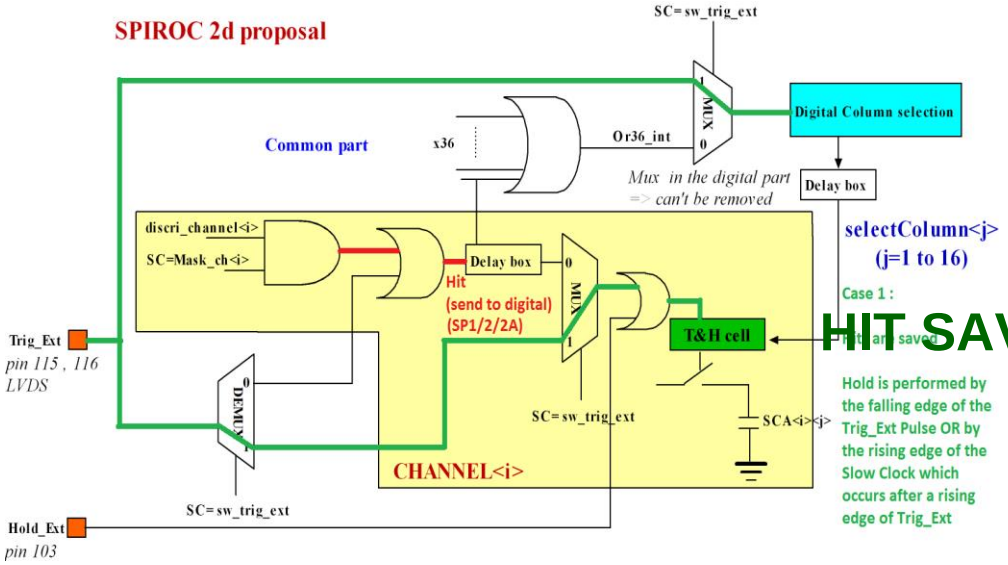
SPIROC2D : Low Gain uniformity



SPIROC2D : Test of the External Trigger : OK





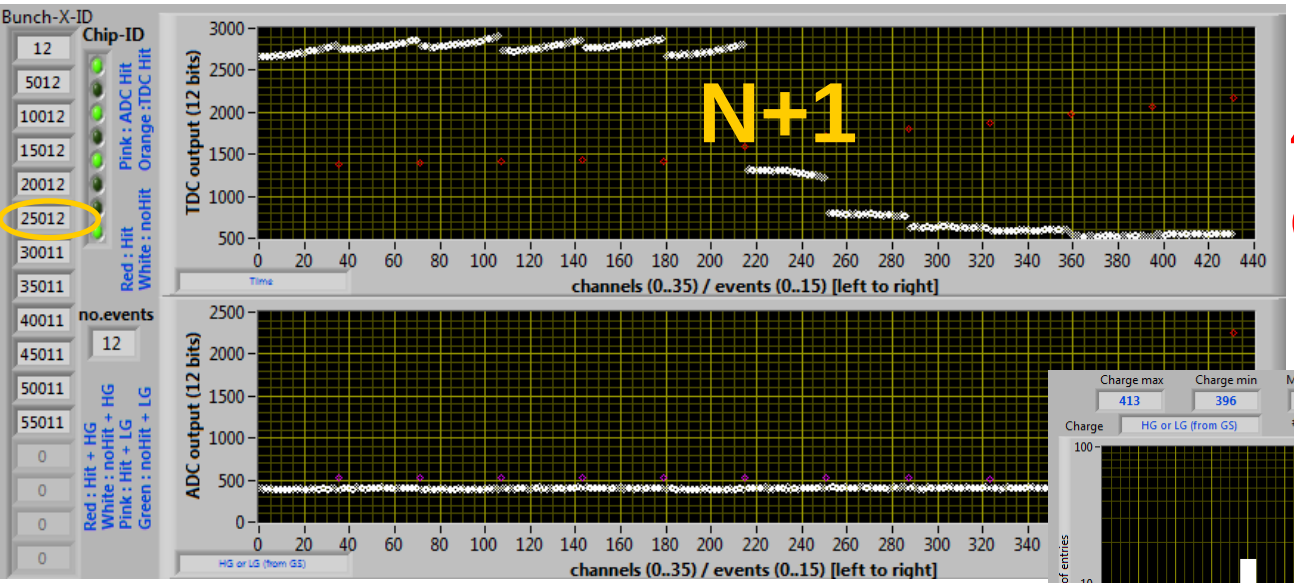


HIT SAVED

Successfully tested on testboard & HBU : **OK**

SPIROC2D : BCID Parity

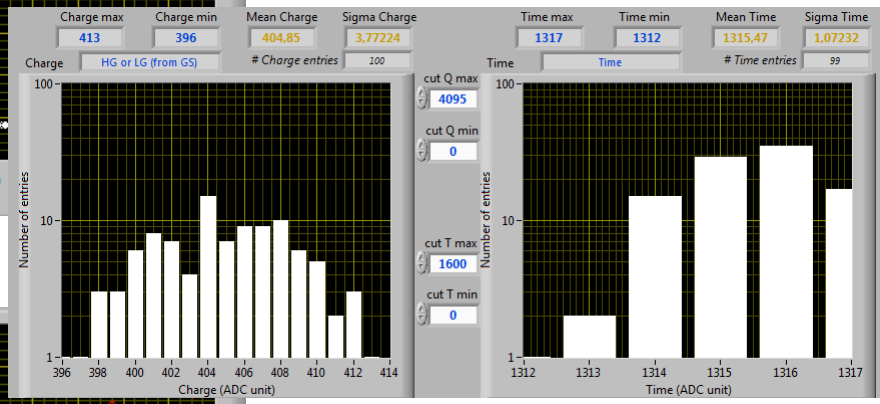
- So far, looking at the BCID value with respect to the delay between the beginning of the acquisition and the charge injection (using auto-trigger and a 5MHz Slow Clock) [test performed on the 1st event and on the 7th event] :
  - I see a 300 ps range where the Chip returns N or N+1
  - For the 199.7 ns remaining, the BCID value is perfectly stable on N
  - *It seems that I have retrigger without Hit in a ~6ns range in the middle of my Bunch Crossing (ie. I have 1 event with Hit @ N & 1 event without Hit @ N+1) : this is very preliminary, further measurements must be performed*
- This is not compliant with the BCID vs TDC measurement seen at DESY, especially as this occurs on both SP2B and SP2D who have different kind of TDCs (NoTrig/RazChn effect ?)
  - Further tests to be performed at DESY and OMEGA, I must do the same plot showing the TDC value measured

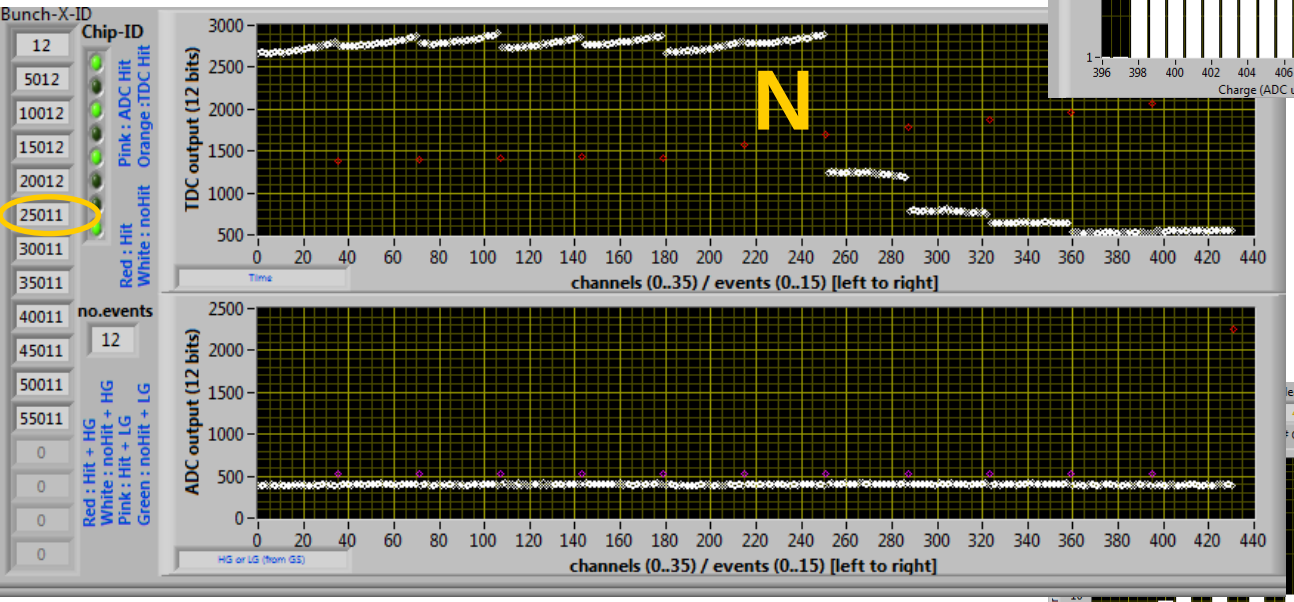


Delay for Q injection
4207.8ns

Qinj 50pe- in ch 35

Histo on ch 5 col 5

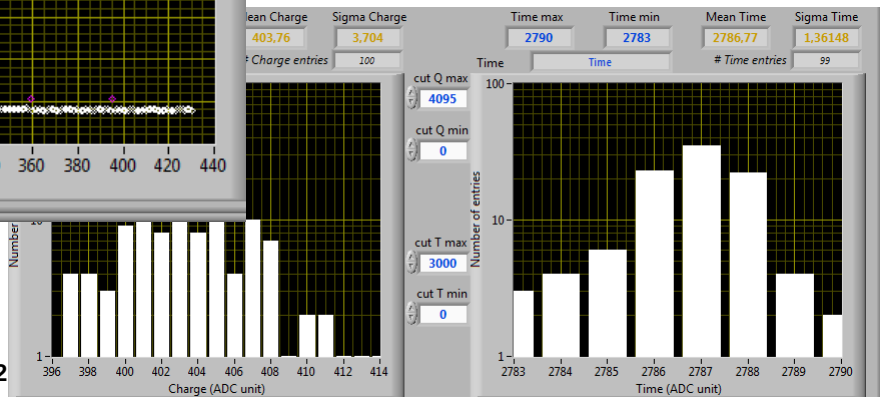




4207.5ns

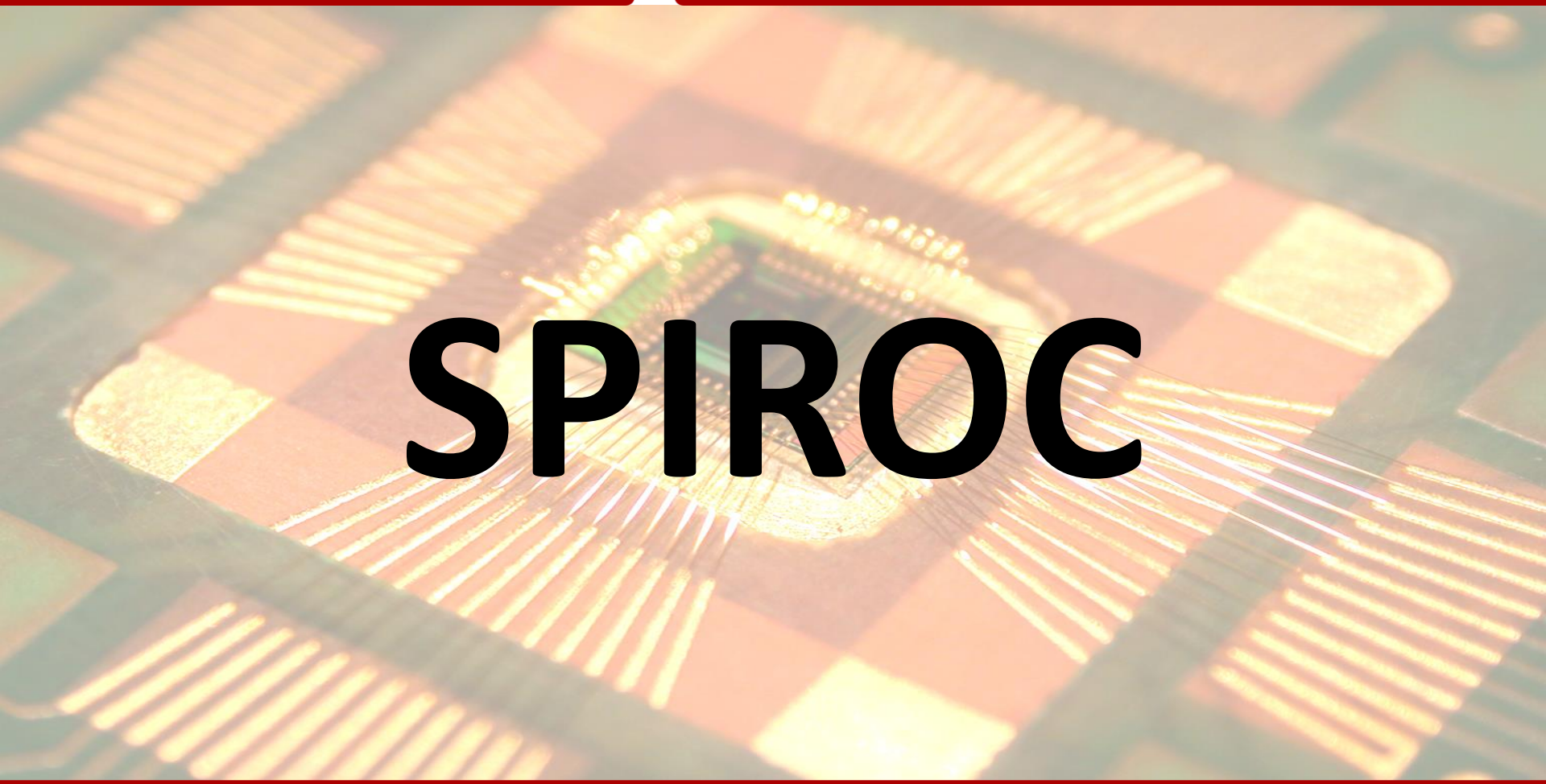
Qinj in ch 35

Histo on ch 5 col 5



Plotted here : 100 acquisitions

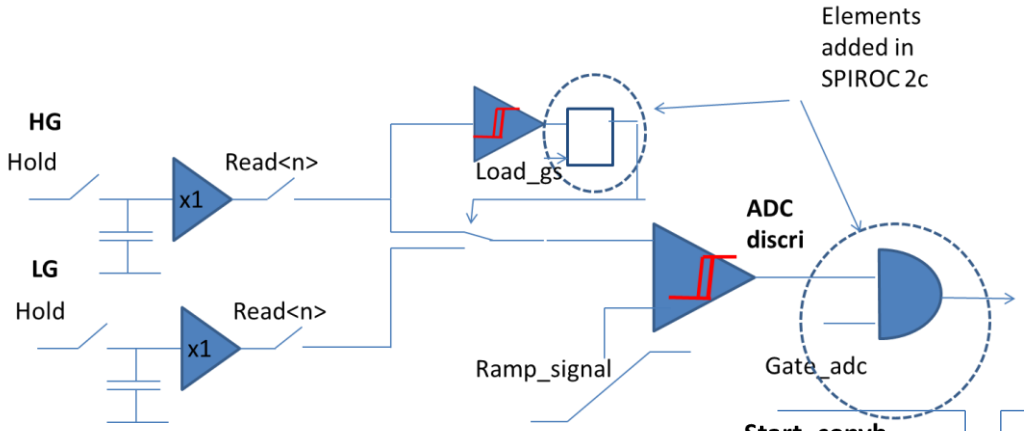
callier@omega.in2

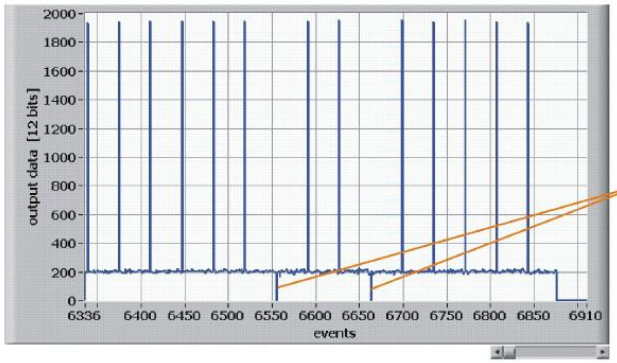


SPIROC

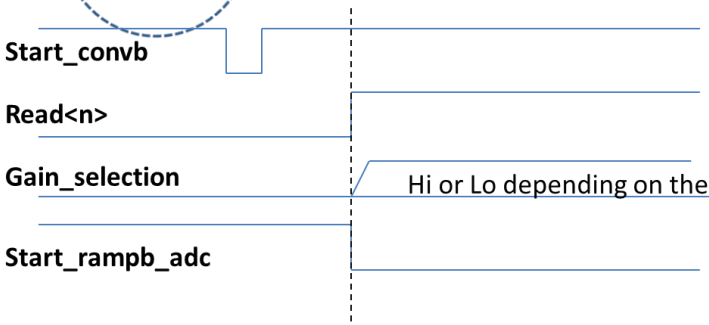
Organization for Micro-Electronics desiGn and Applications

SPIROC 2c : bug fix and improvements

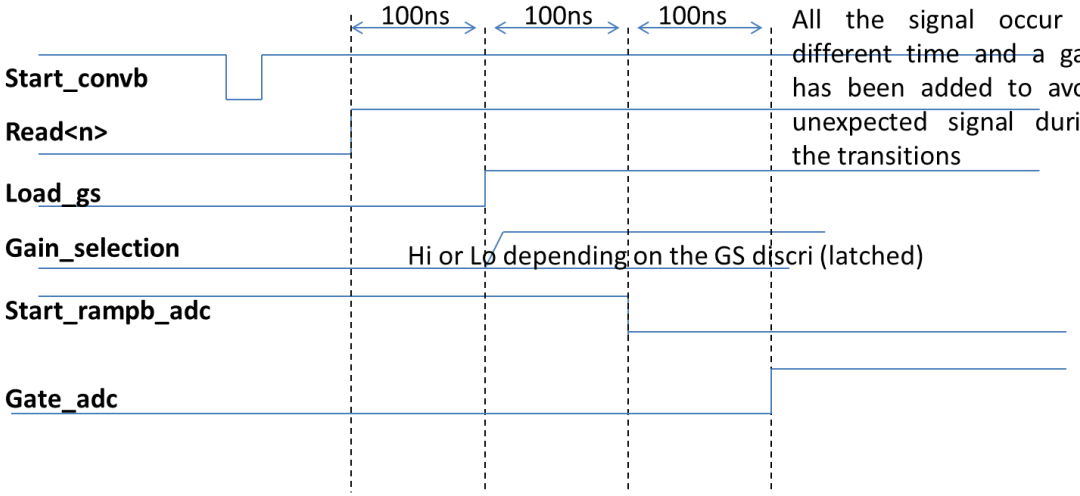




- "zero event" occurs randomly
- Problem solved in SPIROC 2c
- A D-flip-flop, a gate on ADC discri and delays on control signals



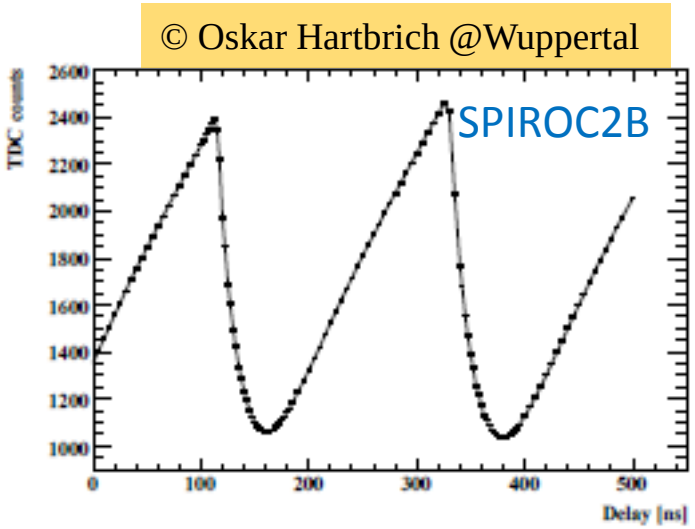
Situation in SPIROC 2b
All the signal occur at the same time

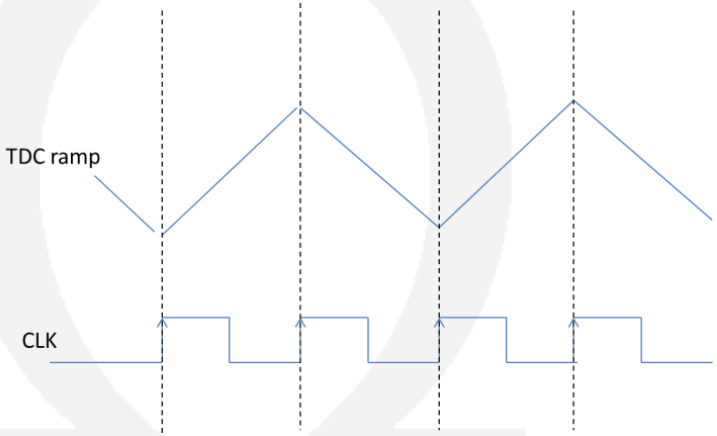


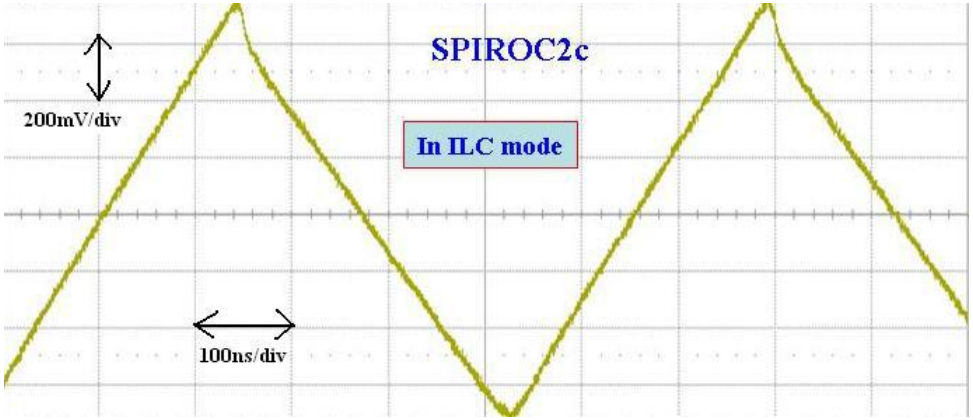
Situation in SPIROC 2c
All the signal occur at different time and a gate has been added to avoid unexpected signal during the transitions

SPIROC 2c: TDC improvements

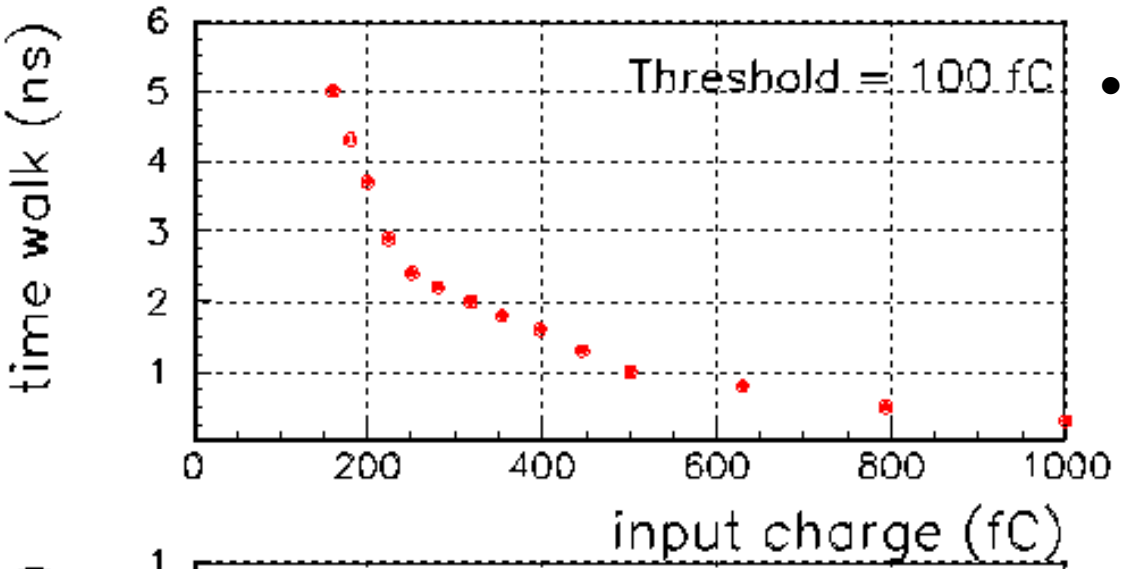
- Modifications on the TDC
  - To decrease dead time during transition => alternation of a rising and a falling ramp implemented
  - Conservative modification but not completely satisfying solution
  - Anyway, a new TDC has to be re-designed in SPIROC 3

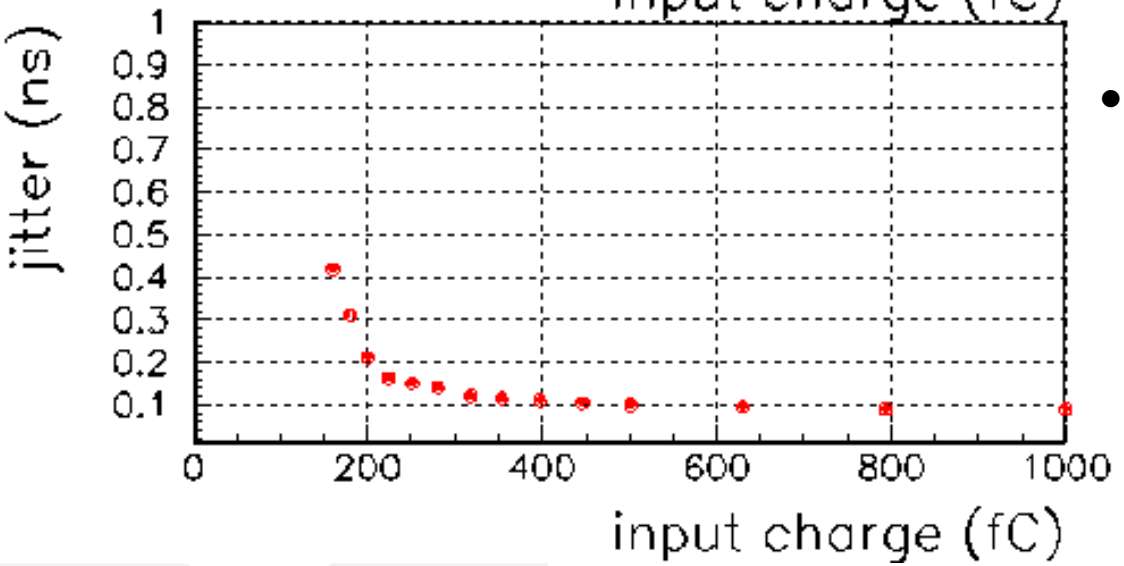






Time considerations : Trigger jitter and trigger time-walk





- Time walk: ~10ns
- Trigger jitter: ~100ps